

Software Development - 3K04
Assignment 2 - Part 1 - Pacemaker

Instructor: Dr. Alan Wassyng
November 26, 2017

Group 7 - “Group 4”

Adam Cool	400032857	coola
Andrew Rehkopf	001412499	rehkopaz
Evan Gagich	400027794	gagiche
Ibrahim Tannir	001204850	tanniri
Michael Henry	400011728	henrym1
Michael Soosaipillai	400034820	soosaipm
Moshiur Howlader	001316948	howlam

Contents

1	Introduction	2
2	Serial Receive	2
2.1	Design Decisions	2
2.2	Future Changes	2
3	Beat Period Calculation Block	2
3.1	Design Decisions	2
3.2	Future Changes	3
4	Pace Sensing	3
4.1	Design Decisions	3
4.2	Future Changes	4
5	Primary Pacing State Flow	4
5.1	Design Decisions	4
5.2	Future Changes	5
6	Electrogram and Serial Output	5
6.1	Design Decisions	5
6.2	Future Changes	5
7	Pulse Width Configuration Block	6
7.1	Design Decisions	6
7.2	Future Changes	6

1 Introduction

The purpose of this part of assignment two is to expand on the original model based design of the pacemaker from assignment one. A variety of pacing modes and functionality are to be added to the design to improve its original form. Unfortunately not all aspects of the design could be implemented as expected as trouble with Simulink serial communication and sampling times consumed a large portion of the project time.

2 Serial Receive

2.1 Design Decisions

As this assignment two part one is built on top of the part one of assignment one, the modular design used in the original assignment can be used to effectively implement new features. The added feature of serial communication can be hidden in the subsystem of the previous part that contained all user input. As long as the new subsystem that contains the serial functionality is providing the same outputs as the old constant system, the serial communication hardware of the pacemaker is hidden.

With the addition of a few new parameters, this new method of setting control variables in the design allows for greater testing as the pacing mode and parameters can be changed at any time. All required parameters for the added pacing modes are passed to the design this way with an additional eight bit code which indicates which egram mode the pacemaker is in. At start-up, an initial mode of VVO is set alongside a set of standard parameters.

This block functions by taking a vector of uint8 values sent from the DCM in a specific order and size. Variables that were scaled prior to sending are scaled here. As this block gave a great deal of trouble, the accuracy of variables was reduced to simplify this system. For example, the amplitude of the ventricular pace is set and sent in millivolts however it is only accurate to the 0.1 of a volt because of the range of values it could be can only be fit into a uint8 using a shift. We are away of bit shifting methods to gain greater accuracy.

Unfortunately, the serial block appears to alter the function of other timing in the device. For example, if the pacing mode is set to VVO and the beat rate 60, there will be a pace approximately every 1.5 seconds if the sampling time on the block is set to 0.001. However if the sampling time is reduced, to 0.1, the correct pacing speed is obtained however all timing in the device is now only accurate to 100ms which effectively renders the entire design useless.

The trade-off was made to set this sample time to 0.001 and as such, the timing in the design is wrong.

2.2 Future Changes

There are many likely requirement changes to this block as it essentially sets the controls of the pacemaker. If the units or size of the variables are to be changed, this block would have to be modified. If the number of parameters passed through it have to change, it would also be required to change. Finally if the method through which the parameters are passed experienced change perhaps for greater accuracy, additional data would have to be processed within it.

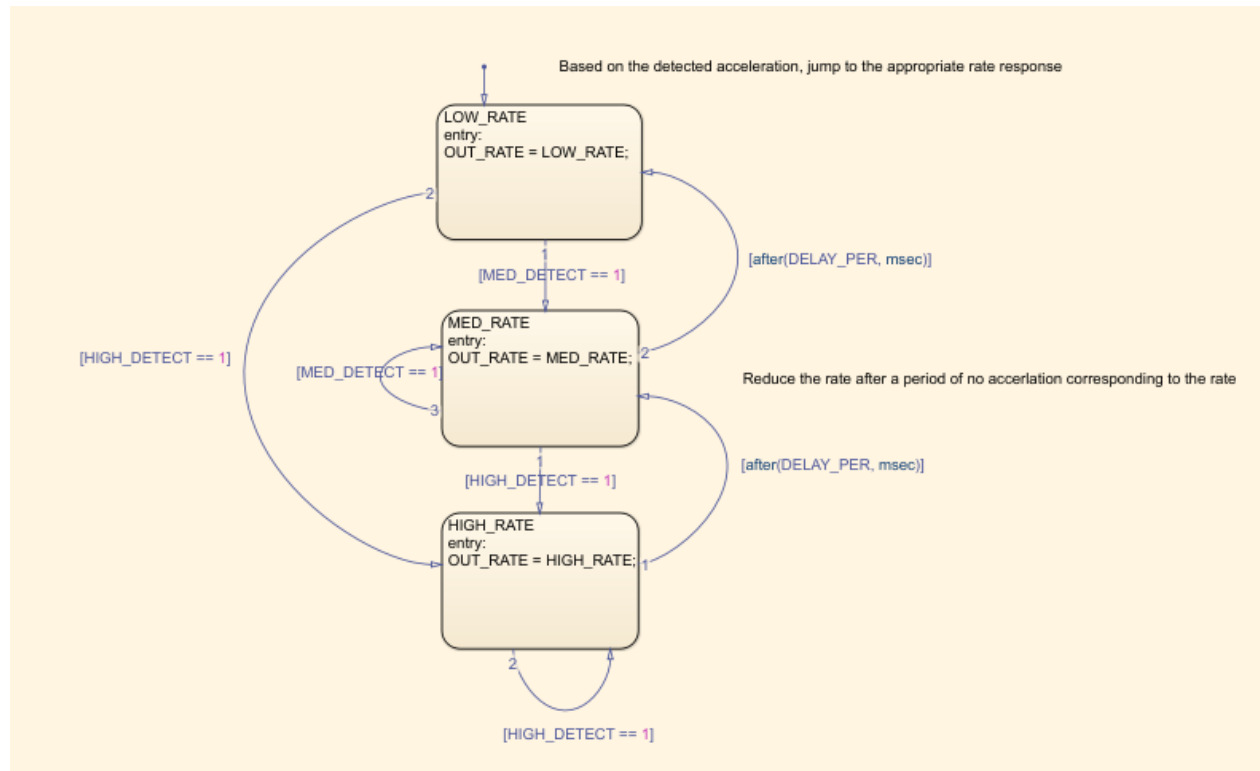
3 Beat Period Calculation Block

3.1 Design Decisions

This block is adapted from assignment 1 where it originally converted a beats per minute value to a millisecond period. As modular design was applied in the original assignment, the block can be repurposed to incorporate greater function with little negative effect on other systems. It still provides a single output however now it receives a few additional inputs to handle rate adaptivity.

The block encompasses the rate adaptivity function of the pacemaker and normal pacing periods. It takes an upper rate and lower rate that it uses for rate adaptivity. If the pace mode is not rate adaptive, it will pace at the lower rate. If the mode is rate adaptive, a function of sort is implemented to change the rate from lower, to an average of lower and upper to the final upper rate. This function is implemented using a state flow that on detection of a g normalized acceleration between 1 and 1.5, will put the pacemaker into its medium rate. When the g detected is greater than 1.5, the pacemaker functions at its upper rate. Below 1 g, it paces at the lower rate.

The g acceleration is calculated using the onboard accelerometer where the absolute values of X, Y and Z acceleration is averaged. When the appropriate acceleration is detected, a controlling state flow will place the pacemaker in its respective pacing speed for five seconds after which the pacing speed will be reduced to the rate which is immediately lower than the current rate. For example, if it detected a 1.5g acceleration it will pace at the upper rate for until no 1.5g acceleration has been detected for 5 seconds after which it will pace at the medium rate until falling again after 5 seconds of little acceleration to its lower rate.



Rate Adaptivity State Flow

We do not take this rate adaptivity seriously in terms of safety as it is simply impractical to the extent it can be implemented with the chosen platform. Pacing the heart at a rate purely determined by acceleration makes no sense as much of the acceleration a human experiences is not due to their own action. Take driving a car for example, should their heart rate increase if they suddenly accelerate? As such, we leave much of this design open to change.

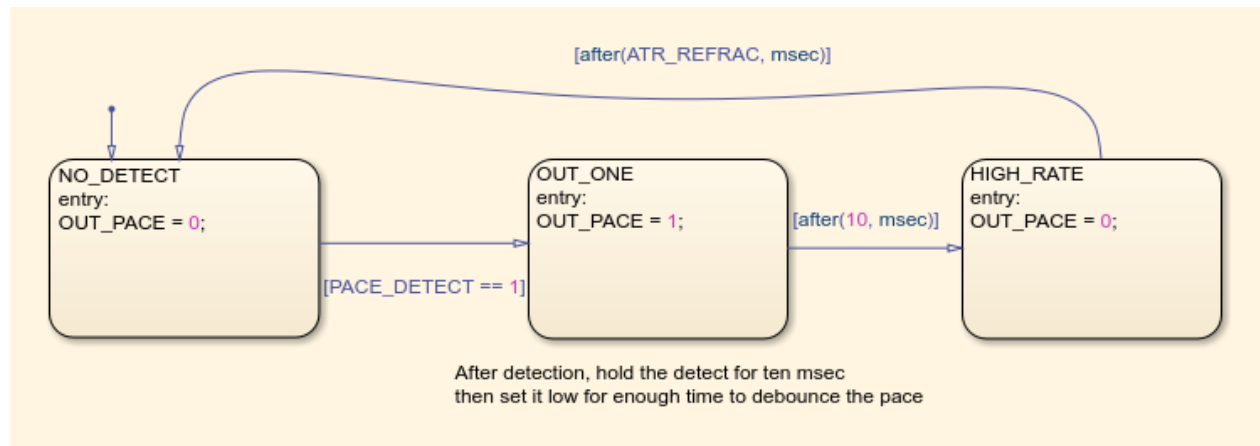
3.2 Future Changes

This block will likely change in many ways to make it more realistic by perhaps adding additional levels to the rate adaptivity. In addition, there may be additional pacing modes that require the system to output different forms of pacing rate. Perhaps adding rate adaptivity to the av delay or refractory periods to implement complex pacing modes.

4 Pace Sensing

4.1 Design Decisions

This subsystem utilizes the sensing circuitry provided in the pacemaker shield. After the sensing circuitry is enabled, there are two digital inputs provided from the shield that output logical high when a pace is sensed within the heart. The threshold of this pace is set using a constant pulse width modulation operation.



Pace Sensing Debounce State Flow for the Atrium

When a pace is detected, the pace is processed using a debounce state flow. On detection, a logical high is set for 10 milliseconds and then the pace detect is set low for the associated chamber refractory period. Since it is known that a pace cannot occur during this period, we can ignore any pace that may happen during this time.

A LED is attached to both chambers pacing sensor to indicate when a pace is sensed.

4.2 Future Changes

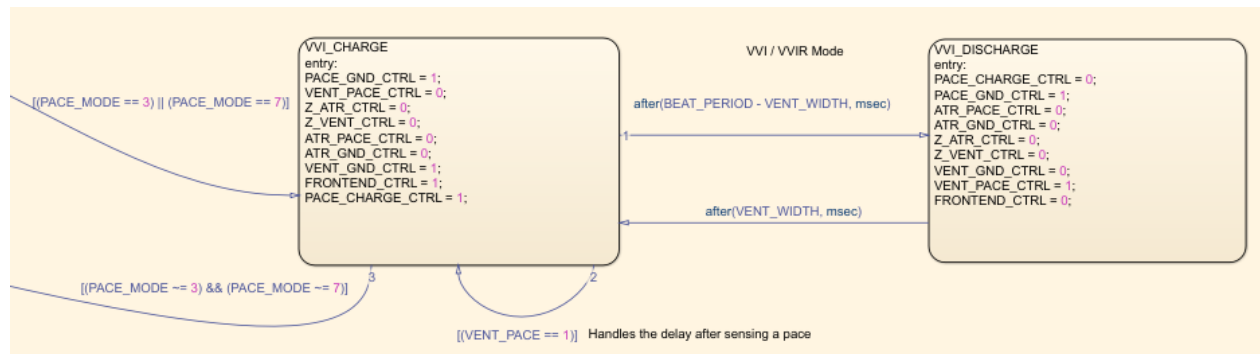
There are few likely changes to this system besides improvements to debouncing and perhaps additional variability added to the detection threshold that perhaps accounts for weaker or variable strength heartbeat voltages as at the moment, this threshold is constant.

5 Primary Pacing State Flow

5.1 Design Decisions

This stateflow encompasses all aspects of pace control as it alone handles nearly all control input and output pins that are used to initiate pacing. The design of this state flow was specifically made to be as simple as possible to minimize the usage of the device resources and for ease of testing. Unfortunately, the timing of this vital portion of the device is hampered by the serial receive block which appears to slow all time calculations by at least a factor of 1.5 (1 second pace period turns into a 1.5 second pace period).

An example pacing mode state transition is given below. The charging occurs during the beat period provided by the rate adaptivity and beat period calculation block followed by a discharge for a period specified in the serial parameter transmission. The rate adaptivity is directly incorporated into the delays between charges and discharges such that the flow for VVO and VVOR can be shared.



The flow of VVI/VVIR mode

To implement pacing modes that require sensing, the pace sensing block is fed into the state flow which is used to reset the counting between discharge and charging states. Finally to allow for dynamic changing of pace mode and parameters, on the event of a new pace mode sent from the DCM not corresponding to any of the current modes it may be operating in, the state flow returns to an idle state for a short period where it can then reassess which mode it must head into. As the above figure demonstrates, if the mode is either VVI or VVIR the pacing will continue with the above form. If the pacing mode changes, the flow returns to the centre state then heads to whichever pacing mode is required.

Effective hardware hiding is implemented with this block as the pacing controls are operated on using only variable names and never referencing specific pins that are unique to the platform in use. It should be noted that pace sensing circuitry is disabled during a discharge to prevent the detection of ones own pace.

5.2 Future Changes

There are many future changes that must be made to this state flow to perhaps include additional pacing modes and modes that use both the atrium and ventricle. In addition, there may be requirements changes for the order with which the outputs are applied. Because of the simplicity of this design, many more pacing modes can be added with minimal resource usage.

6 Electrogram and Serial Output

6.1 Design Decisions

This subsystem is greatly simplified as serial communication caused many problems for this project. As such, the analog pins which monitor the activity of the heart are outputted directly to the serial output block. Little is done to process this data as such efforts only lead to greater problems with the design such as loss of overall function.

The type of electrogram signal is determined by the egram parameter passed during the serial receive. If the value is zero, nothing besides a flat line zero is sent serially. If a egram value of one is received, only the ventricle data is sent. Finally, if a two is sent, the atrium data is serially transmitted. Regardless of the data sent, each is converted to uint8 prior to serial transmission.

6.2 Future Changes

There are many future changes to this block that will likely occur in the next assignments as little is done to process the data to improve its usability. As it stands, the data is sent as once per millisecond which is certainly taxing on the system. Future designs should change the operation such that the data sent is processed and scaled to fit a uint8 value for serial transmission.

Requirements changes for this block are likely as well as perhaps future designs would require both ventricle and atrium data to be sent at the same time which would require a data packaging scheme that could be decoded on the DCM end of the assignment.

As for the serial transmission, there are many changes that should be implemented in future designs. The ability to transmit the parameters that were just written to the pacemaker would enable the DCM to confirm that the parameters

were successfully sent. In addition, the pacemaker should send a unique ID so that the DCM always knows which device it is connected to.

7 Pulse Width Configuration Block

7.1 Design Decisions

This block is a continuation of the PWM control block of assignment 1. The requirements of the block are to set the correct PWM configuration to the three ports that are driven by PWM. These ports are the threshold voltage ports for pace detection for both the atrium and ventricle and the amplitude of the induced pace. This common block encompasses three different PWM calculation blocks for each of these PWM configurations.

The threshold voltages are configured in a constant manner and the amplitude of the pace is set from parameters sent from the DCM. Using the pace mode, the correct amplitude of pace (the ventricle or atrium amplitude sent from the DCM) is written to the PWM port.

7.2 Future Changes

As for potential design changes to this block, the manner through which the pace amplitude is set cannot be continued in future design as the amplitude of pace will not be constant within a given pace mode. For example for any of the dual chamber pacing modes, the pace amplitude must change prior to pacing each chamber of the heart. For this reason, a flag of sort must be set in the primary pacing chart to ensure that the right pace amplitude is given at the right time.