Software Development - 3K04

Assignment 2 - Bonus

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1 Introduction

The bonus was attempted however due to timing issues caused by the serial communication, the timing of ventricle and atrium paces became unreliable. For instance, when the sample rate of the serial receive block was set to 1 ms, the DDO mode would constantly discharge the atrium and ventricle. However, when the sample rate of the block was set to 100 ms, a more reasonable delay in terms of simulation would appear from the board.

2 Design

The DDO and DDOR functionality was added as an additional state in the primary flow chart that controlled all other pace modes. This functionality would take the beat period calculated with or without rate adaptivity and cycle from the atrium discharge state for the atrium pulse width then to the ventricle charge state for the AV delay period. Following this, the ventricle would discharge for its pulse width which would lead to the atrium charging state for the remainder of the beat period (Beat Period – AV Delay – Ventricle PW – Atrium PW). Upon the press of a button, the ventricle discharge would not occur.

3 Future Changes

Obviously something was wrong with this implementation as it did not perform correctly on the board. Perhaps the method of implementation has to be scraped completely or there is an underlying problem with the serial communications. As for requirement changes to this bonus assignment, there are many. One thing likely to change is the rate adaptiveness of the av delay which at the moment is constant. If this delay was altered in the same manner as the rate adaptive beat period, the DDOR mode would be more realistic. In addition, it is clear that the button press is supposed to simulate a ventricle pace being sensed, in future designs this will likely be the equivalent of pace detection of the ventricle and the atrium.

4 Testing

The following cases are tested on the board and in simulation to prove that the the framework of this design is functional in simulation however it does not function on the board.

Test Case	Expected Output	Actual Output	Result
60 BPM, 250 ms AV delay, 2 ms PWs, DOO mode in simulation	Atrium pace then Ventricle pace after AV delay, repeat after correct remainder of beat period	Both paces are seen, delay appears correct	Pass
60 BPM, 250 ms AV delay, 2 ms PWs, DOO mode on board. 0.1 s sample time on serial block	Atrium pace then Ventricle pace after AV delay, repeat after correct remainder of beat period	Atrium and Ventricle pacing far too fast with incorrect intermediary delay	Fail
60 BPM, 250 ms AV delay, 2 ms PWs, DOO mode on board. 0.001 s sample time on serial block	Atrium pace then Ventricle pace after AV delay, repeat after correct remainder of beat period	Atrium and Ventricle pacing all the time, at the same time	Fail