Software Development - 3K04

# Assignment 3 - Part 1 - Pacemaker

**Instructor: Dr. Alan Wassyng**

December 10, 2017

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**Group 7** - "Group 4"

| | | |
|---|---|---|
| **Adam Cool** | 400032857 | coola |
| **Andrew Rehkopf** | 001412499 | rehkopaz |
| **Evan Gagich** | 400027794 | gagiche |
| **Ibrahim Tannir** | 001204850 | tanniri |
| **Michael Henry** | 400011728 | henrym1 |
| **Michael Soosaipillai** | 400034820 | soosaipm |
| **Moshiur Howlader** | 001316948 | howlam |

# Contents

# 1 Introduction

Few changes were made to the pacemaker model from assignment 2 as much of the framework for the final implementation was completed during previous assignments. Assignment 3's pacemaker model primarily solved any bugs present in the previous design and implemented the bonus DDD and DDDR mode.

# 2 Serial Receive

## 2.1 Design Decisions

From assignment 2, this module has not changed with the exception of the electrogram constant being dropped from the serial input. As such, the number of serial uint8 data expected has been reduced. The following table outlines the serial data expected.

| **Serial Data** | **Range** | **Type** |
|---|---|---|
| Pace Mode | 0 - 12 | uint8 |
| Upper Rate | 60 - 175 bpm | uint8 |
| Lower Rate | 60 - 175 bpm | uint8 |
| Atrium Ventricle Delay/10 | 70 - 300 ms | uint8 |
| Ventricle Pace Amplitude/100 | 500 - 5000 mv | uint8 |
| Atrium Pace Amplitude/100 | 500 - 5000 mv | uint8 |
| Ventricle Pulse Width | 1, 2 | uint8 |
| Atrium Pulse Width | 1, 2 | uint8 |
| Ventricle Refractory Period/10 | 150 - 500 | uint8 |
| Atrium Refractory Period/10 | 150 - 500 | uint8 |

Values are scaled to fit their variable size prior to sending to the pacemaker

## 2.2 Future Changes

As for likely requirement changes, there is still the possibility of new parameters expected to be passed to the pacemaker from the DCM. In addition, the data passed is still rounded to fit into a uint8 data package. If increased parameter accuracy is required, this module may have to change to expect more data.

# 3 Beat Period Calculation Block

## 3.1 Special Note about Bug Fix

Assignment 2s implementation of part 1 was plagued by a timing issue that would cause the timing of the pacemaker to be continuously doubled only when deployed to the board. This issue was caused by the 6-axis sensor used for rate adaptivity. The only fix for this issue was to decrease the sampling rate of this block to 100ms instead of 1 ms and use a rate transition block to merge it with the rest of the model.

## 3.2 Design Decisions

Little change has been made to this module. The only change was to ensure that upon new serial data, the original lower rate for rate adaptive pacing was updated. Testing during assignment 3 indicated that the rate adaptive state flow was holding the lower rate even after a new lower rate had been requested from the DCM.

### 3.3 Future Changes

There are many likely requirement changes to this module including increased support for rate adaptivity. At the moment, the rate adaptivity only has three pacing rates based on the acceleration of the device. For a more realistic rate adaptivity, higher graduation can be implemented.

Finally, refractory periods and the atrium ventricle delay is not rate adaptive and no measure is made to ensure that the atrium ventricle delay or refractory periods are not too long such that it would cause them to obscure the pace timing.

## 4 Pace Sensing

No changes were made to this block since assignment 2. Please review assignment 2 documentation for this module .

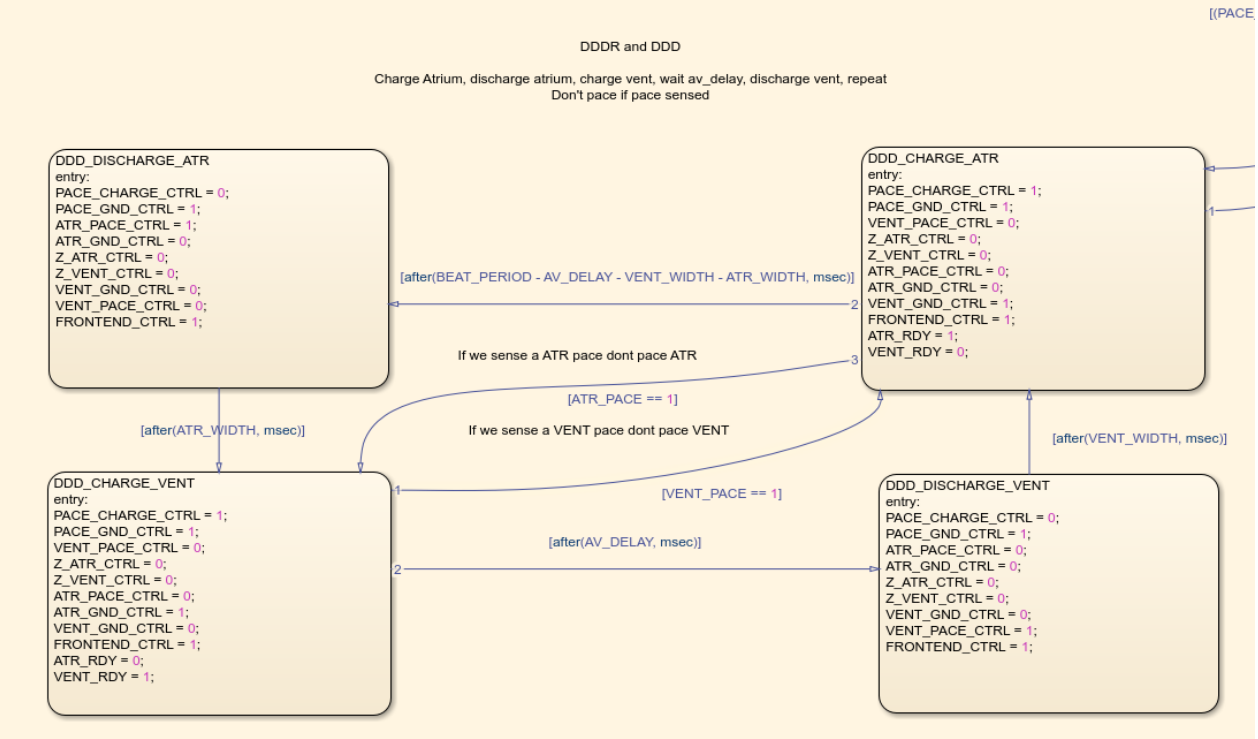
## 5 Primary Pacing State Flow

### 5.1 Design Decisions

The only changes to this state flow is the addition of DDD and DDDR support as well as bug fixes for DOO and DOOR mode. These modes are implemented exactly as any other pacing mode however they pace multiple chambers and as such, require an additional two states. Both dual chamber modes begin charging the atrium followed by its discharge which leads into the charging of the ventricle which then discharges after the set atrium ventricle delay. Obviously the DDD/ DDDR mode prevents the pacing of atrium or ventricle if a natural pace is detected prior to pacing. As a final measure, upon charging the atrium or ventricle, a flag is set to indicate to the PWM configuration module which chamber pace amplitude to use.

### 5.2 DDD/DDDR Design

DDD mode was implemented to check and inhibit both chambers although the description was found to be somewhat ambiguous as it did not mention if the atrium was to be sensed and paced if no natural pace was seen. In addition, the description seemed to indicate that the ventricle was to be paced after the AV delay as long as an atrium pace was detected. We decided that it made more sense to check for a natural ventricle pace prior to pacing the ventricle.




The flow of DDD/DDDR

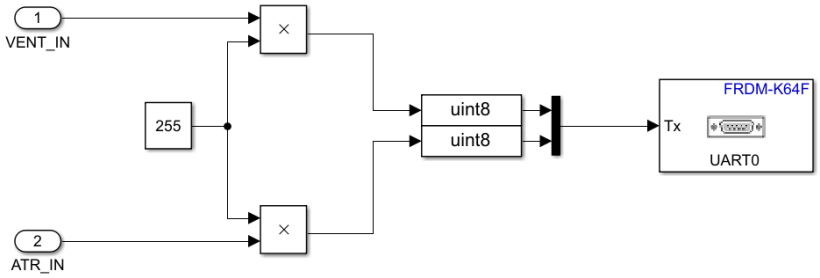
### 5.3 Future Changes

As for likely requirements changes, this stateflow could always add any other pacing modes that are required. Modes that are currently not implemented include any of the monitoring modes although the idle mode acts almost as a pseudo monitoring mode. Perhaps pacing modes specific to conditions such as arrhythmia would be required in later designs.

## 6 Electrogram and Serial Output

### 6.1 Design Decisions

The implementation of electrogram control has changed greatly. The serial out port of the model is now dedicated to sending a two uint8 package of atrium and ventricle data continuously. Both chambers are always sensed and their data are always being streamed to the DCM after scaling to fit the uint8 package (multiply float value 0.0 to 1.0 by 255).




The serial out package is formatted

### 6.2 Future Changes

As for requirement changes, the use of serial out in the model is likely to change in future designs as there are required data that were excluded from the DCM communication such as a handshake package to indicate that the parameters were successfully sent to the pacemaker or an identifier that lets the DCM know that the pacemaker being interfaced has not changed.

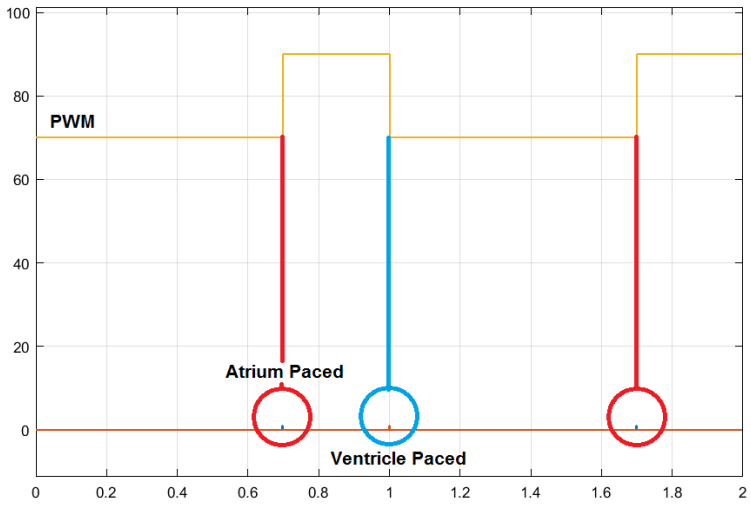
Additional requirements may alter the accuracy of the data being sent where perhaps a uint16 package would sent for each chamber which would offer an additional degree of sensing graduation.

## 7 Pulse Width Configuration Block

### 7.1 Design Decisions

From assignment 2, the only change to this module was to include additional pace modes to the pace amplitude setting and support for a flag set in the primary state flow which indicated the appropriate chamber to set the amplitude for.

This variable PWM amplitude dependant on the chamber that is next to be paced is tested in the following scope output. Clearly when the atrium is next to be paced, the amplitude is set to 70%. After the atrium pace, the amplitude is immediately changed to the ventricle amplitude of 90% until it is paced.




The pace amplitude is changed in real time

## 7.2 Future Changes

After this selective pace amplitude configuration, there are no obvious design changes that may be required at a later time.