1. Introduction (EDIT HERE: report)

1.1. Objective

1.1.1. For funsies

1.1.2. Hear me out, Verilog ???? (signed, Arie)

//State the purpose of developing the MIPS-lite pipeline simulator.

1.2. Scope

1.2.1. 16x magnification :)

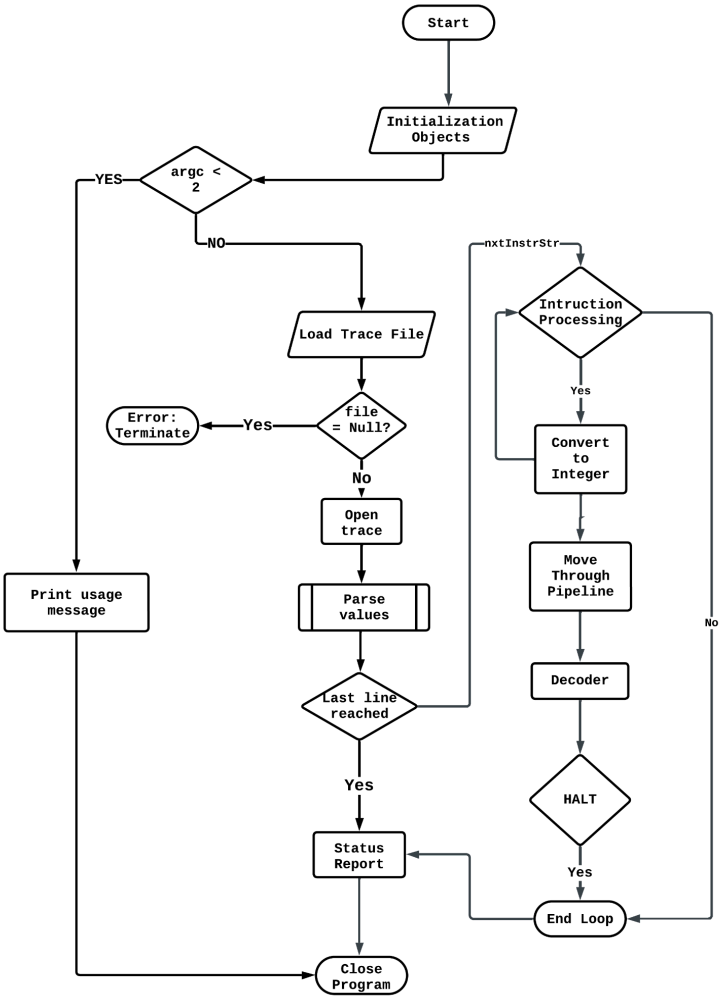
//Includes simulating various instruction types and pipeline behaviors.

2. Methodology

2.1. Simulator Architecture

2.1.1. Program pseudocode (to edit flowcharts)

//Briefly describe the components of the simulator (Decoder, Instructions, Pipeline, Status).



2.2. Implementation

//Touch on the programming language used, the structure of the code, and the key functionalities of each module.

3. Simulation Results

3.1. Total Number of Instructions and Breakdown

//Total Number of Instructions and Breakdown

Maybe a table with the total number of instructions executed and a breakdown by type: Arithmetic, Logical, M

3.2. Final State of System

//Registers and Memory List the final state of the program counter, all general purpose registers, and memory locations that changed during execution. This can be presented in tabular format or as a series of figures.

4. Pipeline Management Analysis

4.1. Stall Conditions

//State the purpose of developing the MIPS-lite pipeline simulator.

4.2. Data Hazards

//State the purpose of developing the MIPS-lite pipeline simulator.

4.3. Execution Time

//State the purpose of developing the MIPS-lite pipeline simulator.

4.4. Speedup Analysis

//State the purpose of developing the MIPS-lite pipeline simulator.

5. Discussion

//State the purpose of developing the MIPS-lite pipeline simulator.

6. Conclusion

//State the purpose of developing the MIPS-lite pipeline simulator.

7. Appendices

//State the purpose of developing the MIPS-lite pipeline simulator.