FPGA development platform black gold

User's manual

AX309

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Issue control

Issue	Modify the contents of records
REV1.0? Create a document?	
REV1.1?? P. 30, J2 expansion port table, 29 instead R1,30 instead R2??	
REV1.2?? Pp. 6, pp. 11, 64Mbit changed to 16Mbit??	
REV1.3? P. 21,?? LED level section describes the correction?	
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Copyright Shen Ming:

Thank you for purchasing black gold development board, before using the product, please read the manual carefully and make sure you know how to properly use the product, illogical operation may damage the development board, use at any time during the reference manual for proper use.

This manual is constantly updated, we recommend that you download the latest version to use.

Software version:

This manual Xilinx The official provided ISE 14.7 Version, from Xilinx Web site to download the correct version to install and use the software version we offer.

Black Gold's official website:

Http://www.alinx.com.cn

Black Gold Power Community:

http://www.heijin.org

Black Gold official Taobao shop:

http://oshcn.taobao.com

Contact information:

021-67676997

Black gold micro-channel public number:

ALINX-HEIJIN

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table of Contents

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FPGA development platform black gold has welcomed a little brother AX309 ,? this development board is attached to the entry-level products, mainly for FPGA beginners. AX309 using XILINX company SPARTAN6 series chip, model XC6SLX9-2FTG256C, is 256 feet FBGA package. Configuration Utility entire development board, there are two black gold standard AX expansion port, a total of 34 * 2 = the IO 68, but also leads to additional power 5V, 3.3V power supply, the GND there are multiple, like for players to DIY that is a very good choice. In addition, many of the black gold accessory modules can also be connected directly to the expansion port The FPGA development board, such as ADDA module, 4.3-inch LCD screen, an audio module, camera, etc., provide more choices for players to learn. Here we are on AX309 do a detailed introduction. ?

?

one, Brief introduction

Here, on this FPGA development platform features a simple introduction. ?

Development board section using a Xilinx's Spartan6 series FPGA, model XC6SLX9,256-pin FBGA package. FPGA resources this section is shown below:?

Device	Logic Cells(1)	Configurable Logic Blocks (CLBs)			DSP48A1 Slices(3)	Block RAM Blocks		CMTs(5)	Memory Controller Blocks (Max)(6)	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices(2)	Flip-Flops	Max Distributed RAM (Kb)		18 Kb(4)	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358

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Among them, the main parameters?

parameter	Numerical
Logical Unit Logic? Cells?	9152?
The multiplier DSP48?	16?
Configurable logic block the CLBs?	90Kb?
Block? RAM?	576Kb?
The clock unit? CMTs?	2?
The number of available IO?	200?
Core voltage?	1.15V-1.25V (recommended 1.2V) ;?
Operating temperature?	0-85 ℃?

?

The picture shows the schematic structure of the entire system shown in FIG. 1.1:?

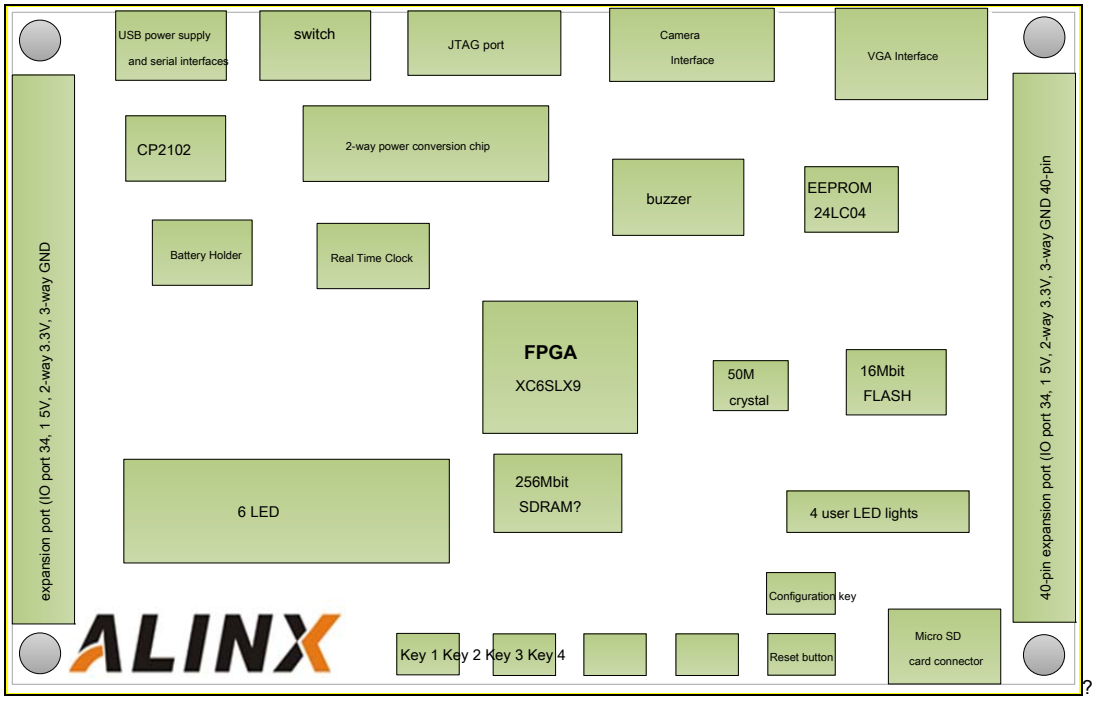

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Figure 1.1 Development board system architecture diagram?

?

Through this schematic diagram, we can see that our development platform can realize the function. ?

- USB interface, power supply, and USB to serial port function;?
- A large-capacity 256Mbit SDRAM, as cached data?;?
- ? A 16Mbit SPI FLASH ,? the FPGA configuration file may be used and the user data stored;?
- A camera interface, you can access OV5640 camera 5 million;?
- One VGA port, VGA port is 16bit, can display 65,536 colors, can display color pictures and other information. ?

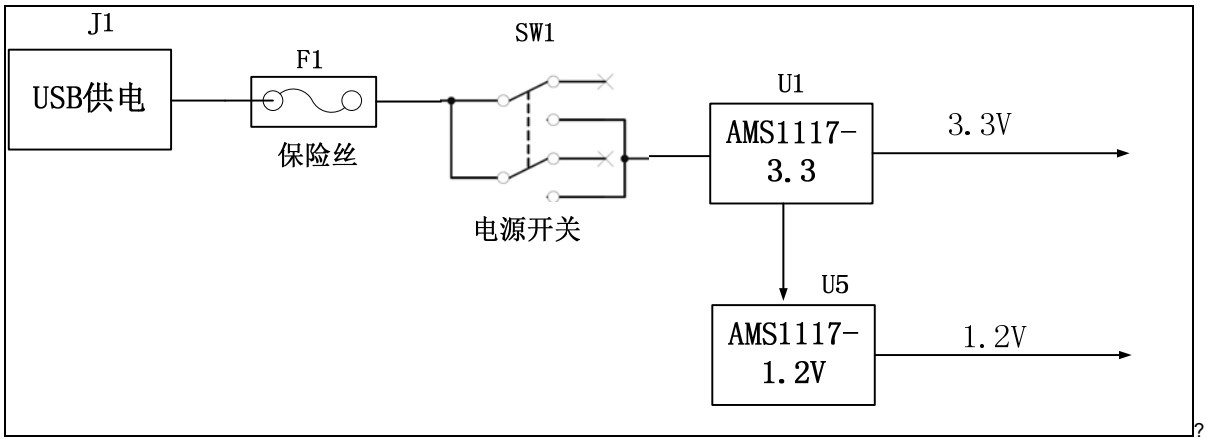
?

? ?

- One of RTC real time clock with battery holders, battery model CR1220. ?
- An EEPROM IIC interface? 24LC04 ;?
- 4 red LED, lamp function may be implemented water;?
- 4 independent user buttons;?
- Onboard 50M active crystal, the development board to provide a stable clock source;?
- 2-way black gold standard 40-pin expansion ports AX (2.54mm pitch), wherein the IO port 34, a 5V power supply path, 3.3V power supply 2-way, 3-way GND. Two expansion modules can be connected simultaneously, for example, 4.3 inch TFT modules and AD / DA module expansion modules. ?
- JTAG port reserved, the FPGA can debug and curing process. ?
- 1 way Micro? SD slot, supports SPI mode. ?
- A 6 digital to be 6-digit dynamic display. ?

two, power supply

AX309 development board, with the MINI? Development board USB cable through the USB connection with the PC USB power supply switch key, power may be a development board. Development board power supply design diagram is as follows: ?



?

Figure 2.1 Schematic of the power connector part?

?

Development board with USB power? LDO power by two chip generates + 3.3V, + 1.2V two power supplies meet BANK core voltage and the voltage of the FPGA. ?

We design the PCB when the 4-layer PCB, reserved independent GND layer, so that the entire development board having a complete ground plane to ensure that the boards having very good stability. We reserve the PCB test points of each power supply, so that the user check the voltage board. ?

? ?

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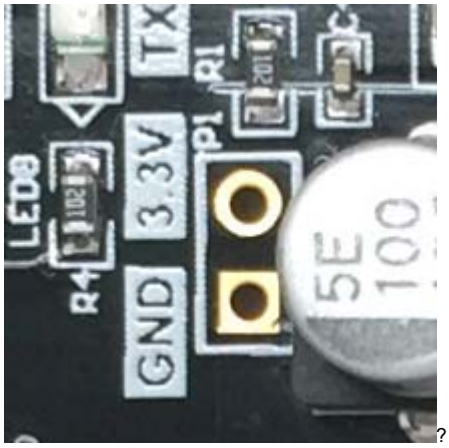

?

Figure 2.2? Power supply test points in the physical map?

three, FPGA

It has been introduced the, FPGA model we use is XC6SLX9-2FTG256C, belonging to the Xilinx Spartan-6 product. This model is a BGA package, 256 pins. Once again at the definition of FPGA pins. Many people use FPGA are non-BGA package, such as 144-pin, 208-pin FPGA chip, they are defined by the pin numbers, for example 1 to 144,1 to 208, etc., and when we use the BGA package after the chip, pin name changed from **Letters + numbers** Form, such as E3, G3, etc., so when we look at the schematic, see **letter + digital** This form is to represent the pins of the FPGA. Having this, we look at a relationship with the function of each part of the FPGA. FIG 3.1 FPGA chip development board is a pictorial diagram used. ?

?

Figure 3.1? FPGA chip in kind?

1) JTAG interface

First of all us FPGA configuration and debugging interface: JTAG interface. JTAG interface is the role of the compiled Cheng

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Order (.bit) downloaded to the FPGA or the FLASH configuration program (.mcs) downloaded to SPI? FLASH, Bit file download to FPGA, will be lost after power-down, power needs to re-download can. But after the MCS file downloaded to FLASH, after power-down is not lost, after re-power FPGA reads the configuration file and run the FLASH. ?

Figure 3.2 is a schematic diagram of part of the JTAG port, which involves TCK, TDO, TMS, TDI four signals. Four signals ohmic resistor 33 connected to the JTAG connector, protect the FPGA chip by leads extending through the FPGA. ?

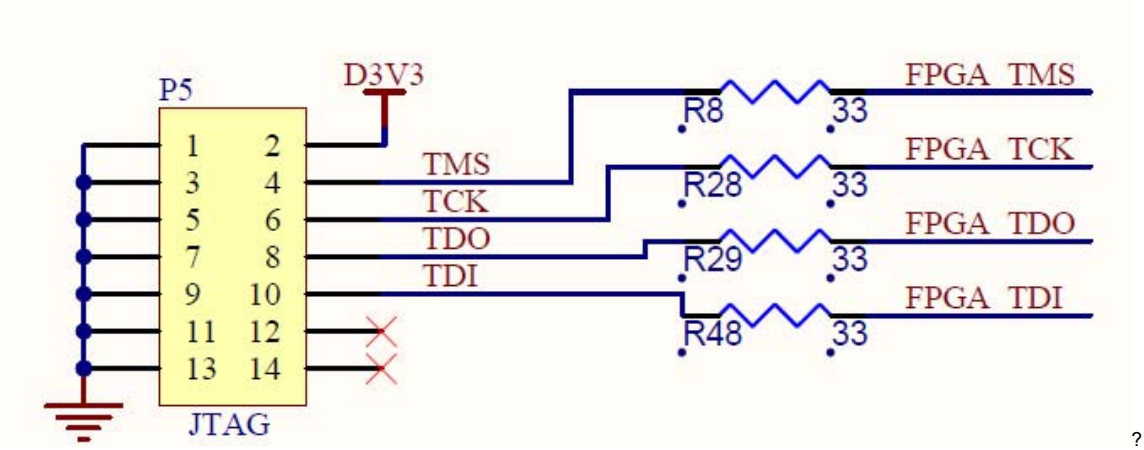

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Figure 3.2? Schematic JTAG interface part?

Using a 2.0mm standard JTAG interface 14 pin connector, FIG. 3.3 is a development board JTAG interface physical map?

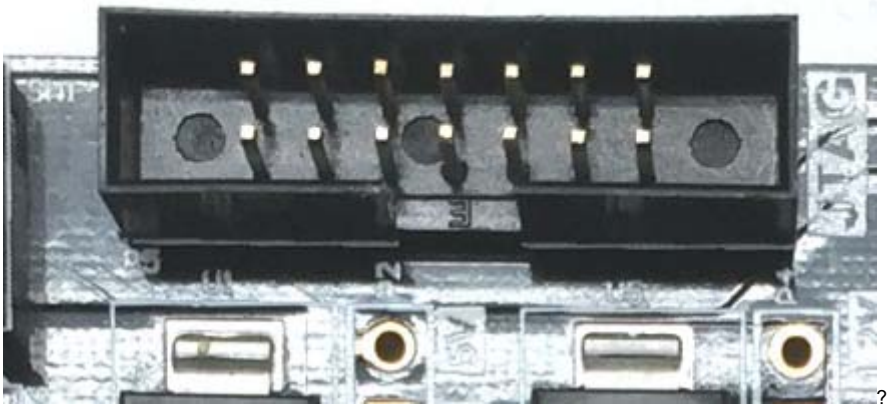

?

Figure 3.3? JTAG interface to the physical map?

?

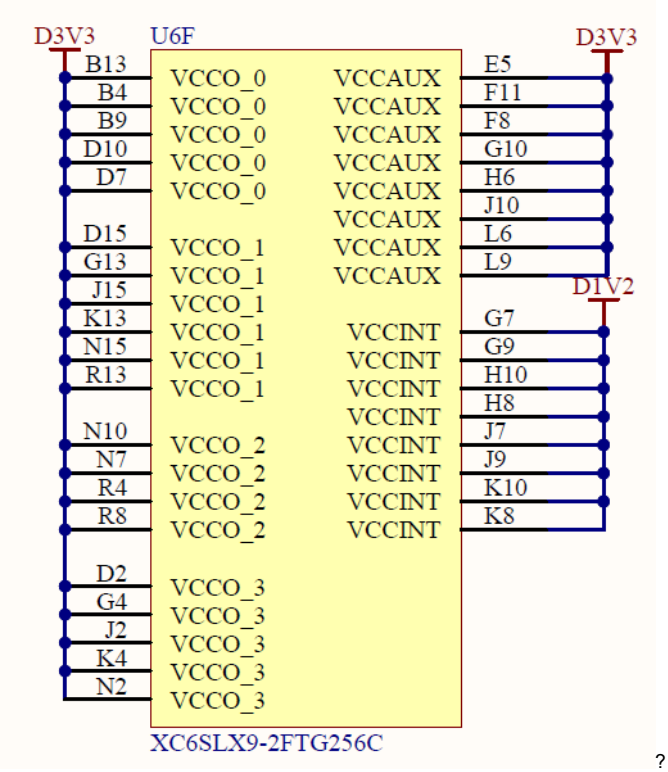
2) FPGA Power and GND Pin

Next, we talk about FPGA power pin portion, wherein each bank includes a power pin, the core pin voltage and auxiliary voltage pin, the VCCINT supply pins for the FPGA core, then 1.2V; VCCAUX the FPGA auxiliary power pin, 3.3V or 2.5V ,? can take our pick here is 3.3V ;? VCCIO supply voltage of each of the FPGA BANK, which is BANK0 VCCIO0 supply pins of the FPGA, empathy, VCCIO1 ~? VCCIO3 respectively the FPGA is BANK ~ BANK3 supply pin, the development board, are connected to the VCCIO voltage of 3.3V, that is to say, this opening

? ?

?

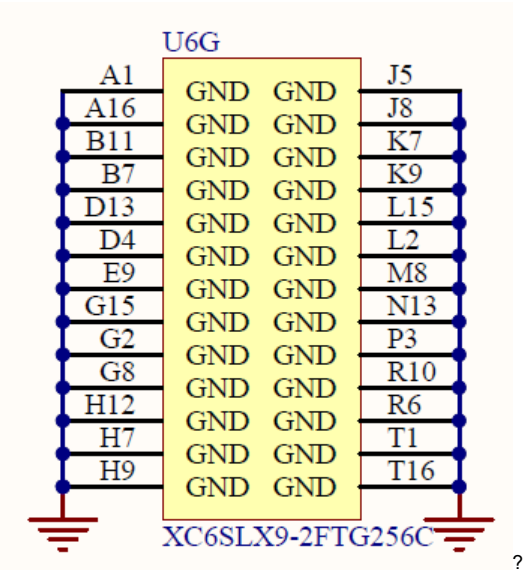
FPGA development board input and output pins are 3.3V. FIG connector shown in Figure 3.4. ?



?

Figure 3.4? FPGA power pins?

Further, FPGA requires many pins connect GND, to ensure a smooth FPGA internal ground reference. Connected to the FPGA GND, shown in Figure 3.5. ?



?

Figure 3.5? FPGA? GND pin?

?

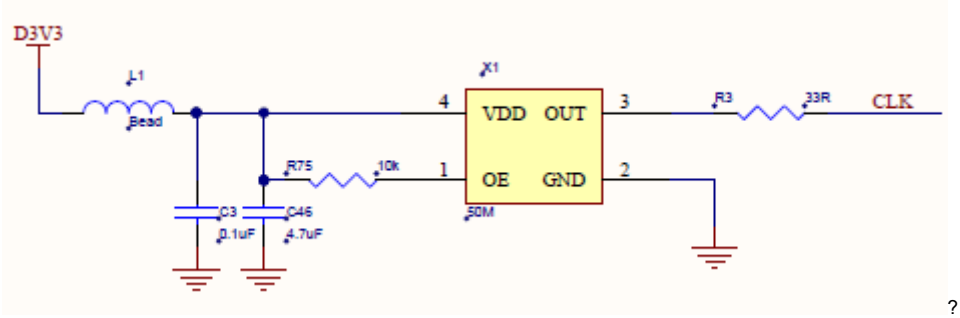
four, 50M active crystal

Figure 4.1 is the development board us to provide the above-mentioned clock source 50M Active crystal oscillator circuit. The oscillator output is connected to the FPGA global clock (GCLK? Pin? T8), it can be used to drive the GCLK in FPGA logic for user, the user

?

? ?

May be achieved by a higher clock arranged inside the FPGA PLLs and DCMs. ?



?

Figure 4.1? 50M active crystal?

Figure 4.2 is active crystal physical map?

?

?

Figure 4.2? 50M active crystal physical map?

Clock pin assignment:

Pin Name	FPGA pin
CLK	T8?

?

Fives, QSPI Flash

Development board using a piece of 16Mbit sizes SPI? FLASH chip, model M25P16, which uses 3.3V? CMOS voltage standard. Because of its non-volatile characteristic, in use,? SPI? FLASH FPGA as the system boot image. These images include the FPGA bit file? Soft-core application code, and other user data files. ?

SPI? FLASH specific model and related parameters in Table 5.1. ?

Tag	Chip Type	capacity	factory
U8	M25P16?	16M? Bit?	ST?

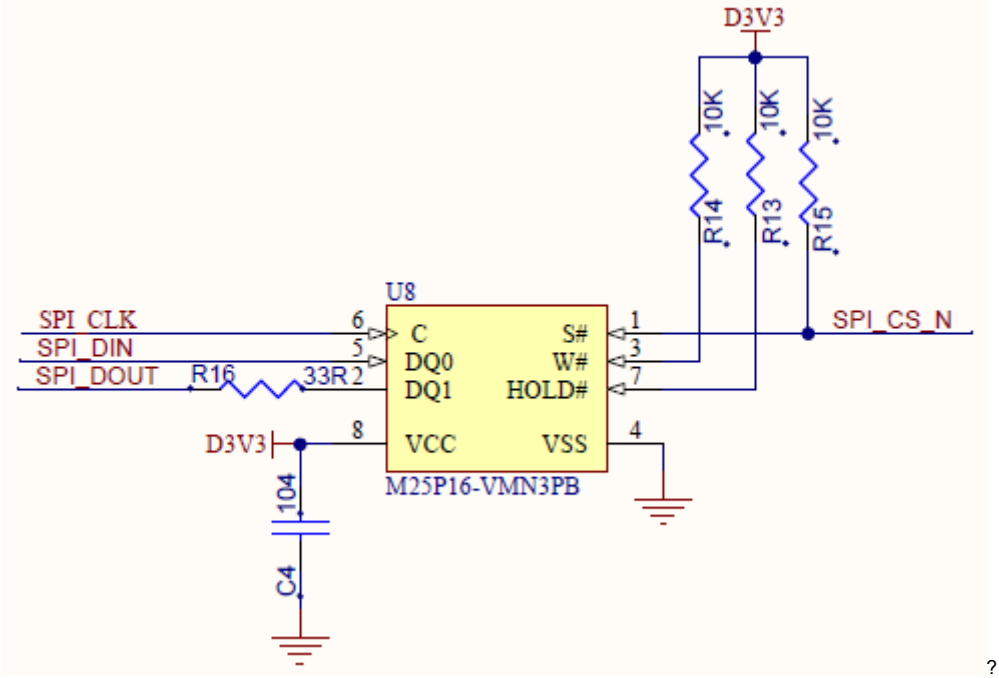
Table 5.1? SPI? Flash models and parameters?

??

? ?

?

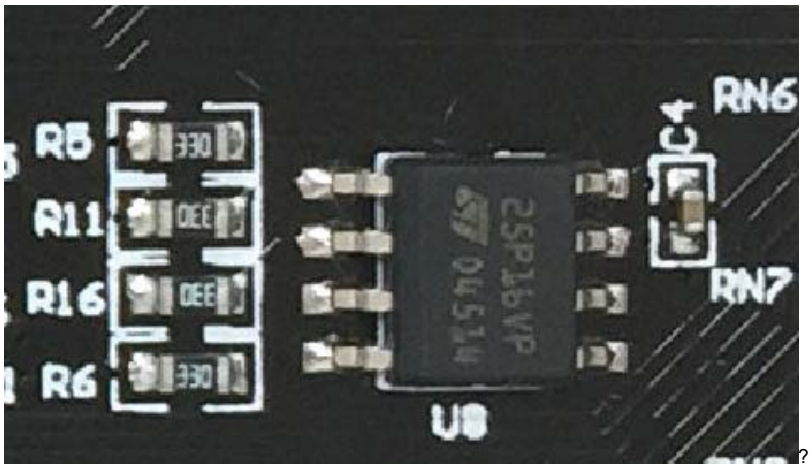
SPI? Flash schematic diagram shown in Figure 5.2,?



?

Figure 5.2? SPI? Flash connection diagram?

SPI? Flash hardware physical map, shown in Figure 5.3?



?

Figure 5.3? SPI? Flash physical map?

Configure the chip pin assignments:

Pin Name	FPGA pin
SPI_CLK	R11?
SPI_CS_N	T3?
SPI_DIN	T10?
SPI_DOUT	P10?

six, SDRAM

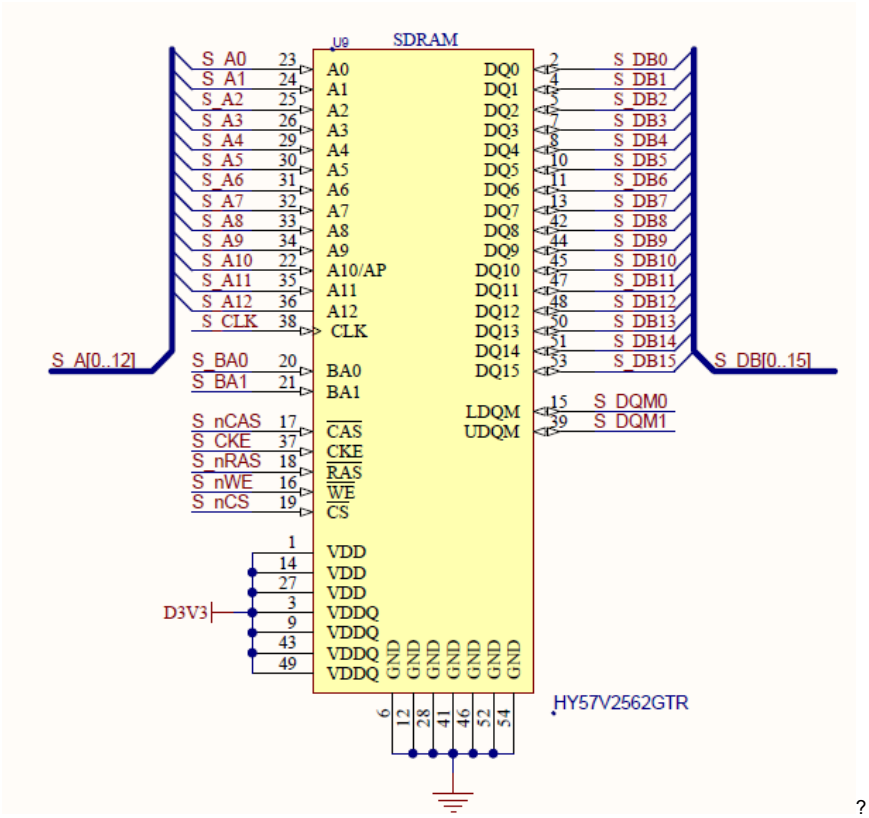
A development board onboard SDRAM chip, model: HY57V2562GTR, Capacity: 256Mbit (16M * 16bit),

?

? ?

16bit bus. SDRAM data cache may be used, such as the camera collects data, temporarily stored in the SDRAM, and then displayed by the VGA interface. There SDRAM is used for data cache. ?

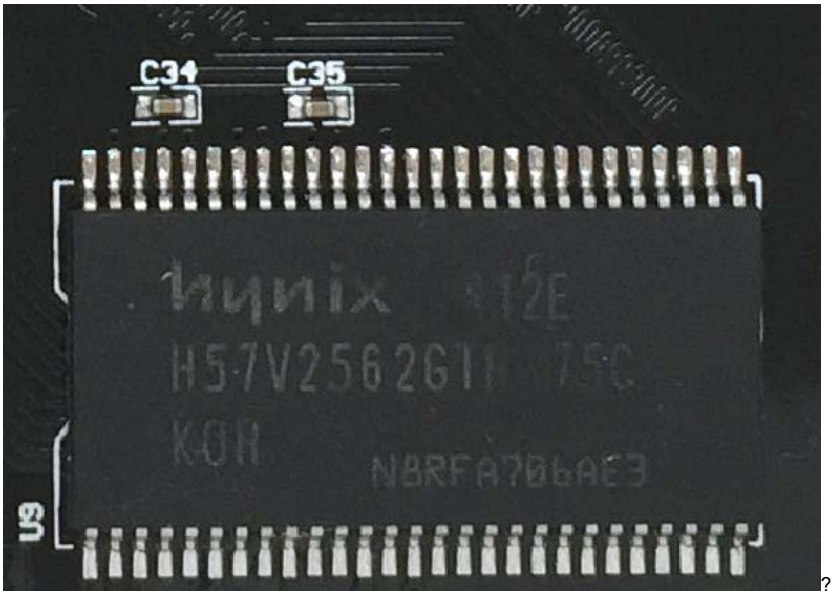
SDRAM hardware connections shown in Figure 6.1?



?

Figure 6.1? DDR3? DRAM schematic section?

Figure 6.2 is DDR3? DRAM physical map?



?

Figure 6.2? DDR3? DRAM physical map?

? ?

?

DDR3 DRAM pin assignments:

Pin Name	FPGA pin
S_CLK	H4?
S_CKE	H2?
S_NCS	G1?
S_NWE	E1?
S_NCAS	F2?
S_NRAS	F1?
S_DQM <0>	E2?
S_DQM <1>	H1?
S_BA <0>	G6?
S_BA <1>	J6?
S_A <0>	J3?
S_A <1>	J4?
S_A <2>	K3?
S_A <3>	K5?
S_A <4>	P1?
S_A <5>	N1?
S_A <6>	M2?
S_A <7>	M1?
S_A <8>	L1?
S_A <9>	K2?
S_A <10>	K6?
S_A <11>	K1?
S_A <12>	J1?
S_DB <0>	A3?
S_DB <1>	B3?
S_DB <2>	A2?
S_DB <3>	B2?
S_DB <4>	B1?
S_DB <5>	C2?
S_DB <6>	C1?

?

?

?

S_DB <7>	D1?
S_DB <8>	H5?
S_DB <9>	G5?
S_DB <10>	H3?
S_DB <11>	F6?
S_DB <12>	G3?
S_DB <13>	F5?
S_DB <14>	F3?
S_DB <15>	F4?

?

Seven, EEPROM 24LC04

Development of an On-board EEPROM, model 24LC04, capacity: 4Kbit (2 * 256 * 8bit), a block composed of two 256byte, communicate via IIC bus. On-board EEPROM is to learn communication IIC bus. EEPROM is generally used in instruments, such as design, as some of the storage parameters, non-volatile. The chip is simple to operate, highly cost-effective, so although the capacity is high, but the price is very cheap, the cost for those demanding products, is a good choice. Figure 7.1 is a schematic of EEPROM?

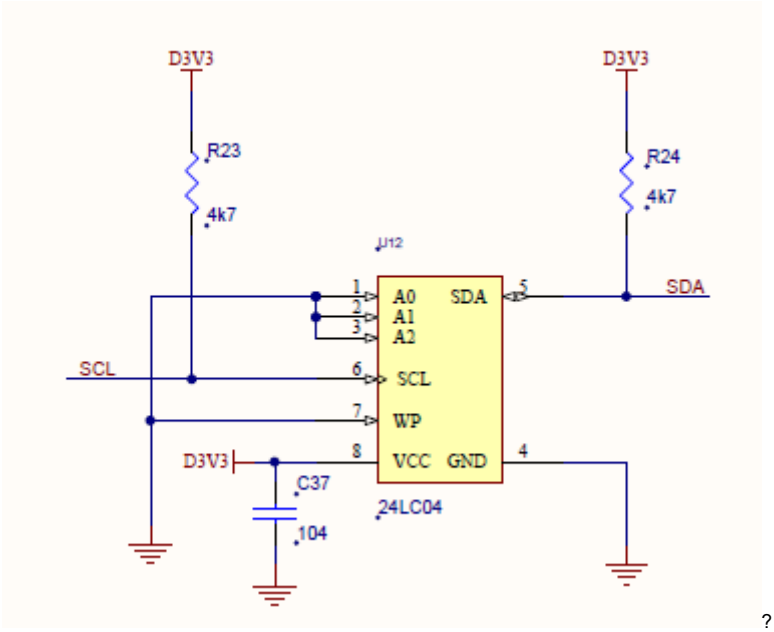


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Figure 7.1? EEPROM schematic section?

Figure 7.2 is EEPROM physical map?

? ?

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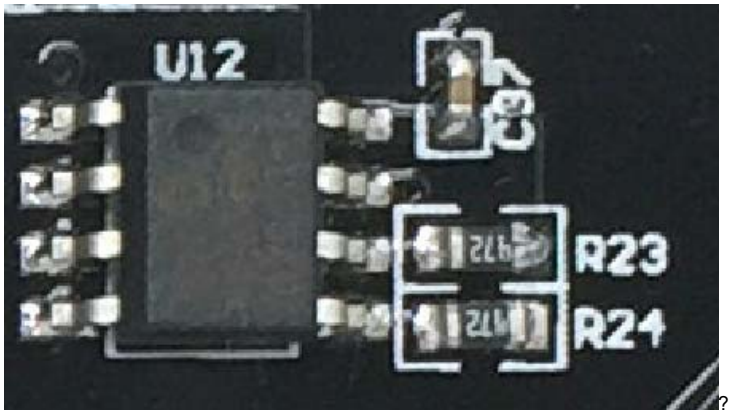

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Figure 7.2EEPROM physical map?

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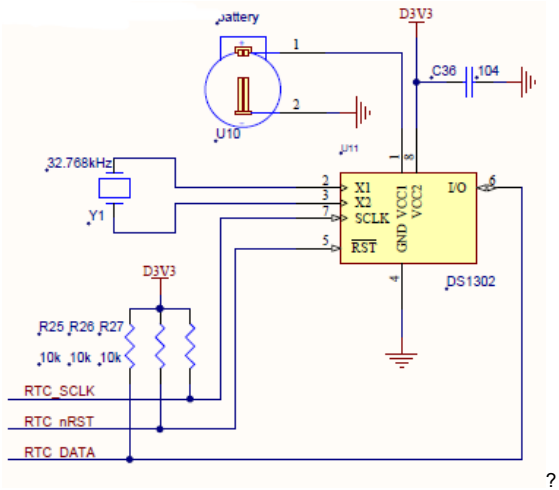
EEPROM pin assignments:

Pin Name	FPGA pin
SDA	P12?
SCL	N12?

?

Eight, DS1302 Real Time Clock

Development board onboard a real-time clock RTC chip, model DS1302, his function is to provide to the calendar year of 2099, year, month, week, day, hour there. If the system takes time, then the RTC will need to relate to the product. He needs to take a passive external clock a 32.768KHz provide accurate clock source to the clock chip, so as to allow RTC to provide accurate clock information to the product. Meanwhile, in order after the product down, real-time clock can also be run properly, with a general need another battery to power the clock chip, U7 Figure 8.1 for the battery holder, we will **button batteries (Model CR1220, 3V voltage) Placed after, when the system is out of batteries, button batteries can power supply to the DS1302, so,** regardless of whether the product powered DS1302 are running, uninterrupted, continuous time can provide information. Figure 8.1 is a schematic DS1302?



?

Figure 8.1? DS1302 schematics?

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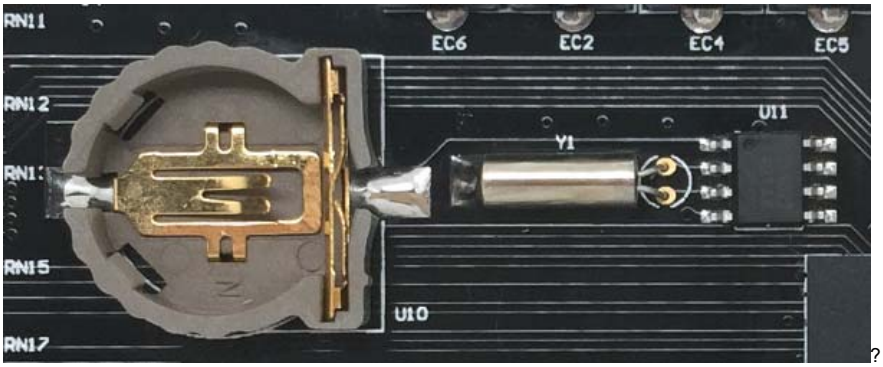
8.2 A DS1302 physical map?



?

Figure 8.2? DS1302 physical map?

DS1302 interface pin assignment:

Pin Name	FPGA pin
RTC_SCIK	E13?
RTC_nRST	C13?
RTC_DATA	D14?

nine, USB to serial

Board includes a Silicon? Labs? CP2102GM the USB-UAR chip,? USB interface using the MINI? USB interface, the USB interface, i.e. the power supply to achieve the function, the function can USB to serial port, a USB cable can be connected to it to the PC's USB port for serial data communication?.

Serial schematic diagram shown in Figure 9.1?

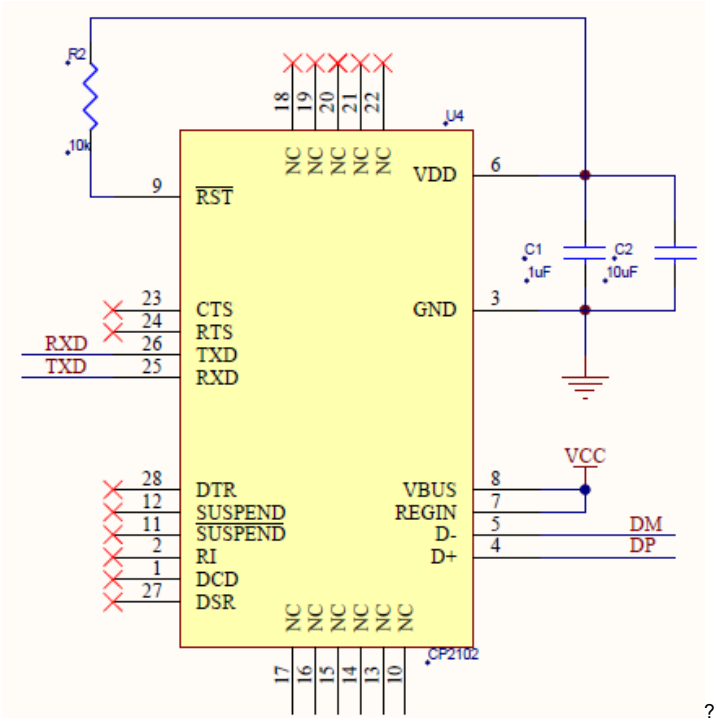


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Figure 9.1? USB to serial port schematics?

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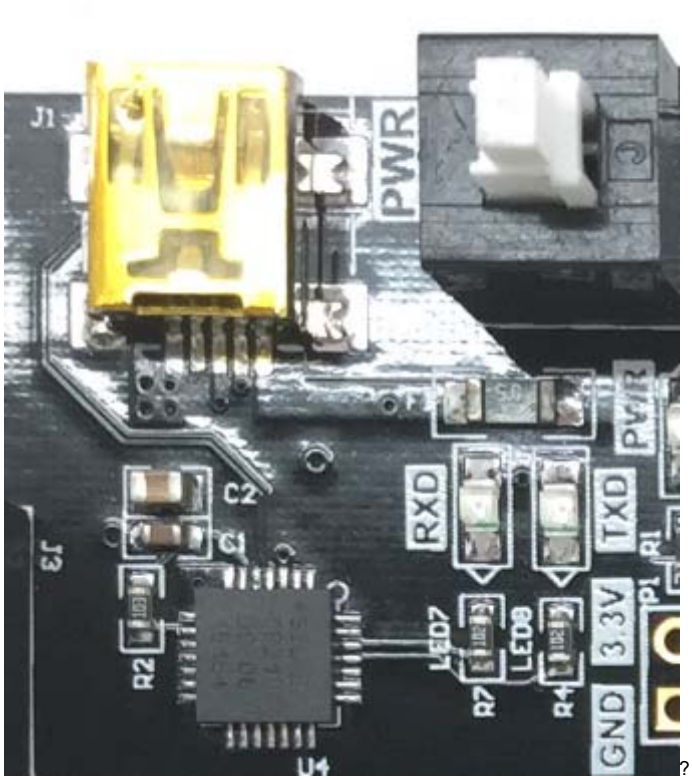
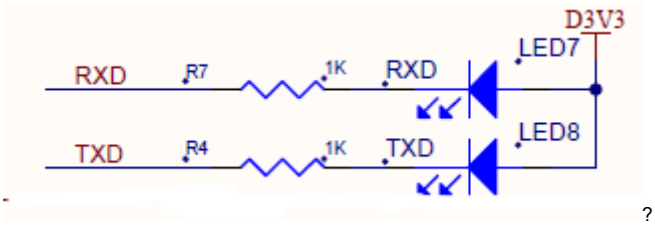
Figure 9.2 is a USB to serial physical map?



?

Figure 9.2? USB to serial physical map?

While the serial signal provided two led indicators (LED7, LED8) ,? LED7 and a serial port for LED8 data indicates whether data is sent or accepted, shown in Figure 9.3,?



?

Figure 9.3? USB-to-serial signal indicator?

?

Serial port pin assignments:

Pin Name	FPGA pin
RXD	C11?
TXD	D12?

?

ten, VGA Interface

Speaking VGA port, I believe many of my friends are not unfamiliar, because this is the most important interfaces on the computer monitor interfaces, starting with a huge block header CRT monitor era, VGA interface is being used, and has been in use ever since, in addition to VGA interface also It is referred to as D-Sub connector. ?

?

? ?

VGA interface is a D-type interface, the above pinhole 15, divided into three rows of five. 3 is a more important RGB component signal and two color scanning synchronization signal HSYNC and VSYNC pin. ?

Pins 2, 3 are the three primary colors red, green and blue analog voltage is 0 ~ 0.714V peak-peak (peak - peak)?, 0V representative of a colorless, 0.714V representative of full colors. Some non-standard display using? 1Vpp full-color level. ?

Trichromatic source and termination resistors are 75 ohms. Figure 10.1?

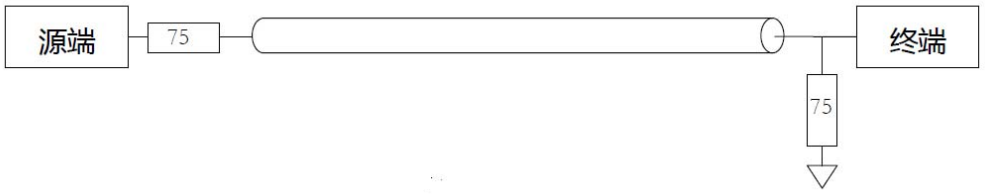


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FIG 10.1? VGA video signal transmission schematic?

HSYNC and VSYNC line data are data synchronization and frame synchronization, the TTL level. FPGA can output a digital signal, and the VGA required R, G, B analog signals, digital signals to analog VGA is implemented by a simple resistive circuit. The resistor circuit 32 may generate a gradient levels of red and blue signal level gradient and 64 green signal (RGB? 5-6-5), VGA interface portion circuit as shown in FIG 10.2?

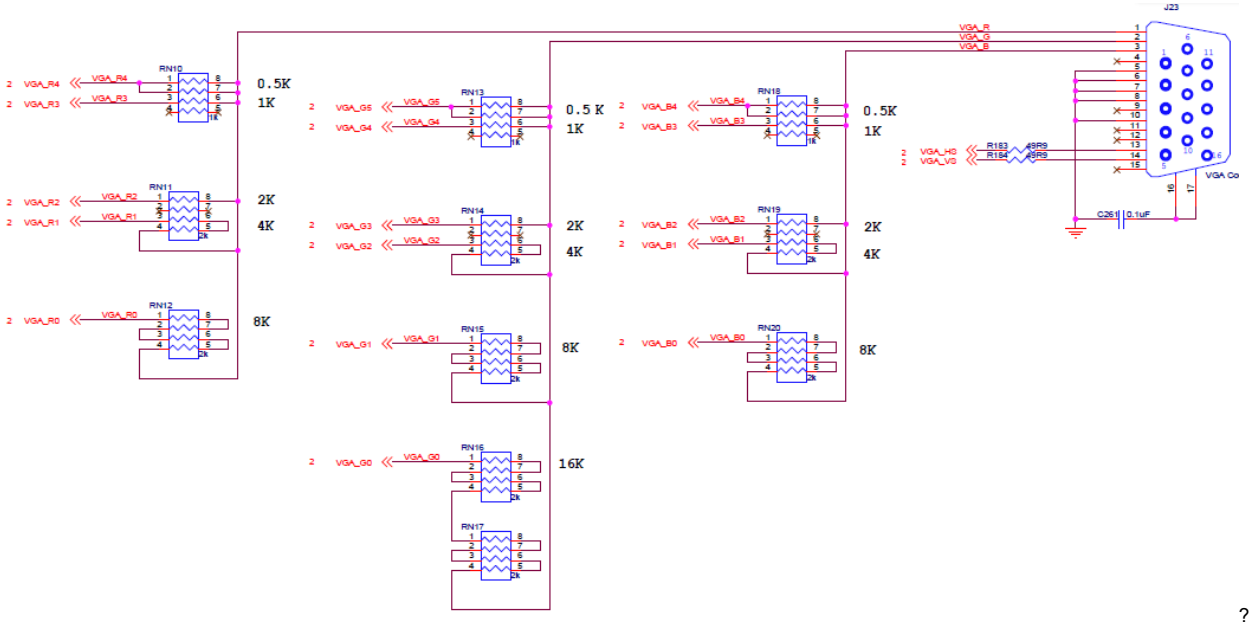

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Figure 10.2? VGA interface portion of the schematic?

Figure 10.3 is a VGA port physical map?

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10.3? VGA Interface physical map?

? ?

?

VGA connector pin assignment?

Pin Name	FPGA pin	Remark
VGA_D <0>	P7?	BLUE <0>?
VGA_D <1>	M7?	BLUE <1>?
VGA_D <2>	P8?	BLUE <2>?
VGA_D <3>	N8?	BLUE <3>?
VGA_D <4>	L7?	BLUE <4>?
VGA_D <5>	M9?	GREEN <0>?
VGA_D <6>	N9?	GREEN <1>?
VGA_D <7>	P9?	GREEN <2>?
VGA_D <8>	L10?	GREEN <3>?
VGA_D <9>	M10?	GREEN <4>?
VGA_D <10>	P11?	GREEN <5>?
VGA_D <11>	M11?	RED <0>?
VGA_D <12>	M12?	RED <1>?
VGA_D <13>	L12?	RED <2>?
VGA_D <14>	N14?	RED <3>?
VGA_D <15>	M13?	RED <4>?
VGA_HS	M14?	Line synchronization signal?
VGA_VS	L13?	And vertical sync signals?

?

eleven, SD card slot

SD card (Secure? Digital? Memory? Card) is a technology based on semiconductor flash memory cards, conducted in 1999 by the Japanese Panasonic-led concept, participants Toshiba and American SanDisk Corporation essence of R & D and complete. In 2000 these companies initiated the establishment of the SD Association (Secure? Digital? Association referred SDA), a strong, attracting a large number of companies to participate. These include IBM, Microsoft, Motorola, NEC, Samsung and so on. Driven by these leading manufacturers, SD card consumer digital equipment has become the most widely used kind of memory card. ?

SD cards are now very commonly used storage devices, we extend out of the SD card, supports SPI mode, the SD card MicroSD card. Figure 11.1 shows the principle of FIG. ?

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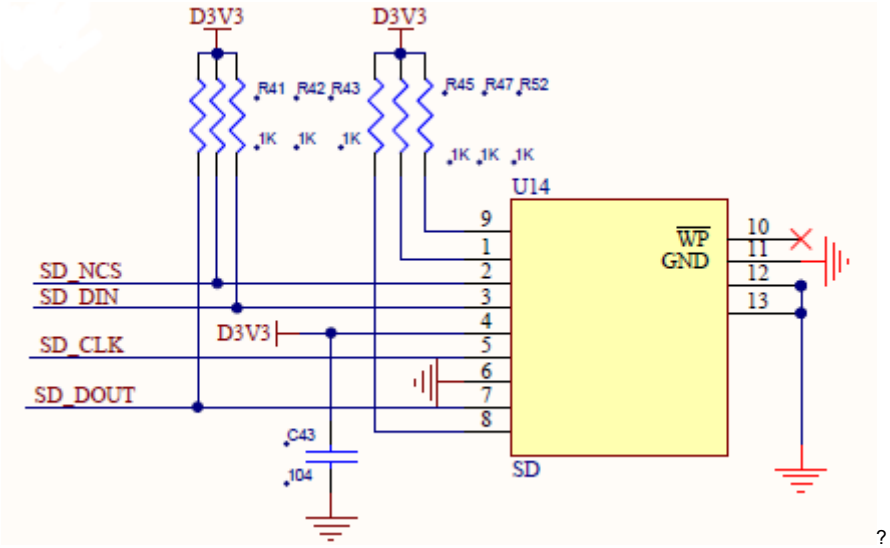

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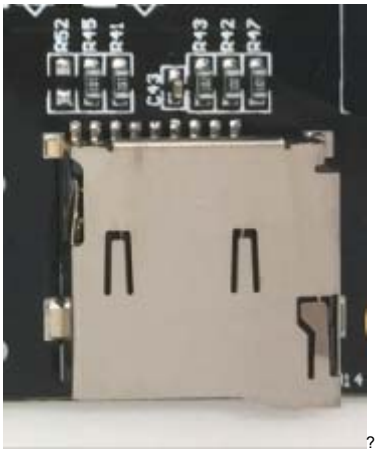
Figure 11.1? SD card slot schematics?

Figure 11.2? SD card slot physical map?



?

Figure 11.2? SD card slot physical map?

SD card slot pin assignment

SD mode	
Pin Name	FPGA pin?
SD_NCS	N3?
SD_DIN	L5?
SD_CLK	M3?
SD_DOUT	L4?

?

twelve, led

On-board development of a light-emitting diode LED 4 users. 4 user LED schematics FIG portion 12.1, when the FPGA pin output is a logic 0, turns off LED. Output is a logic 1, LED is illuminated. ?

? ?

?

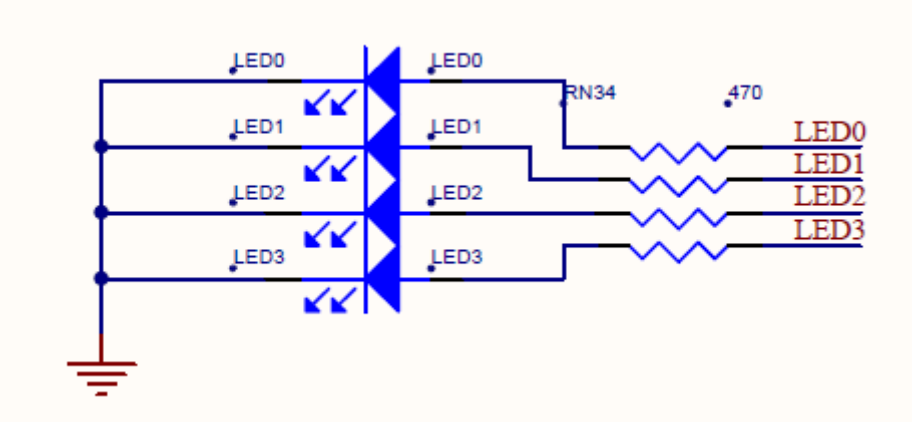


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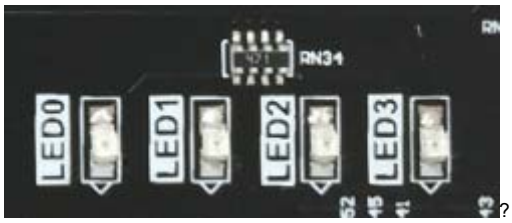
Figure 12.1? LED user schematics?

Figure 12.2 LED physical map?



?

Figure 12.2?? 4? LED physical map?

LED pin assignments:

Pin Name	FPGA pin
LED <0>	P4?
LED <1>	N5?
LED <2>	P5?
LED <3>	M6?

?

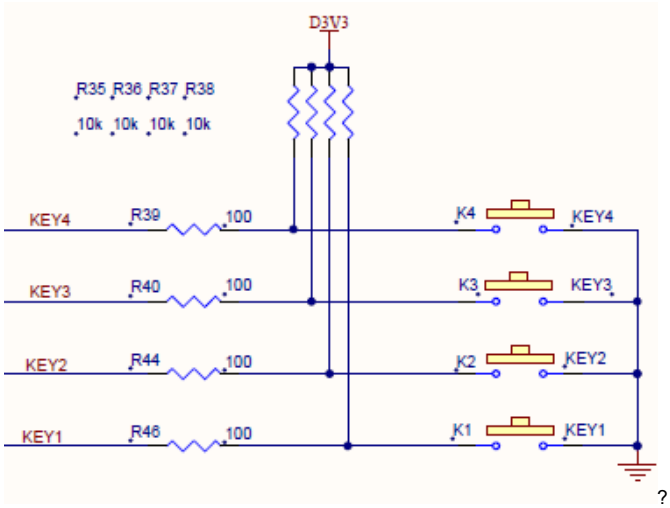
thirteen, button

On-board development of six independent buttons, four user keys (KEY1 ~ KEY4), 2 function keys (PROG and RESET).

Keys are active low , Four user keys schematic diagram shown in Figure 13.1?

?

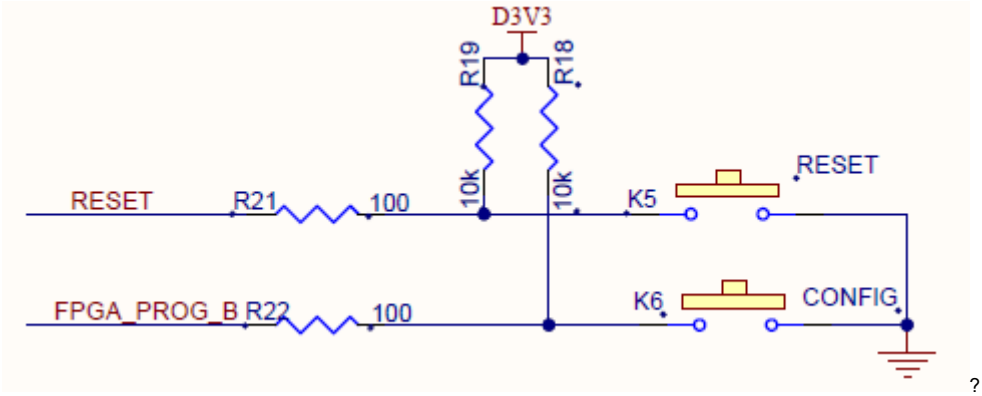
? ?



?

Figure 13.1? 4 user keys schematics?

Principle two function keys is shown in Figure 13.2,? Wherein the FPGA program is connected to the Reset button for normal IO reset FPGA, the FPGA connected to the CONFIG button FPGA_PROGRAM_B dedicated pins for reconfiguring the FPGA program. ?

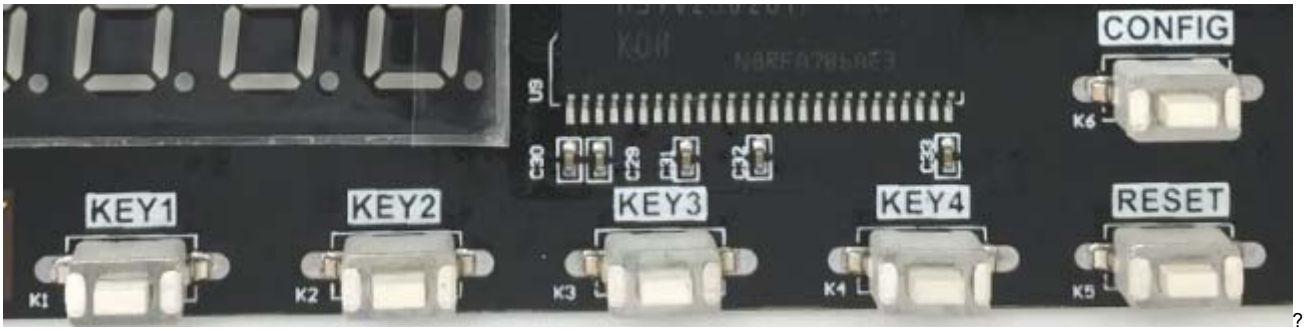


?

Figure 13.2? 2 function keys schematics?

?

Figure 13.3 is? 6 independent key physical map?



?

Figure 13.3? 6 independent key physical map?

Button pin assignments:

Key Name	FPGA pin	Key label
KEY1	C3?	KEY? 1?

? ?

?

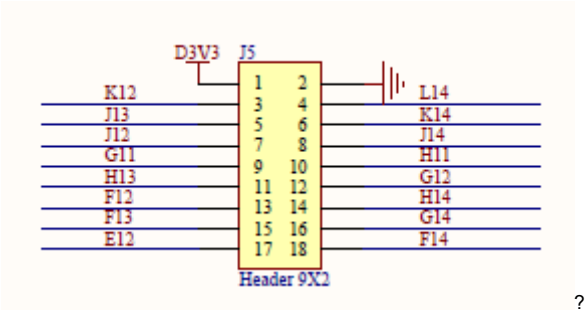
KEY2	D3?	KEY? 2?
KEY3	E4?	KEY? 3?
KEY4	E3?	KEY? 4?
RESET	L3?	KEY6?
PROG	T2?	KEY5?

?

fourteen, Camera Interface

Board includes a 18-pin CMOS camera interface, the camera module can be connected OV7670 and OV5640 camera module, video capture function can be realized, after collection, may be displayed by a TFT LCD display or VGA interface. OV7670,30W pixel output resolution of 640 * 480;? OV5640,500W pixel output resolution up to 2592 * 1944. Selected on the camera, the user can purchase according to their actual needs. ?

CMOS camera interface schematic diagram of Figure 14.1 shows?



?

Figure 14.1? Camera interface schematics?

Physical map shown in FIG 14.2 (**The camera module is optional**)?


?

Figure 14.2? Camera interface physical map?

Camera Interface pin assignment:

Pin Name	FPGA pin
CMOS_SCLK	K12?

?

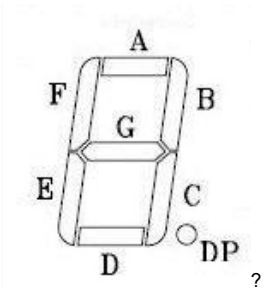
? ?

CMOS_SDAT	L14?
CMOS_VSYNC	J13?
CMOS_HREF	K14?
CMOS_PCLK	J12?
CMOS_XCLK	J14?
CMOS_D <7>	G11?
CMOS_D <6>	H11?
CMOS_D <5>	H13?
CMOS_D <4>	G12?
CMOS_D <3>	F12?
CMOS_D <2>	H14?
CMOS_D <1>	F13?
CMOS_D <0>	G14?
CMOS_RESET	E12?
CMOS_PWDN	F14?

?

fifteen, Digital Tube

LED is a very common type of display device, generally divided into seven segments and eight digital tube, distinction being made between eight digital tube than a "point" than the seven-segment LED. We use digital as six one eight digital tube, digital tube segment structure of 15.1?



?

Figure 15.1? Segment digital tube structure?

We are using a common anode digital tube, When a field corresponding to the pin is low, the corresponding field on the light, when a field corresponding to the pin is high, the corresponding field is not bright . ?

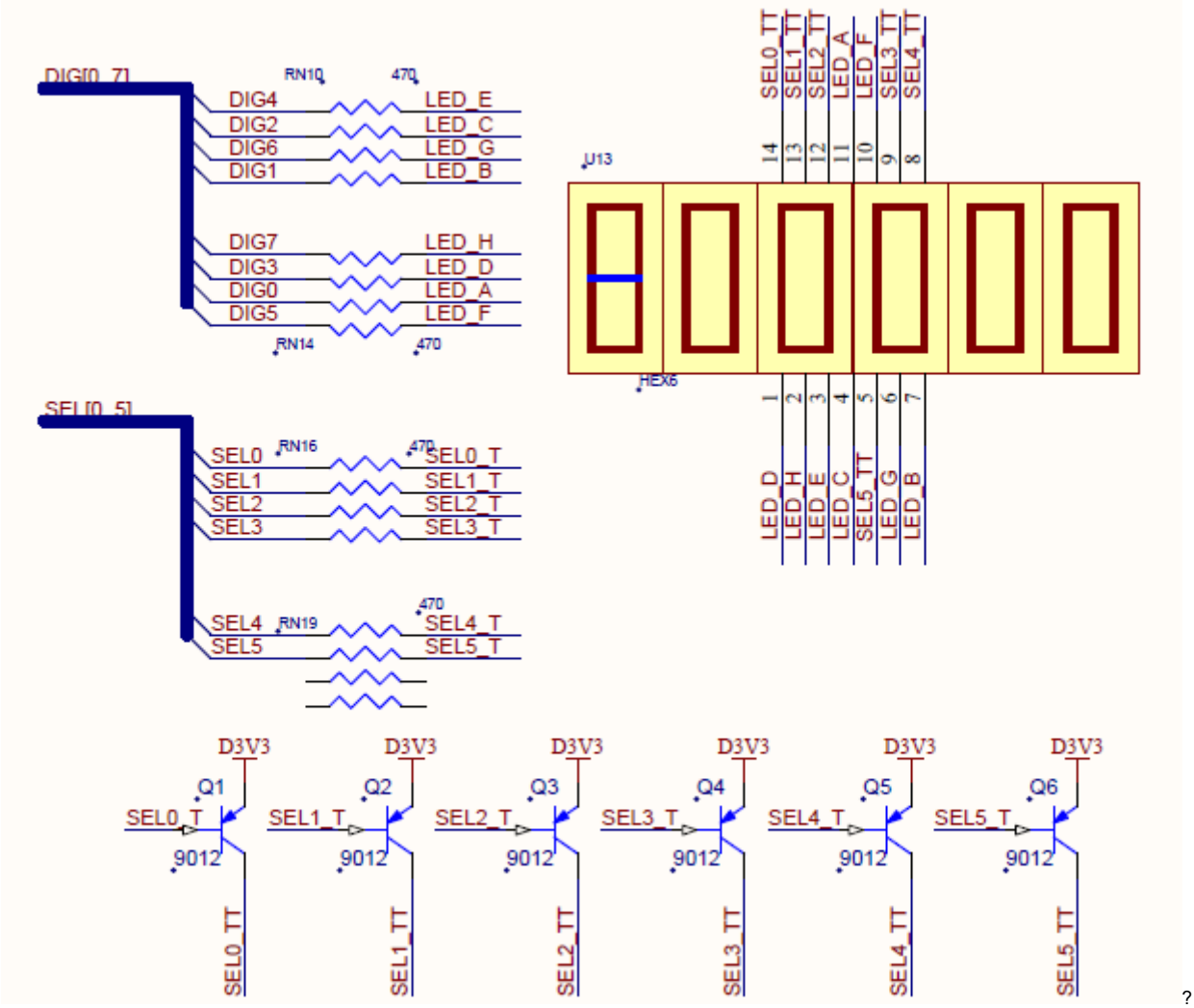
Having the above diagram, we look at the design of our development board. ?

Six in One digital tube display is part of a dynamic, because the human visual persistence of the phenomenon and Yu Hui effects of light-emitting diodes, despite the fact that not everybody LED lights at the same time, but as long as the scan speed is fast enough, giving the impression that a group of stable display data, there will be no light flashes. ?

? ?

?

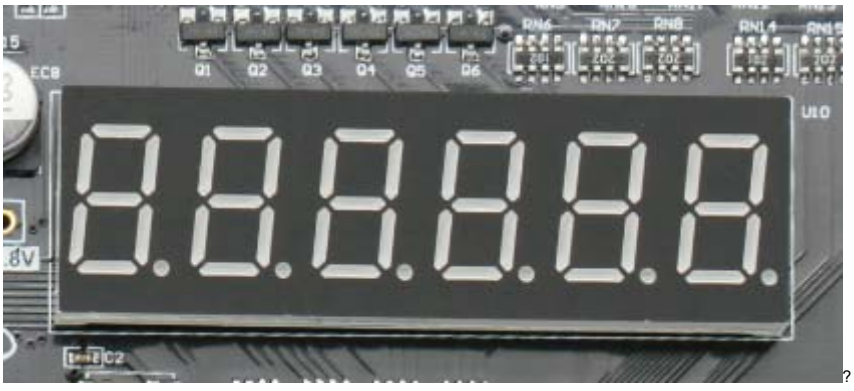
Six same segment are integrally connected to the digital together, a total of 8 pins, then add 6 control signal pins, a total of 14 pins, as shown in FIG 15.2, wherein DIG [0. .7] a corresponding digital tube, B, C, D, E, F, G, H (i.e., point DP); SEL [0..5] is six six digital control pins, and also low effective level, when the control pin is low, with the corresponding LED supply voltage, so that LED to light up, or segment regardless of how changes in the digital control, fails to ignite the corresponding LED. ?



?

Figure 15.2? Digital schematics?

Figure 15.3 for the digital physical map?



?

Figure 15.3? LED physical map?

?

?

?

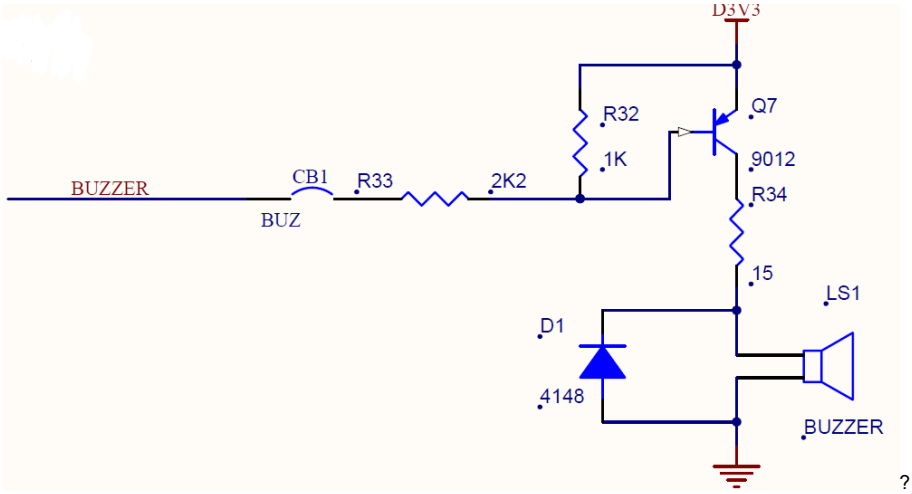
?

Digital pin assignment?

Pin Name	FPGA pin	Remark
DIG [0]	C7?	Corresponding segments of A?
DIG [1]	E6?	The corresponding segment B?
DIG [2]	C5?	Corresponding to the segment C?
DIG [3]	F7?	Corresponding segments D?
DIG [4]	D6?	The corresponding segment E?
DIG [5]	E7?	Corresponding segments F?
DIG [6]	D5?	The corresponding section G?
DIG [7]	C6?	The corresponding point DP?
SEL [0]	D8?	From the number of the first LED to the right?
SEL [1]	E8?	The second digital number from the right?
SEL [2]	F9?	The third digital number from the right?
SEL [3]	F10?	The fourth digital number from the right?
SEL [4]	E10?	The fifth number of digital tube from the right?
SEL [5]	D9?	From the right number of digital tube sixth?

sixteen, buzzer

Buzzer much explanation, we design time, by controlling a transistor, when a low level, the transistor is turned on, buzzer; if high, the transistor is turned off, the buzzer does not sound; **For convenience, we've added a jumper cap (CB1) between the buzzer with FPGA, if annoying buzzer, can jump cap can be removed** . Schematic in Figure 16.1?



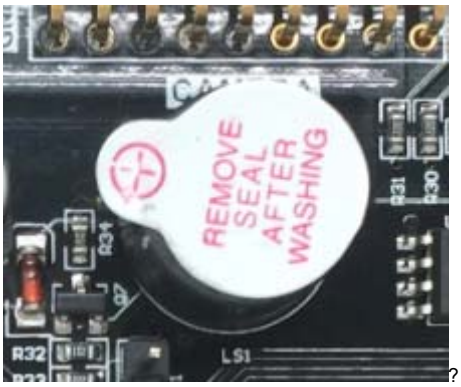
?

Figure 16.1? Buzzer schematics?

? ?

?

Figure 16.2 is a pictorial diagram of the buzzer, the buzzer yellow jumper connector pins and FPGA, if the buzzer does not want, to unplug. ?



?

Figure 16.2? Buzzer schematics?

Buzzer pin assignments:

Pin Name	FPGA pin
BUZZER	J11?

XVII Expansion port

Development board aside two expansion port, expansion port 40 signal, wherein, 5V supply channel 1, 3.3V power supply 2-way, 3-way manner, the IO port 34 passage. These are independent IO port IO port, no multiplexing with other devices. IO port is connected to the FPGA pin level is 3.3V. **Never directly with 5V devices are directly connected, so as not to burn the FPGA. If the device to be connected to 5V, then the level conversion chip requires.**

Between the expansion port and the FPGA 33 ohm connected in series with the exclusion, for protecting the external voltage or current FPGA avoid damage caused by excessive, expansion port J2, J3 circuit in FIG 17.1? 17.2 As shown in?

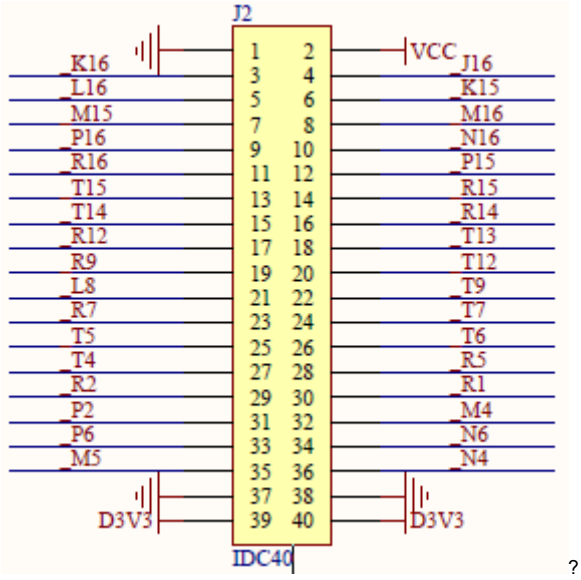


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Figure 17.1? J2 expansion port schematics?

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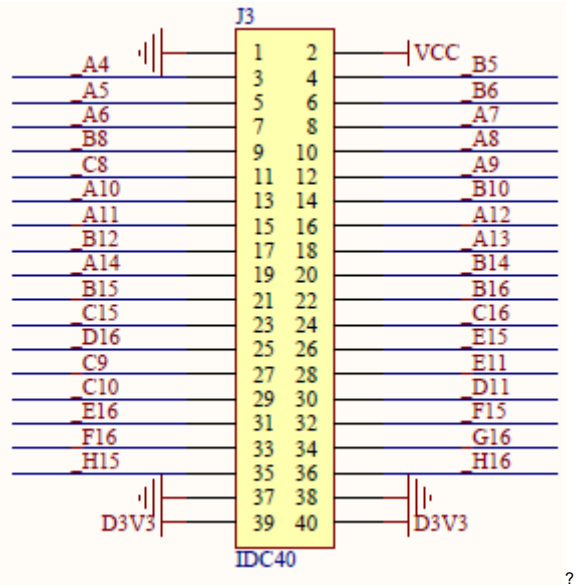

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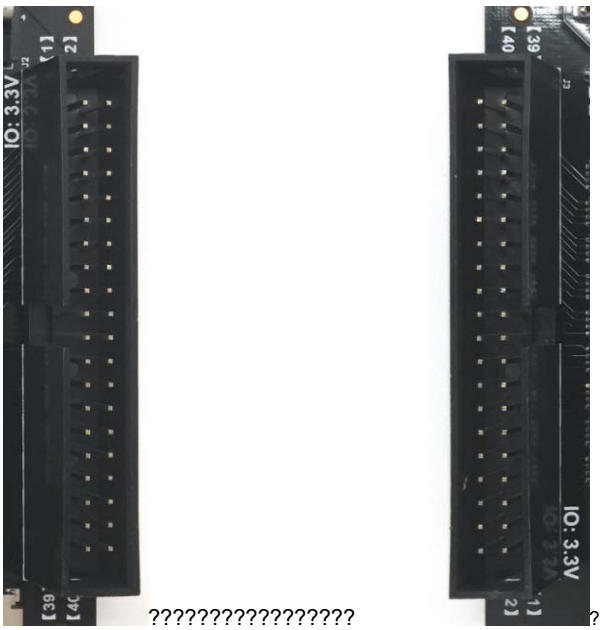
Figure 17.2? J3 expansion port schematics?

?

FIG 17.3 J2, J3 FIG physical expansion port, the expansion port Pin1, Pin2 and Pin39, Pin40 been marked out on the board. ?



?????? ??????????????????

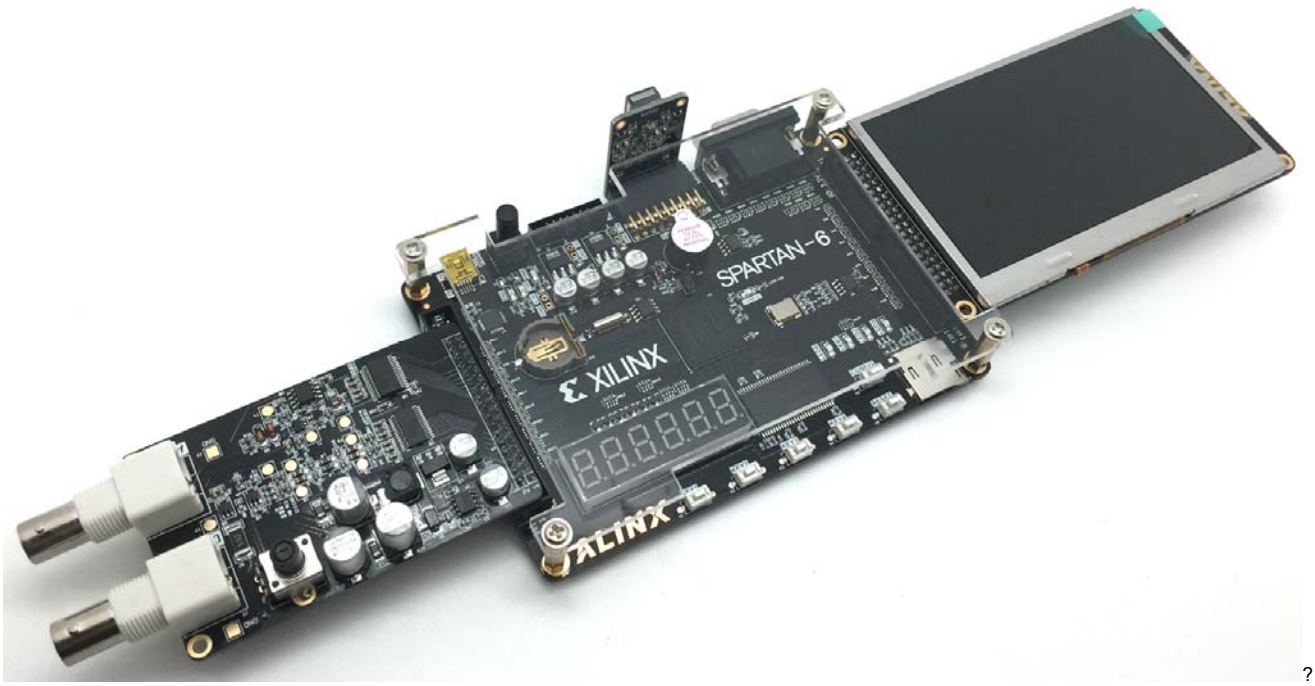
?

Figure 17.3? J2,? J3 expansion port physical map?

In this connection our expansion port expansion module, when the direction shown in Figure 17.4, 1,2 feet above the interface (note identification on PCB). ?

? ?

?



?

Figure 17.4? J3 expansion port physical map?

J2 expansion port pin assignments

Pin Number	FPGA pin	Pin Number	FPGA pin
1	GND?	**2**	VCC5V?
3	K16?	**4**	K15?
5	L16?	**6**	K15?
7	M15?	**8**	M16?
9	P16?	**10**	N16?
11	R16?	**12**	P15?
13	T15?	**14**	R15?
15	T14?	**16**	R14?
17	R12?	**18**	T13?
19	R9?	**20**	T12?
twenty one	L8?	**twenty two**	T9?
twenty three	R7?	**twenty four**	T7?
25	T5?	**26**	T6?
27	T4?	**28**	R5?
29	R1?	**30**	R2?
31	P2?	**32**	M4?
33	P6?	**34**	N6?

?

? ?

35	M5?	**36**	N4?
37	GND?	**38**	GND?
39	D3V3?	**40**	D3V3?

?

J3 expansion port pin assignments

Pin Number	FPGA pin	Pin Number	FPGA pin
1	GND?	**2**	VCC5V?
3	A4?	**4**	B5?
5	A5?	**6**	B6?
7	A6?	**8**	A7?
9	B8?	**10**	A8?
11	C8?	**12**	A9?
13	A10?	**14**	B10?
15	A11?	**16**	A12?
17	B12?	**18**	A13?
19	A14?	**20**	B14?
twenty one	B15?	**twenty two**	B16?
twenty three	C15?	**twenty four**	C16?
25	D16?	**26**	E15?
27	C9?	**28**	E11?
29	C10?	**30**	D11?
31	E16?	**32**	F15?
33	F16?	**34**	G16?
35	H15?	**36**	H16?
37	GND?	**38**	GND?
39	D3V3?	**40**	D3V3?

?

?

? ?