# ITI CMOS Analog IC Design 2024
# Lab 06
# Differential Amplifier

# Part 1: Differential Amplifier Design

1. We want to design a resistive loaded differential amplifier with the specifications below.

| **Parameter** | |
|---|---|
| **Supply ($V_{DD}$)** | ***1.8 V*** |
| **Bias Current (*Iss*)** | ***40 µA*** |
| **Deferential gain** | ***8*** |
| **CM output level** | ***$V_{DD}$/3*** |
| **Load capacitance** | ***1 pf*** |

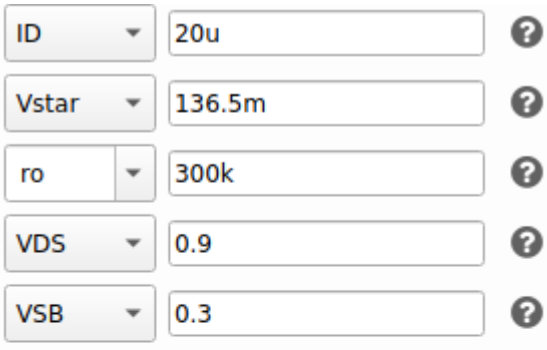
2. Since the required output level is closer to the ground rail, we will use a PMOS input stage
3. **Choose *RD*** to meet the CM output level spec. As we want CM output level = .6 V so ***Iss/2*RD=.6*** so ***RD***=30 kΩ
4. The differential amplifier gain is given by $|Av| \approx gm(RD||ro)$
5. We will choose $L$ to set $ro \gg RD \rightarrow ro = 10 * RD$

$$|Av| \approx 0.91 \times gm * RD = 0.91 \times \frac{2ID}{V*} \times RD = \frac{1.82VRD}{V*}$$

6. ***Choose*** $V*$ *to meet the differential gain spec.*

$$V* = \frac{1.82VRD}{|Av|} \; as \; VRD = .6V \; and \; |Av| = 8 \; so \; V* = 1.82 * \frac{.6}{8} = 136.5mV$$

7. Assume we will set $VDS$ of the tail current source to $300mV$ to allow more output swing. Report the input pair sizing
   - So, we need L=350 nm and W=30.33 µm to meet the above specs for input pair
8. Given the above assumption for $VDS$ of the tail current source, **calculate** the required CM input level
   - As we set $VDS$ of the tail current source = 300mV and Vgs is 940 mV so the CM input level = 1800-300-940 =560 mV

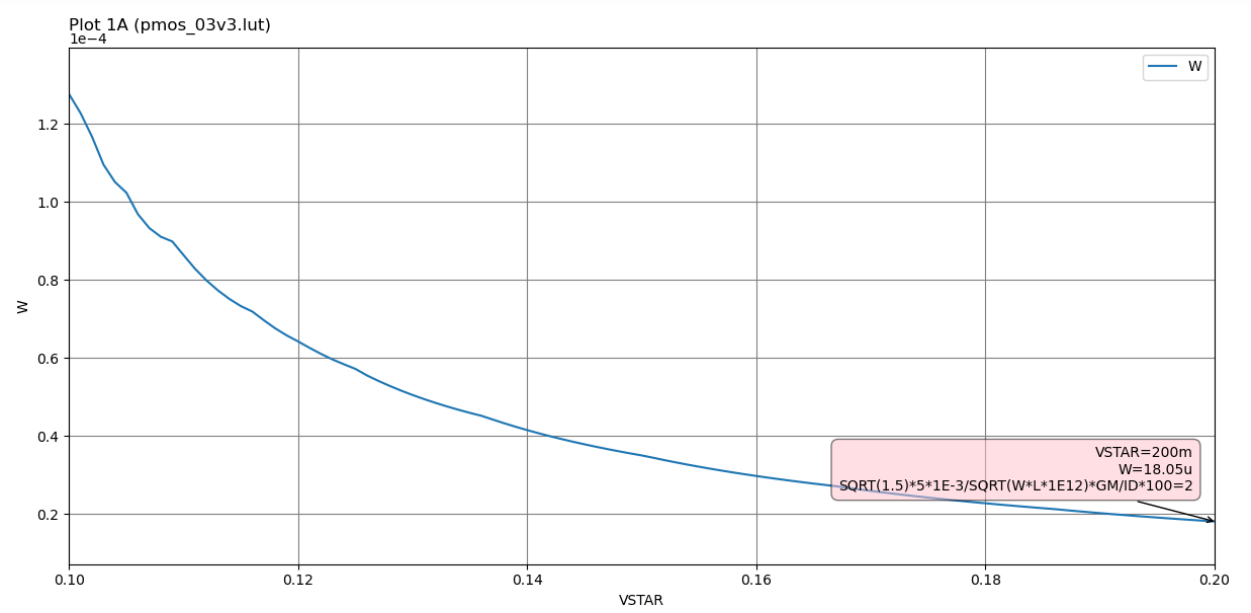


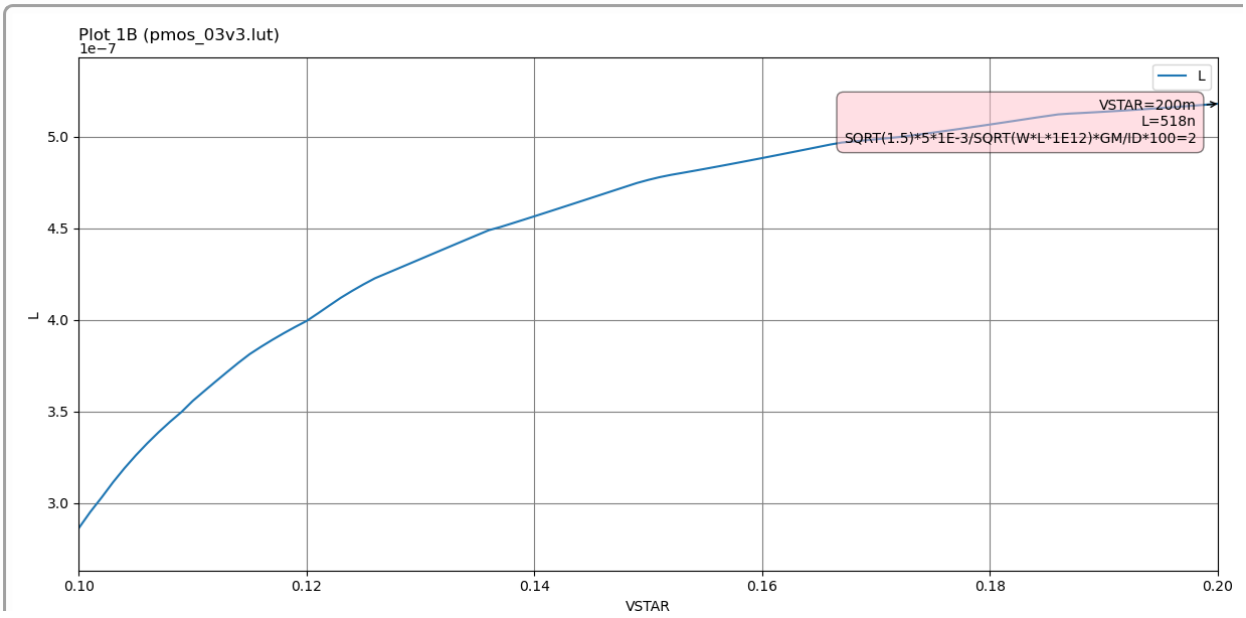

| | Name | TT-27.0 |
|---|---|---|
| 1 | ID | 20u |
| 2 | IG | N/A |
| 3 | L | 350n |
| 4 | W | 30.33u |
| 5 | VGS | 940.4m |

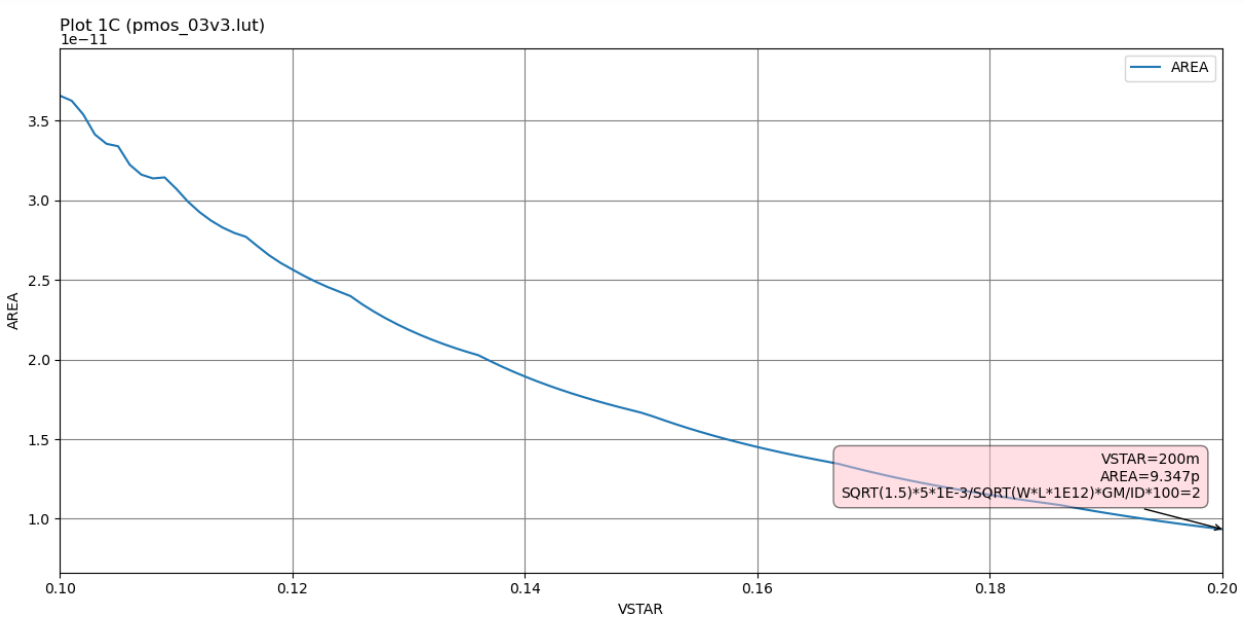
9. The tail current source has the following specifications:

| Parameter | |
|---|---|
| **Input current** | $20\mu A$ |
| **Percent mismatch: $\sigma(I_{out})/I_{out}$** | ≤ 2% |
| **Compliance voltage** | ≤ $200mV$ |
| **Area** | Minimize |

10. Use SA to plot the sizing at a constant $\boldsymbol{\sigma(Iout)}/Iout$.



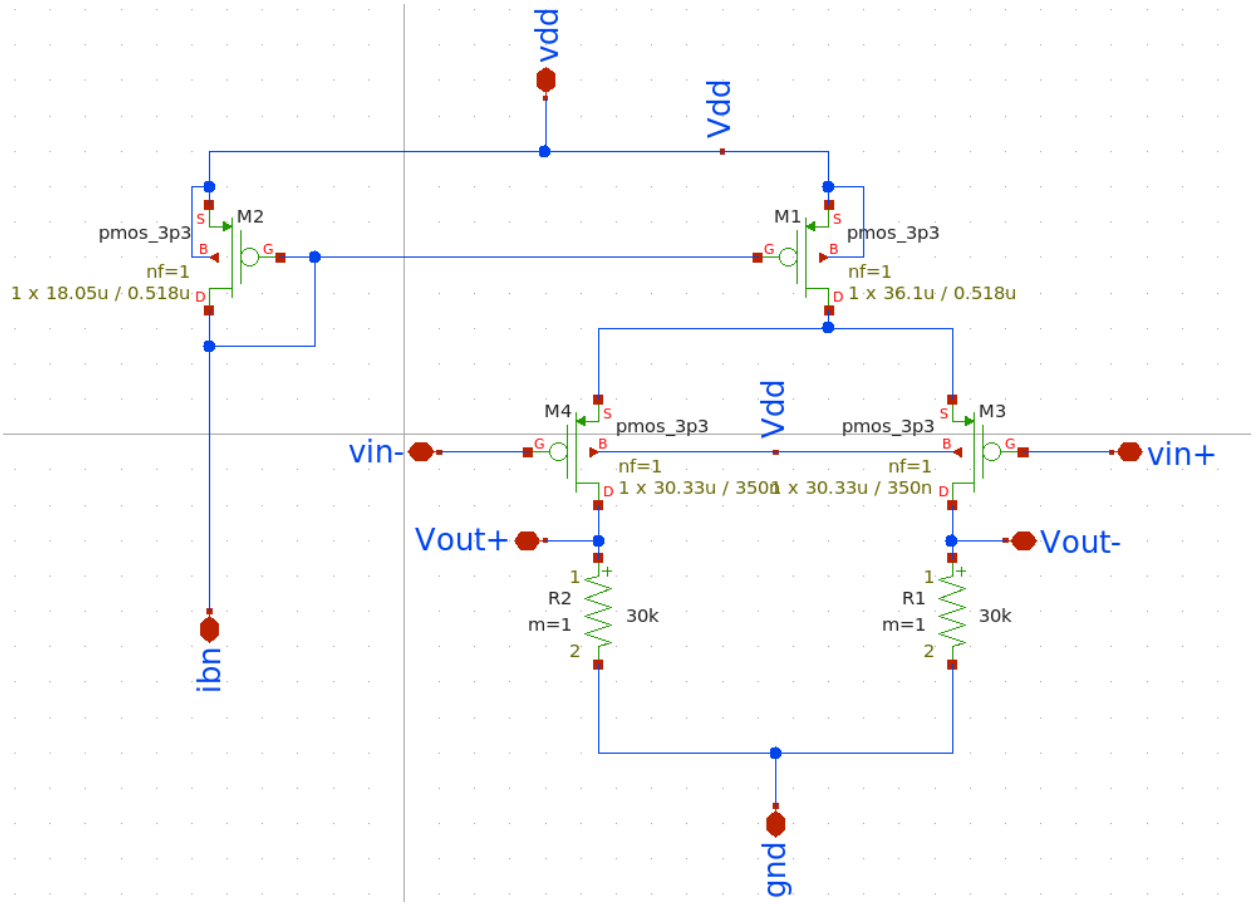





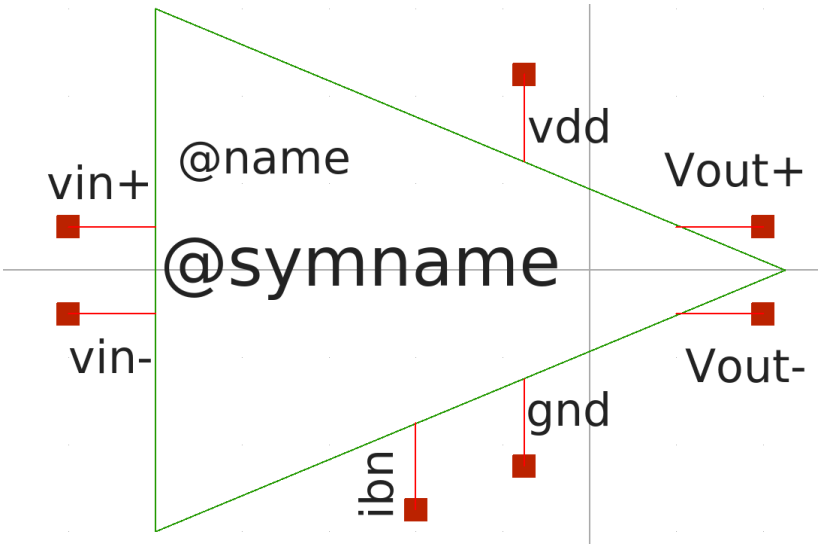

11. As seen in the plot above, for a given mismatch requirement, the minimum area is achieved at the max $V*$
12. The plot also shows that at a given $V*$ (compliance voltage), going for lower mismatch necessitates longer $L$
13. Given the compliance voltage spec
- As we choose $V^*=200\ mV$ so we need L=518 nm &W=18.05 µm
14. **Calculate** the min and max CM input levels. Is the previously selected CM input level in the valid range?
- the minimum =- Vth+VRD
- Vth ≈ 870 mV so minimum = -870+600=-270 mV
- The max CM input level = 1800-200-940 =660 mv
- So, 560 mV as an input is in the valid range

# Part 2: Differential Amplifier Simulation

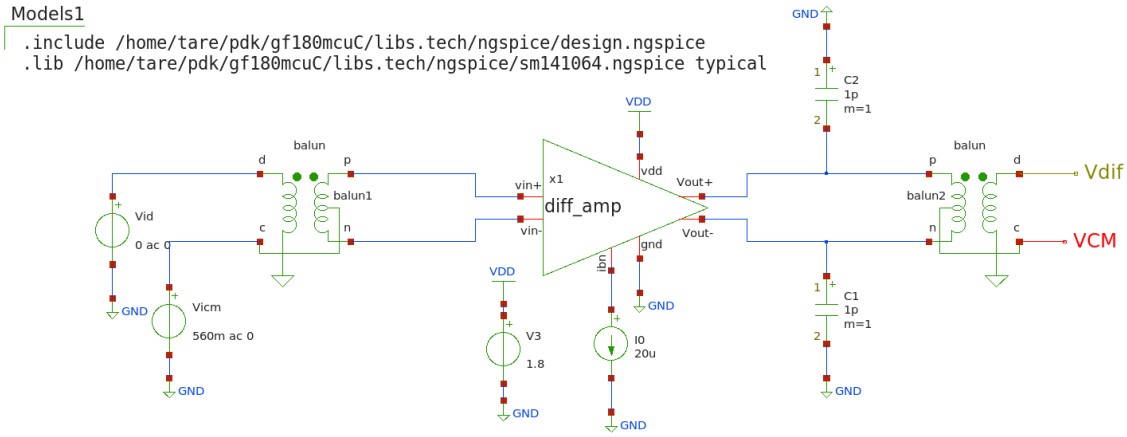
1. Create the schematic of a differential amplifier “lab_06_diff_amp”.




2. Create a symbol for the diff pair



3. Create a new cell for the testbench




# 1. OP (Operating Point) Analysis

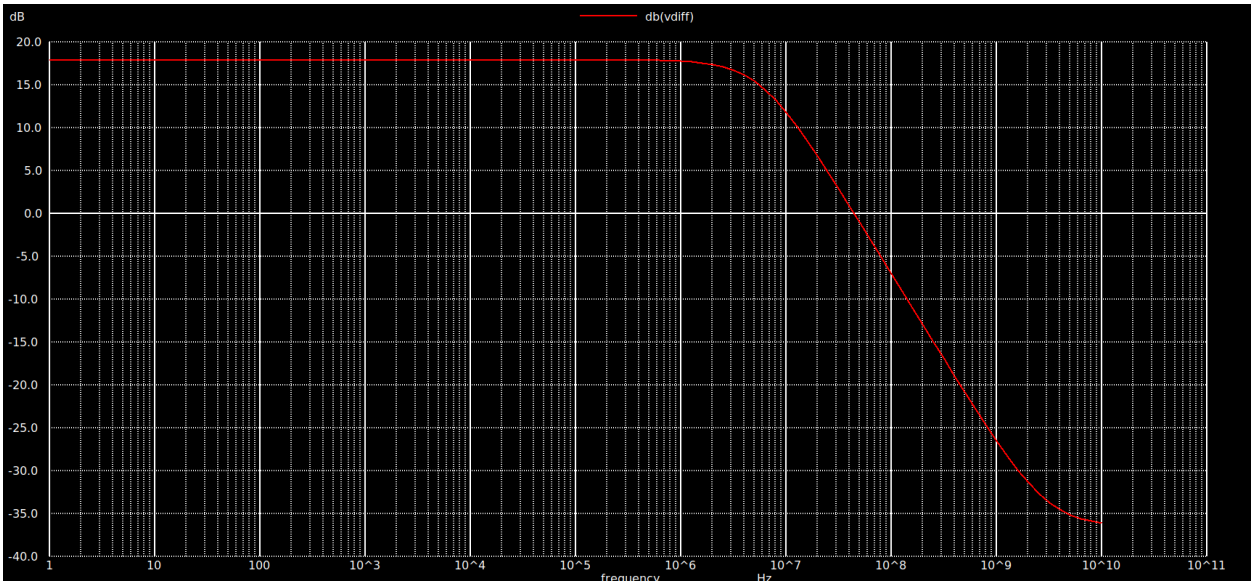
```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm2.m0           m.x1.xm1.m0           m.x1.xm3.m0
     model           pmos_3p3.13           pmos_3p3.13           pmos_3p3.12
        id                  2e-05           3.99621e-05           2.01658e-05
       vgs              0.943347              0.943347              0.940154
       vds              0.943346              0.299842              0.895181
       vth              0.792643              0.788519              0.871942
     vdsat              0.166242                0.1693              0.120203
        gm           0.000205196           0.000400795           0.000292557
       gds           1.01221e-06           6.26859e-06            3.2354e-06
      gmbs           9.18684e-05           0.000179579           9.52331e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm4.m0
     model           pmos_3p3.12
        id           1.97963e-05
       vgs              0.940154
       vds              0.906264
       vth              0.873229
     vdsat              0.119342
        gm           0.000288765
       gds           3.17534e-06
      gmbs           9.39851e-05
```

- As Vds > 1.2*Vdsat for all transistor so all transistors are in saturation region

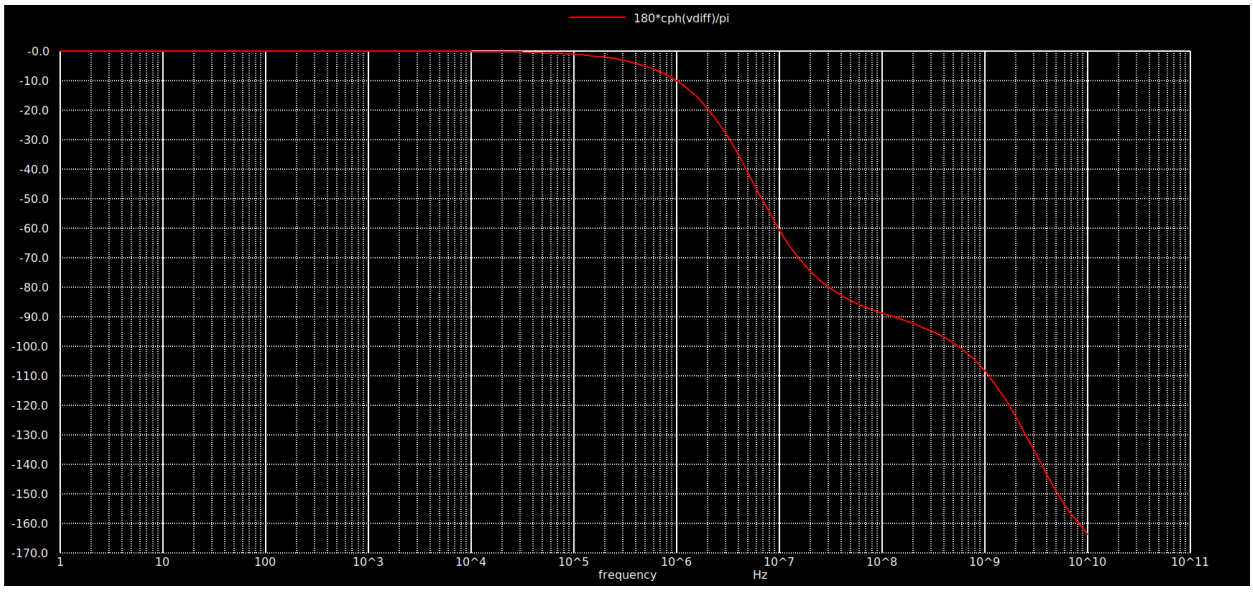
# 2. Diff small signal ccs:

- Use AC magnitude = 1 for the diff source (and AC magnitude = 0 for the CM source)
- Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).

- Report the Bode plot of small signal diff gain.
- Magnitude




- phase




- Bandwidth and gain from simulation

```
gain                =   7.856643e+00 at=  1.000000e+00
bw                  =   5.686016e+06
```

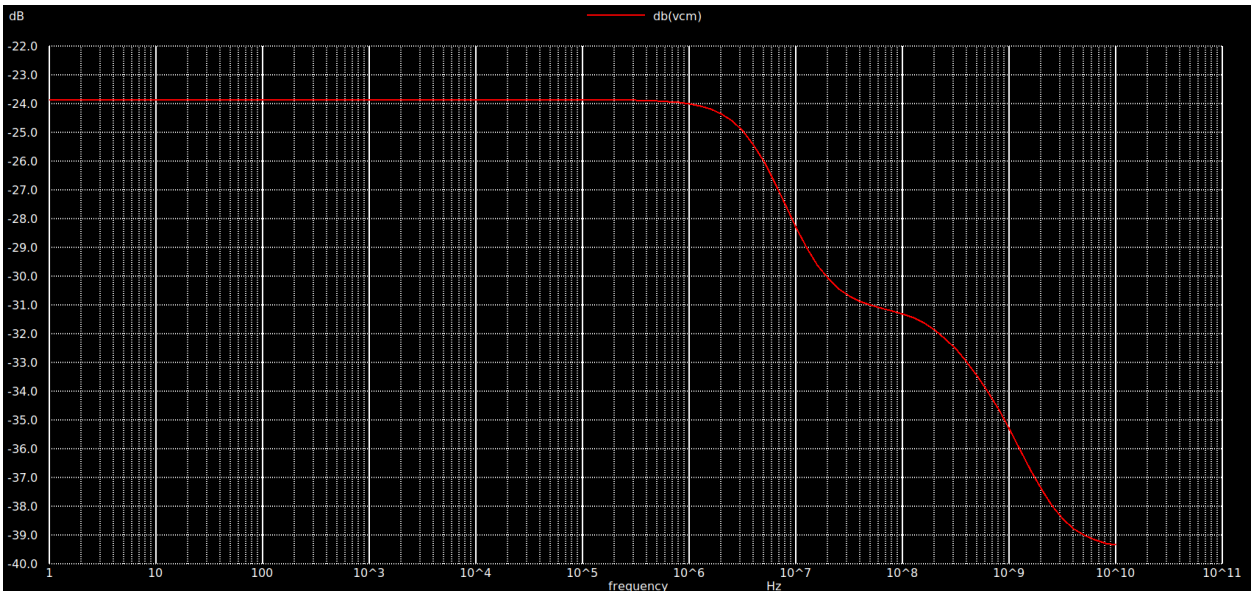
- hand analysis for gain: as gm4≈gm3≈290µS and gds4≈gds3≈3.2µS so gain =gm*(RD||1/gds)=7.94

- for bandwidth:$\omega = \frac{1}{2\pi*(RD||ro)CL} = 5.81\ MHz$

| | Analytical | Simulation |
|---|---|---|
| **Gain** | **7.94** | **7.86** |
| **Bandwidth(*MHz*)** | **5.81** | **5.69** |

## 3. CM small signal ccs:

- Use AC magnitude = 1 for the CM source (and AC magnitude = 0 for the diff source).
- Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
- Report the Bode plot of small signal CM gain.




```
cmgain                =  6.404001e-02 at=  1.000000e+00
```

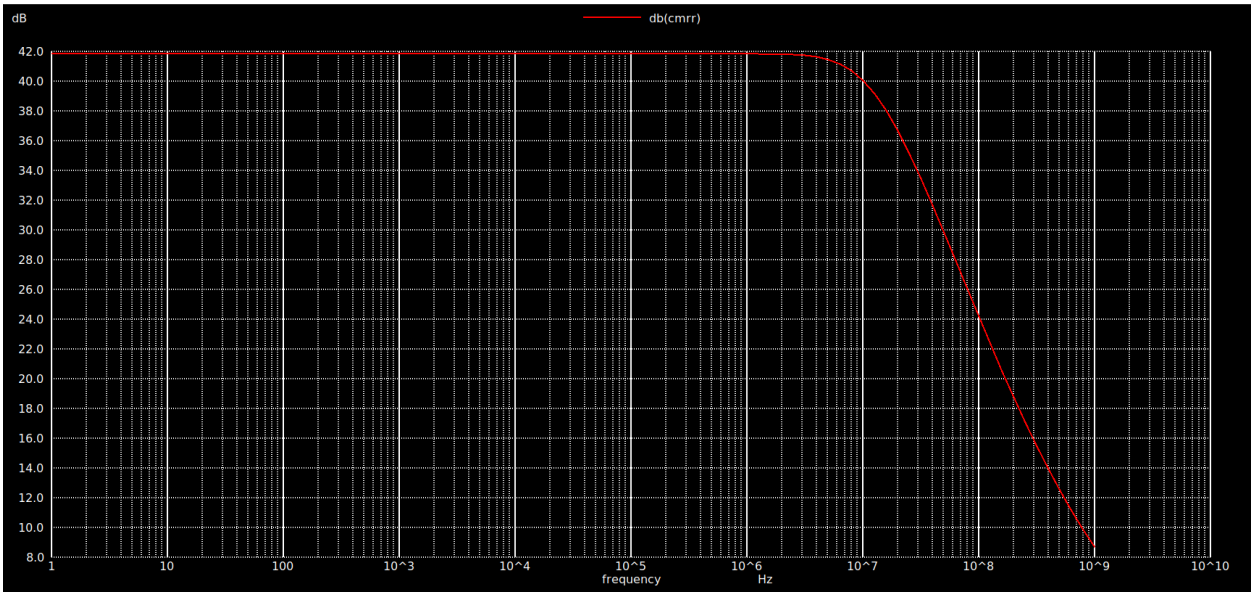
- Compare the DC CM gain with hand analysis in a table.
- As gm4≈gm3≈290µS and gmbs4≈gmbs3≈95µS CM gain

$$Avcm = \frac{gm * RD}{(1 + (gm + gmb) * 2Rss} = .070$$

| | Analytical | Simulation |
|---|---|---|
| **Avcm** | .07 | .64 |

- The gain is less than 1 as the differential amplifier attenuate the CM signal and complete cancel it when we subtract Vout+ - Vout-
- As there are pole around 5.6MHz the magnitude decreases after it but there are zero from the tail current source as it has a resistance and there is a bypass capacitance in this node, and this make the magnitude flat and decrease again as there are other poles in the circuit in the same node

- Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.




```
No. of Data Rows : 91
cmgain              =  6.298184e-02 at=  1.000000e+00
diffgain            =  7.702708e+00 at=  1.000000e+00
cmrr_val = 1.223005e+02
```

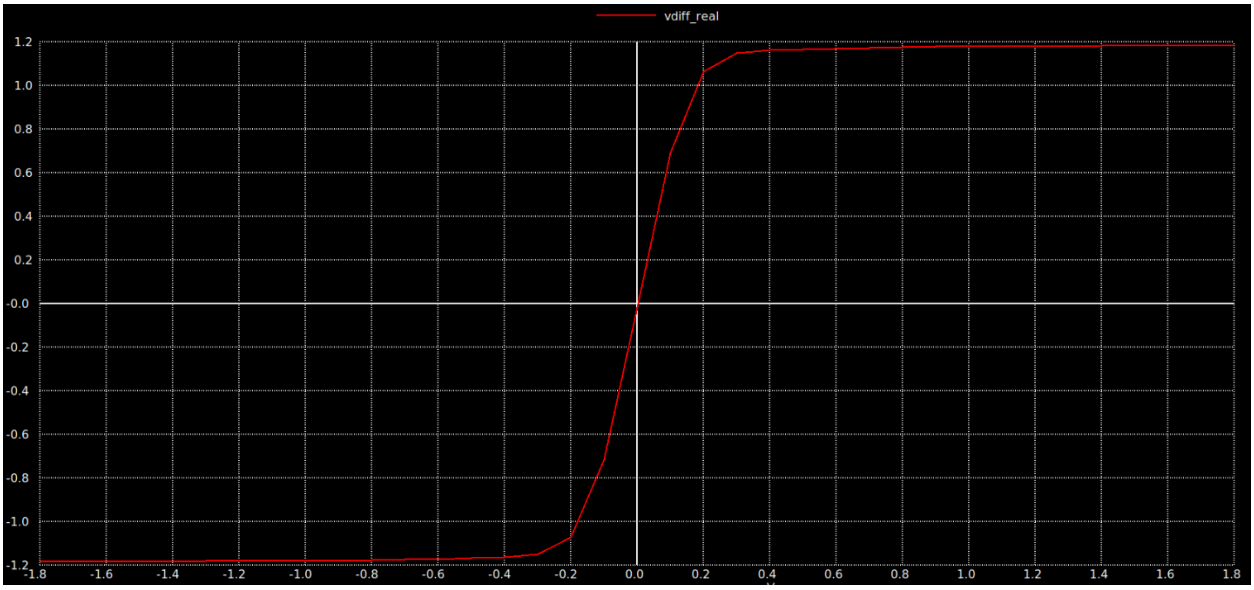
- $CMRR = (gm + gms) * 2Rss = (290 + 90) * 10^{-6} * \frac{2}{6.269*10^{-6}} = 121.23$

| | Analytical | Simulation |
|---|---|---|
| **CMRR** | 121.23 | 122.3 |

- As the Avd and Avcm decrease with the same ratio after the pole around 5.6MHz the CMRR don't decrease at this pole but at the zero in the tail current source and attach Rss to the ground and make Avcm don't decrease as Avd anymore it's decrease with low rate than Avd so CMRR decrease as Avd don't increase at this zero as differential amplifier acts as a virtual ground at this node and don't see Rss and the cacitance in this node

## 4. Diff large signal ccs:

- Use dc sweep (not parametric sweep) for Vid = -VDD:10m:VDD



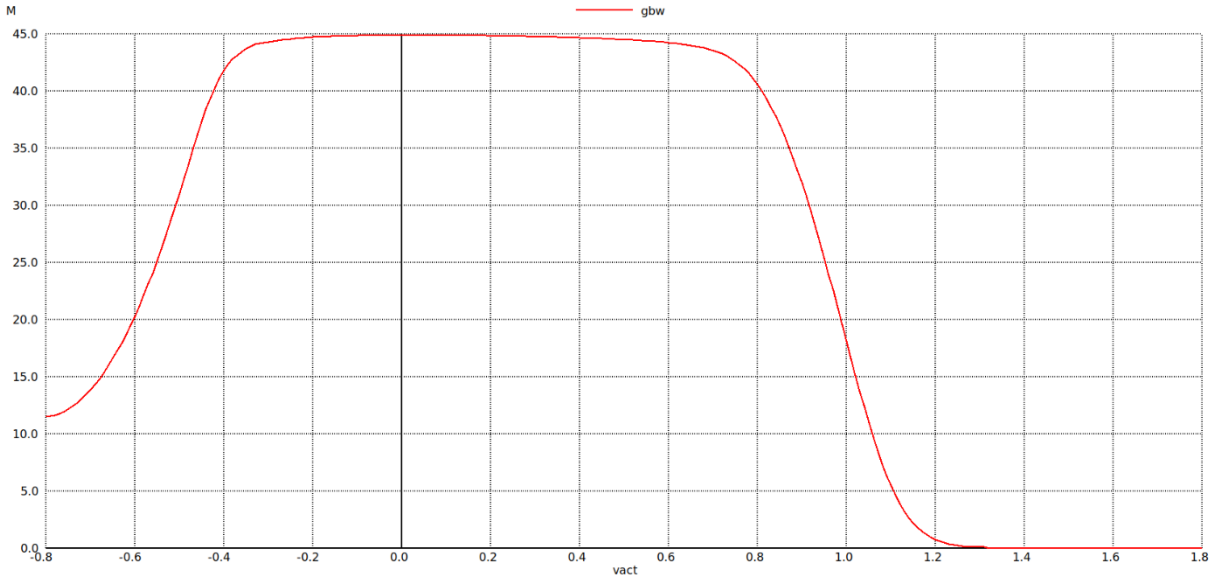

```
No. of Data Rows : 37
vdifflow              =  -1.182298e+00 at=  -1.800000e+00
vdiffzer0             =  -1.651474e-02
vdiffhigh             =  1.182144e+00 at=  1.700000e+00
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device           m.x1.xm2.m0           m.x1.xm1.m0           m.x1.xm3.m0
      model           pmos_3p3.13           pmos_3p3.13           pmos_3p3.12
         id                 2e-05           3.94097e-05           1.11617e-20

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device           m.x1.xm4.m0
      model           pmos_3p3.12
         id             3.941e-05
```

- As we see the current at Vid=VDD =39.41 µA so Vdiff@Vid =VDD = 39.41µA *30kΩ - 0 =1.18V and at Vid=-VDD the current will be the same but in the other branch so Vdiff@Vid=-VDD = 0- 39.41µA *30kΩ = -1.18V at Vid=0 the same current will through in each branch so the Vdiff = 0

| | Analytical | Simulation |
|---|---|---|
| **Vdiff@Vid=-VDD** | -1.18 | -1.182 |
| **Vdiff@Vid=0** | 0 | -0.0165 |
| **Vdiff@Vid=VDD** | 1.18 | 1.1182 |

## 5. CM large signal ccs (GBW vs Vicm):

- We will use parametric sweep on AC analysis to get GBW.
- Report CM large signal ccs (GBW vs VICM)




```
vicmmax = 7.100000e-01
vicmmin = -4.00000e-01
```

- the minimum =- Vth+VRD
- Vth ≈ 870 mV so minimum = -870+600=-270 mV
- The max CM input level =VDD-Vdsat1-Vgs3,4= 1800-169-940 =691 mv

| | Analytical | Simulation |
|---|---|---|
| **VICM max (mV)** | 691 | 710 |
| **VICM min (mV)** | -270 | -400 |