Analog IC Design – Xschem/Ngspice
Lab 04
Common Drain Frequency Response

Intended Learning Objectives

- Learn how to do ac, DC, and transient simulations of a CD amplifier.
- Investigate the ringing and peaking problem in a capacitive-loaded CD amplifier with a large signal source resistance (Rsig) and learn how to solve it.
- Use PMOS input transistor to avoid body effect in a CD amplifier.

Part 1: Sizing Chart Using ADT SA

1) We can show that the intrinsic gain of a MOSFET is given by

$$|A_v| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{1}{\lambda I_D} = \frac{2}{\lambda V_{ov}}$$

Interestingly, the gain only depends on λ and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device,$V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2}{\lambda V^*}$$

The lower the V^* the higher the gain, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

2) We want to design a CD amplifier with the parameters below.

Parameter	0.13um CMOS	0.18um CMOS
Input transistor	PMOS	PMOS
$\boldsymbol{L}$	$1\mu m$	$1\mu m$
$\boldsymbol{V^*}$	$200mV$	$200mV$
Supply	$1.2V$	$1.8V$
Current consumption	$10\mu A$	$10\mu A$

3) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from ADT.

Using ADT Sizing Assistant, plot the following design charts vs Vgs for PMOS. Set $V_{DS} = V_{DD}/2$, $L = 1\mu m$, and $w = 10\mu m$. Sweep Vgs from 0 to $\approx V_{TH} + 0.4V$.

4) Plot V^* and V_{ov} overlaid vs VGS. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.

5) An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$. On the $V^*$and V_{ov} chart locate the point at which $V^* = 200mV$. Find the corresponding V_{ovQ} and V_{GSQ}.

6) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.

7) Now back to the assumption that we made that $W = 10\mu\text{m}$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 10\mu\text{A}$ as given in the specs. Calculate W as shown below.

W	I_D
$10\mu m$	I_{DX} @ V_Q^* (from the chart)
?	$I_{DQ} = 10\mu A$ (from the specs)

8) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is inversely proportional to $W(I_D)$ as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

Part 2: CD Amplifier

1. OP (Operating Point) Analysis

1) Create a new schematic for the CD amplifier (the schematic is not included in the lab document and is left for the student as an exercise). Use a PMOS and use a $10\mu\text{A}$ ideal current source for biasing (note that the current source will be connected to the source terminal). Connect the source to the bulk. Use $L = 1\mu\text{m}$ and W as determined in Part 1. Use $C_L = 2pF, R_{\text{sig}} = 2M\Omega$, (in xschem resistor, use "value =2 meg", and a DC input voltage $= 0$ V.
(Don't forget to insert a "code_shown" for the model file of GF PDK, as discussed in the previous labs)

2) Simulate the OP point. Report a snapshot clearly showing the following parameters using the following code (in another "code_shown" dedicated for simulations only).

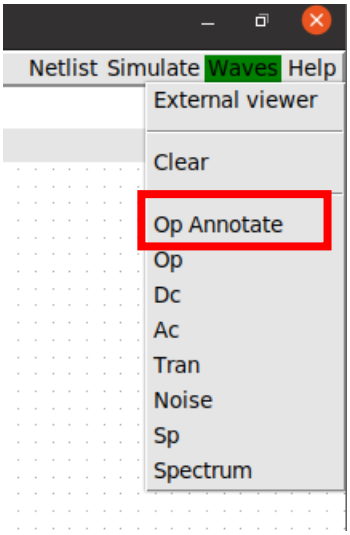
```
.option savecurrents
.control
save all
save i(@m.xm1.m0[id])
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save v(@m.xm1.m0[vgs])
```

```
save v(@m.xm1.m0[vth])
save v(@m.xm1.m0[vds])
save v(@m.xm1.m0[vdsat])
op
remzerovec
write lab4.raw
show m : gm : gds : id : vgs : vth : vds : vdsat : gmbs : cdb : cgd : cgs : csb
.endc
```

We will use “ngspice_get_value.sym” from devices to print the DC OP parameters which is defined as follows.

```
name=r4 node=i(@m.xm1.m0[id])
descr="Id=".
```

To Show the Annotation, you should load the file in which you write your OP from the “Op Annotate” option as shown below.



3) Check that the transistor operates in saturation.

2. AC Analysis

1) Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz) (For ignoring previous code, add ** in the begging of each line. Always let .control and .endc) Report Bode plot magnitude in dB vs frequency.

```
name=V1 value="dc 0 ac 1"
savecurrent=true
```

Source setup

```
.control
save all
ac dec 10 1 1G
plot vdb(out)
meas ac peak1 MAX vdb(out) FROM=1 TO=1.5G
remzerovec
write lab4_ac.raw
.endc
```

code to place inside code block

2) Do you notice frequency domain peaking?

3) Analytically calculate quality factor (use approximate expressions). Is the system underdamped or overdamped?

4) (Optional) Perform parametric sweep: CL = 2p, 4p, 8p.
   - Report Bode plot magnitude overlaid on same plot.
   - Report the peaking vs CL.
   - Comment.
5) (Optional) Perform parametric sweep: Rsig = 20k, 200k, 2M.
   - Report Bode plot magnitude overlaid on same plot.
   - Report the peaking vs CL.
   - Comment.

3. Transient Analysis

1) Use a pulse source as your transient stimulus and set it as follows (delay = 2us, initial = 0V, period = 8us, pulse_value = 100mV, t_fall = 1ns, t_rise = 1ns, width = 4us). Run transient analysis for 10us to investigate the time domain ringing. Report Vin and Vout overlaid vs time.

```
name=V2 value="PULSE(0 100m 2u 1n 1n 4u 8u)"
savecurrent=true
```

Source setup

```
.control
save all
save v(@m.xm1.m0[vgs])
tran 10n 10u
meas tran peak1 MAX out FROM=0 TO=10u
let os=((peak1-(v(@m.xm1.m0[vgs])+100m))/v(@m.xm1.m0[vgs]))*100
meas tran overshoot MAX os FROM=5u TO=6u
write lab4_tran.raw
remzerovec
.endc
```

code to place inside code block

2) Calculate the DC voltage difference (DC shift) between Vin and Vout.
   - What is the relation between the DC shift and VGS of the transistor?
   - How to shift the signal down instead of shifting it up?

3) Do you notice time domain ringing? How much is the overshoot?

4) [Optional] Perform parametric sweep: CL = 2p, 4p, 8p.
   - Report Vout vs time overlaid on same plot.
   - Report the overshoot vs CL.
   - Comment.
5) [Optional] Perform parametric sweep: Rsig = 20k, 200k, 2M.
   - Report Vout vs time overlaid on same plot.
   - Report the overshoot vs Rsig.
   - Comment.

4. [Optional] Z_{out} (Inductive Rise)

1) We want to simulate the CD amplifier output impedance. Replace CL with an current source (isource) with ac magnitude = 1. Remove the AC input signal.

name=I1 value="dc 0 ac 1"

Source setup

2) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade). The voltage across the AC current source is itself the output impedance.
3) Plot the output impedance (magnitude and phase) vs frequency. Do you notice an inductive rise? Why?
4) Does Z_{out} fall at high frequency? Why?
   Hint: C_{gd} appears in parallel with R_{sig}.
5) Analytically calculate the zeros, poles, and magnitude at low/high frequency for Z_{out}. Compare with simulation results in a table.

5. [Optional] How to solve the peaking/ringing problem?

1) Place the input/output poles away from each other (as we did when we swept CL and Rsig).
2) A compensation network can be used to compensate for the negative input impedance and prevent overshoots. Read [Johns and Martin, 2012] Section 4.4 and try to implement the compensation network.

Lab Summary

In Part 1 you learned:

- How to design a PMOS common-drain amplifier.
- How to find transistor sizing using the Sizing Assistant (SA).

In Part 2 you learned:

- How to do AC, DC and transient simulations of a CD amplifier.
- How the peaking in the frequency response of a CD amplifier changes with the load capacitor and source resistance.
- How the ringing in the transient response of a CD amplifier changes with the load capacitor and source resistance.
- How the output impedance of a CD amplifier shows inductive behavior.

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