Analog IC Design – Xschem/Ngspice and ADT
Lab 03
Cascode Amplifier

Intended Learning Objectives

This lab is divided into three parts:

- In Part 1 you will
  - o Use ADT IC design and SA tools in design to size transistors.
  - o Design and simulate single and cascode amplifier.
  - o Set bias current of the cascode amplifier.

- In Part 2,3 (Optional) you will
  - o Investigate the gain, the bandwidth, and the GBW of a cascode amplifier

NOTE: To get access to the Sizing Assistant please register at https://adt.master-micro.com/ and create a support ticket from your dashboard. Verified instructors may also request access to an editable MS Word version of the lab and the lab model answer.

NOTE: The values and charts used in the lab document assume the provided 180 nm educational device models and 1.8 V supply. Other models/technologies can be used by applying reasonable adjustments to the lab values.
For 2024 lab3 we will use gf180muc. ADT is set upped on the machine.

Part 1: Device Sizing using ADT SA

Theoretical background

1) From the square law, we have

$$g_m = \frac{2I_D}{V_{ov}} \rightarrow V_{ov} = \frac{2}{g_m/I_D}$$

For a real MOSFET, if we compute V_{ov} and $\frac{2}{g_m/I_D}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2}{g_m/I_D} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

The lower the V^* the higher the g_m, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

2) Although the V^* is a nice parameter that is inspired by the square-law, it does not have an intuitive or a physical meaning (it is not an actual voltage in the circuit). We actually defined V^* in order to be able to define a relation between the g_m and I_D. Thus, the real parameter that we should care about is the g_m over I_D ratio (g_m/I_D).

If the square-law is valid

$$g_m = \frac{2I_D}{V_{ov}} \rightarrow \frac{g_m}{I_D} = \frac{2}{V_{ov}}$$

Using V^*

$$\frac{g_m}{I_D} = \frac{2}{V^*}$$

A small g_m/I_D means large V_{ov} (biasing in strong inversion) and a large g_m/I_D means small V_{ov} (biasing in weak inversion).

3) There are many good things about using the g_m/I_D as a design knob:
   - The g_m/I_D gives a direct relation between the most important MOSFET parameter (gm) and the most valuable resource (ID). For example, a $g_m/I_D = 10\ S/A$ means you get $10\ \mu S$ of g_m for every $1\ \mu A$ of bias current.
   - The g_m/I_D is a normalized knob: it has a limited search range (typically from 5 to 25 S/A) independent of the technology or the device type.
   - The g_m/I_D is intuitive because it tells you directly about the inversion level (bias point) and consequently all related trade-offs. For example, $g_m/I_D = 5\ S/A$ means strong inversion (SI), $g_m/I_D = 15\ S/A$ means moderate inversion (MI), and $g_m/I_D = 25\ S/A$ means weak inversion (WI).
   - The g_m/I_D is an orthogonal knob: If we define the g_m/I_D then we define the inversion level (bias point). If you change I_D or L while keeping g_m/I_D fixed, then the inversion level (bias point) is kept fixed. The W is treated as an output variable instead of being treated as an input variable.
   - The higher the g_m/I_D (the lower the V^*) the higher the efficiency and the headroom (the available swing), but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $g_m/I_D = 10\ S/A$ ($V^* = 200mV$).

4) **We want to design a common source (CS) amplifier that has ideal current source load with the following parameters**.

Parameter	Value
$A_v = g_m r_o$	50
g_m/I_D	$10\ S/A$
Supply (V_{DD})	$1.8\ V$
Quiescent (DC) output voltage	$V_{DD}/2 = 0.9\ V$
Current consumption	$20\ \mu A$

5) Since the square-law is not accurate, we cannot use it to calculate the sizing. Instead, we will use the Sizing Assistant (SA) which is a powerful analog calculator that uses LUTs that are pre-generated from the simulations. The input and output of SA are shown below. We will use the same sizing (L and W) to build a cascode amplifier.

Solution Steps

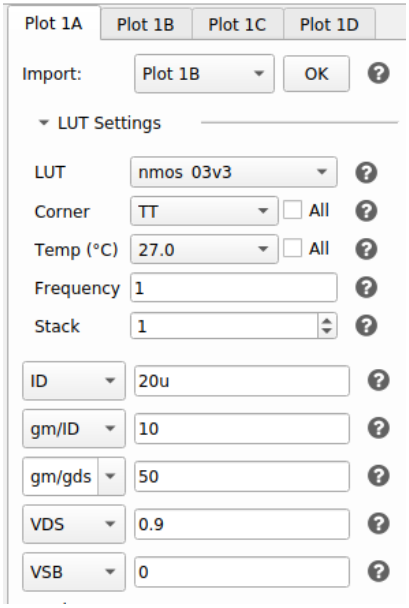
1. CS design specs

- From square law $\boldsymbol{V^* = \frac{2\,I_D}{g_m}}$, $\boldsymbol{\frac{g_m}{I_D} = \frac{2}{V^*}}$
- $\boldsymbol{g_m r_o = 50}$, $\boldsymbol{I_B = 20\mu A}$
- $V_{DS} = 0.9V\ (half\ of\ the\ supply)$

2. Design steps

- From VM tare open ADT
  1. Open a terminal in the directory:
     "/home/tare/ADT_Working_Directory"
  2. Run the command: "./start_adt.sh"

- Load LUTs files (file - load LUT - open nmos_3p3
- Open Sizing Assistant and choose nmos_3p3 LUT
- Set specs for CS (you can adjust gm/gds to meet the specs)
- Take the values of L,W and VGS0 to xschem



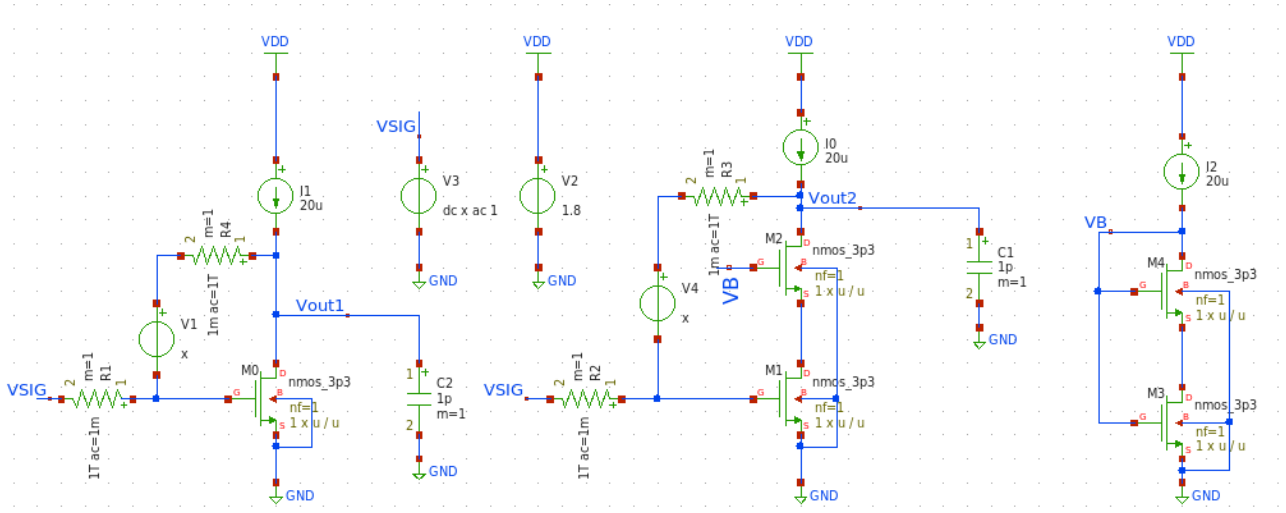
PART 2: Cascode for Gain

1. OP Analysis

Create a new schematic. Construct the circuit shown below. Use $I_B = 20\mu A$. Use L and W as selected in Part 1 for M0, M1, M2, and M4. Use the same W for M3 but it will have different L as will be shown later. Use $C_L = 1pF$

For R1-4 value= "<dc value> ac= <ac value>"

Replace X with its appropriate values

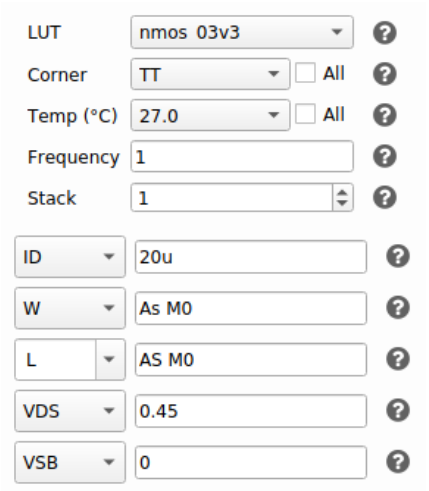


1) **Set NGspice gf180muc models**.We need to bias transistors in saturation; however, the output node is a high impedance node; thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations (use the AC property in ideal_resistor). The input transistor is diode connected for DC simulation (always in saturation), while in AC simulation the feedback is disconnected, and the AC input source is connected. **Set the feedback resistance $1m\Omega$ DC and $1T\Omega$ AC and set the source resistance oppositely**. We will study how to do biasing practically later in this course inshaAllah.

   Solution step: let $Vdc1 = Vout1Q - VGS0Q$ and $Vdc4$ to $Vout2Q - VGS1Q$ to set Vout to 0.9

2) For the cascode amplifier, we will design $\boldsymbol{V_B}$ **to set** $\boldsymbol{V_{DS1} \approx V_{DS2} \approx 0.45\ V}$ as will be shown shortly.

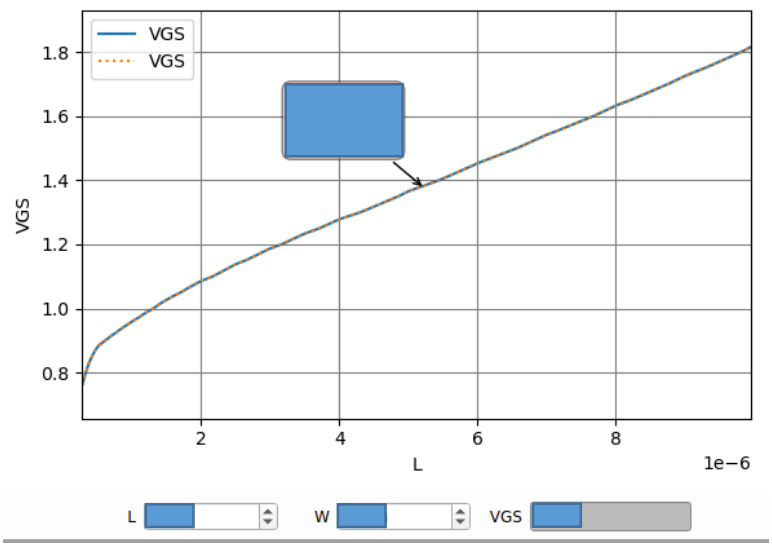
3) To calculate V_B we need to find V_{GS2} because $\boldsymbol{V_B = V_{GS2} + V_{DS1}}$. Note that M2 experiences body effect, so its V_{GS} will be higher than M0 and M1.

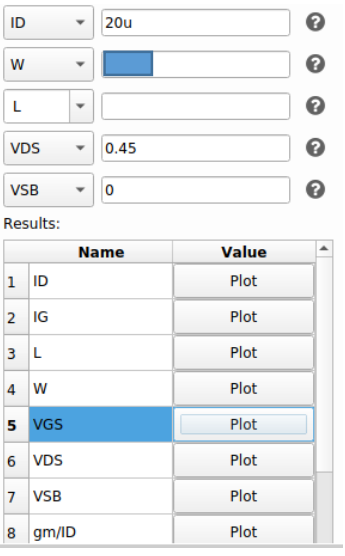


4) M3 and M4 are used to generate the cascode bias voltage. Note that M4(same aspect ratio) is always in saturation and M3(same W)is always in triode.We need to find the L of M3, so we set a sweep for M3 as shown below.

   Solution step: find L3 at $\boldsymbol{V_{GS} = V_B = V_{GS2} + V_{DS1}}$ using W3,ID

   Then plot VGS vs L changing L to fit VGS





```
MODELS

.include $::180MCU_MODELS/design.ngspice
.lib $::180MCU_MODELS/sm141064.ngspice typical
```

5) Simulate the DC OP point of the above CS and cascode amplifiers **(ngspice interactive)**. **Report a snapshot showing the following parameters for M0 to M4 in addition to DC node voltages clearly annotated**.

Solution step: to annotate DC voltage nodes (simulation – graphs – Annotate operating points)

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB

Simulation step

```
"
.option savecurrents
.control
save all
op

let Igain0 = @m.xm0.m0[gm]/@m.xm0.m0[gds]
save Igain0
print Igain0
let gm = @m.xm2.m0[gm] +@m.xm2.m0[gmbs]
let Igain1 = (@m.xm1.m0[gm]*gm)/(@m.xm1.m0[gds]*@m.xm2.m0[gds])
save Igain1
print Igain1
remzerovec
write lab3.raw
show m : id : vgs : vds : vth : vdsat : gm : gds : gmbs : cdb : Cgd : cgs : csb
.endc
"
```

We can also use “ngspice_get_value.sym” from devices to print the DC OP parameters to annotate them on schematic which is defined as follows.

```
name=r4 node=i(@m.xm2.m0[id])
descr="Id="
```

“node” field should be replaced by the parameter you wish to print (you could get this syntax from the above code).
“descr” is just referring to display name.

Use this for each device

6) Put the OP of all transistors in a table with the appropriate units
   NOTE: "vdsat" is the minimum drain-source voltage required to bias the transistor in saturation. It is equal to V_{ov} for a square-law device. It is also referred to as "vdss" (drain-source saturation voltage) in some models. It is considered an ambiguous parameter because the transition from triode to saturation is gradual, not abrupt.

7) Check that all transistors operate in saturation. Does any transistor operate in triode? Why?
   Solution step: Check VDS > Vdsat*1.2.
8) Do all transistors have the same vth? Why?

   NOTE: use $\gg$ or $\ll$ if the difference is 10 times or more (one order of magnitude).
9) What is the relation $(\ll, <, \approx, >, \gg)$ between gm and gds?
10) What is the relation $(\ll, <, \approx, >, \gg)$ between gm and gmb?
11) What is the relation $(\ll, <, \approx, >, \gg)$ between cgs and cgd?
12) What is the relation $(\ll, <, \approx, >, \gg)$ between csb and cdb?

2. AC Analysis

1) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
2) create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to interactive.
3) Report the Bode plot (magnitude) of CS and cascode appended on the same plot.
4) Using small signal parameters from OP simulation or SA, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.
6) Comment on the results**.**

Simulation steps

- Add graph waves and launcher from simulation "netlist" + "simulate" then Waves -> Ac -> select your raw file (we can also use plot)
- Press A on graph to vertical curser
- Do hand analysis and compare it with the simulations
- Put the results in Table
- Comment

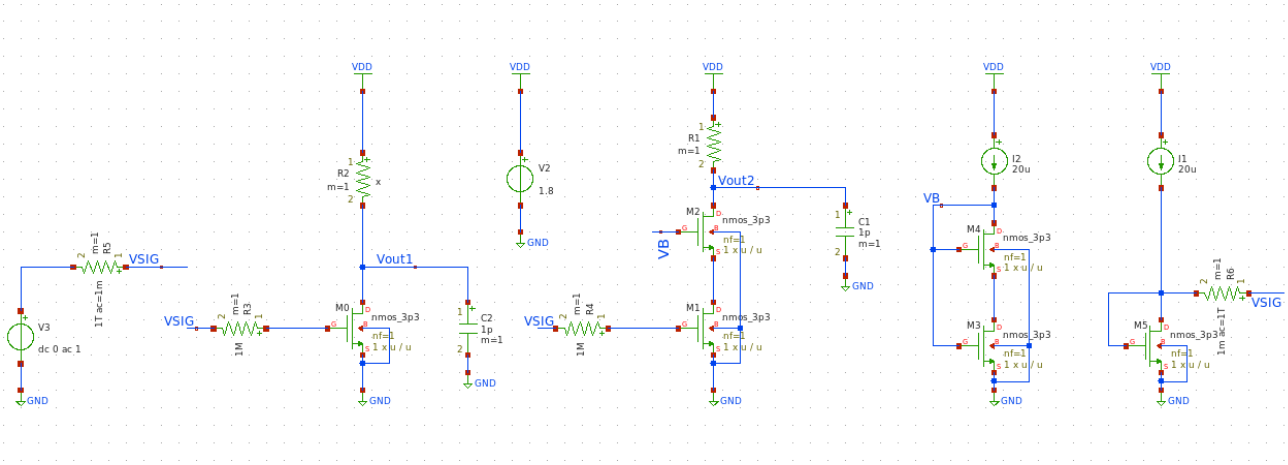
```
"
.control
save all
ac dec 10 1 10G

let AV_CS =abs(v(Vout1))
meas ac peak1 MAX vmag(vout1) FROM=1 TO=1.5G
let ff1=peak1*0.707
meas ac f3db1 WHEN vmag(Vout1)=ff1 FALL =1
meas ac UGF1 WHEN vmag(Vout1)=1 FALL =1
```

```
let GBW1 = Peak1*f3db1
print GBW1

let AV_CASCODE =abs(v(Vout2))
meas ac peak2 MAX vmag(vout2) FROM=1 TO=1.5G
let ff2=peak2*0.707
meas ac f3db2 WHEN vmag(Vout2)=ff2 FALL =1
meas ac UGF2 WHEN vmag(Vout2)=1 FALL =1
let GBW2 = Peak2*f3db2
print GBW2
plot AV_CS AV_CASCODE
plot vdb(Vout1) vdb(vout2) xlog
remzerovec
write lab3_ac.raw

*let phase= 80*cph(vout1)/pi
*plot phase xlog
.endc
"
```

Part 3: "Optional" Cascode for BW

1. OP Analysis

1) Create a new schematic. Copy the old schematic instances to the new one. Make the following modifications:
   - Remove the feedback connection used to set the DC output voltage. The DC output voltage is going to be set by the voltage drop on the resistance.
   - Replace the current source with a resistor load R_D.
   - Create a diode connected transistor (M5) that is used to generate the DC bias input voltage of the two amplifiers. This voltage is connected to the amplifier in DC only. In AC analysis, the AC input source is connected.
   - Set $C_L = 1fF$ and the signal source resistance $R_{sig} = 10M\Omega$. This will make the dominant pole the input pole instead of the output pole.



2) Calculate R_D analytically such that the voltage drop on it is $\approx V_{DD}/2$ (the current remains roughly the same as in Part 2 because we are using the VGS generated by M5). Note that the DC voltage of the output node is set by the resistance (R_D); thus, we don't need a feedback loop as in the previous case.
3) Simulate the DC OP point of the new CS and cascode amplifiers. Report a snapshot showing the following parameters for M0 to M5 in addition to DC node voltages clearly annotated.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

4) Check that all transistors operate in saturation. Does any transistor operate in triode? Why?

2. AC Analysis

1) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
2) Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them.
3) Report the Bode plot (magnitude) of CS and cascode **appended on the same plot**.
4) Using small signal parameters from OP simulation or SA, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis. **Comment** on the results.

Lab Summary

In Part 1 you learned:

- How to find transistor sizing using the Sizing Assistant (SA).
- How to design a common-source and a cascode amplifier.

In Part 2 you learned:

- How to build a testbench for a cascode amplifier with current-source load.
- How to use cascode to boost the amplifier's gain.
- How to simulate the gain, the bandwidth and the GBW of a cascode amplifier with current-source load.

In Part 3 you learned:

- How to build a testbench for a cascode amplifier with resistive load.
- How to use cascode to boost the amplifier's bandwidth.
- How to simulate the gain, the bandwidth and the GBW of a cascode amplifier with resistive load.

Acknowledgements

Thanks to all who contributed to these labs. Special thanks to Dr. Sameh A. Ibrahim for reviewing and editing the labs. If you find any errors or have suggestions concerning these labs, please contact Hesham.omran@eng.asu.edu.eg.