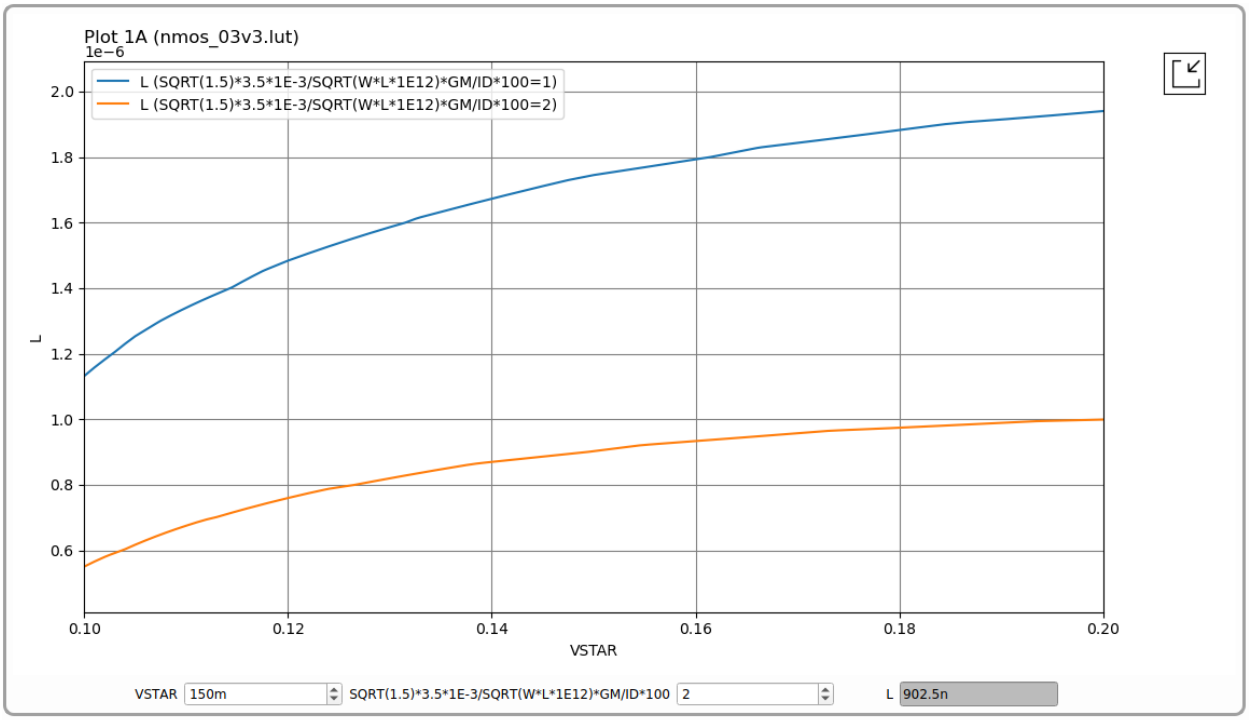
ITI CMOS Analog IC Design 2024
Lab 05
Simple vs Wide Swing (Low Compliance) Cascode Current Mirror

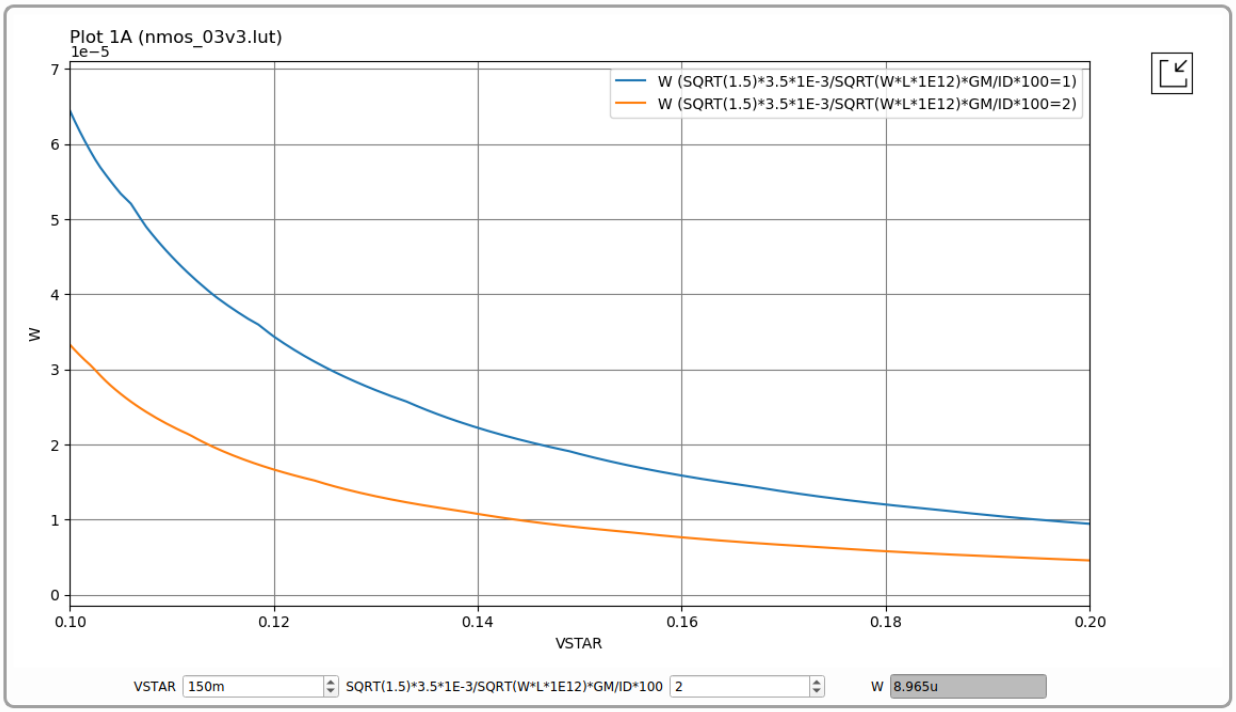
Part 1: Exploring Sizing Tradeoffs Using SA

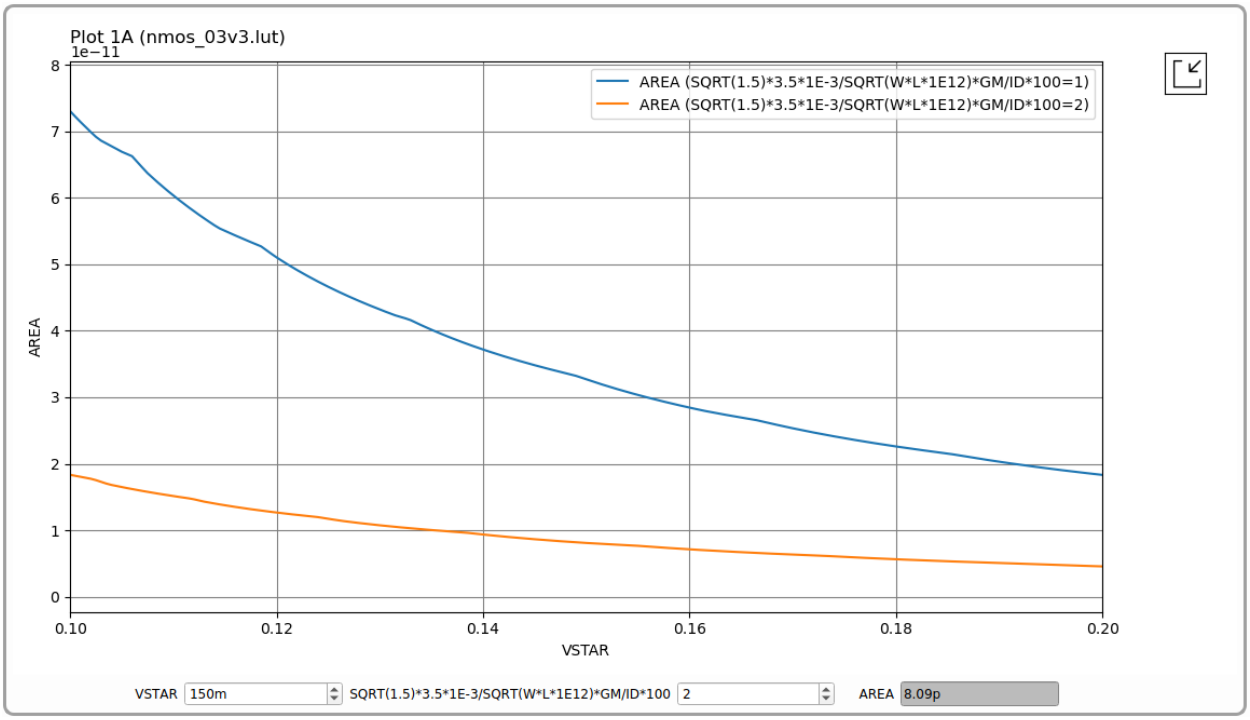
1. We want to design a simple current mirror with the following specs

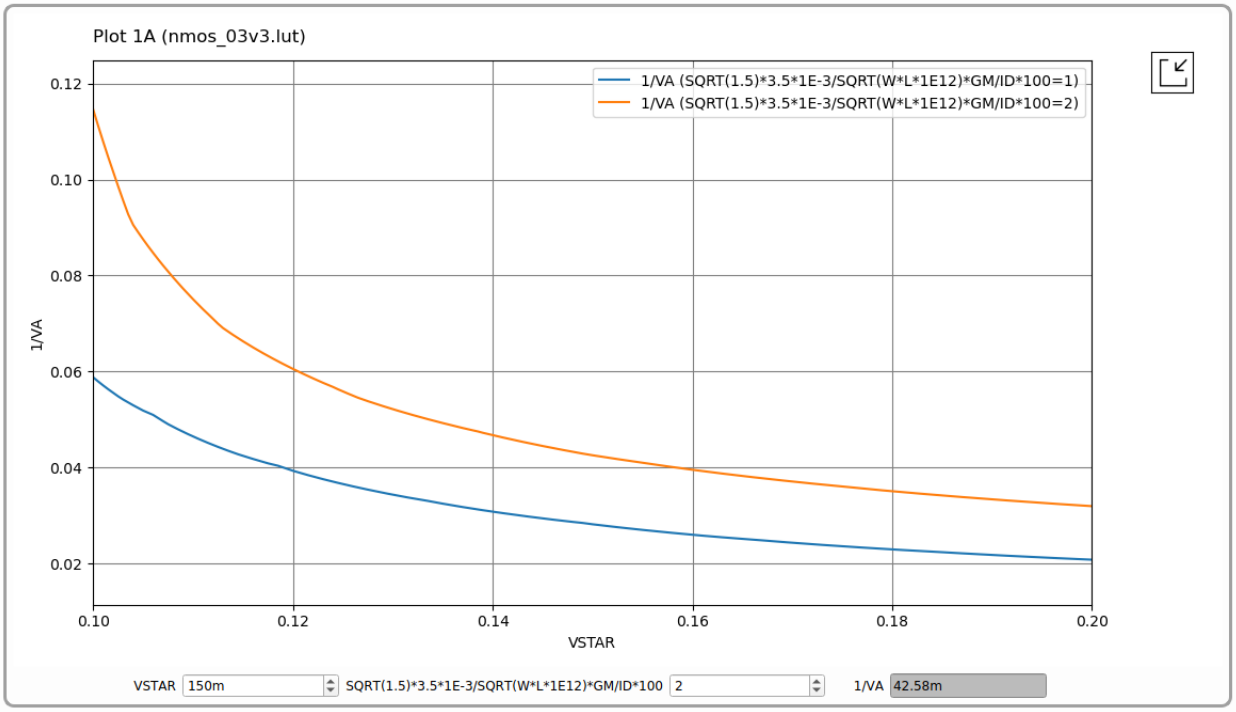
Parameter	
Current direction (source/sink)	**Sink**
Input Current	**10 µA**
Output Current	**20 µA**
% Change in Current for $\Delta Vout = 1V$	**< 10%**
Percent mismatch: $\sigma(Iout)/Iout$	**≤2%**
Compliance voltage	**≤150 mV**
Area	**minimize**

2. Sinking current means NMOS
3. The % Change in current translates to a spec on the $\lambda = 1/VA$ of the device. So we need λ<.1
4. The current mirror design trade-offs

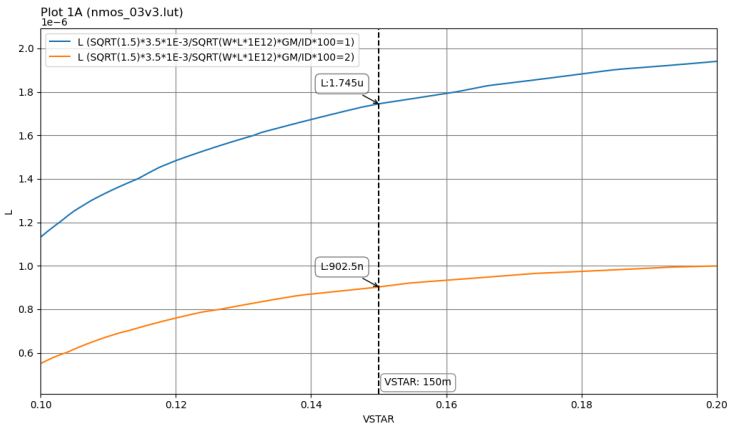


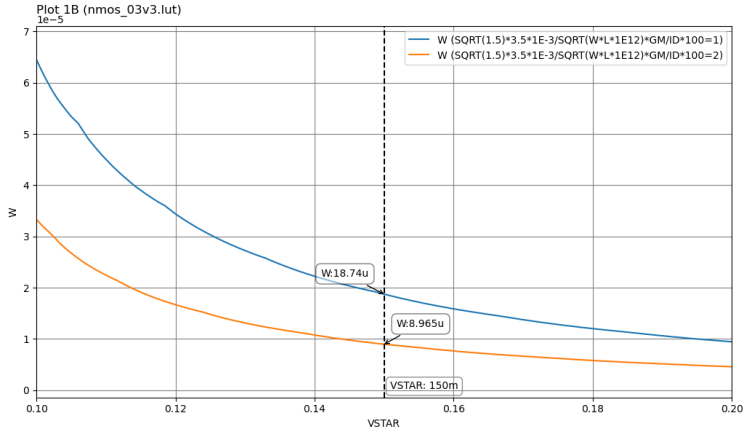

Plot 1A (nmos_03v3.lut)
1e−5
W (SQRT(1.5)*3.5*1E-3/SQRT(W*L*1E12)*GM/ID*100=1)
W (SQRT(1.5)*3.5*1E-3/SQRT(W*L*1E12)*GM/ID*100=2)
W
VSTAR
0.10
0.12
0.14
0.16
0.18
0.20
VSTAR 150m
SQRT(1.5)*3.5*1E-3/SQRT(W*L*1E12)*GM/ID*100 2
W 8.965u

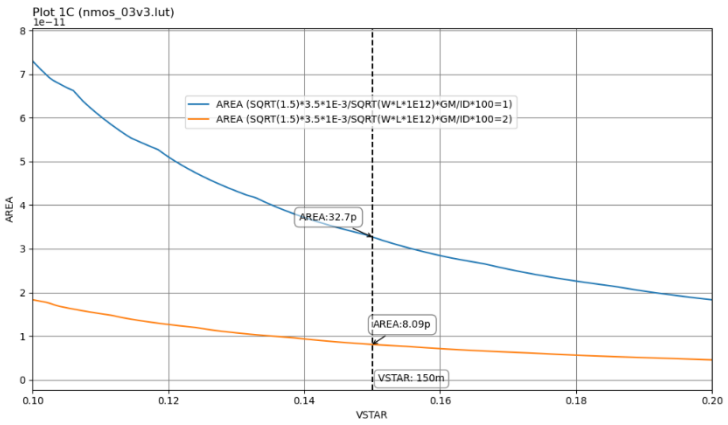

Plot 1A (nmos_03v3.lut)
1e−11
AREA (SQRT(1.5)*3.5*1E-3/SQRT(W*L*1E12)*GM/ID*100=1)
AREA (SQRT(1.5)*3.5*1E-3/SQRT(W*L*1E12)*GM/ID*100=2)
AREA
VSTAR
0.10
0.12
0.14
0.16
0.18
0.20
VSTAR 150m
SQRT(1.5)*3.5*1E-3/SQRT(W*L*1E12)*GM/ID*100 2
AREA 8.09p

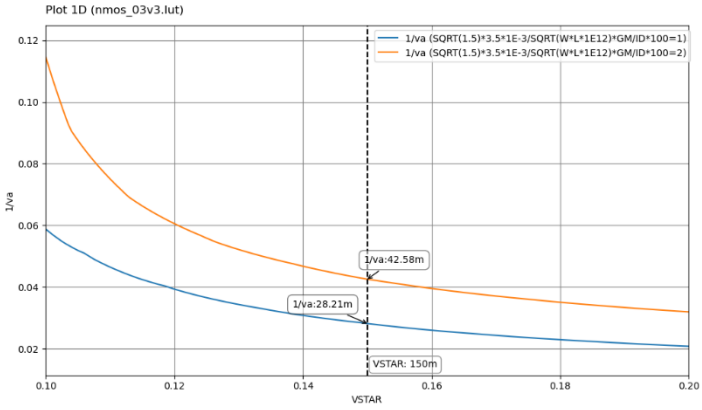


5. To get minimize area we will choose Percent mismatch=2 so we choose L=902.5 nm ,w=8.965 µm and λ=42.58m
6. If we can do in another spice tools, I think it will be very difficult as spice tools we can change property like length, width, Vds, Vgs or Id not property like gm/id or Percent mismatch
7. The above results mean that the highest $V*$ is desirable from the perspective of mismatch, area, and λ. Thus, $V*$ will be limited by the required compliance voltage. So we choose $V*$=150 mV
8. **Report** the above plot with a cursor added at the required $V*$









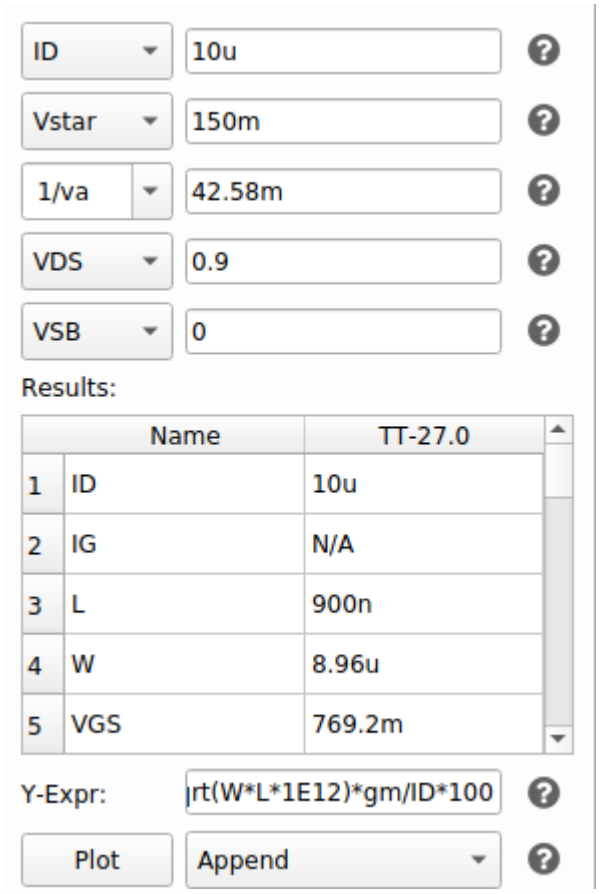
- So L=902.5 nm, W=8.965 µm, Area=8.09 pm^2, λ=42.58mS/A

9. As we choose λ=42.58mS/A

```
The resultant point 'sqrt(1.5)*3.5*1E-3/sqrt(W*L*1E12)*gm/ID*100 = 1.992'
The resultant point 'sqrt(1.5)*3.5*1E-3/sqrt(W*L*1E12)*gm/ID*100 = 1.992'
The resultant point 'sqrt(1.5)*3.5*1E-3/sqrt(W*L*1E12)*gm/ID*100 = 1.992'
```

- We confirm that the Percent mismatch is less than 2% and we meet the spics

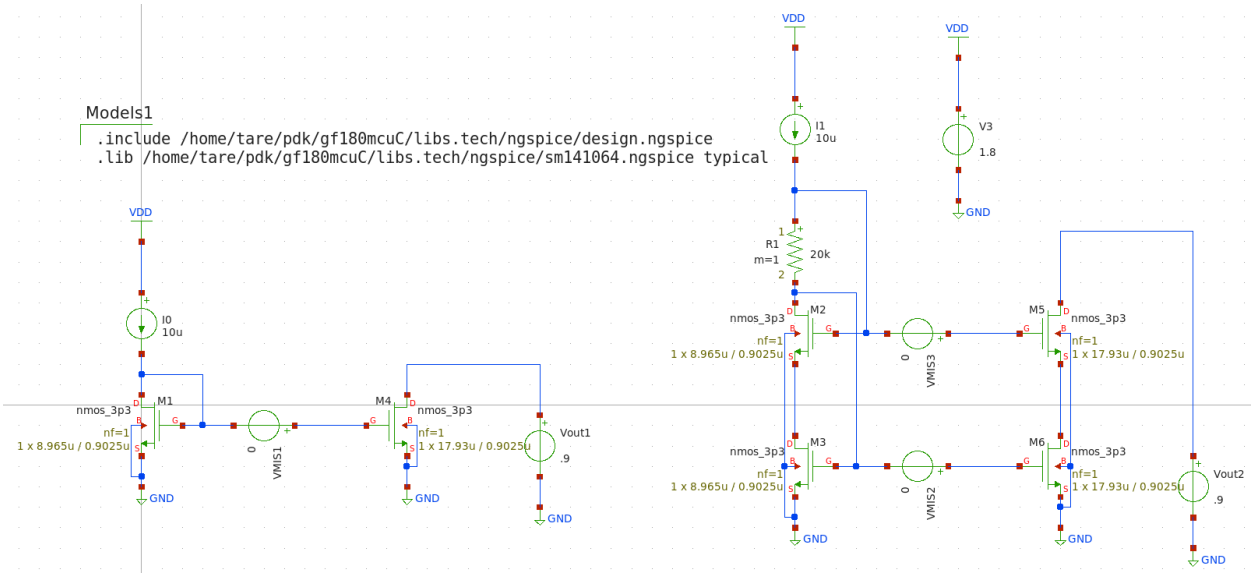
10. From the figure we see that w=8.96 um and L=900 nm and Percent mismatch =1.992



Part 2: Current Mirror Simulation

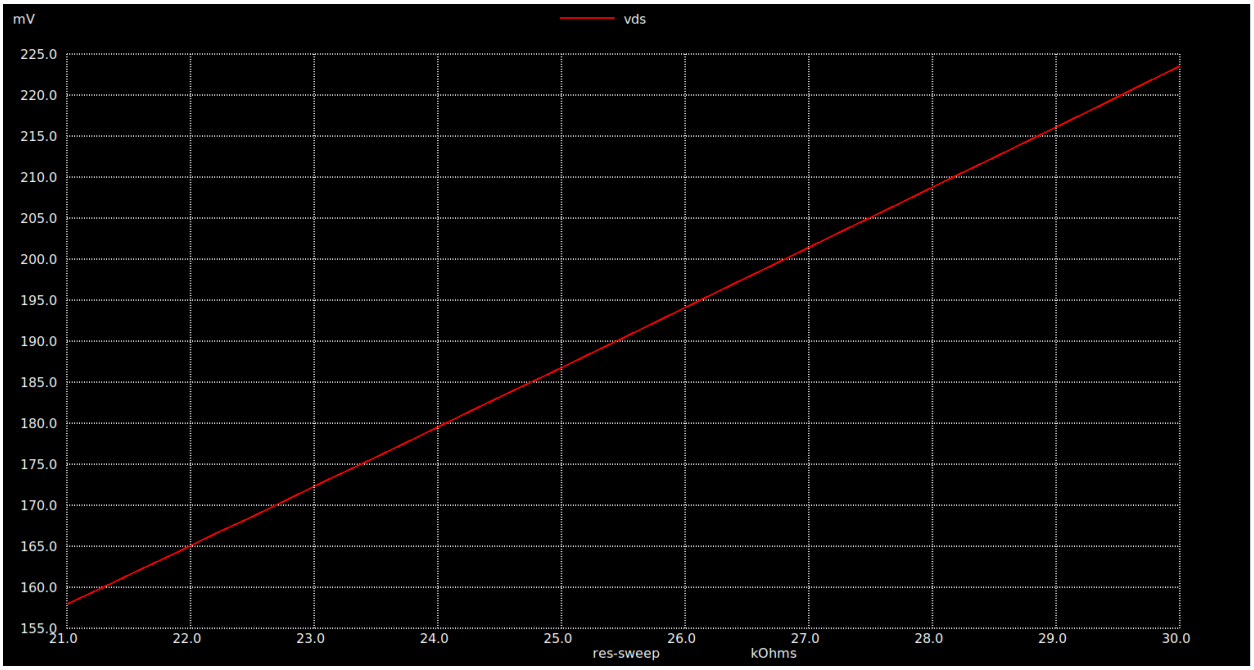
1. OP (Operating Point) Analysis

1. Schematic



- As V*=150 mV so Vds6=200mV So Rb=200mV/20µA=20kΩ

2. Perform DC sweep (not parametric sweep) for RB



- So to achieve $50mV$ saturation margin requirement. Then we need

- Rb =26.8KΩ.

```
No. of Data Rows : 31
rb                =  2.681449e+04
```

- The value we need is bigger than analytical because Vgs2= Vgs3+VRb we choose that VRb in analytical to achieve 200mV on Vds3 the problem is Vgs3 is not enough to turn on M2 as M2 need more than it as it has suffered from body effect, so we increase Rb to solve this effect.

3. Simulate the OP point

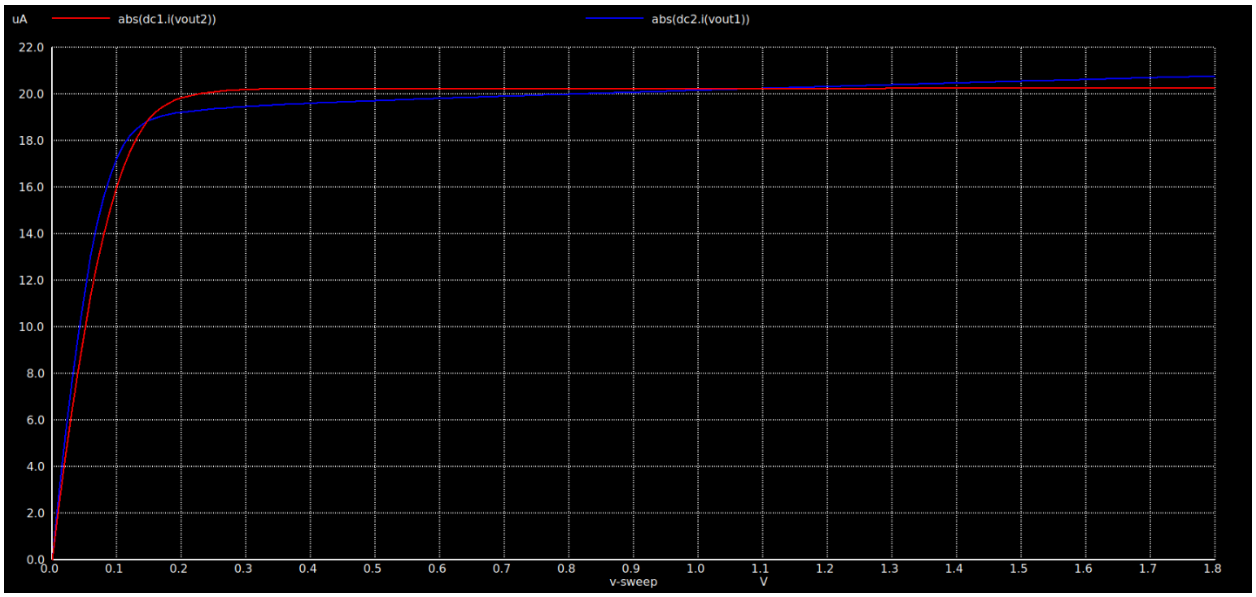
```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device             m.xm6.m0             m.xm5.m0             m.xm4.m0
     model          nmos_3p3.13          nmos_3p3.13          nmos_3p3.13
        id          1.94437e-05          1.94437e-05          1.91744e-05
        gm          0.000259988          0.000263281          0.000260859
       gds          3.98422e-06          8.62765e-07           8.0591e-07
       vgs             0.769619             0.836685             0.765156
       vth              0.69274              0.76226             0.692522
       vds             0.200932             0.699063             0.899997
      gmbs          9.88352e-05          9.05935e-05           9.9208e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device             m.xm3.m0             m.xm2.m0             m.xm1.m0
     model           nmos_3p3.9           nmos_3p3.9           nmos_3p3.9
        id                1e-05                1e-05                1e-05
        gm          0.000132229          0.000133988          0.000134103
       gds          2.22032e-06          4.83172e-07          4.37836e-07
       vgs             0.769619             0.839963             0.765156
       vth             0.690306             0.762724             0.688744
       vds             0.197654             0.571961             0.765154
      gmbs          5.02639e-05          4.61656e-05          5.09874e-05

----------------------
M1 gm/id=13.4102 vstar=0.14914
M2 gm/id=13.3988 vstar=0.149268
M3 gm/id=13.2229 vstar=0.151252
M4 gm/id=13.6046 vstar=0.147009
M5 gm/id=13.5407 vstar=0.147703
M6 gm/id=13.3713 vstar=0.149574
```

- For all transistor V*≈150 mV are less than Vds for all transistor so the region of them are the saturation region.

4. As we see Vds>Vstar for all transistor so all of them are work in saturation

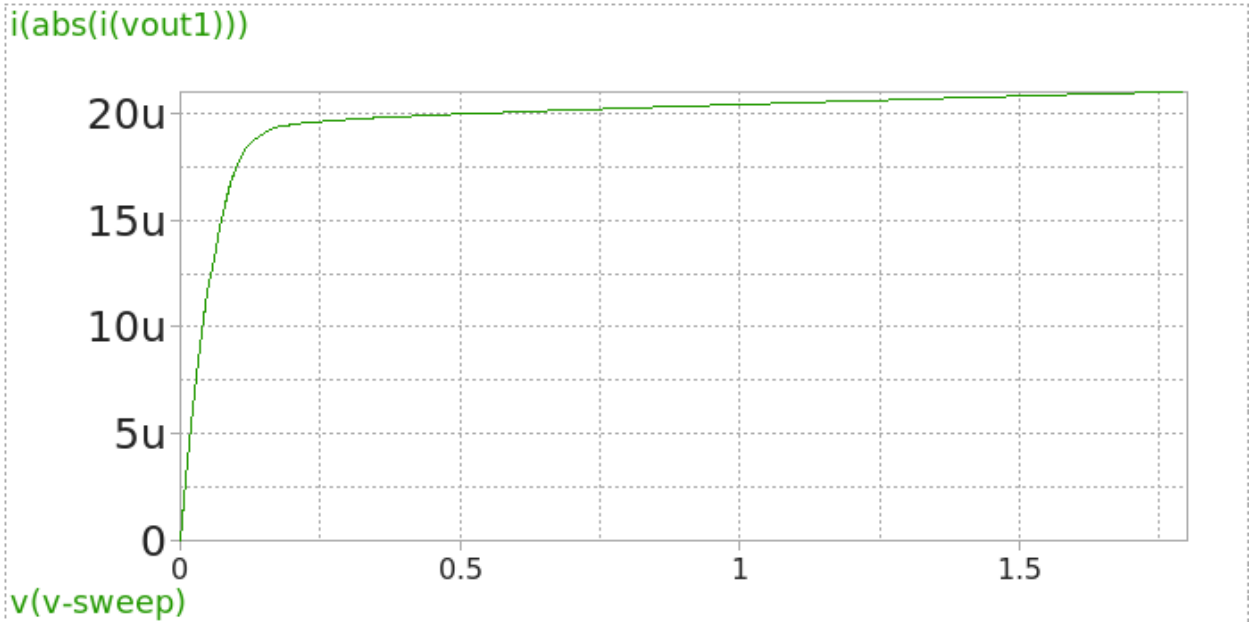
2. DC Sweep (Iout vs VOUT)

1. Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report $Iout$ vs VOUT for the two CMs overlaid in the same plot.

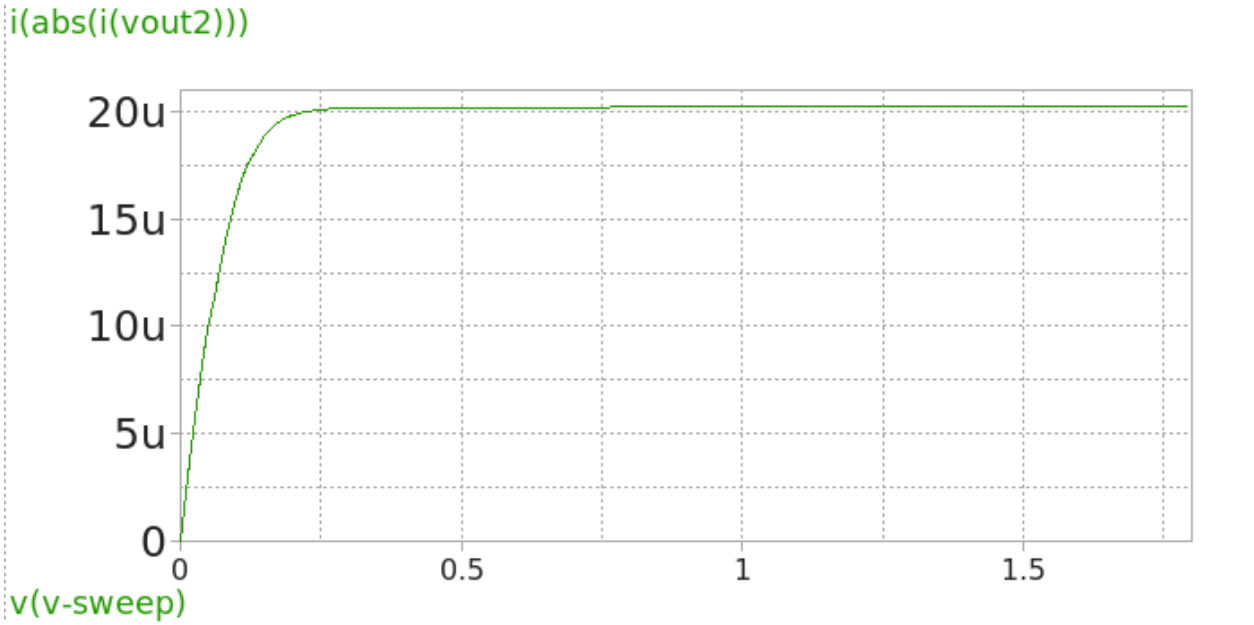


- we see that wide swing CM don't affect by Vds as simple CM but it reach the value after the simple.
- For the simple current mirror compliance voltage around 140mV for wide swing current mirror around 250 mV
- So we notice wide swing current mirror has a higher compliance voltage

- For simple CM(CM = Current Mirror)



- For wide swing current mirror

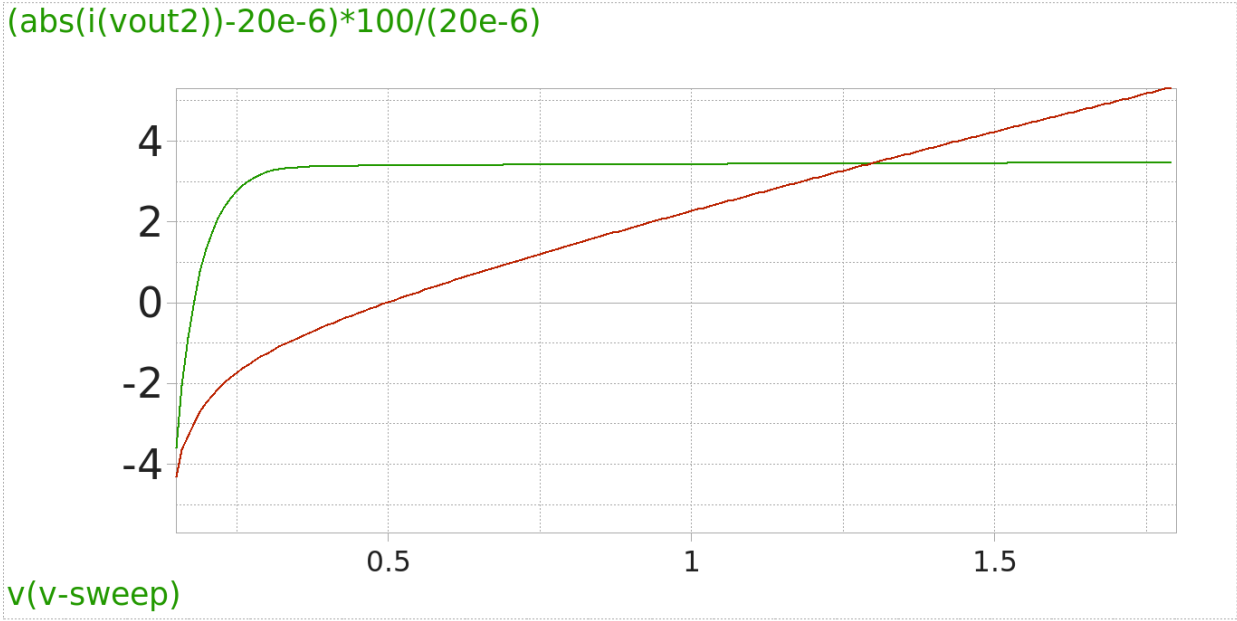


- For a simple current mirror, it has one value equal =20 µA because it has low Rout so the current changes a little with Vds

2. From ngspice terminal we calculate Id @ .5V and Id @1.5V and $\lambda = \frac{\Delta ID}{\Delta Vds} = 41.5\ mS/A$ and it meet the spics we choose

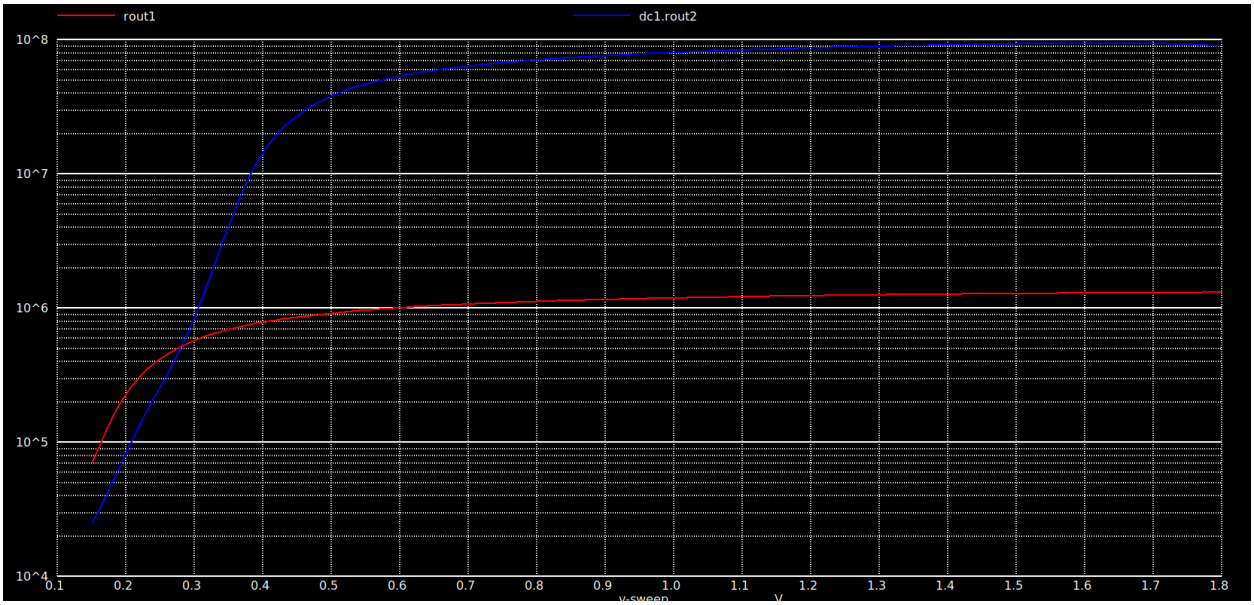
```
i.5v                    =  -1.955710e-05
i1.5v                   =  -2.038806e-05
lambda = 4.154800e-02
```

3. Percent of error in $Iout$ vs VOUT for the two CMs



- The red line for simple CM and the green for wide swing CM
- We see that the simple CM has variable precent of error and increase as vds of the transistor increase. For wide swing CM has approximately constant precent of error as vds exceed compliance voltage for each of CMs
- This effect because of the transistor has Rout and has a finite value and not infinite for ideal transistor wide swing has less variation with Vds because has high Rout than Simple CM

4. Rout vs VOUT for the two CMs (VOUT $\approx V*$to VDD)



- Rout for two CMs at Vout=VDD/2

```
Rout at Vds=.9V
for Simple CM: Rout=1.21079E+06
for wide swing CM: Rout=1.10147E+08
```

- The rout for wide swing are around 100 times bigger than simple CM
- The value of Rout Change with Vout as V_A change with the change of Vds on the transistor

5. Analytical solution

- Rout for simple CM: Rout=1/gds4 =1.24 MΩ
- Rout for Wide swing CM: Rout=Ro6(1+(gm6+gmb6)*Ro5) =104.6 MΩ

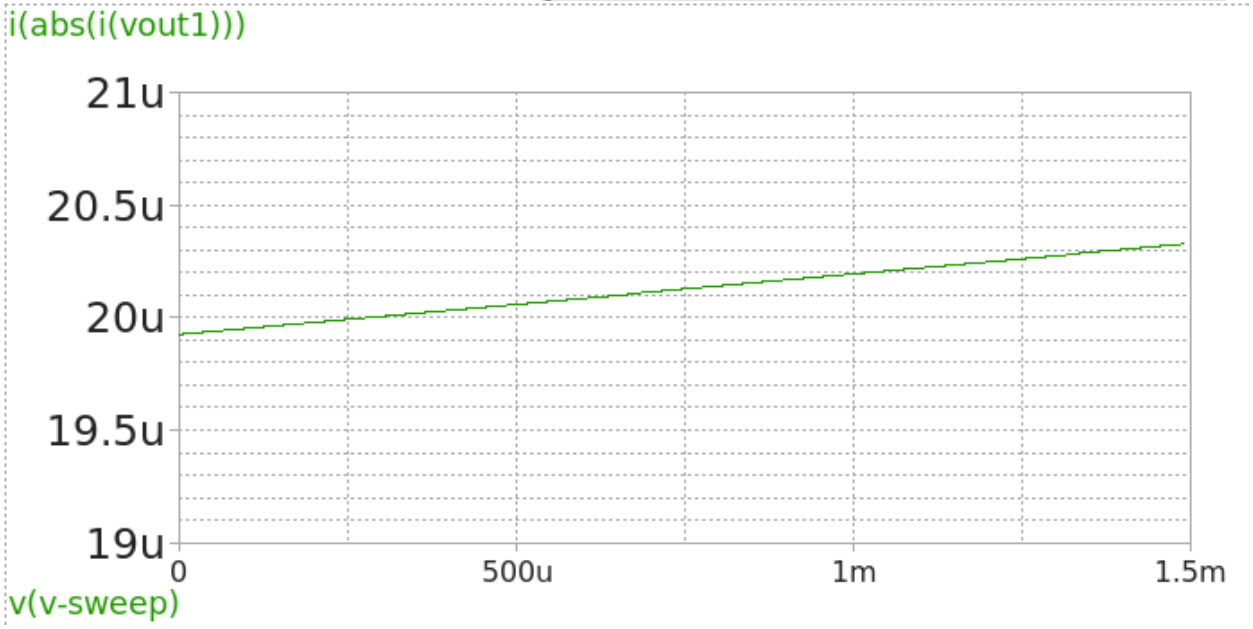
	analytical	simulation
Simple CM (MΩ)	1.24	1.21
Wide swing CM (MΩ)	104.6	110.1

3. Mismatch

1. Perform DC sweep for VMIS1 and VMIS2 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12) set VMIS3 = 0. This models the standard deviation of the mismatch in VTH for the current mirror devices. Find the percent change in $Iout$.

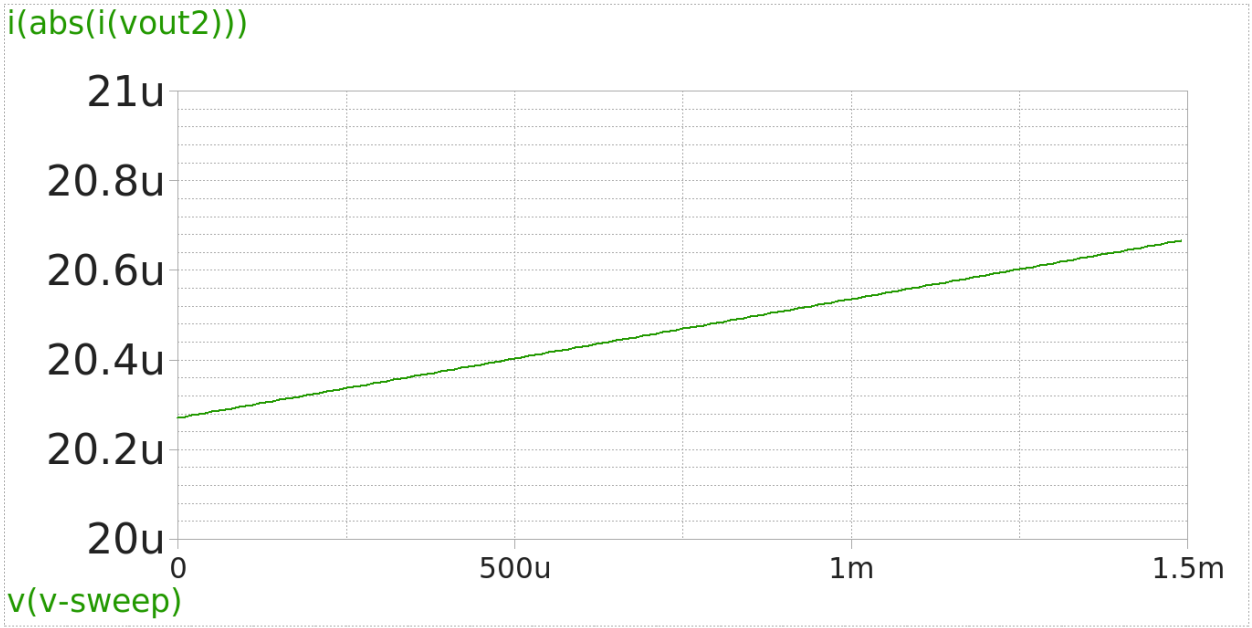
```
if                =  -1.977247e-05
is                =  -1.937566e-05
mis = -1.98405e-02
```

- For simple CM



- For Wide swing CM

```
if                =  -2.066931e-05
is                =  -2.027109e-05
mis = -1.99110e-02
```



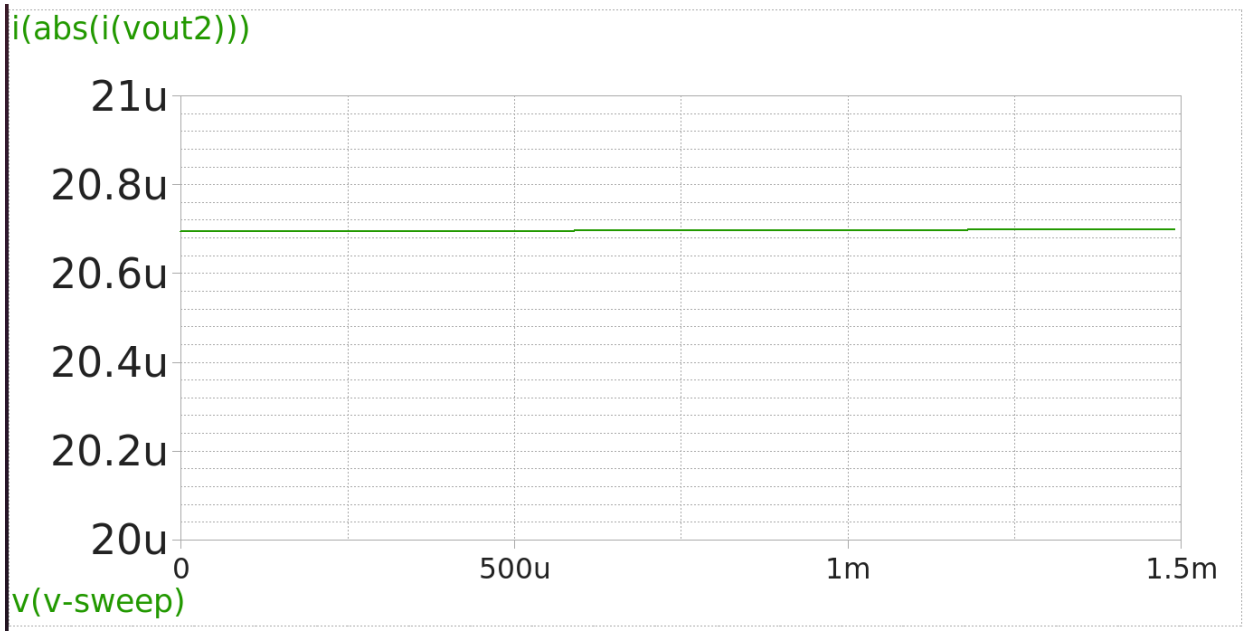
2. Analytically calculate the percent change in $Iout$

- For simple CM: $gm3 = \frac{\Delta Iout}{\Delta vin}$ so $\frac{\Delta Iout}{Iout} = \frac{-3.91*10\text{^}-7}{20*10\text{^}-6} = -.01955$
- For wide swing CM: $\frac{gm6*vin}{Iout} = \frac{\Delta Iout}{Iout} = \frac{-2.9*10^{-7}}{20*10^{-6}} = -.0195$

	Analytical	Simulation
Simple CM	-.01955	-.0198
Wide swing CM	-.0195	-.0199

- We can see that mismatch is less than 2% and this meet the specs in each circuit.
- For simple and wide swing CM they change similarly with the same change of Vth as they approximately have the same Gm=-gm and same gm

3. Set VMIS1 = VMIS2 = 0 and perform DC sweep for VMIS3 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12). This models the standard deviation of the mismatch in VTH for the cascode devices. Find the percent change in $Iout$




```
if                  =  -2.069863e-05
is                  =  -2.069347e-05
mis = -2.58000e-04
```

4. Analytically calculate the percent change in $Iout$ and compare it to the simulation result. $Gm = \frac{-gm5}{1+(gm5+gmb5)Ro6} = -2.93\ \mu s, so\ \frac{\Delta Iout}{Iout} = \frac{-4.397*10^{-9}}{20*10^{-6}} = -2.2 * 10^{-4}$

	Analytical	Simulation
Wide swing CM (10^{-6})	-220	-258

5. The pronounced change is in the VMIS1&VMIS2 at the mirror device, because the mirror device is changing in the vgs directly so it affects the Iout by large amount but in case of VMIS3 the change in current is very small because it changes the Vgs of the degenerated Common Source has Ro6 as Rs so it has low Gm and less effect on the current but Gm for M6 and M4 is larger as it is common source and don't have a degenerated resistance at source
6. The better design decisions is setting the same W and L for simple CM and wide swing CM to make sure that the devices is matched and having the expected current from the ratio.