وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design – Xschem/Ngspice and ADT
Lab 05
Simple vs Wide Swing (Low Compliance) Cascode Current Mirror

Intended Learning Objectives

In this lab you will:

- Explore current mirror sizing trade-offs using Sizing Assistant (SA).
- Bias a cascode device using a series resistance.
- Design and simulate simple and wide swing (low-voltage) current mirrors.
- Compare simple and wide swing current mirrors.
- Investigate the effect of mismatch on a wide swing current mirror.

NOTE: To get access to the Sizing Assistant (SA) please register at https://adt.master-micro.com/ and create a support ticket from your dashboard. Verified instructors may also request access to an editable MS Word version of the labs and the model answers.

NOTE: The values and charts used in the lab document assume the provided 180 nm educational device models and 1.8 V supply. Other models/technologies can be used by applying reasonable adjustments to the lab values whenever necessary.

Part 1: Exploring Sizing Tradeoffs Using SA

1) We want to design a simple current mirror with the following specs.

Parameter	
Current direction (source/sink)	Sink
Input Current	$10\mu A$
Output Current	$20\mu A$
% Change in Current for $\Delta V_{out} = 1V$	$< 10\%$
Percent mismatch: $\sigma(I_{out})/I_{out}$	$\leq 2\%$
Compliance voltage	$\leq 150mV$
Area	Minimize

2) Sinking current means which device type? NMOS or PMOS?

3) The % Change in current translates to a spec on the $\lambda = 1/V_A$ of the device. How much is the required λ?

4) The current mirror design trade-offs are summarized in the table below.

Parameter	Higher gm/ID (lower V^*)	Lower gm/ID (higher V^*)
Area	☹	😊
Dependence on V_{DS} (output resistance, $\lambda = 1/V_A$)	☹	😊
Random mismatch	☹	😊
Systematic mismatch	☹	😊
Compliance voltage (headroom)	😊	☹

5) Examine these trade-offs using SA. Use SA to plot the sizing at a constant $\boldsymbol{\sigma(I_{out})/I_{out}}$ which is given by

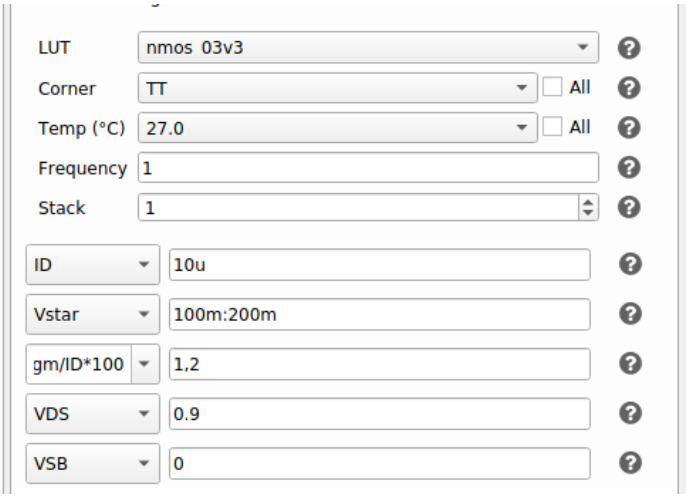
$$\frac{\boldsymbol{\sigma(I_{out})}}{\boldsymbol{I_{out}}} = \frac{\sqrt{\mathbf{1}+\frac{\mathbf{1}}{\boldsymbol{m}}} \times \frac{\boldsymbol{A_{V_T}}}{\sqrt{WL}} \times \boldsymbol{mg_m}}{\boldsymbol{mI_D}} \times \mathbf{100}$$

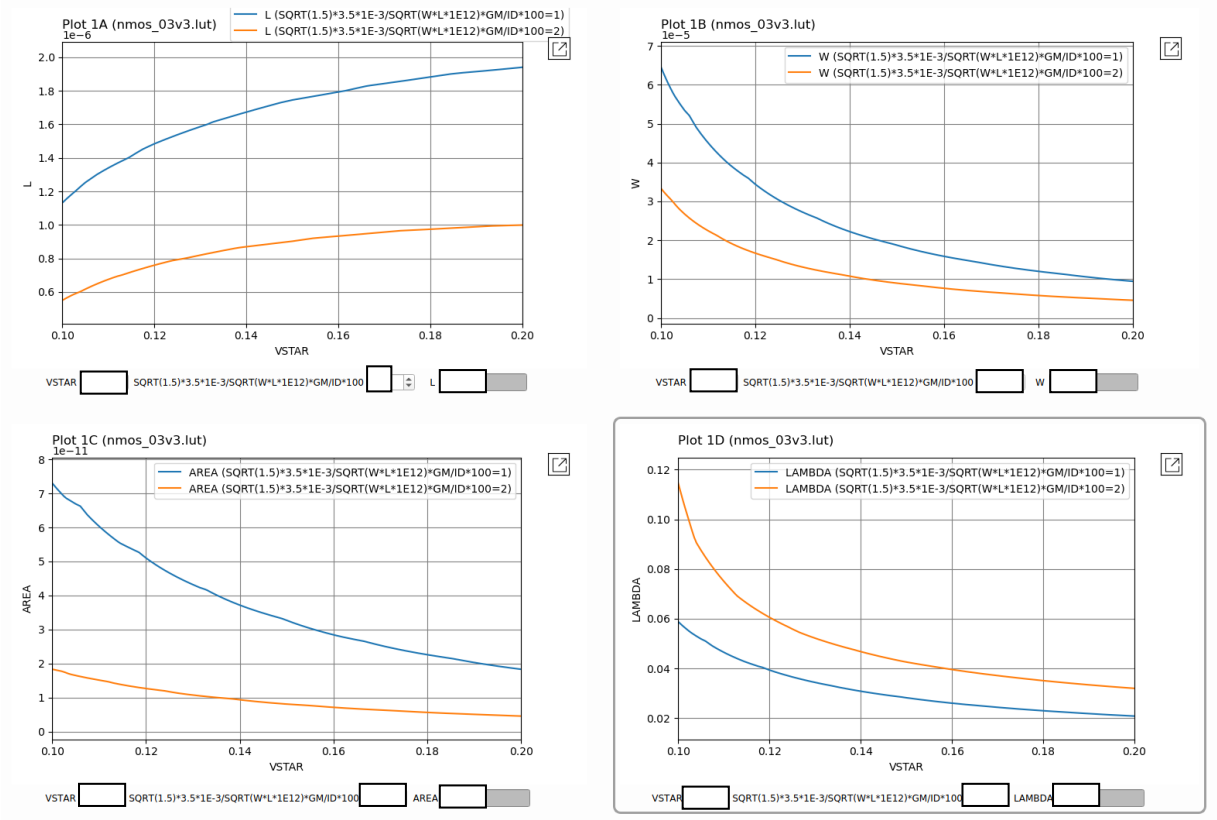
Where m is the mirroring ratio, $\boldsymbol{A_{V_T} = 3.5mV \cdot \mu m}$ is Pelgrom's coefficient, and the $\sqrt{1+\frac{1}{m}}$ factor is due to taking into account the effect of two random variables (V_{TH} of the two current mirror transistors).

- From VM ware open ADT
  1. Open a terminal in the directory: "/home/tare/ADT_Working_Directory"
  2. Run the command: "./start_adt.sh"
- Load LUTs files (file - load LUT - open nmos_3p3).
- Open Sizing Assistant and set the parameters as shown below.
- to plot the sizing at a constant $\boldsymbol{\sigma(I_{out})/I_{out}}$ = 1,2 set a parameter with this value:

sqrt(1.5)*3.5*1E-3/sqrt(W*L*1E12)*gm/ID*100

➔ ADT Hint: If the LUT contains mismatch data, we can directly use the parameter idmis in SA to get the standard deviation of the current random variations **'idmis_% = sqrt(1.5)*idmis/ID*100'**. The mismatch data can be added to any LUT using ADT by using an appropriate Monte Carlo mismatch model file.





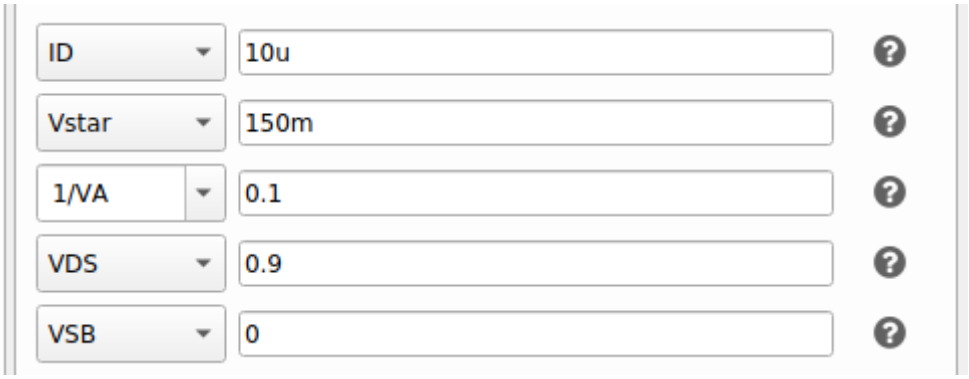
6) Can we do the previous design trade-offs exploration sweeps using a standard SPICE simulator, i.e., sweep Vstar at a constant $\boldsymbol{\sigma(I_{out})}/I_{out}$? Why?

7) The above results mean that the highest V^* is desirable from the perspective of mismatch, area, and λ. Thus, V^* will be limited by the required compliance voltage.
NOTE: We assume that the compliance voltage $\approx V_{DSsat} \approx V^*$.

8) **Report** the above plot with a cursor added at the required V^*. Does this point satisfy the mismatch and λ constraints?

9) If the λ constraint is not satisfied at $\boldsymbol{\sigma(I_{out})}/I_{out} = 2\%$, i.e., it needs a longer L, we can use SA to find the required design point as shown below.

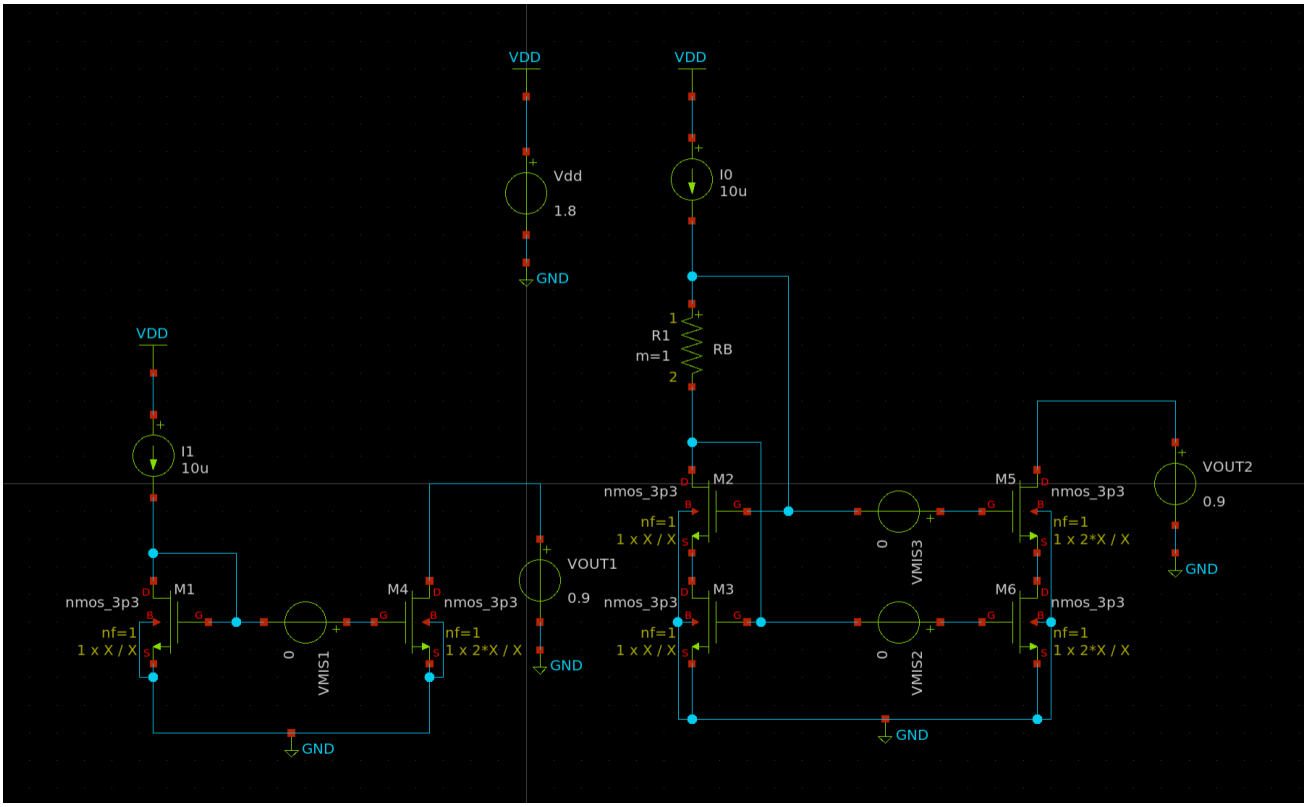
Since all constraints are satisfied at $\boldsymbol{\sigma(I_{out})}/I_{out} = 2\%$, no need to redesign but in case the conditions were not satisfied we will do as following



10) **Report** the device sizing and $\boldsymbol{\sigma(I_{out})}/I_{out}$ at the selected design point.

Part 2: Current Mirror Simulation

1) Create a new schematic. Construct the circuit shown below.



2) The current mirror takes input current IB and generates output current = 2*IB (note the multiplier setting in the output branch).
3) Instead of using a wide-swing bias transistor (a magic battery) to generate VB, we use a resistor RB in series with the input branch.
4) Unless otherwise stated, set VOUT = VDD/2 and VMIS1 = VMIS2 = VMIS3 = 0.

1. Design and OP (Operating Point) Analysis

1) Assume we want to set a $50mV$ saturation margin for M6 and M3, i.e., $V_{DS6} \approx V_{DS3} \approx V^* + 50mV$. Ignore the body effect and **calculate** a rough value for RB.
   Hint: $R_B = \frac{V_{GS5}+V_{DS6}-V_{GS6}}{I_B} \approx \frac{V_{DS6}}{I_B}$
   Hint: The purpose of doing rough analysis is not to reach a final design point, but to calculate a value that makes sense and can be used to determine a reasonable range for a simulator sweep.
2) Perform DC sweep (not parametric sweep) for RB. Choose a reasonable sweep range given the rough value computed in the previous step. **Report** V_{DS6} vs R_B. **Choose** R_B to satisfy the $50mV$ saturation margin requirement. Is the selected R_B value larger or smaller than the rough analytical value? Why?

(NOTE: Take care for the device name in the code depends on your schematic)

```
.control
save all
save @m.xm6.m0[vds]
dc R1 21K 30K 300
remzerovec
write CM_TB_final.raw
show m : id : gm : gds : vgs : vth : vds
.endc
```

During Lab05 to show the plots the same steps below should applied

- Netlist
- Simulate
- Waves then choose DC and then choose the raw file in which you save the data and in the waveform graph choose the output you want to plot

➔ Hint: The DC sweep is performed in a simulator inner loop, so it is very fast and takes small disk space. The parametric sweep is an outer loop repetitive calling of the simulator, so it is much slower and takes much larger disk space.

3) Simulate the OP point. Report a snapshot clearly showing the following parameters.

ID
VGS
VDS
VTH
VDSAT
Vstar = 2/(gm/ID)
gm/ID
GM
GDS
GMB
Region

```
.control
save all
save @m.xm1.m0[gm]
op
show m : id : gm : gds : vgs : vth : vds : gmbs
.endc
```

4) Do all transistors operate in saturation?

2. DC Sweep (I_{out} vs VOUT)

1) Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report I_{out} vs VOUT for the two CMs overlaid in the same plot.
    - Comment on the difference between the two circuits.

To plot the I_{out} vs VOUT for the two current mirrors overlaid use this code:

```
.control
dc vout2 0 1.8 0.01
remzerovec
write CM_TB_final.raw abs(i(vout2))
set appendwrite
dc vout1 0 1.8 0.01
remzerovec
write CM_TB_final.raw abs(i(vout1))
.endc
```

- From the plot, find an estimate for the compliance voltage of each current mirror.

We need to plot I_{out} of each current mirror separately, to plot the current of simple only use the code below

```
.control
op
show m : id : gm : gds : vgs : vth : vds : gmbs
dc vout1 0 1.8 0.01
remzerovec
write CM_TB_final.raw abs(i(vout1))
.endc
```

to plot the current of Wide swing only use the code below

```
.control
op
show m : id : gm : gds : vgs : vth : vds : gmbs
dc vout2 0 1.8 0.01
remzerovec
write CM_TB_final.raw abs(i(vout2))
.endc
```

- I_{out} of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?

HINT: use the code of simple current mirror above

2) For the simple current mirror, calculate the percent change in I_{out} when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1.

HINT: use the code of simple current mirror above

3) Report the percent of error in I_{out} vs VOUT (ideal I_{out} should be IB*2) for the two CMs in the current mirror operating region (VOUT $\approx V^*$to VDD) overlaid in the same plot.
   Hint: Calculate percent of error as (simulated – ideal)/ideal * 100
   - Comment on the difference between the two circuits.

```
.control
dc vout2 0.15 1.8 0.01
remzerovec
write CM_TB_final.raw (abs(i(vout2))-20u)*100/20u
set appendwrite
op
show m : id : gm : gds : vgs : vth : vds : gmbs
dc vout1 0.15 1.8 0.01
remzerovec
write CM_TB_final.raw (abs(i(vout1))-20u)*100/20u
.endc
```

4) Report Rout vs VOUT (take the inverse of the derivative of I_{out} plot) for the two CMs in the current mirror operating region (VOUT $\approx V^*$to VDD) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2.
    - Comment on the difference between the two circuits.
    - Does Rout change with VOUT? Why?

➔ Cadence Hint: Rout can also be simulated using AC analysis. The value we used here should be similar to the AC analysis result at low frequencies.

```
.control
dc vout2 0.15 1.8 0.01
remzerovec
write CM_TB_final.raw 1/deriv(abs(i(vout2)))
set appendwrite
op
show m : id : gm : gds : vgs : vth : vds : gmbs
dc vout1 0.15 1.8 0.01
remzerovec
write CM_TB_final.raw 1/deriv(abs(i(vout1)))
.endc
```

5) Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.

3. Mismatch

NOTE: Usually we study the mismatch using Monte Carlo simulation as will be shown in the next section. However, in this section, we will manually add mismatch in the circuit.

1) Perform DC sweep for VMIS1 and VMIS2 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12) using the code below and set VMIS3 = 0. This models the standard deviation of the mismatch in V_{TH} for the current mirror devices. Find the percent change in I_{out}.

For simple current mirror use the code below

```
.control
dc VMIS1 0 1.50m 0.01m
remzerovec
write CM_TB_final.raw abs(i(vout1))
op
show m : id : gm : gds : vgs : vth : vds : gmbs
.endc
```

For Wide swing CM us the code below

```
.control
dc VMIS2 0 1.50m 0.01m
remzerovec
write CM_TB_final.raw abs(i(vout2))
op
show m : id : gm : gds : vgs : vth : vds : gmbs
.endc
```

2) Analytically calculate the percent change in I_{out} and compare it to the simulation result.
Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a cascode amplifier.

3) Set VMIS1 = VMIS2 = 0 and perform DC sweep for VMIS3 from 0 to sqrt(1.5)*3.5m/sqrt(W*L*1e12). This models the standard deviation of the mismatch in V_{TH} for the cascode devices. Find the percent change in I_{out}.

```
.control
dc VMIS3 0 1.50m 0.01m
remzerovec
write CM_TB_final.raw abs(i(vout2))
op
show m : id : gm : gds : vgs : vth : vds : gmbs
.endc
```

4) Analytically calculate the percent change in I_{out} and compare it to the simulation result.
   Hint: The voltage change at the gate can be considered as a small signal. Thus, the change in the current can be calculated using the G_m of the circuit. In this case, the circuit can be considered as a ***degenerated*** common source amplifier.

5) Which mismatch contribution is more pronounced? Why?

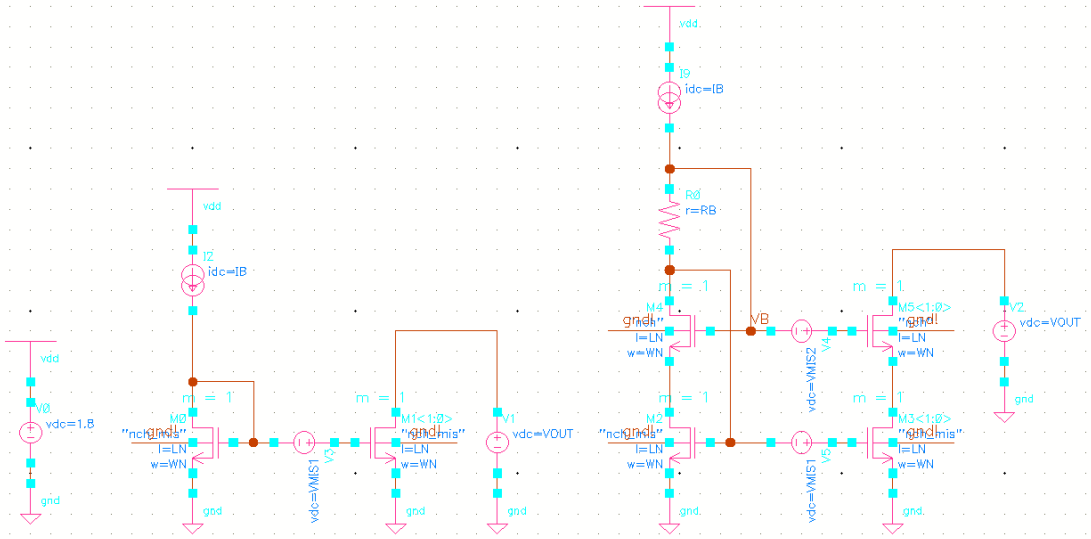
6) Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?

4. Monte Carlo (MC) Simulation (OPTINAL) (for Cadence only)

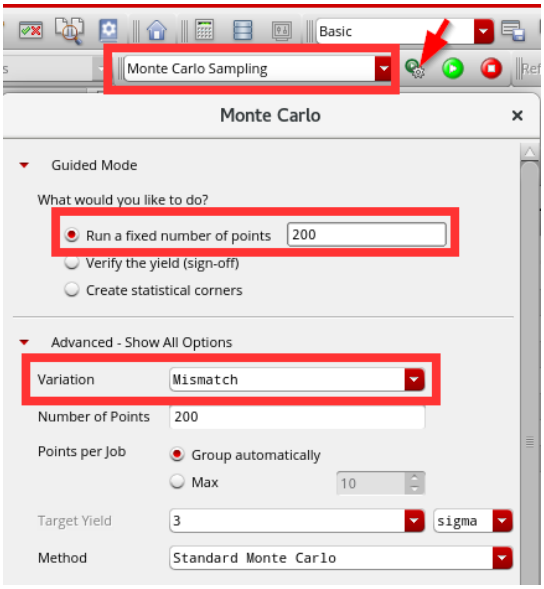
NOTE: Use the model file ee214b_mis.sp which includes the mismatch models of the devices.

NOTE: Using the multiplier parameter can give wrong mismatch results for the given model file because the errors from the parallel devices will be correlated. Thus, set m = 1, and name the device as an array of two devices 'Mx<1:0>' as shown in the schematic below. Check this article for more information.

NOTE: In this section we will set both VMIS1 and VMIS2 to zero.



1) Change the model name of the mirror devices to be 'nch_mis' to include their mismatch effect. Keep the model of the cascode devices as 'nch'.
   Hint: Open the model file and see how the mismatch is modeled in the nch_mis subcircuit.
2) From ADE, set up Monte Carlo (MC) simulation for mismatch only as shown below.



3) Report a plot for the histogram of I_{out}.
   Hint: You can measure the OP current of the voltage source connected to the output node.
   Ex: abs(pv("V1" "i" ?result "dcOpInfo"))
4) Calculate the standard deviation percentage $\boldsymbol{\sigma(I_{out})/I_{out}}$.
5) Compare the MC simulation result to the expected analytical result.
6) Set the mirror devices model to 'nch' and the cascode devices model to 'nch_mis'. Repeat all the above steps.

Lab Summary

In Part 1 you learned:

- How to use SA to examine current mirror design trade-offs.
- How to design a simple current mirror.

In Part 2 you learned:

- How to design a wide swing (low-voltage) current mirror.
- How the behavior of a simple current mirror changes with the output voltage.
- How the behavior of a wide swing current mirror changes with the output voltage.
- The effect of mismatch on a wide swing current mirror.
- How to perform Monte Carlo simulations for a current mirror circuit.

Acknowledgements

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