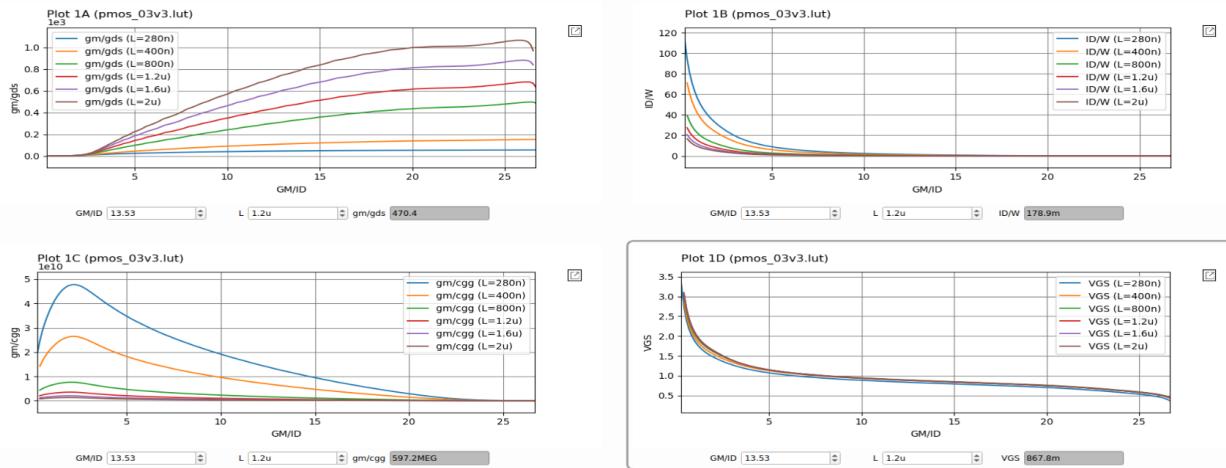


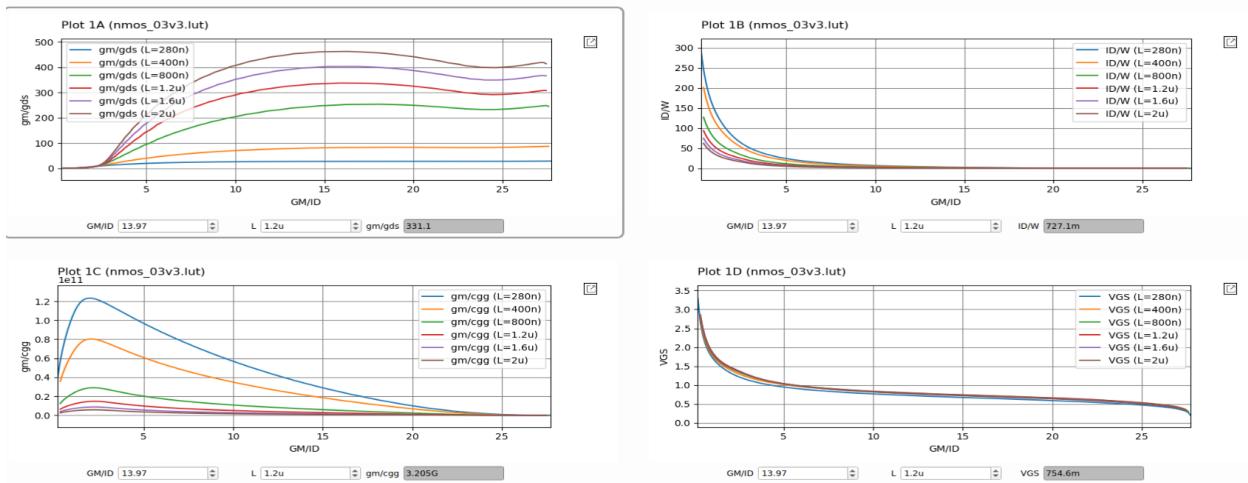
ITI CMOS Analog IC Design 2024
Lab 09 (**Mini Project 01**)
Two-Stage Miller OTA

PART 1: gm/ID Design Charts

- Plotting design charts vs gm/ID for PMOS.



- Plotting the following design charts vs gm/ID for NMOS.



PART 2: OTA Design

By using gm/Id methodology to design a differential input, single-ended output **two-stage Miller-compensated OTA**. The OTA is to be used as a buffer (unity gain feedback configuration) to probe sensitive internal signals in a complex mixed-signal design. The OTA should achieve the specs below.

Technology	0.18μm
Supply voltage	1.8V
Static gain error	<= 0.05%
CMRR @ DC	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°
OTA current consumption	<= 60μA
CMIR – high	>= 1V
CMIR – low	<= 0.2V
Output swing	0.2 – 1.6V
Load	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns
Slew rate (SR)	5V/μs

- Use an ideal external 10μA DC current source in your test bench (not included in the OTA current consumption spec), but design your own bias circuit (current mirrors). Create a schematic and an appropriate symbol for the OTA.

Design Procedure

- As the CMIR is near to the ground rail and far from VDD rail must choose PMOS as input pair for the first stage
- for the second stage must use NMOS to get the same voltage of the NMOS load current in the first stage to cancel the dc offset between the two transistors.
- A reasonable starting point for C_C is $0.5C_L$
- Calculate the unity gain frequency (UGF) from the rise time requirement ($t_{rise} = 2.2\tau$)

$$2.2\tau = t_{rise} \text{ and } t_{rise} \leq 70\text{ns} \rightarrow \tau \leq 31.8\text{ns} \rightarrow f_u = \frac{A_{CL}}{2\pi\tau_{CL}}$$

$$= \frac{1}{2\pi * 31.8\text{ns}} = 5\text{MHz}$$

$$f_u = \frac{g_{m1}}{2\pi C_c} \rightarrow g_{m1} = 2\pi * f_u * C_c = 78.54\mu S \approx 80\mu S$$

- From the SR requirement, calculate the current required in the first stage

$$(I_{B1}): SR = \frac{I_{B1}}{C_C}$$

$$SR = 5V/\mu s = \frac{I_{B1}}{C_C} \rightarrow I_{B1} = \frac{5V}{\mu s} * 2.5pF \rightarrow I_{B1} = 12.5 \mu A$$

let's choose $I_{B1} = 15\mu A$ then $I_{D1,2} = 7.5\mu A$ and $I_{B2} \leq 45\mu A$

$$\frac{g_m}{I_D} = 10.67 \rightarrow \text{let's choose } \frac{g_m}{I_D} = 12 \text{ to get high efficiency then } g_m = 90\mu S$$

it'll make higher bandwidth but less V_{GS} to try less the error in CMIR

- From static error specs $\epsilon_s \approx \frac{1}{\beta A_{OL}} \leq .05\% = \frac{1}{1*A_{OL}} \leq .0005 \rightarrow A_{OL} \geq 2000$

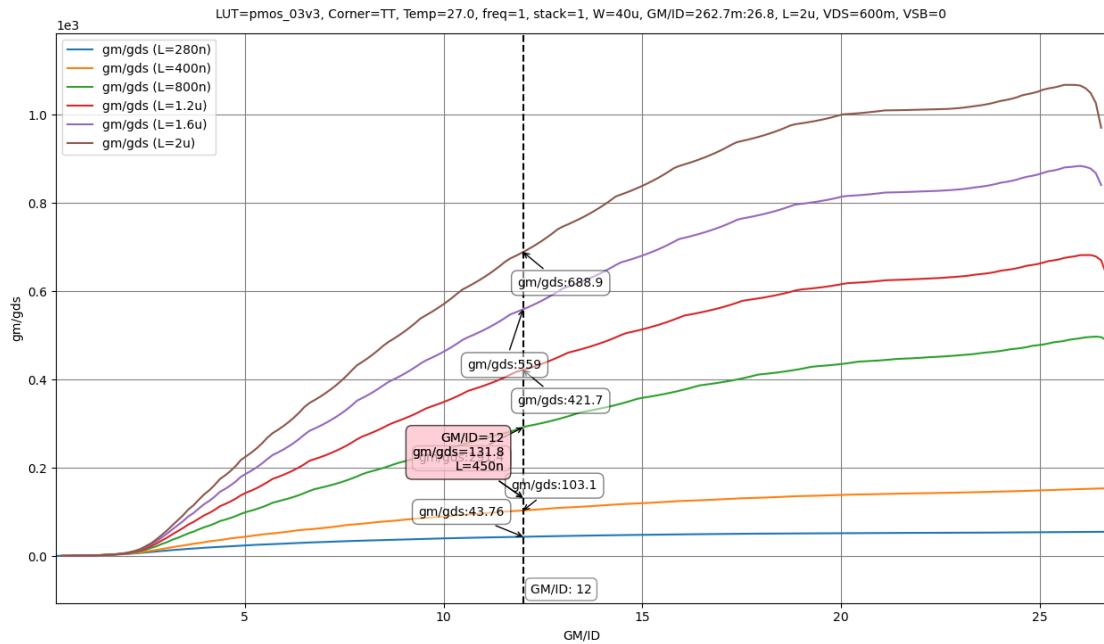
*gain = $20 * \log(2000) = 66dB$ by assume the 1_{st} stage has double the*

gain so $A_{v1} = 36dB$ and 2_{nd} stage $A_{v2} = 30dB$

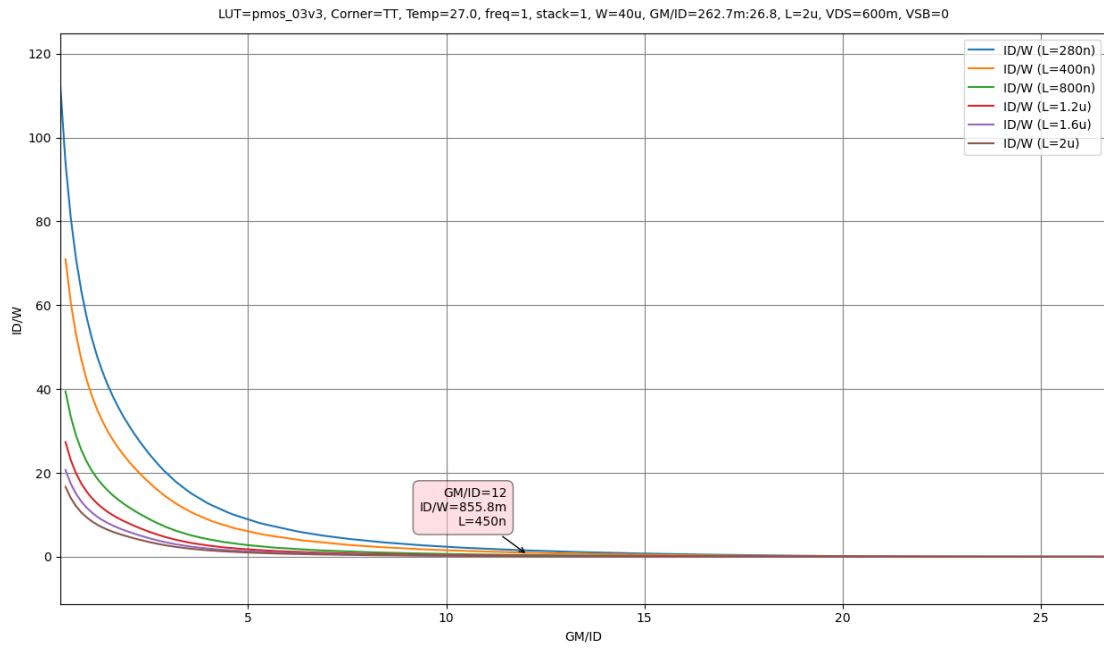
- As we need the gain from the first stage and the swing from the second stage
- By assuming input pair and load current mirror has the same gds
- calculate L (channel length) of the 1st stage input
- Note: I cancel the body effect by connect bulk with source to reduce Vgs of the input pair to get high CMIR

Design charts for PMOS input pair

$$A_{v1} = 36dB \approx 63 = \frac{g_{m1}}{2g_{ds1}} \rightarrow \frac{g_{m1}}{g_{ds1}} = 126 \rightarrow g_{ds1} = 684.5nS$$



- So, L=450nm for the first stage
- Determine the Width of the input pair



- For input pair we need $\frac{g_m}{I_D} = 12$ & $L = 450nm$ and $W = \frac{7.5\mu A}{.8558} = 8.8\mu m$
- Given the PM spec, calculate gm/ID of the second stage input transistor
- For $PM \geq 72$ we need $\frac{\omega_{p2}}{\omega_u} \geq 3$

$$\omega_{p2} \geq 3\omega_u \rightarrow \frac{g_{m2}}{C_L} \geq \frac{3g_{m1}}{C_C} \rightarrow g_{m2} \geq 3g_{m1} * \frac{C_L}{C_C} \geq 540\mu S \text{ & } I_{B2} \leq 45\mu A$$

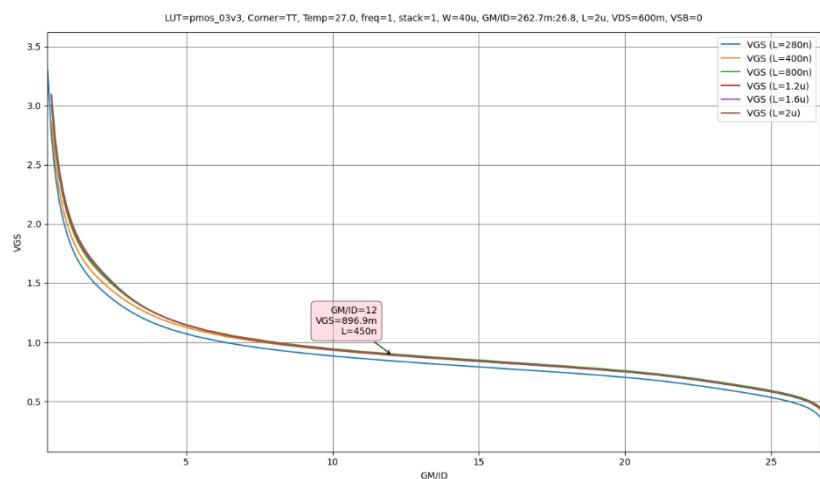
$$\frac{g_{m2}}{I_{D2}} \geq 12 \text{ let's design for } \frac{g_m}{I_D} = 13 \text{ and } I_{B2} = 45\mu A \text{ so } g_m = 585\mu S$$

$$VICM_{high} \geq V_{DD} - V_{dsat5} - |V_{GS1,2}|$$

$$V_{dsat5} \geq V_{DD} - |V_{GS1,2}| - VICM_{high}$$

$$V_{dsat5} > 1.8 - .897 - 1 > -97mV$$

- and this is not realistic value and it's not achievable as Vth for this technology bigger than 800mV so for reasonable value I reduce CMIR high to 750mV to get good biasing for input pair and tail current source



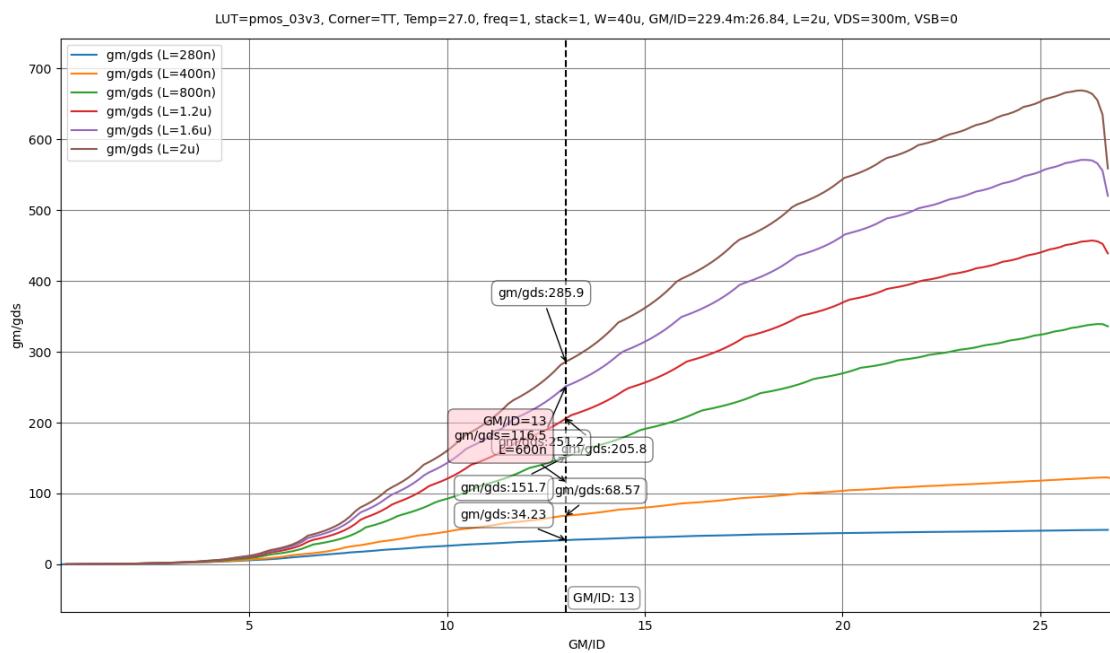
$CMIR_{high} = .75$ and this make $V_{dsat5} > 153mV$

- For output load $V_{dsat7} = V_{DD} - \text{high outputswing} = 1.8 - 1.6 = 200mV$
- So we will take V_{dsat} of the tail current source
- Use the CMRR spec to find gds of the tail current source

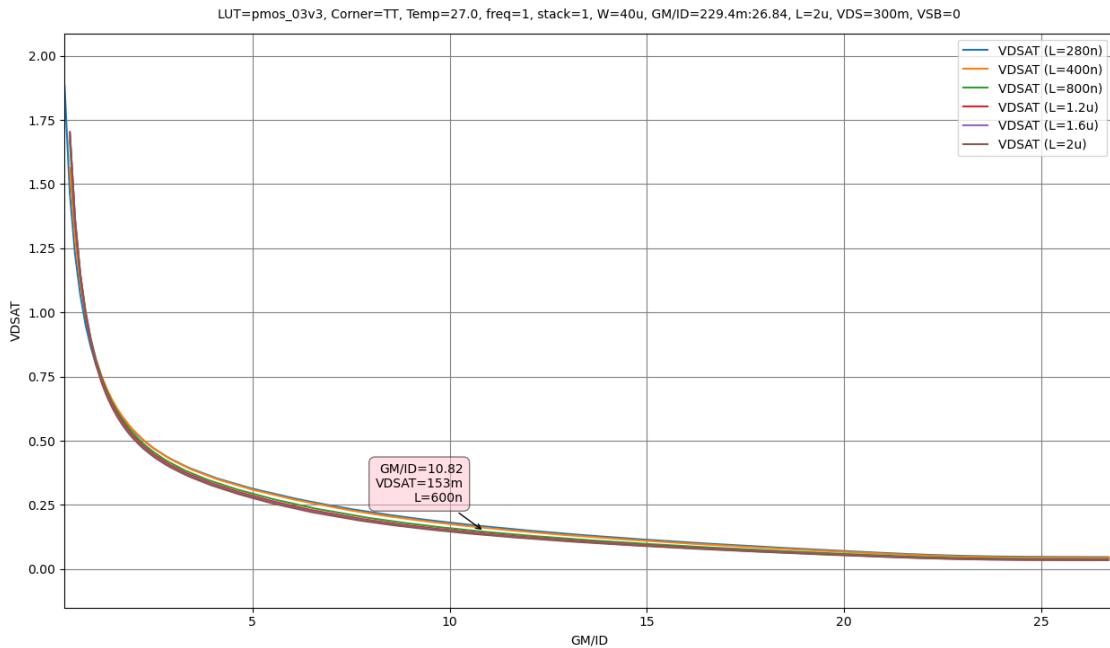
$$\frac{1}{2g_{m3,4} * R_{SS5}} < -38dB < .0126 \rightarrow \text{let's assume } \frac{g_{m3}}{I_{D3}} = 10 \rightarrow g_{m3,4} = 75\mu S$$

$$g_{ds5} < 1.89\mu S \rightarrow \frac{g_{m5}}{g_{ds5}} > 103.175$$

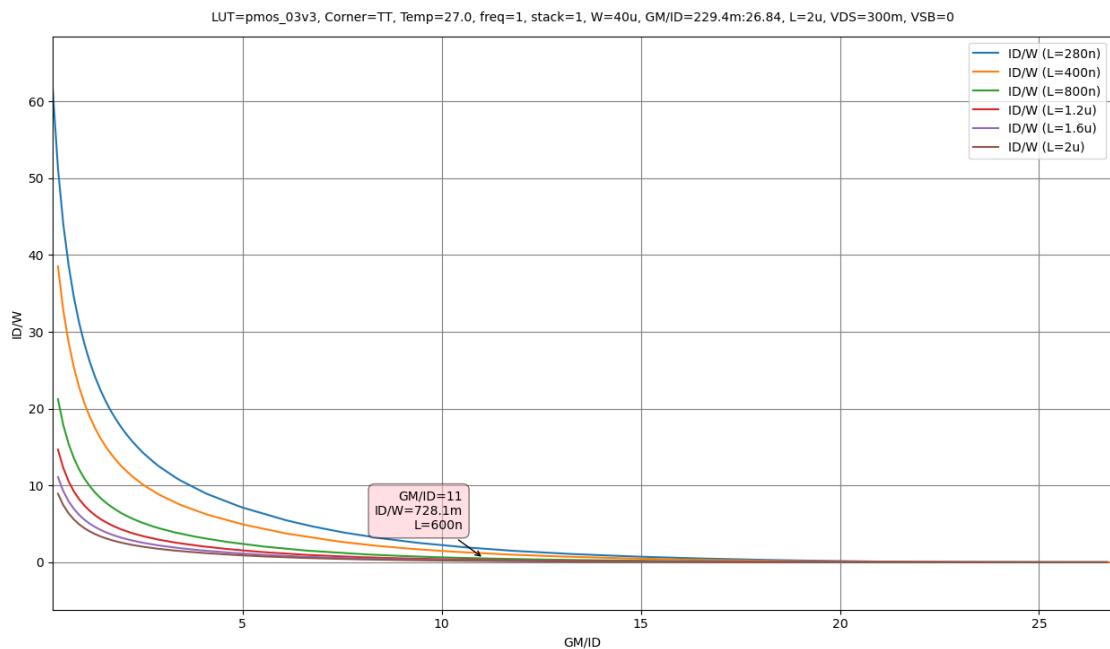
Design Charts for PMOS tail current source



- L=600nm for tail current source

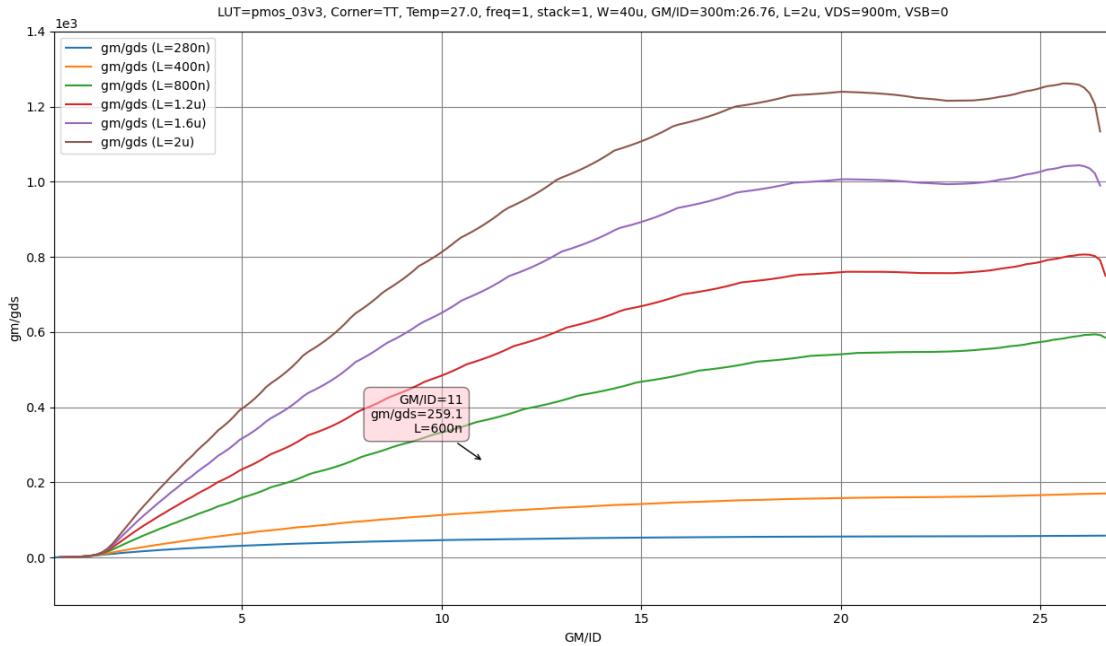


$$\frac{g_m}{I_D} > 10.82 \rightarrow \frac{g_m}{I_d} = 11$$



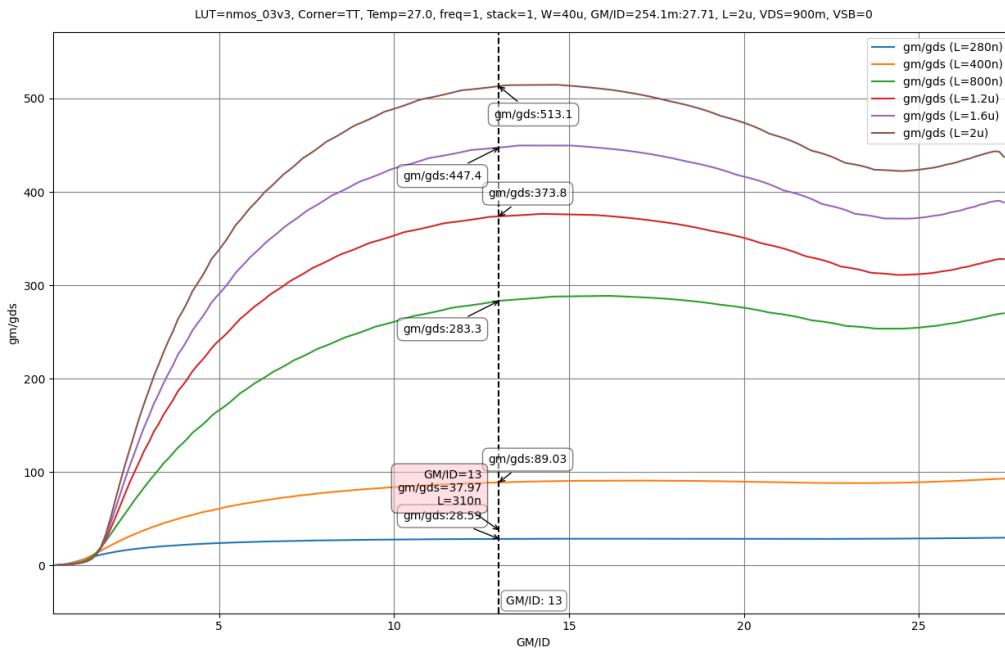
- For $5\mu A$ in the unit transistor we need $W = \frac{5}{.7281} = 6.87\mu m$ & $L = 600nm$ and $\frac{g_m}{I_D} = 11$

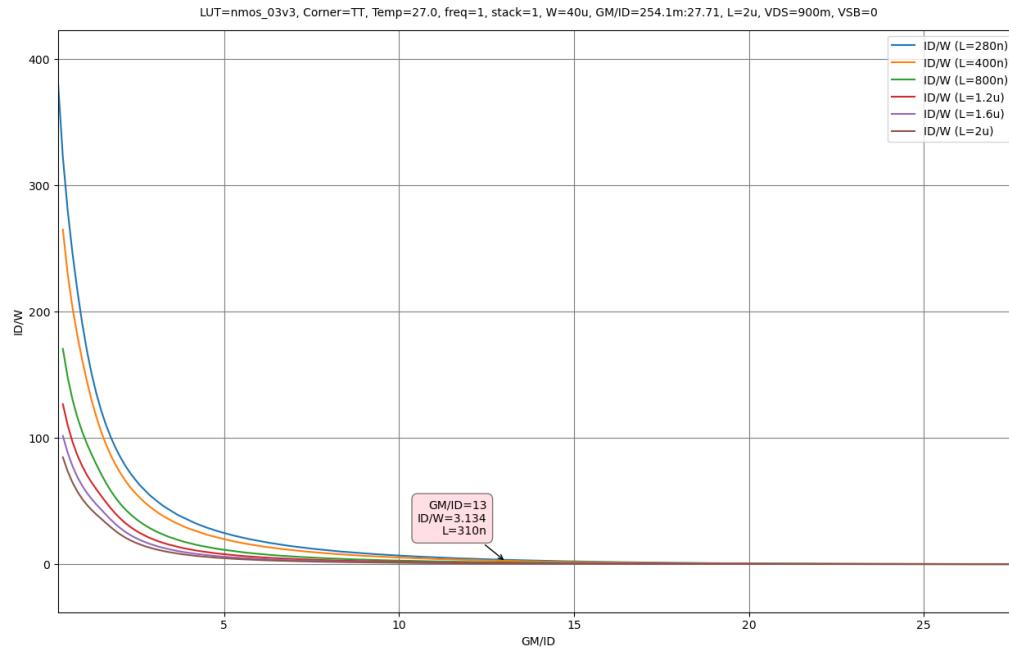
Design for NMOS input for second stage



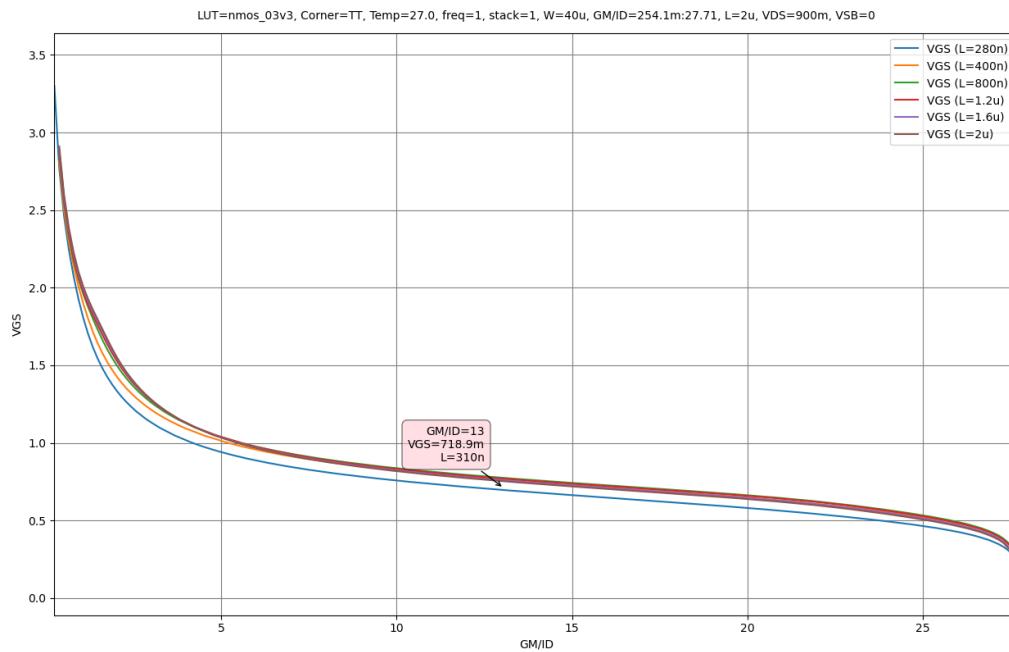
$$g_{ds7} = \frac{g_{m7}}{259.1} = \frac{\frac{g_m}{I_D} * I_{B2}}{259.1} = \frac{11 * 40\mu S}{259.1} = 1.7\mu S$$

$$g_{m6} * \left(\frac{1}{g_{ds6}} \parallel \frac{1}{g_{ds7}} \right) = 32 \rightarrow g_{ds6} = 15.8\mu S \rightarrow \frac{g_{m6}}{g_{ds6}} \geq 37$$



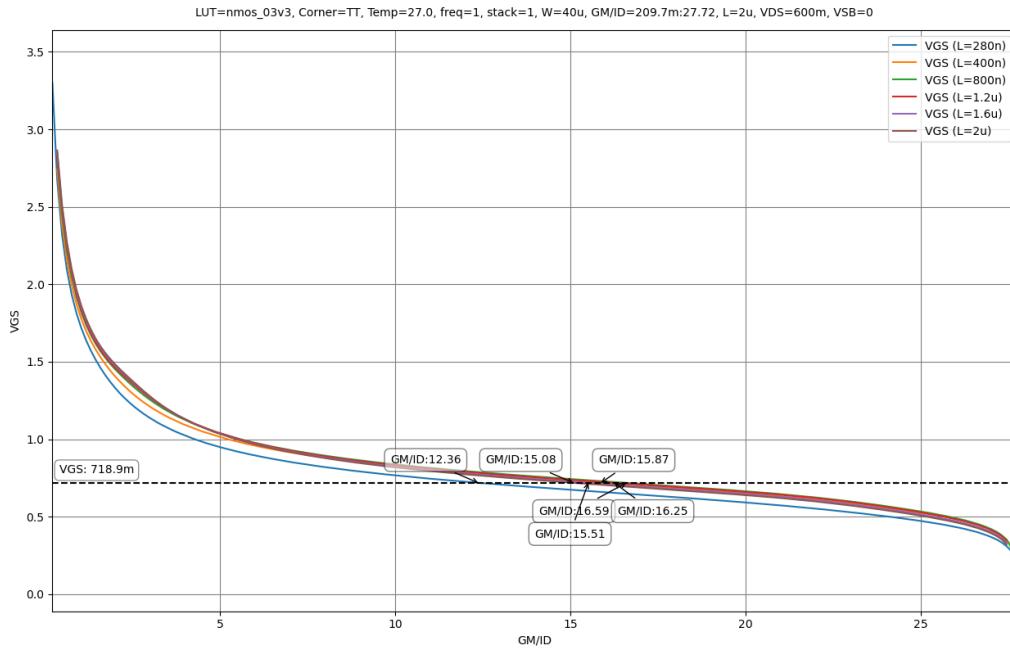


- $- W = \frac{45\mu A}{3.134} = 14.36\mu m$ and $L = 310nm$ and $\frac{g_m}{I_D} = 13$



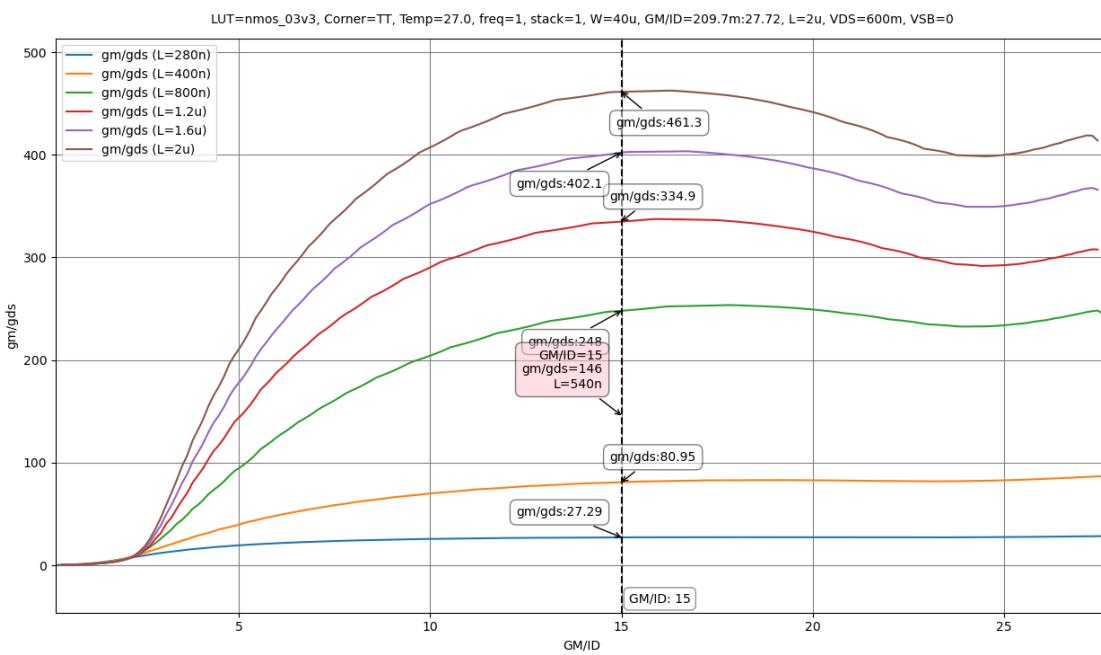
- Then for the load current mirror in the first stage need $V_{GS}=718.9mV$
- To achieve minimum output swing need $V^* < 200mV$ then $\frac{g_m}{I_D} > 10$

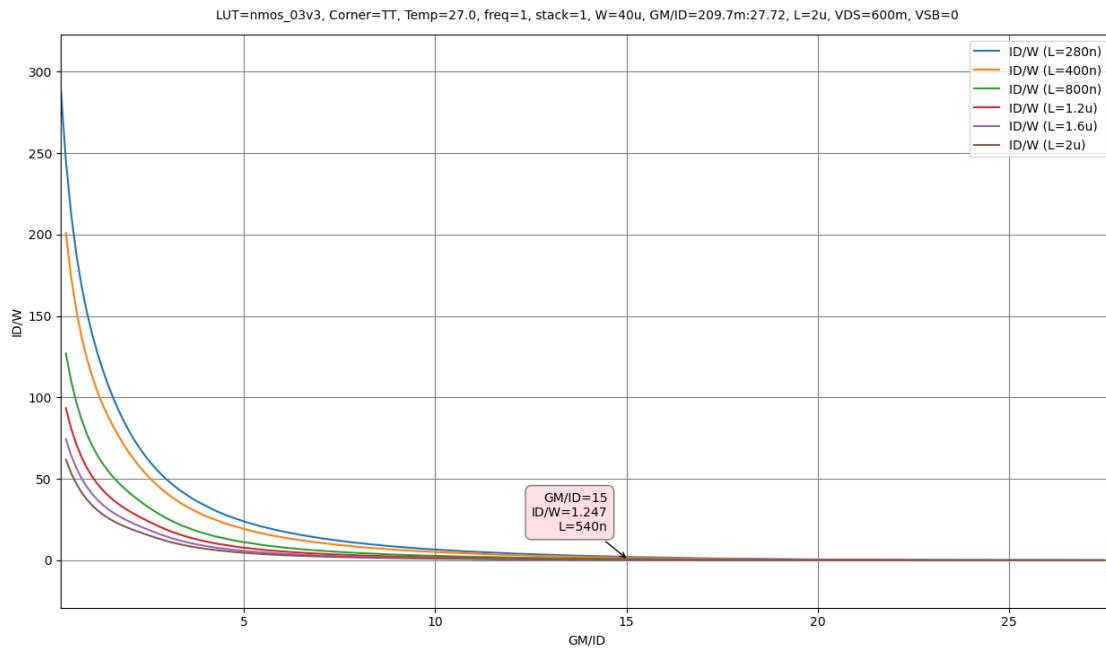
Design for NMOS current mirror load



- For the same Vgs need $gm/ID \approx 15$

$$\begin{aligned}
 & \text{from gain of 1st stage } g_{ds3,4} = 744\mu S \text{ and } g_{m3,4} = \frac{g_m}{I_D} * I_D \\
 & = 15 * 7.5\mu A = 112.5\mu S \text{ then } \frac{g_m}{g_{ds}} \geq 145.35
 \end{aligned}$$

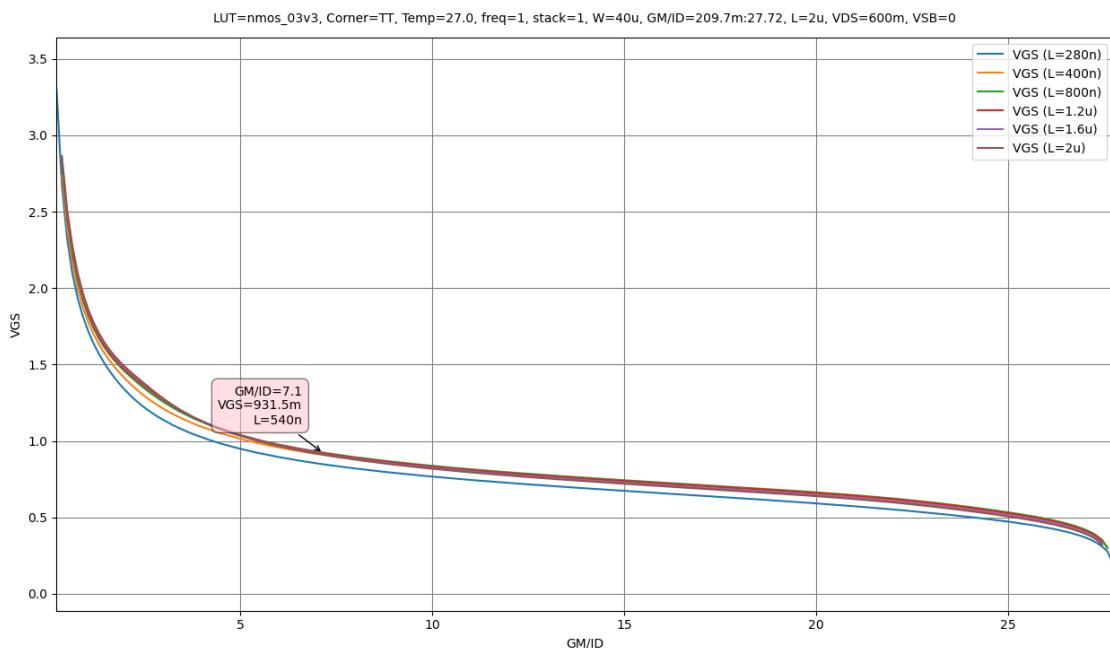




- $W = \frac{7.5\mu A}{1.247} = 6\mu m$ and $L = 540nm$ and $\frac{g_m}{I_D} = 15$
- To achieve CMI_{RLOW}

$$VICM_{min} = -|V_{GS1}| + V_1^* + V_{GS3max} \rightarrow V_{GS3max} = VICM_{min} + |V_{GS1}| - V_1^*$$

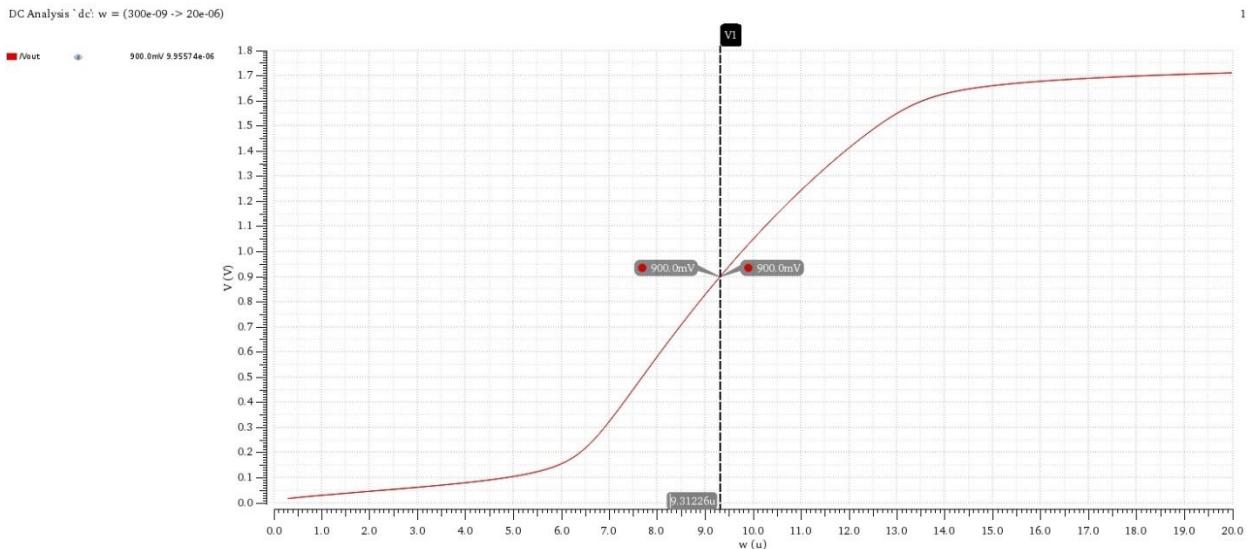
$$V_{GS3max} = .2 + .897 - .167 = .93$$



- Then $\frac{g_m}{I_D} > 7.1$

transistor	<i>L</i>	<i>W</i>	<i>g_m/I_D</i>	<i>I_D</i>	<i>g_m</i>	<i>V_{dsat}</i>	<i>V_{ov}</i>	<i>V[*]</i>
M1&M2	450nm	8.8μm	12S/A	7.5μA	90μS	143.9mV	114.9mV	166.67mV
M3&M4	450nm	9.31μm	15S/A	7.5μA	112.5μS	119.8mV	16.03mV	133.33mV
M6	310nm	14.36μm	13S/A	45μA	585μS	120.4mV	63.42mV	153.85mV
M5	600nm	6.87μm x2	11S/A	10μA	110μS	151.2mV	135.4mV	181.8mV
M7	600nm	6.87μm x3	11S/A	15μA	165μS	151.2mV	135.4mV	181.8mV
M8	600nm	6.87μm x9	11S/A	45μA	495μS	151.2mV	135.4mV	181.8mV

- For R_Z need to put pole in infinite, so we choose $R_Z = \frac{1}{g_{m6}} = \frac{1}{585\mu S} = 1.7k\Omega$
- Sweep W for load current mirror to get output voltage at 900mV so
W=9.31μm



- Note: I use multiplier for M5&M7&M8
- Verifying CMIR and output swing

$$CMIR_{LOW} = -|V_{GS1}| + V_{dsat1} + V_{GS3} = -.897 + .1439 + .72 = -33.1mV$$

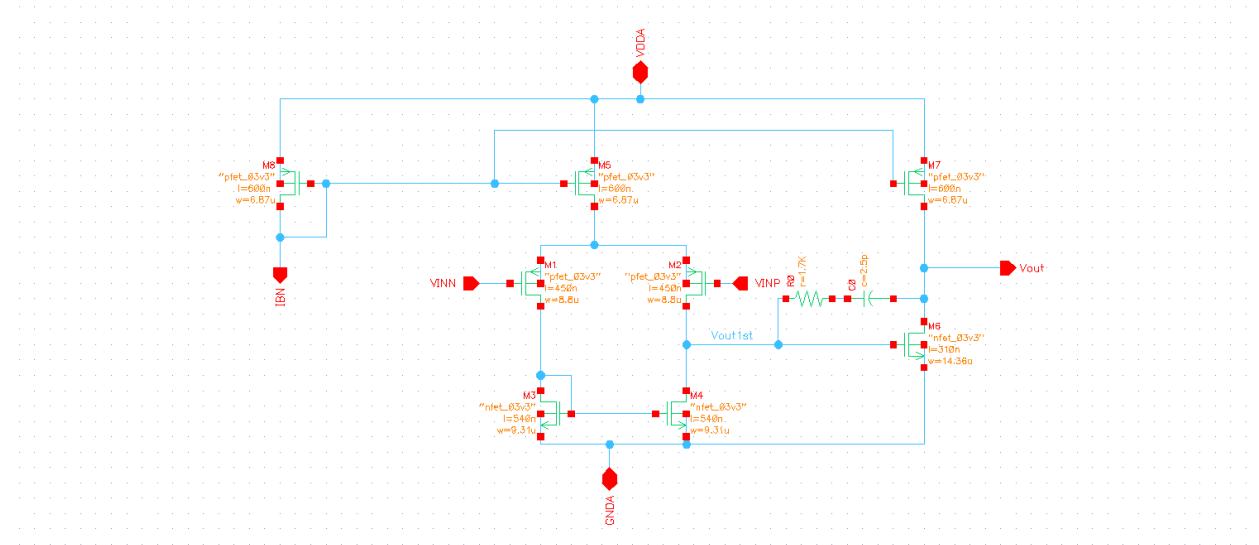
$$CMIR_{HIGH} = V_{DD} - V_{dsat5} - |V_{GS1}| = 1.8 - .1512 - .897 = 751.8mV$$

$$SWING_{MIN} = V_{dsat6} = 120.4mV$$

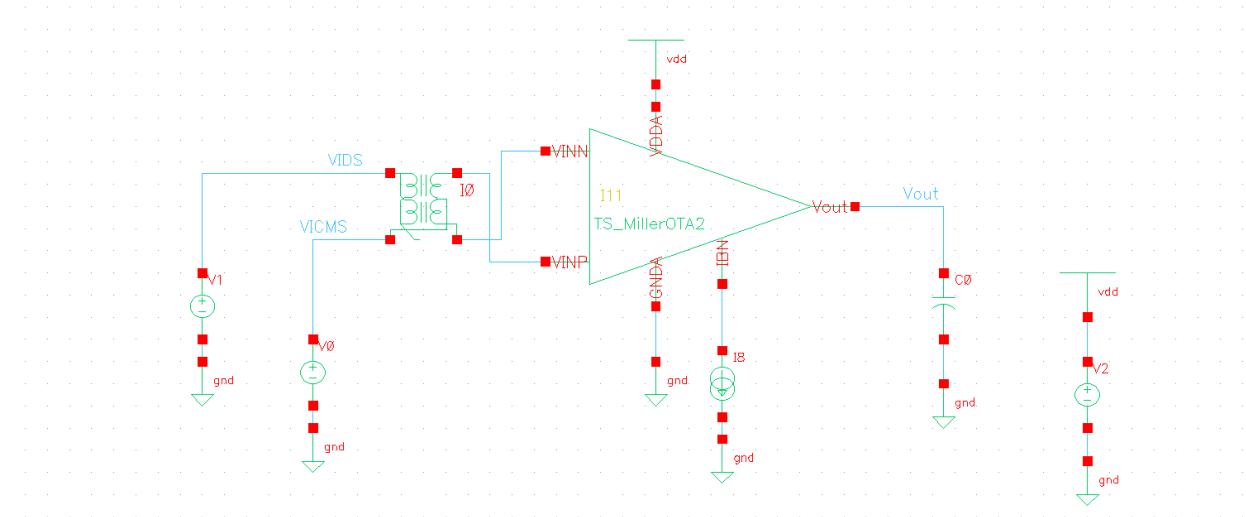
$$SWING_{MAX} = V_{DD} - V_{dsat7} = 1.8 - .1512 = 1.6488V$$
- Achieving CMIR and output swing I designed

PART 3: Open-Loop OTA Simulation

- The design of two stage miller OTA

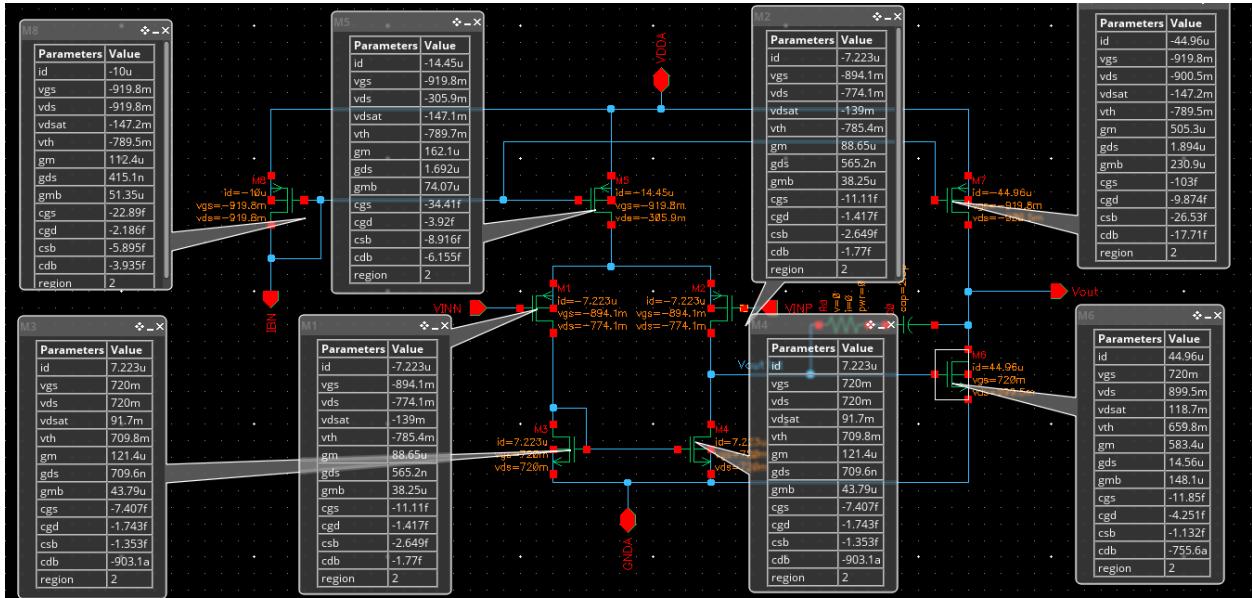


- Note: for tail current and load and current mirror I use multiplier 2 for current mirror and 3 for tail current and 9 for load current source
- Test Bench



1. OP (Operating Point) Analysis

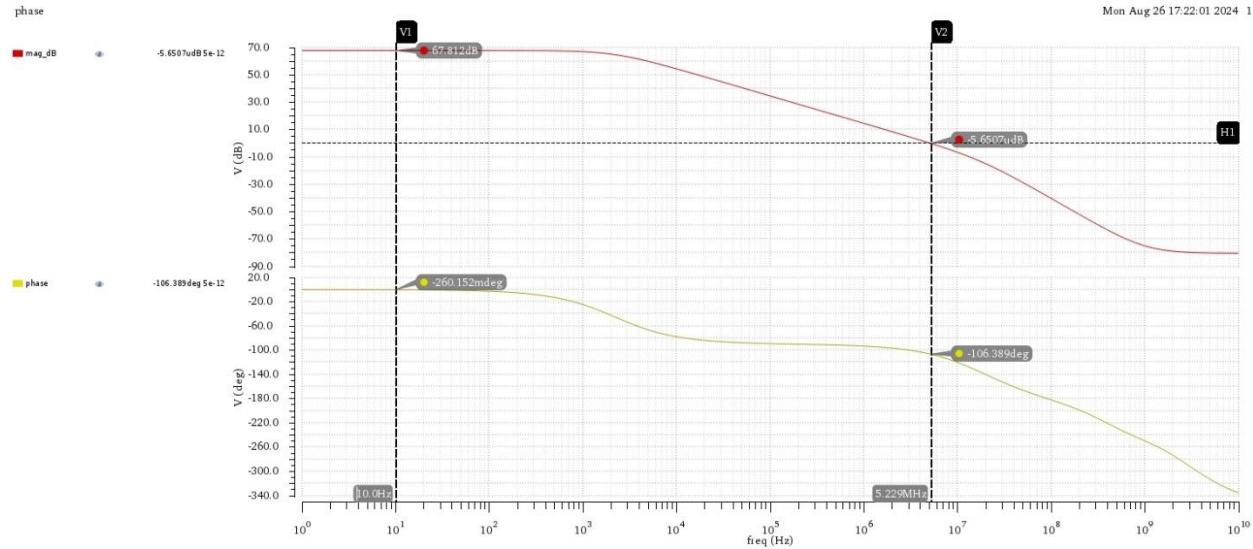
- Schematic of the OTA with DC node voltages clearly annotated



- the current and gm in the two input pair are exactly equal because symmetric of the circuit
- dc voltage of the output of the first stage equal to the Vgs of the load current mirror of the OTA as Vout follow mirror node in Common Mode because the current split equally between the two branches so Vds of M4 must be equal to the Vgs of M3
- the output voltage of second stage equal to 900mV as choosing the W for load current mirror to cancel the dc offset between the input of the second stage and Vgs of the load current mirror

2. Diff small signal ccs:

- Plotting differential gain (in dB) and phase vs frequency



- Simulation result for gain and bandwidth and GBW and UGF and phase margin

ITI_Su2024:TS_MillerOTA_tb:1	Ao	2.458k
ITI_Su2024:TS_MillerOTA_tb:1	Ao_db	67.81
ITI_Su2024:TS_MillerOTA_tb:1	BW	2.205k
ITI_Su2024:TS_MillerOTA_tb:1	UGF	5.252M
ITI_Su2024:TS_MillerOTA_tb:1	GBW	5.42M
ITI_Su2024:TS_MillerOTA_tb:1	PM	73.68

- Hand analysis for gain and bandwidth and GBW

$$A_{v_{diff}} = g_{m1,2} * R_{out1} * g_{m6} * R_{out2} = \\ 88.65\mu S * \left(\frac{1}{565.2nS} || \frac{1}{709.6nS} \right)^{-1} * 583.4\mu S * \left(\frac{1}{1.894\mu S} || \frac{1}{14.56\mu S} \right)^{-1} = 2465$$

$$BW = \frac{1}{2\pi * R_{out1} * (g_{m2} * R_{out2}) * C_C} = \\ \frac{1}{2\pi \left(\frac{1}{565.2nS} || \frac{1}{709.6nS} \right)^{-1} * 583.4\mu S * \left(\frac{1}{1.894\mu S} || \frac{1}{14.56\mu S} \right)^{-1} * 2.5pF} = 2.29kHz$$

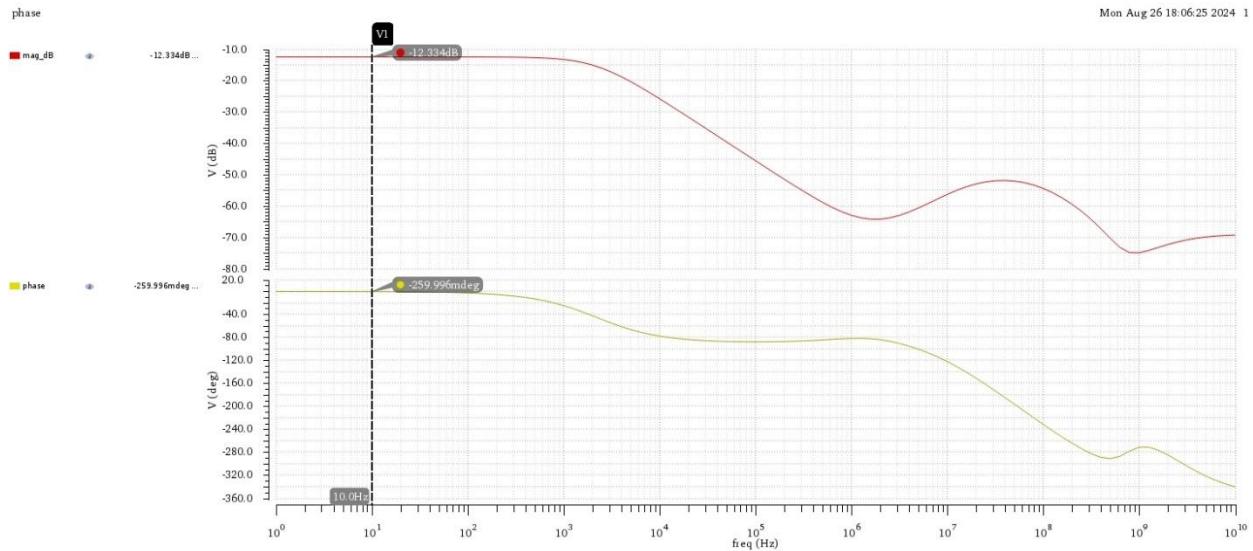
$$GBW = A_v * BW = 5.645MHz$$

4. Comparing simulation results with hand calculations in a table.

	Simulation	Analysis
Gain	2458	2465
Bandwidth	2.205kHz	2.29kHz
GBW	5.42MHz	5.645MHz

3. CM small signal ccs:

1. Plotting CM gain in dB vs and phase frequency



2. Simulation result for gain and bandwidth and GBW.

ITI_Su2024:TS_MillerOTA_tb:1	Ao	241.7m
ITI_Su2024:TS_MillerOTA_tb:1	Ao_db	-12.33
ITI_Su2024:TS_MillerOTA_tb:1	BW	2.205k
ITI_Su2024:TS_MillerOTA_tb:1	GBW	533

3. Hand analysis for gain and bandwidth and GBW

$$A_{v_{CM}} = \frac{1}{2g_{m3,4} * R_{SS_5}} * g_{m6} * R_{out2} = \\ \frac{1.692\mu S}{2 * 121.4\mu S} * 583.4\mu S * \left(\frac{1}{1.894\mu S} || \frac{1}{14.56\mu S} \right)^{-1} = .247$$

$$BW = \frac{1}{2\pi * R_{out1} * (g_{m2} * R_{out2}) * C_C} = \\ \frac{1}{2\pi \left(\frac{1}{565.2nS} || \frac{1}{709.6nS} \right)^{-1} * 583.4\mu S * \left(\frac{1}{1.894\mu S} || \frac{1}{14.56\mu S} \right)^{-1} * 2.5pF} = 2.29kHz$$

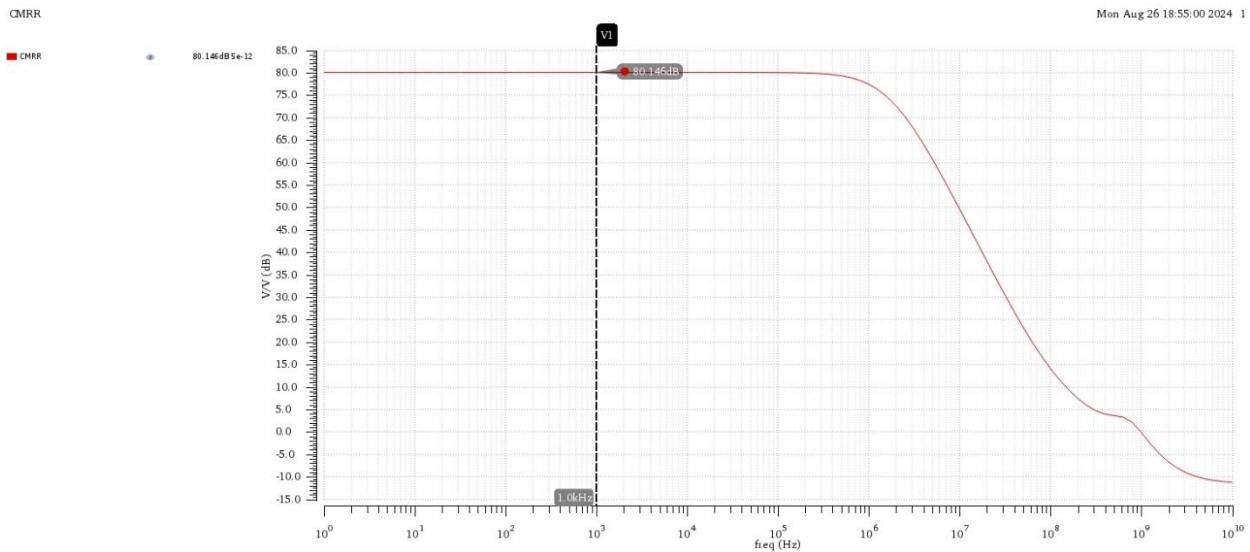
$$GBW = A_v * BW = 565.8\text{Hz}$$

4. Comparing simulation results with hand calculations in a table.

	Simulation	Analysis
Gain	.2417	.247
Bandwidth	2.205kHz	2.29kHz
GBW	533Hz	565.8Hz

4. (Optional) CMRR:

1. Plotting CMRR in dB vs frequency



2. Simulation result for CMRR

ITI_Su2024:TS_MillerOTA_tb:1 | CMRR_dB 80.15

3. Hand analysis for CMRR

- Second stage don't effect on CMRR so CMRR for 5T_OTA

$$CMRR = 20 \log(88.65\mu S * \left(\frac{1}{565.2nS} || \frac{1}{709.6nS} \right)^{-1} * \frac{2*121.4\mu S}{1.692\mu S}) = 79.982dB$$

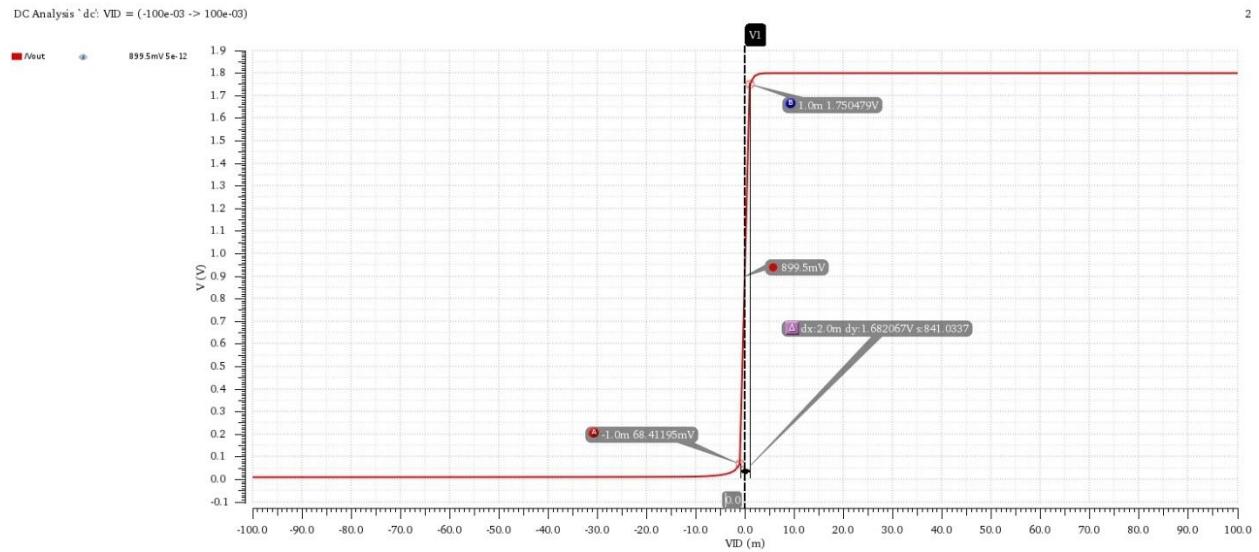
4. Comparing simulation results with hand calculations in a table.

	Simulation	Analysis
CMRR	80.15dB	79.982dB

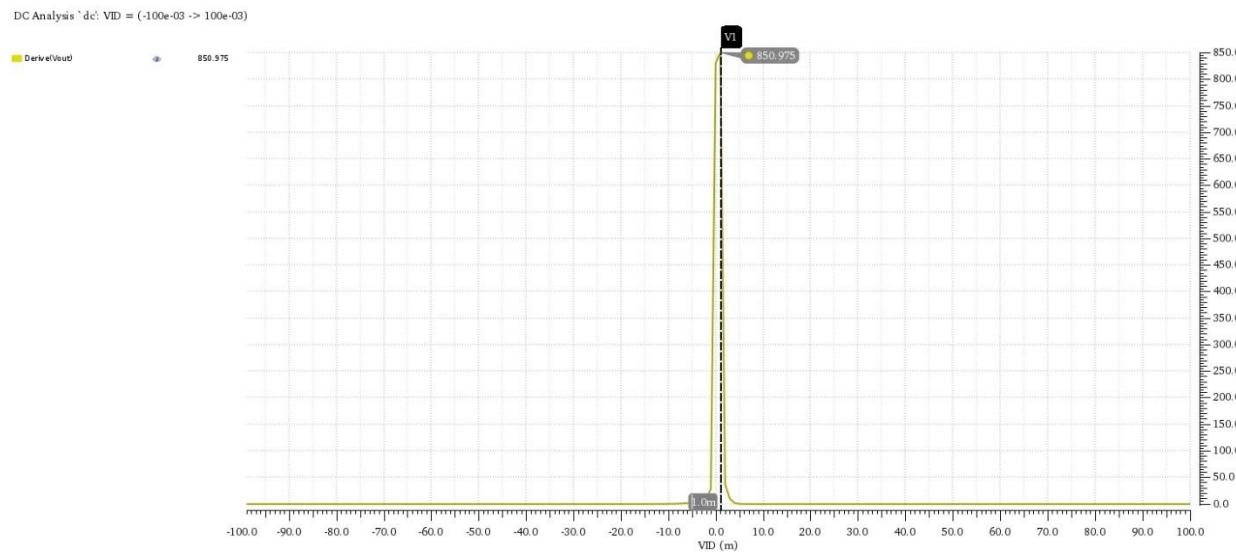
- From the result the design meets the specs of CMRR>74dB

5. (Optional) Diff large signal ccs:

1. Use DC sweep VID = -0.1:1m:0.1 and Plotting VOUT vs VID



2. The value of Vout at VID=0 is the same from OP analysis 899.8mV
3. Plotting derivative of VOUT vs VID



4. The peak of the derivative is less than the gain from the diff small signal
 - As the amplifier has very high gain so it has very small range to amplify with its nominal value from diff small signal as 1mV change in small signal it will lead to out as 2.4V as small signal linearize the mosfet and don't sense that mosfet get out saturation region so in large signal as step is

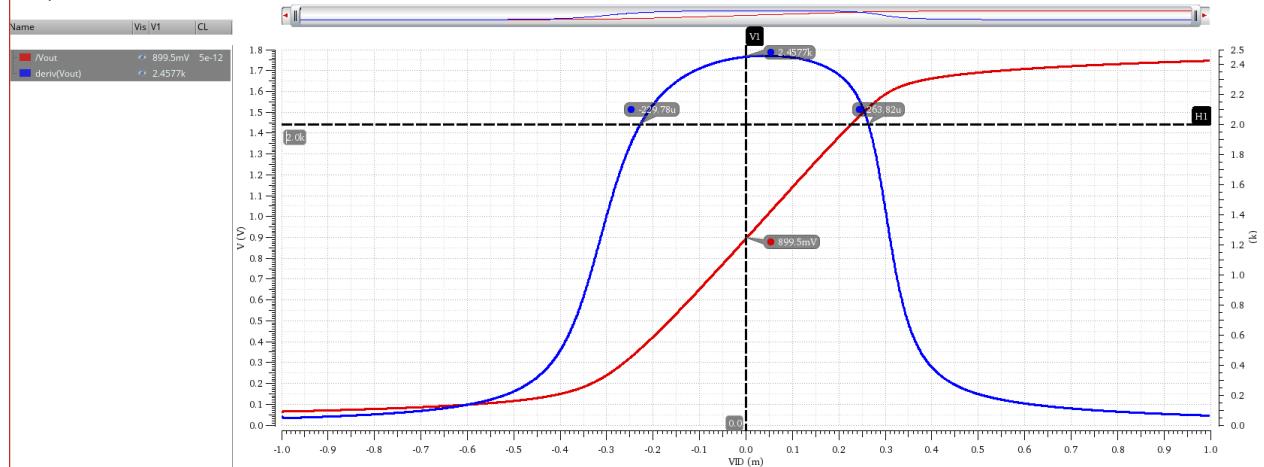
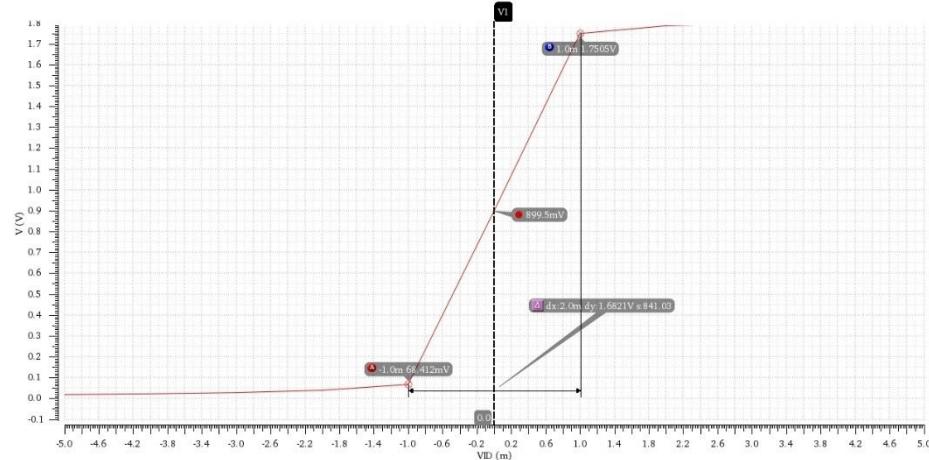
1mV it take approximately the average as seen from the Vout Vs VID is equal to 841

- By zooming in the range from VID=-5m:5m we see that the change in Vout is approximately linear and this is't the real of the amplifier by rebeat the analysis again but

$$\text{VID} = -1\text{m}:0.01\text{m}:1\text{m}$$

As approximately the signal change from 0 to VDD from -1mV to 1mV

- Use DC sweep VID = -1m:10 μ :1m and Plotting VOUT vs VID and the derivative

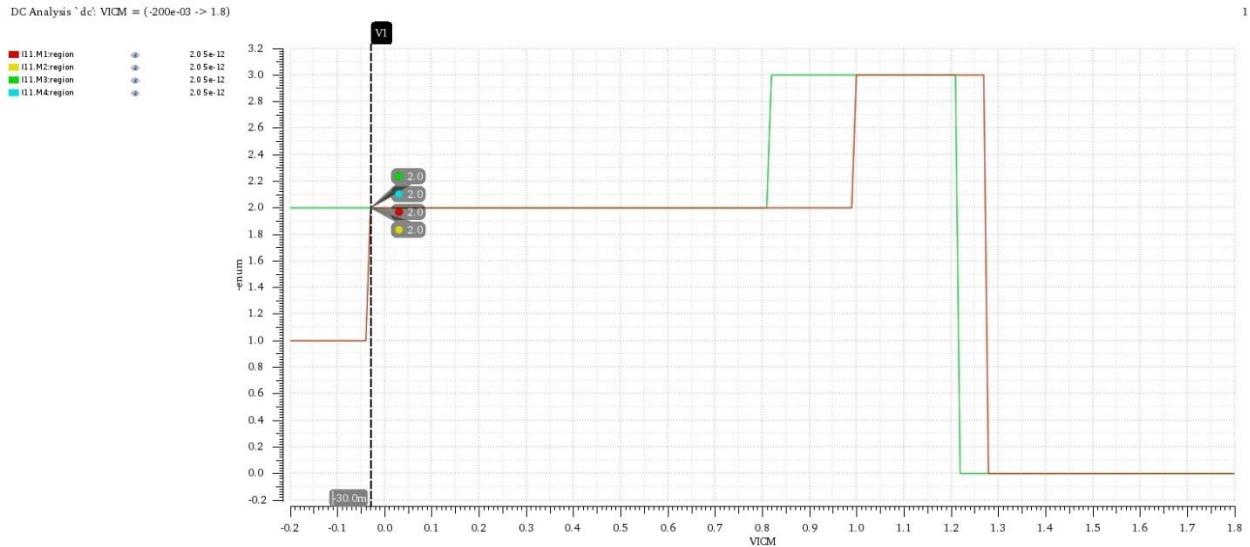


- As we see most of change occurs between -.3m to .3m and the peak is around 2.458k and it's the same value we get from diff smal signal

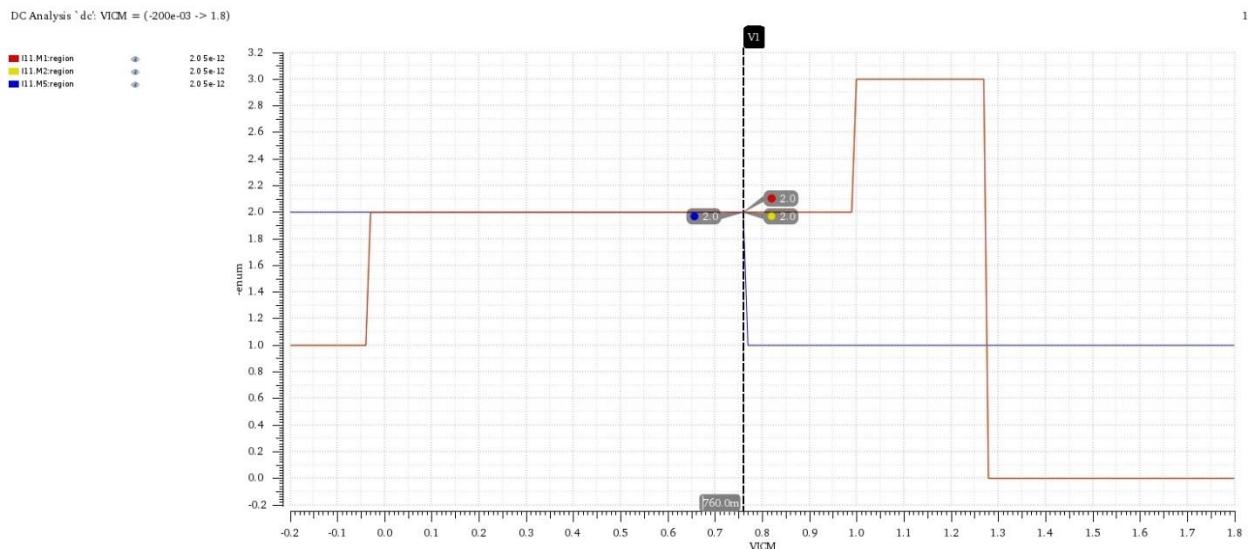
6. CM large signal ccs (region vs VICM):

1. Use DC sweep VICM = -200m:10m:VDD.

- Plot “region” OP parameter vs VICM for the input pair and the load current mirror to determine the $CMIR_{LOW}$



- So $CMIR_{LOW} = -30mV$
- Plot “region” OP parameter vs VICM for the input pair and the tail current source to determine $CMIR_{HIGH}$



- So $CMIR_{HIGH} = 760mV$

2. Hand analysis for CMIR

$$CMIR_{LOW} = -|V_{GS1,2}| + |V_{dsat1,2}| + V_{GS3,4} = -894.1 + 139 + 720 = -35.1mV$$

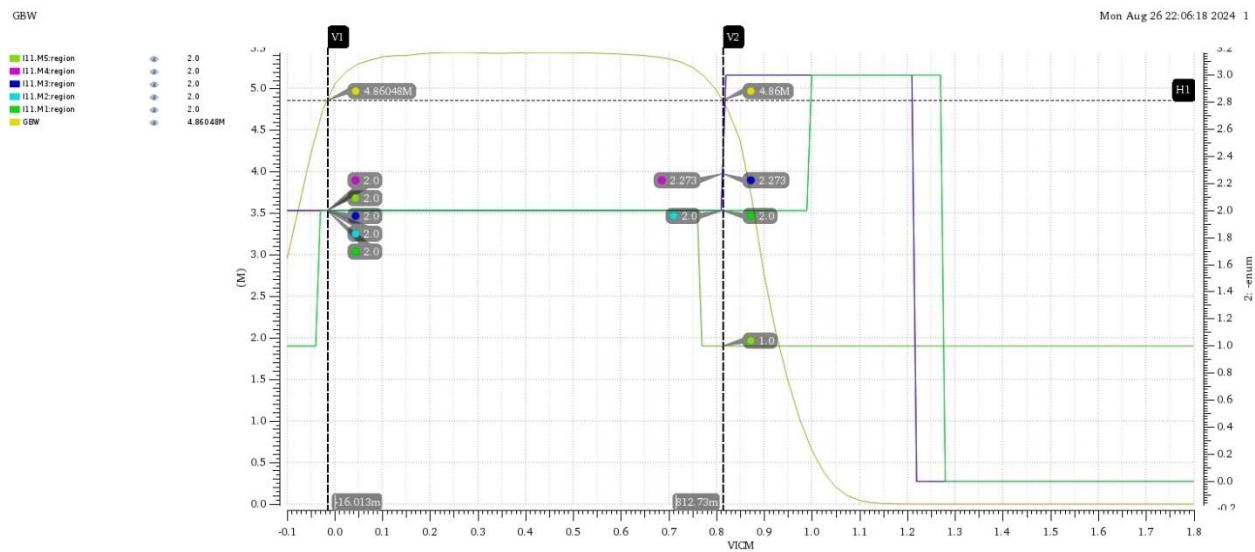
$$CMIR_{HIGH} = -|V_{GS1,2}| - |V_{dsat5}| + V_{DD} = -894.1 - 147.1 + 1800 = 758.8mV$$

3. Comparing between simulation and hand analysis

	Simulation	Analysis
$CMIR_{LOW}$	-30mV	-35.1mV
$CMIR_{HIGH}$	760mV	758.8mV

7. (Optional) CM large signal ccs (GBW vs VICM):

1. Plotting GBW vs VICM



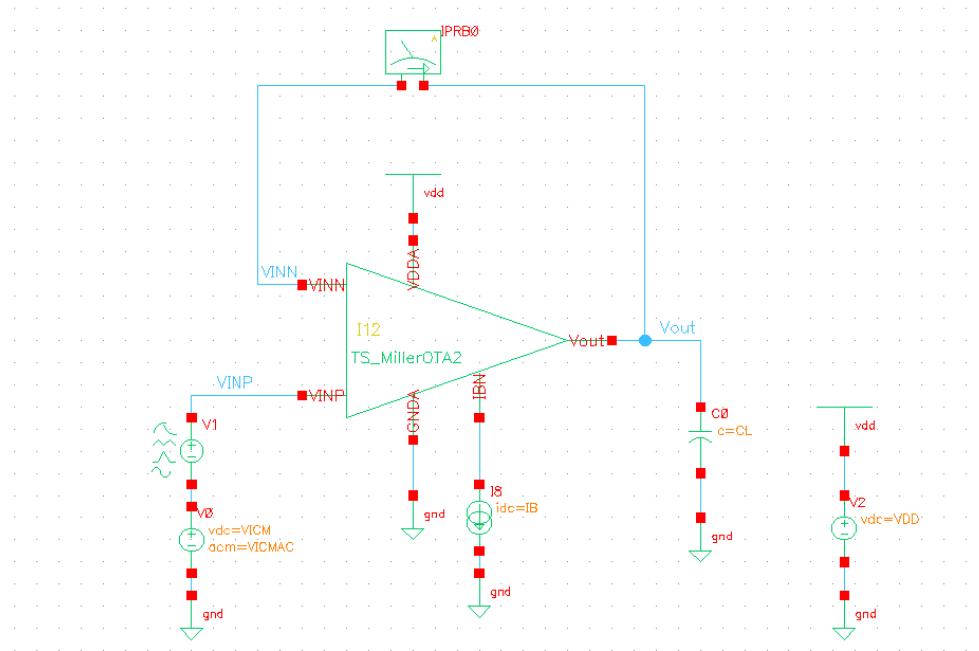
- As $GBW = 5.4MHz$ so $90\% * GBW = 4.86MHz$ so CMIR range
 $-16.01mV \leq VICM \leq 812.73mV$
- From the result of this part and above the design meets the specs of CMIR

PART 4: Closed-Loop OTA Simulation

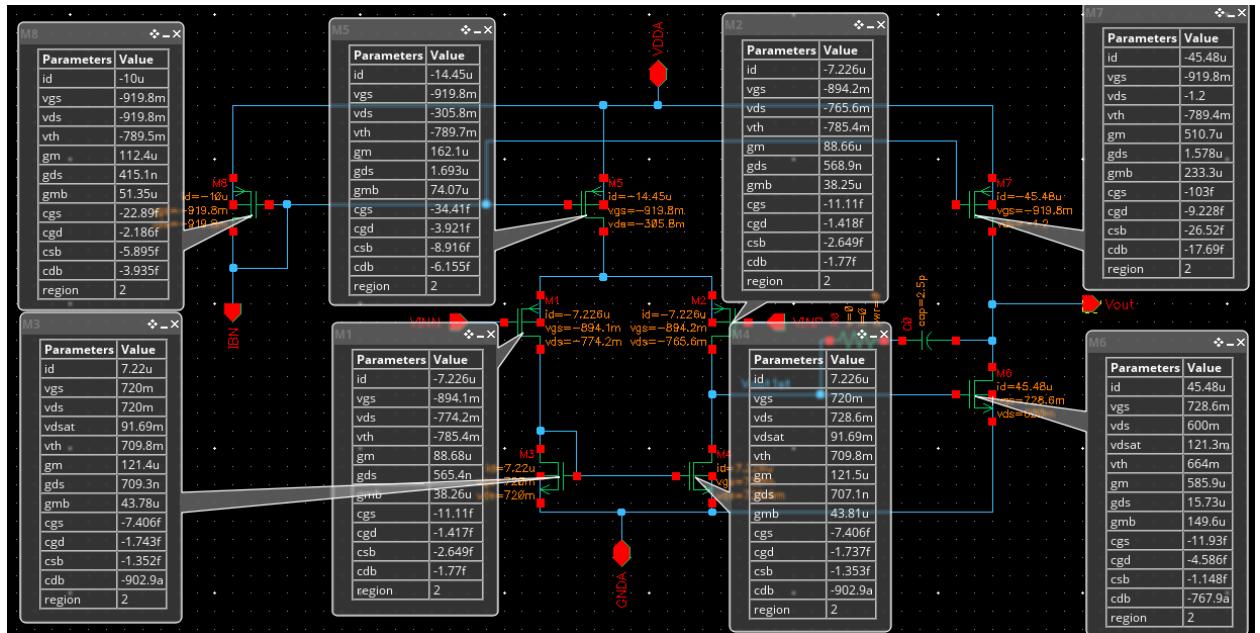
1. OP Analysis

- Schematic of the OTA with DC OP point clearly annotated

- Schematic



- DC OP point annotated



2. The DC voltages at the input terminals of the op-amp isn't exactly equal as there are V_{err} difference between them to change the Vout from 900mV to 600mV

/VINP (V)	/VINN (V) ▲
1 600.000000E-3	600.04781E-3

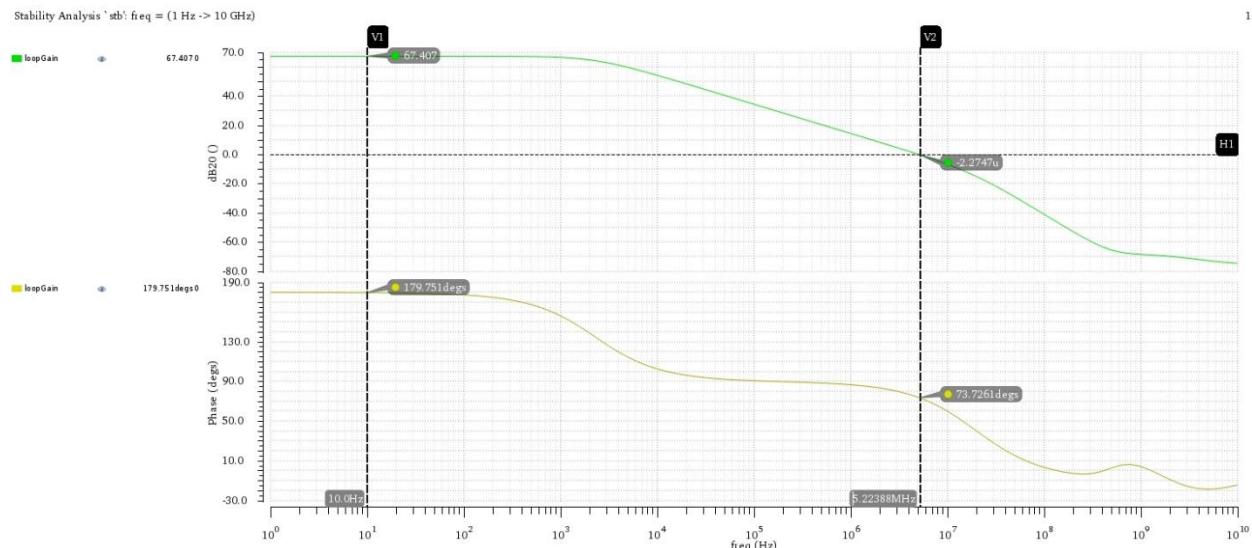
3. DC voltage at the output of the first stage isn't exactly equal to the open loop simulation as the voltage on the two terminals are difference so there will be difference in the current in the two branch and this will lead to difference in V_{ds} of the two current mirror load and difference in dc output voltage
 4. the current (and gm) in the input pair isn't exactly equal

I12.M2:id	I12.M1:id	I12.M2:gm	I12.M1:gm ▲
1 -7.22584E-6	-7.22649E-6	88.6602E-6	88.6805E-6

- V_{err} difference between the two terminals make the current and gm slightly different in the two pair

2. Loop gain:

- Plot loop gain in dB and phase vs frequency.



2. Simulation result of DC gain, BW, UGF, GBW, and Phase margin

ITI_Su2024:TS_MillerOTA_UGBtb:1	LG	2.346k
ITI_Su2024:TS_MillerOTA_UGBtb:1	LG_db	67.41
ITI_Su2024:TS_MillerOTA_UGBtb:1	BW	2.307k
ITI_Su2024:TS_MillerOTA_UGBtb:1	UGF	5.247M
ITI_Su2024:TS_MillerOTA_UGBtb:1	GBW	5.413M
ITI_Su2024:TS_MillerOTA_UGBtb:1	PM	73.77

3. Comparing DC gain, UGF, and GBW with those obtained from open-loop simulation.

	Open loop	Closed loop
Gain	2458	2346
UGF	5.252MHz	5.247MHz
GBW	5.42MHz	5.413MHz

- The values of the two simulations are approximately equal
- The gain is less than open loop simulation because of the change of op parameters for mosfet in closed loop

4. Compare phase margin with hand calculations

$$\frac{\omega_{p2}}{\omega_u} = \frac{g_{m6}}{C_L} * \frac{C_C}{g_{m1,2}} = \frac{583.4\mu S}{5pF} * \frac{2.5pF}{88.65\mu S} = 3.29$$

- @ $\frac{\omega_{p2}}{\omega_u} = 3 \rightarrow PM = 72.4$ and @ $\frac{\omega_{p2}}{\omega_u} = 4 \rightarrow PM = 76.3$
- By iteration $PM = \frac{76.3 - 72.4}{4-3} * (3.29 - 3) + 72.4 = 73.53$

	Simulation	Analysis
PM	73.77	73.53

- As $PM < 76.3$ then the system is underdamped system

5. Hand analysis for gain and GBW and BW

$$A_{OL} = g_{m1,2} * R_{out1} * g_{m6} * R_{out2} = \\ 88.66\mu S * \left(\frac{1}{568.9nS} || \frac{1}{707.1nS} \right)^{-1} * 585.9\mu S * \left(\frac{1}{1.578\mu S} || \frac{1}{15.73\mu S} \right)^{-1} = 2352$$

$$UGF = GBW = \frac{g_{m1,2}}{2\pi C_C} = \frac{88.65\mu S}{2.5pF} = 5.645MHz$$

$$\epsilon_s = \frac{1}{\beta A_{OL}} * 100 = \frac{1}{1 * 2346} * 100 = .0426\% \rightarrow \epsilon_s < .05\%$$

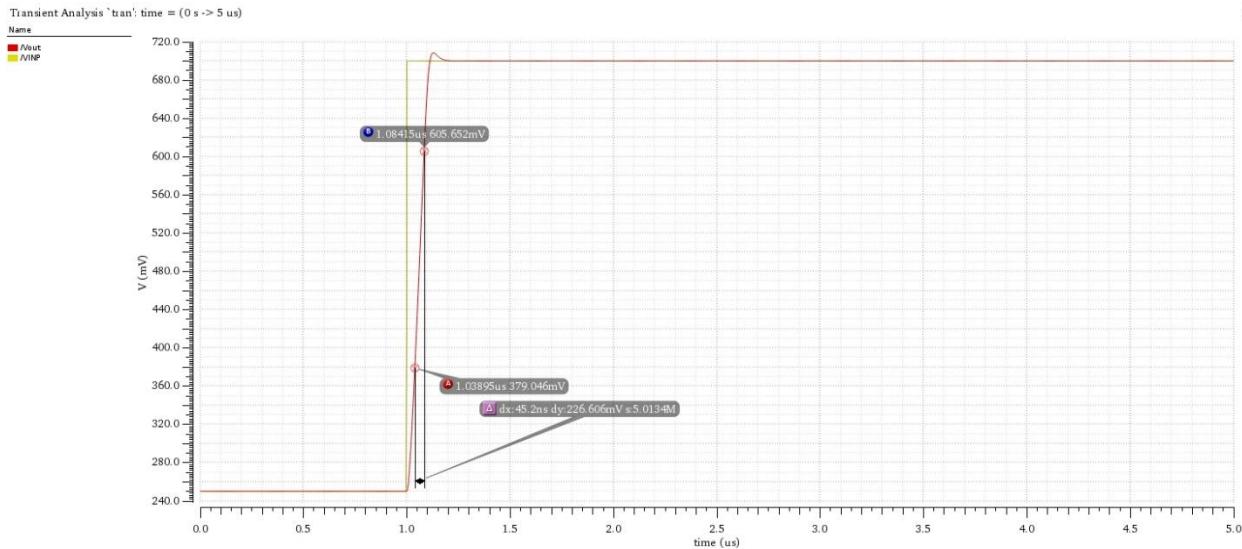
- From the above result the design meet the specs of Static gain error and phase margin

6. Comparing simulation results with hand calculations in a table

	Simulation	Analysis
Gain	2346	2352
UGF	5.247MHz	5.645MHz
GBW	5.413MHz	5.645MHz

3. Slew rate:

- Plotting Vin and Vout overlaid.



- Reporting the slew rate

- Simulation

ITI_Su2024:TS_MillerOTA_UGBtb:1	SR	5.195M
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- Hand analysis

$$SR = \frac{I_{B1}}{C_C + C_1} = \frac{14.45\mu S}{2.5pF} = 5.78V/\mu s$$

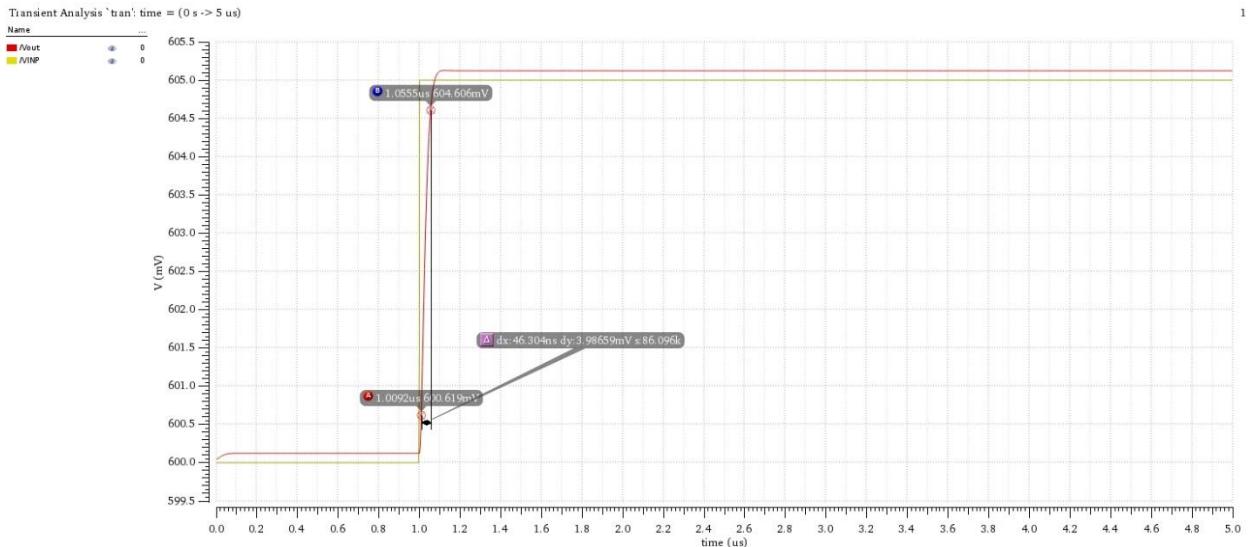
- Compare simulation results with hand calculations in a table

	Simulation	Analysis
SR	5.195V/ μ s	5.78V/ μ s

- From the above result the design meet the specs of Slew Rate

4. Settling time:

1. Plotting Vin and Vout overlaid



2. Reporting the rise time

- Simulation

ITI_Su2024:TS_MillerOTA_UGBtb:1	Trise	46.81n
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- Hand analysis

$$\tau = \frac{1}{\omega_u} = \frac{1}{2\pi * UGF} = \frac{1}{2\pi * 5.252MHz} = 30.3ns$$

$$t_{rise} = 2.2\tau = 2.2 * 30.3ns = 66.6ns$$

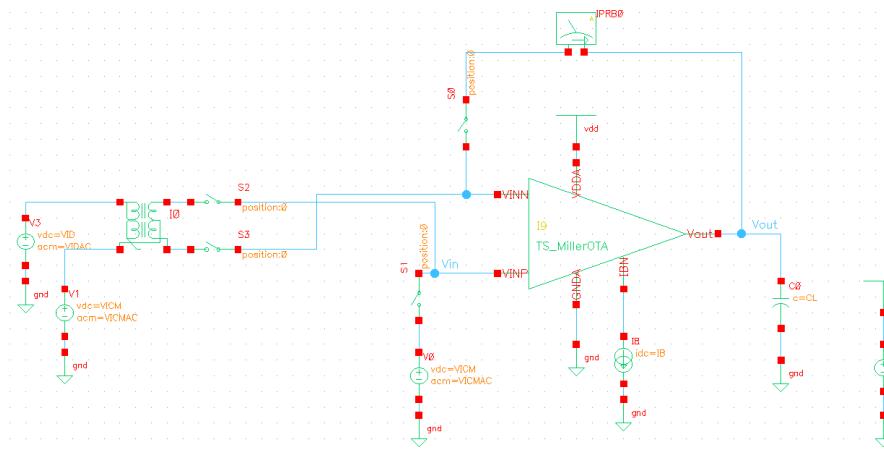
- The simulation result is better as for hand analysis we assume it as first order system but it's second order system and settle to its final value faster than first order system
 - The t_{rise} for buffer connection is less than 70ns and this meet the specs
3. Compare simulation results with hand calculations in a table.

	Simulation	Analysis
t_{rise}	46.81ns	66.6ns

4. There is no ringing as ringing occurs when $Q \geq .707 \rightarrow PM \leq 65.5$
- But there is an overshoot as overshoot canceled when $Q \leq 0.5 \rightarrow PM \geq 76.3$
 - As $PM = 73.7$ then there is no ringing but there are overshoot in the system

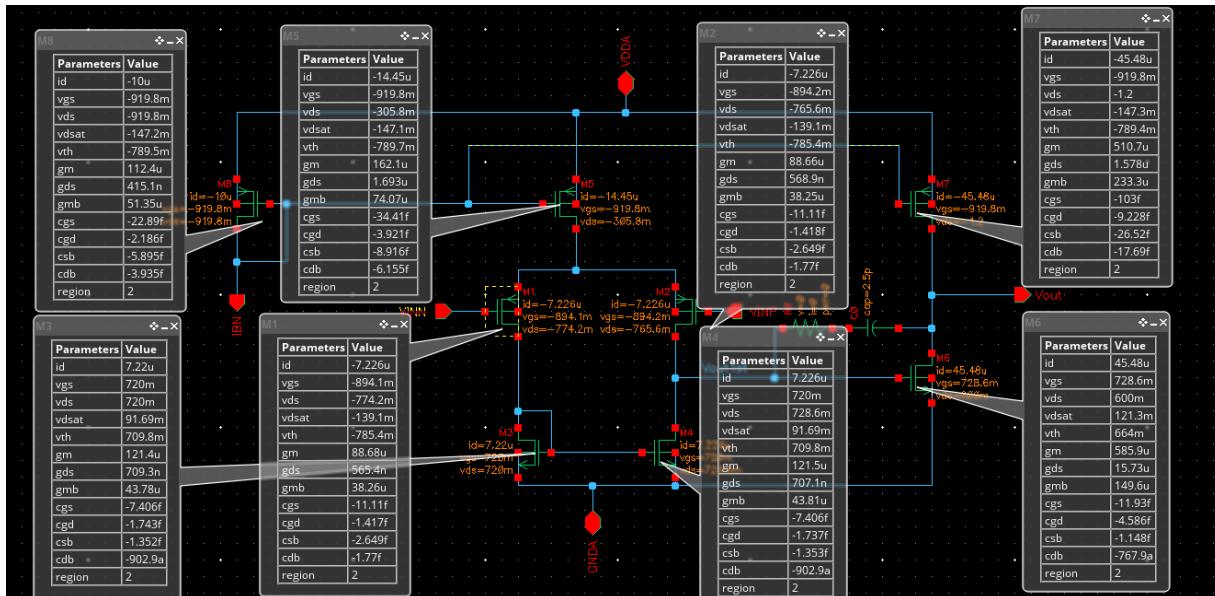
Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation

- ### - Test Bench



1. OP (Operating Point) Analysis

- ### 1. Schematic of the OTA with DC node voltages clearly annotated



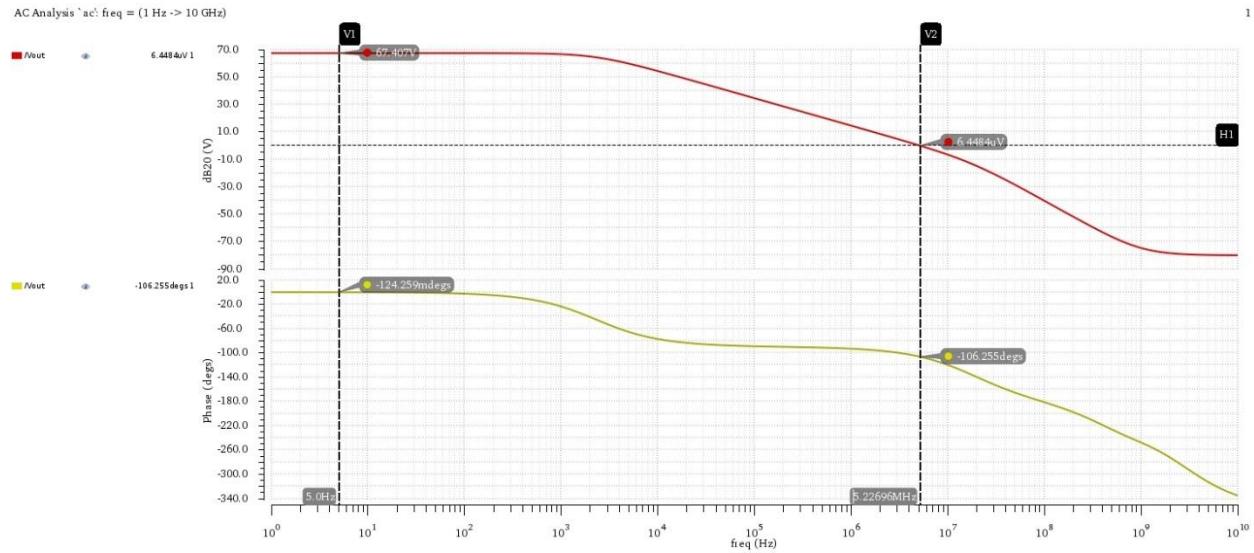
- the current and gm in the two input pair are slightly different because V_{err} between the two input
 - dc voltage of the output of the first stage approximately equal to the V_{gs} of the load current mirror of the OTA as V_{out} follow mirror node in Common

Mode because the current approximately split equally between the two branches so Vds of M4 \approx Vgs of M3

- the output voltage of second stage equal to 600mV as the buffer connection force the second terminal and output terminal to equal input voltage

2. Diff small signal ccs:

- Plotting differential gain (in dB) and phase vs frequency



- Simulation result for gain and bandwidth and GBW and UGF and phase margin

ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_Ao	2.346k
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_Ao_dB	67.41
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_BW	2.307k
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_UGF	5.25M
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_GBW	5.413M
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_PM	73.81

- Hand analysis for gain and bandwidth and GBW

$$A_{v_{diff}} = g_{m1,2} * R_{out1} * g_{m6} * R_{out2} = \\ 88.66\mu S * \left(\frac{1}{568.9nS} || \frac{1}{707.1nS} \right)^{-1} * 585.9\mu S * \left(\frac{1}{1.578\mu S} || \frac{1}{15.73\mu S} \right)^{-1} = 2352$$

$$BW = \frac{1}{2\pi * R_{out1} * (g_{m2} * R_{out2}) * C_C} = \\ \frac{1}{2\pi \left(\frac{1}{568.9nS} || \frac{1}{707.1nS} \right)^{-1} * 585.9\mu S * \left(\frac{1}{1.578\mu S} || \frac{1}{15.73\mu S} \right)^{-1} * 2.5pF} = 2.39kHz$$

$$GBW = A_v * BW = 5.621MHz$$

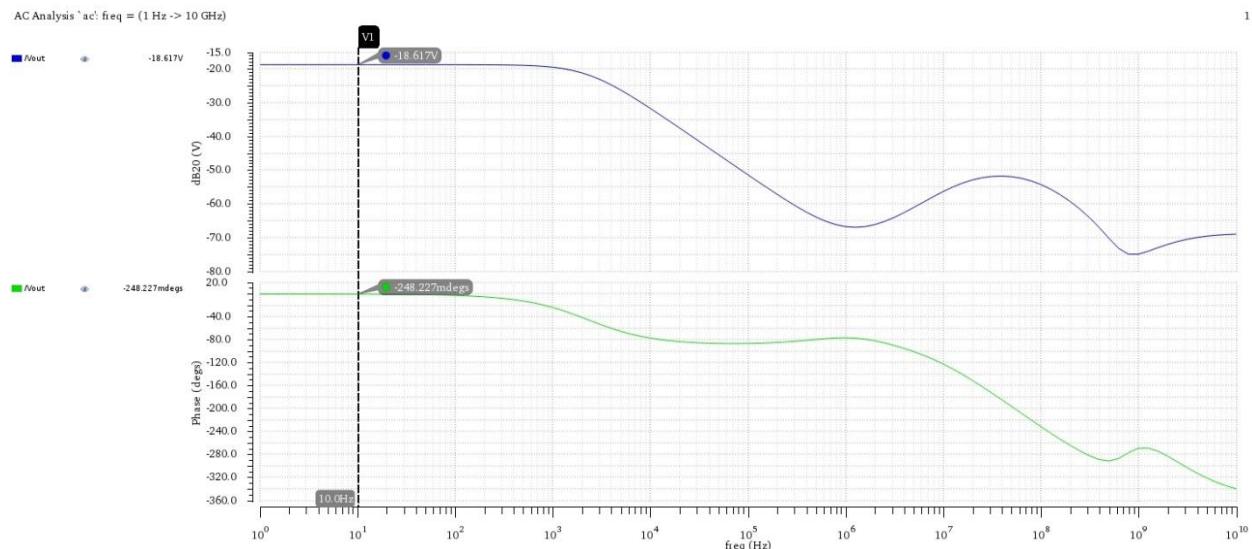
- The result changes a little bit as the operating point of transistor change by small value

4. Comparing simulation results with hand calculations in a table.

	Simulation	Analysis
Gain	2346	2352
Bandwidth	2.307kHz	2.39kHz
GBW	5.413MHz	5.621MHz

3. CM small signal ccs:

1. Plotting CM gain in dB vs and phase frequency



2. Simulation result for gain and bandwidth and GBW.

ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_Ao	117.3m
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_Ao_dB	-18.62
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_BW	2.307k
ITI_Su2024:TS_MillerOTA_UGBtb:1	AC_GBW	270.5

3. Hand analysis for gain and bandwidth and GBW

$$A_{v_{CM}} = \frac{1}{2g_{m3,4} * R_{SS_5}} * g_{m6} * R_{out2} = \\ \frac{1.693\mu S}{2 * 121.5\mu S} * 585.9\mu S * \left(\frac{1}{1.578\mu S} || \frac{1}{15.73\mu S} \right)^{-1} = .235$$

$$BW = \frac{1}{2\pi * R_{out1} * (g_{m2} * R_{out2}) * C_C} =$$

$$\frac{1}{2\pi \left(\frac{1}{568.9nS} \parallel \frac{1}{707.1nS} \right)^{-1} * 585.9\mu S * \left(\frac{1}{1.578\mu S} \parallel \frac{1}{15.73\mu S} \right)^{-1} * 2.5pF} = 2.39kHz$$

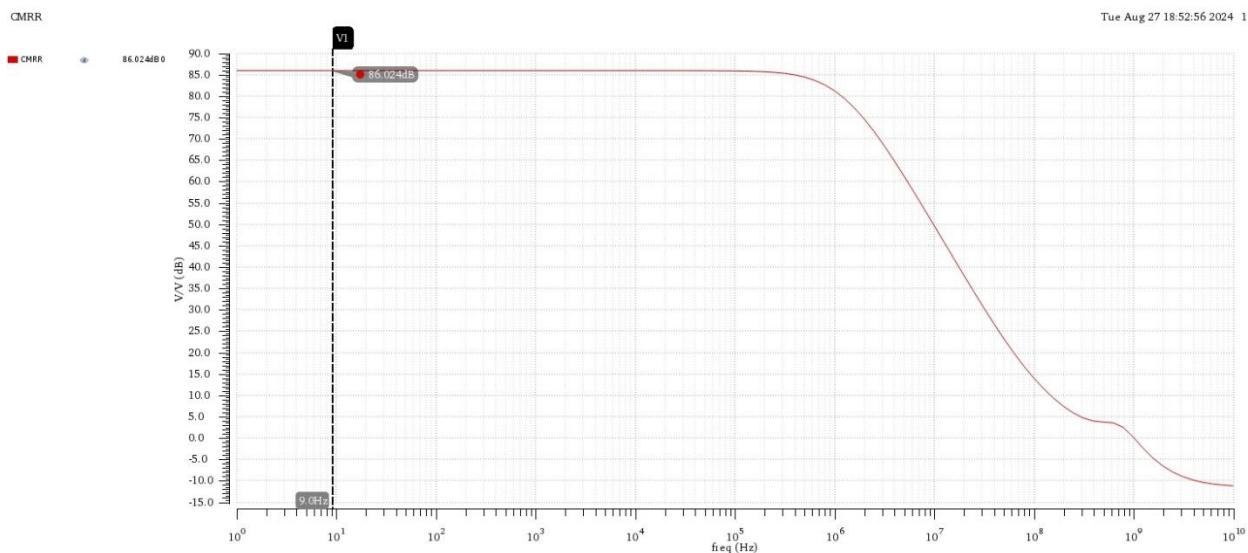
$$GBW = A_v * BW = 561.65Hz$$

4. Comparing simulation results with hand calculations in a table.

	Simulation	Analysis
Gain	.117	.235
Bandwidth	2.307kHz	2.39kHz
GBW	270.5Hz	561.65Hz

4. (Optional) CMRR:

1. Plotting CMRR in dB vs frequency



2. Simulation result for CMRR

ITI_Su2024:TS_MillerOTA_UGBtb:1	CMRR_max	86.02
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3. Hand analysis for CMRR

- Second stage don't effect on CMRR so CMRR for 5T OTA

$$CMRR = 20 \log \left(88.65\mu S * \left(\frac{1}{565.2nS} \parallel \frac{1}{709.6nS} \right)^{-1} * \frac{2*121.4\mu S}{1.692\mu S} \right) = 79.982dB$$

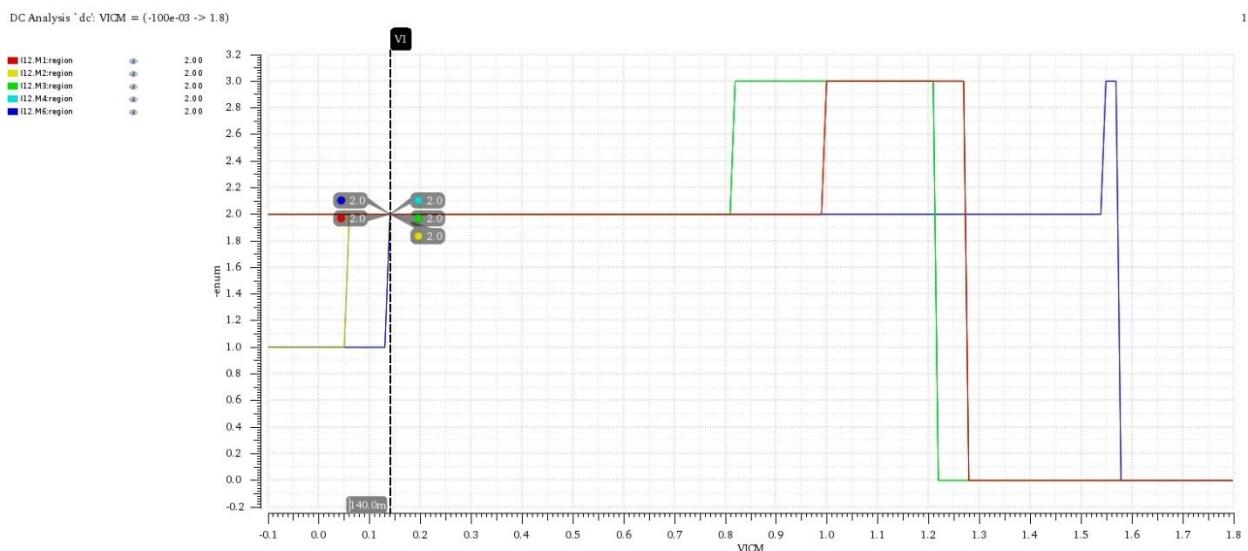
4. Comparing simulation results with hand calculations in a table.

	Simulation	Analysis
CMRR	86.02dB	79.982dB

5. CM large signal ccs (region vs VICM):

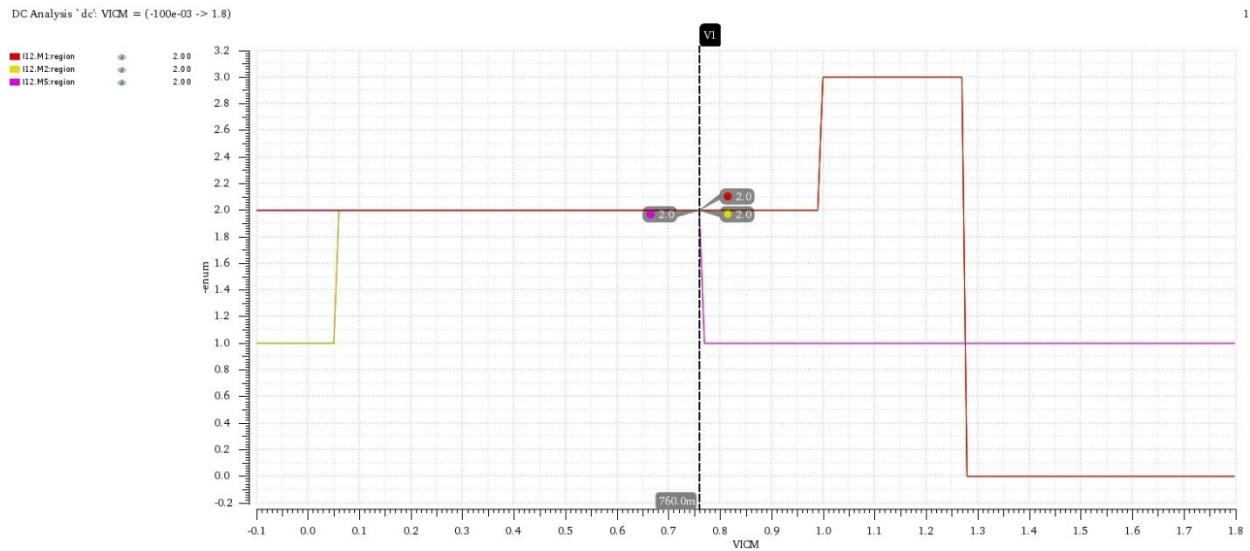
4. Use DC sweep VICM = -100m:10m:VDD.

- Plot “region” OP parameter vs VICM for the input pair and the load current mirror **and the input of the second stage** to determine the $CMIR_{LOW}$



- So $CMIR_{LOW} = 140mV$
- The CMIR low change as the buffer connection force the output to equal the input and when the input become less the V_{dsat6} M6 get out of the saturation and this limit CMIR high for this connection

- Plot “region” OP parameter vs VICM for the input pair and the tail current source to determine $CMIR_{HIGH}$



- So $CMIR_{HIGH} = 760mV$

5. Hand analysis for CMIR

$$CMIR_{LOW} = V_{dsat6} = 120.4mV$$

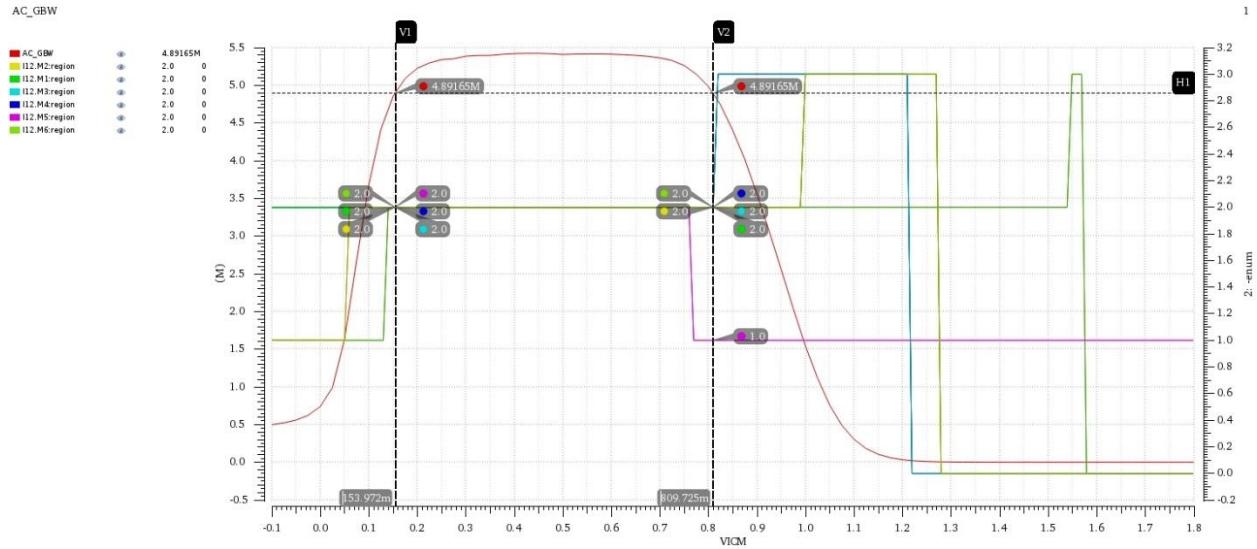
$$CMIR_{HIGH} = -|V_{GS1,2}| - |V_{dsat5}| + V_{DD} = -894.1 - 147.1 + 1800 = 758.8mV$$

6. Comparing between simulation and hand analysis

	Simulation	Analysis
$CMIR_{LOW}$	140	120.4mV
$CMIR_{HIGH}$	760mV	758.8mV

6. (Optional) CM large signal ccs (GBW vs VICM):

2. Plotting GBW vs VICM



- As $GBW = 5.4MHz$ so $90\% * GBW = 4.86MHz$ so CMIR range
 $153.972mV \leq VICM \leq 812.73mV$

Compare between needed specs and achieved

Specs	Needed	Achieved
Technology	0.18μm	0.18μm
Supply voltage	1.8V	1.8V
Static gain error	<= 0.05%	0.0426%
CMRR @ DC	>= 74dB	80.15dB
Phase margin (avoid pole-zero doublets)	>= 70°	73.77°
OTA current consumption	<= 60μA	60μA
CMIR – high	>= 1V	0.76V
CMIR – low	<= 0.2V	-0.15V
Output swing	0.2 – 1.6V	.124 – 1.649V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	46.81ns
Slew rate (SR)	>=5V/μs	5.195V/μs

- the only design specs that not achieved is the $CMIR_{HIGH}$ as this technology has a very high V_{TH} and has a strong body effect so changing the value to reasonable value for this technology.