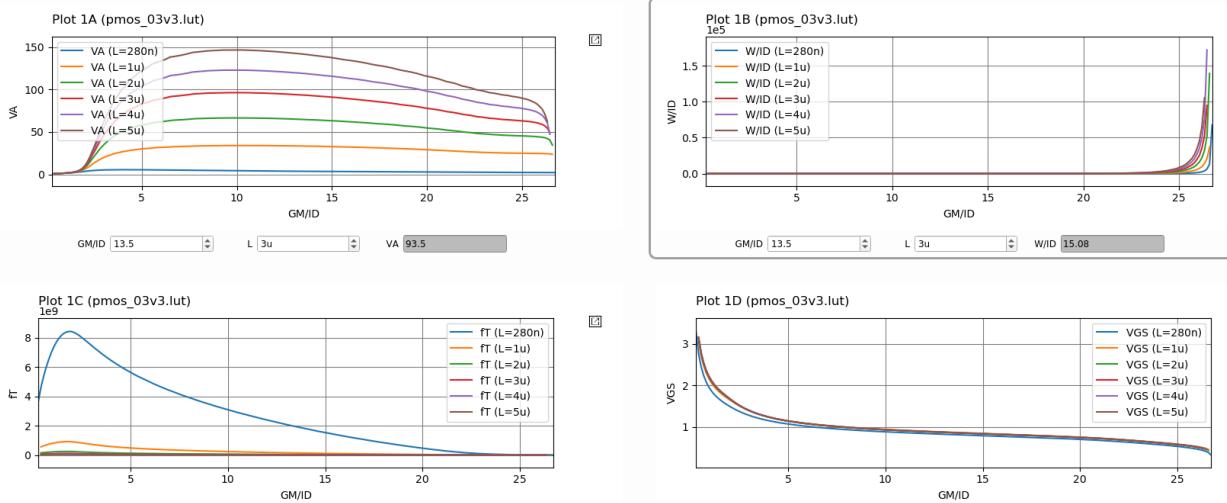


ITI CMOS Analog IC Design 2024  
Lab 11 (**Mini Project 02**)

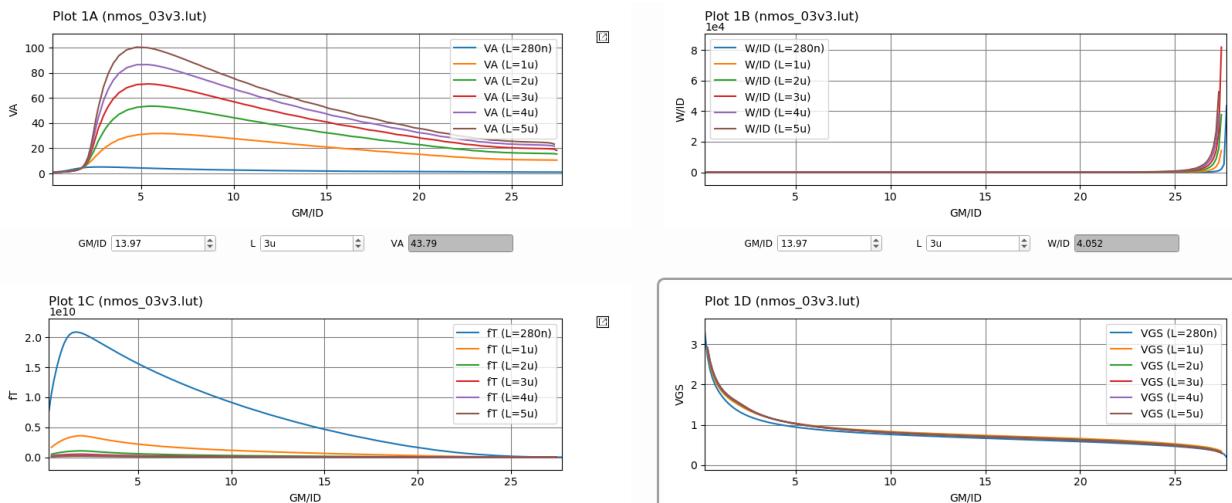
Fully-Differential Folded Cascode OTA

# PART 1: gm/ID Design Charts

- Plotting design charts vs gm/ID for PMOS.



- Plotting design charts vs gm/ID for NMOS.



## PART 2: OTA Design

Design a fully-differential folded cascode OTA with capacitive feedback that meets the specifications below.

Technology	GF180MCU
Supply voltage	2.5V
Closed loop gain	2
Phase margin at the required ACL	≥ 70°
CM input range – low	≤ 0
CM input range – high	≥ 1V
Differential output swing	1.2Vpk-to-pk
Load	500fF
DC Loop gain	60dB
CL settling time for 1% error	100ns

- From the above specs of closed loop we calculate specs for open loop

$$\text{for capacitive feedback } \beta = \frac{C_F}{C_F + C_S + C_{in}} \text{ by assuming } C_{in} \ll C_S \text{ as we will use minimum } L \text{ for input pair and as } A_{CL} = \frac{C_S}{C_F} = 2 \rightarrow C_S = 2C_F \rightarrow \beta = \frac{C_F}{C_S + C_F} = \frac{1}{3}$$

$$LG = 60dB = \beta A_{OL} \rightarrow A_{OL} = 69.5dB = 3000$$

$$\tau = \frac{t_{rise}}{4.6} = \frac{100ns}{4.6} = 21.7ns \rightarrow BW_{CL} = \frac{1}{2\pi * \tau} = \frac{1}{2\pi * 21.7ns} = 7.33MHz$$

$$BW_{OL} = \frac{BW_{CL}}{1 + LG} = \frac{7.33MHz}{1001} = 7.32kHz$$

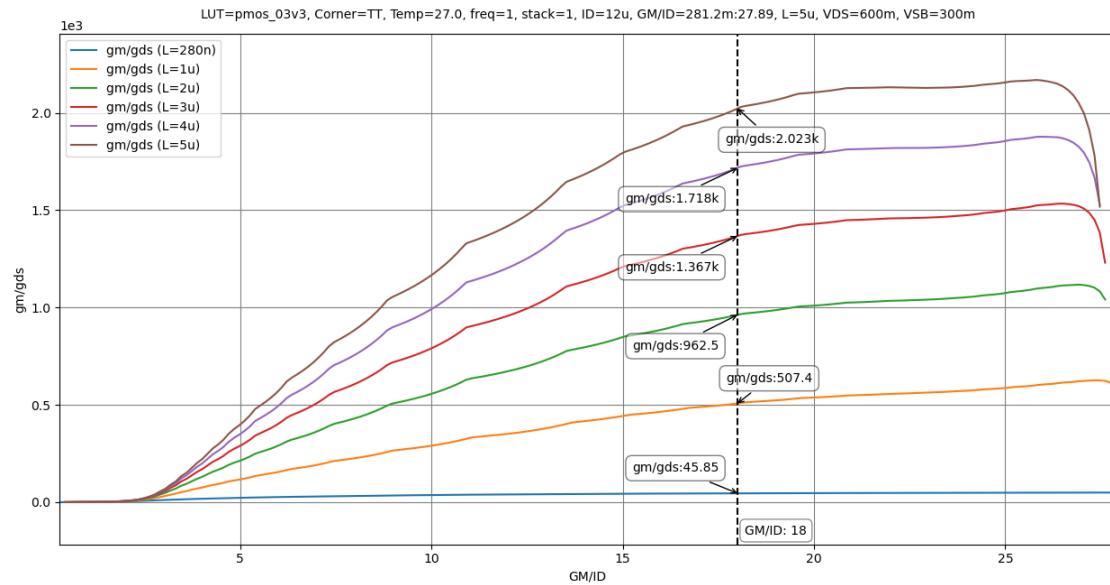
by taking the loading effect of feedback to ensure the same bandwidth for CL  
as  $C_{OUT} = C_L + (C_F || (C_S + C_{in})) = .5pF + (1pF||2pF) = .5pF + .667pF = 1.17pF$

$$GBW = A_{OL} * BW_{OL} = 3000 * 7.3kHz = 22MHz = \frac{g_m}{2\pi C_{OUT}} \rightarrow g_m = 2\pi C_{OUT} * 22MHz \approx 160\mu S$$

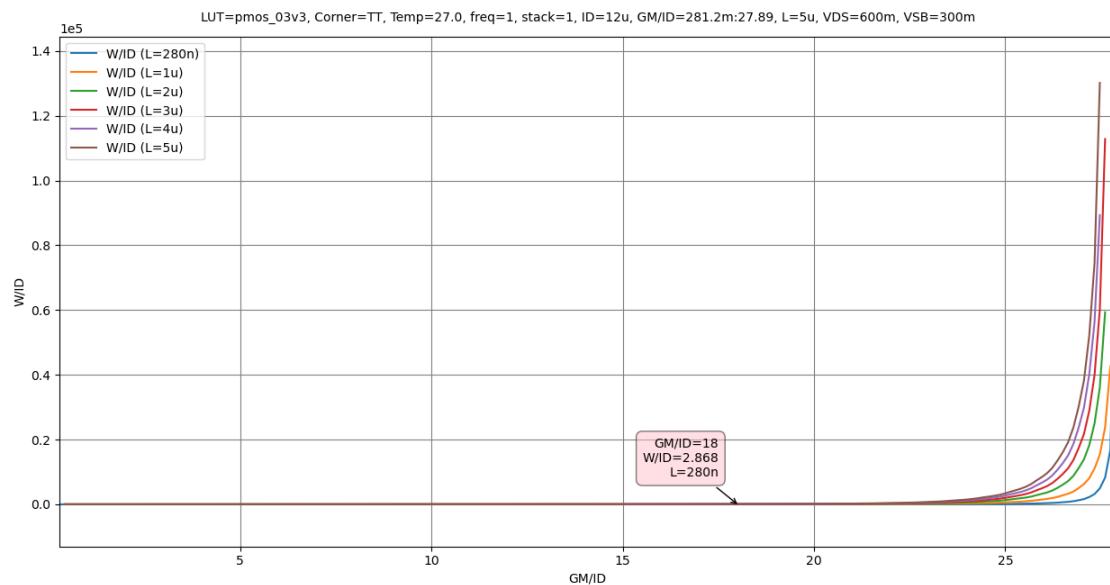
let's choose  $\frac{g_m}{I_D} = 18$  for input pair and  $I_D = 10\mu A$  so  $gm = 180\mu S$

### Design of Input Pair

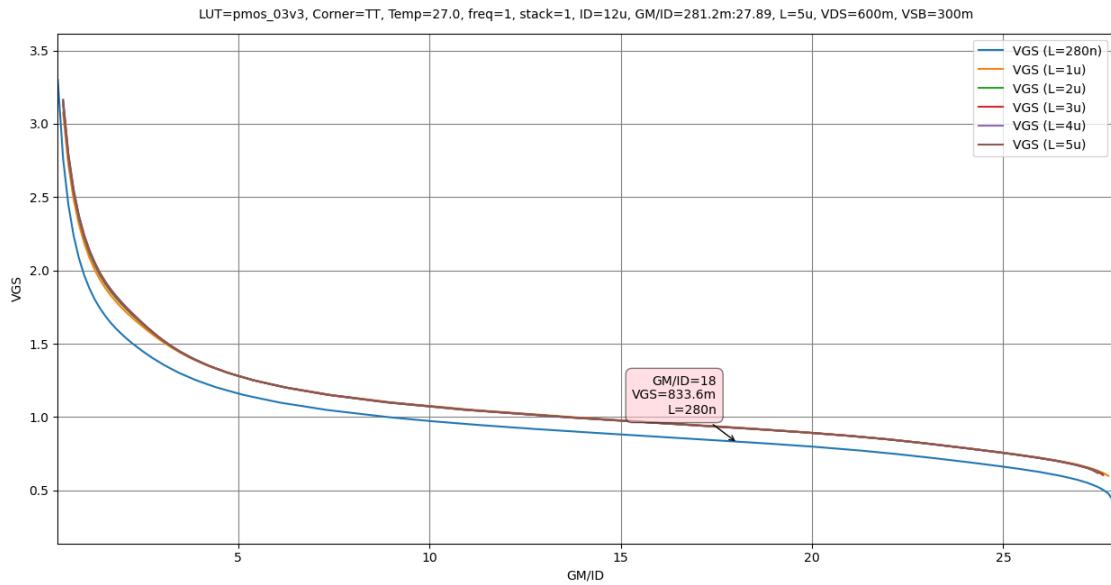
- From the CMIR spec we find that we need a PMOS input stage.
- For the input pair use short L and bias it in MI or WI. This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG)



$$- g_{ds} = \frac{180\mu S}{45.85} = 5.02\mu S$$

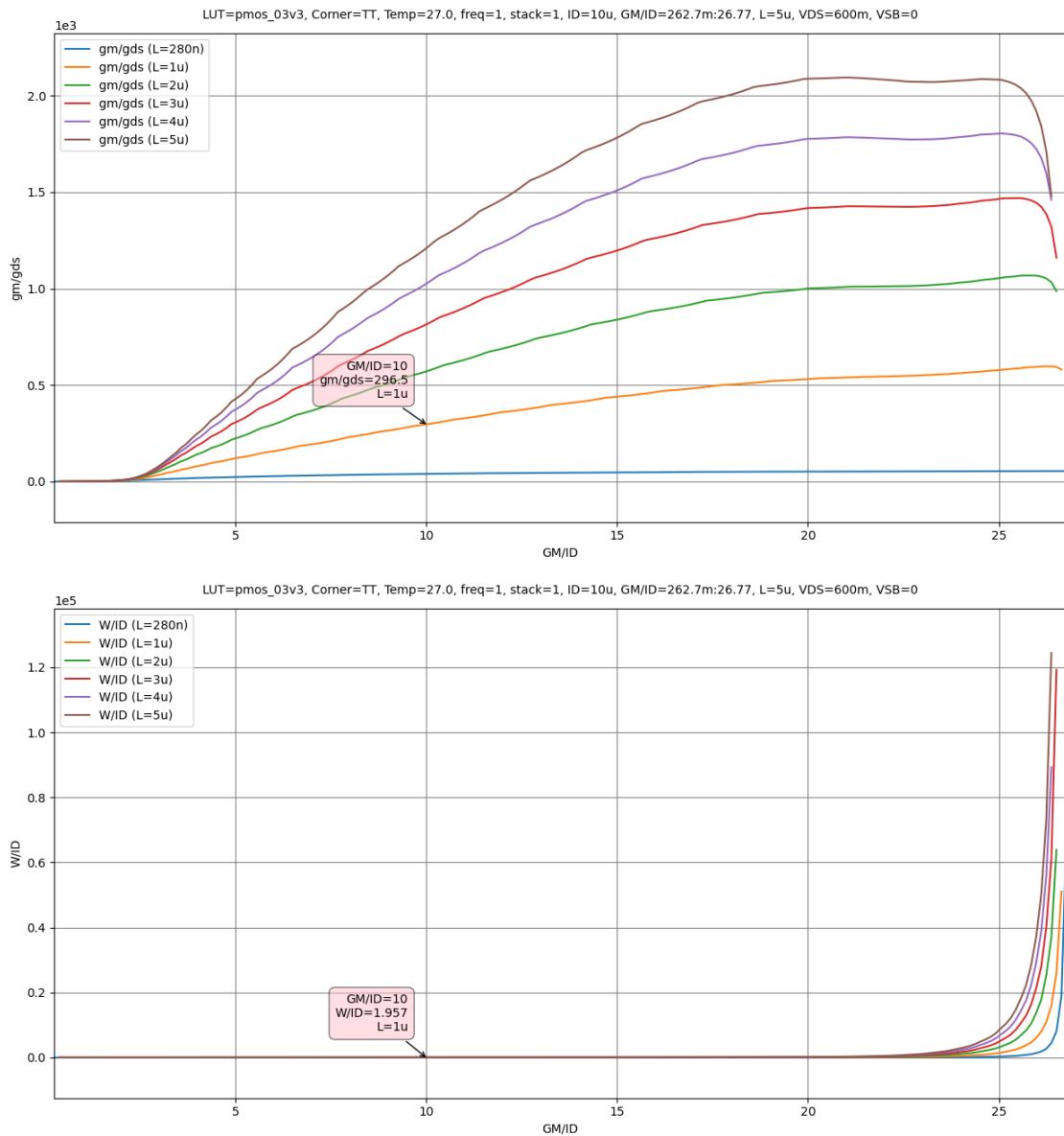


- $L = 280nm$  and  $\frac{g_m}{I_D} = 18$  and  $W = 2.868 * 10\mu A = 28.68\mu m$



### ***Design of PMOS Current Mirror***

- From the CMIR High specs  
 $CMIR_{HIGH} = -|V_{GS1}| - |V_{6max}^*| + V_{DD} \rightarrow |V_{6max}^*| = -|V_{GS1}| - CMIR_{HIGH} + V_{DD}$   
 $|V_{6max}^*| = -834mV - 1000mV + 2500mV = 666mV \rightarrow \frac{g_m}{I_D} > 3$
- For the current source transistors use relatively long L and bias them in SI, e.g.,  
 $L = 1\mu m$  and  $\frac{g_m}{I_D} = 10$ . These transistors contribute significant offset and noise.  
A large gm will not help the gain but will increase the offset and noise.



- Using unit transistor carry  $I_B = 5\mu A$
- $W = 1.957 * 5\mu A = 9.8\mu m$  and  $L = 1\mu m$  and  $\frac{g_m}{I_D} = 10$

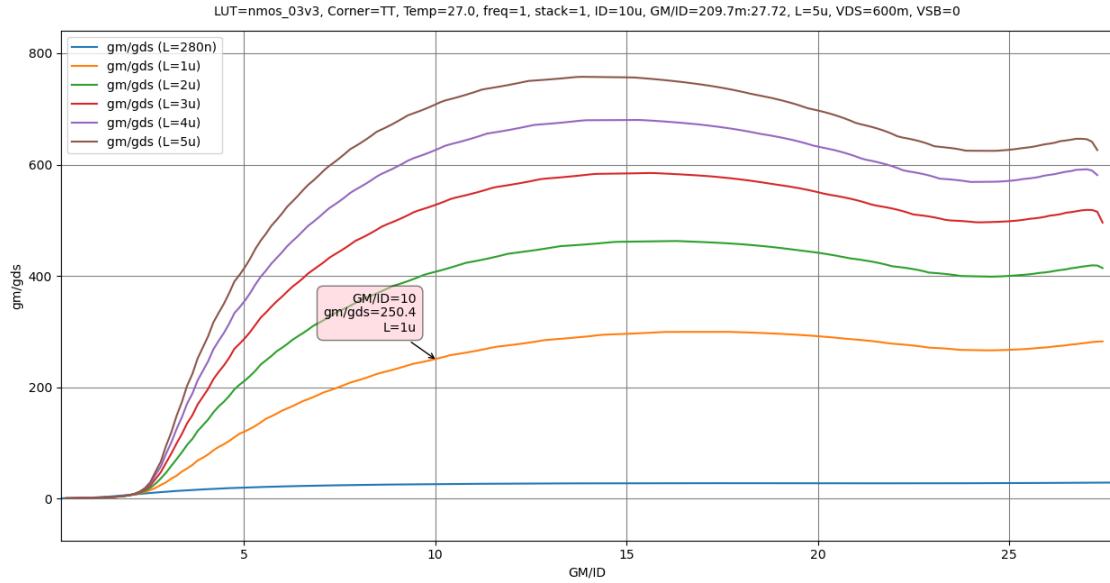
### Design of NMOS Current Mirror

- From CMIR LOW

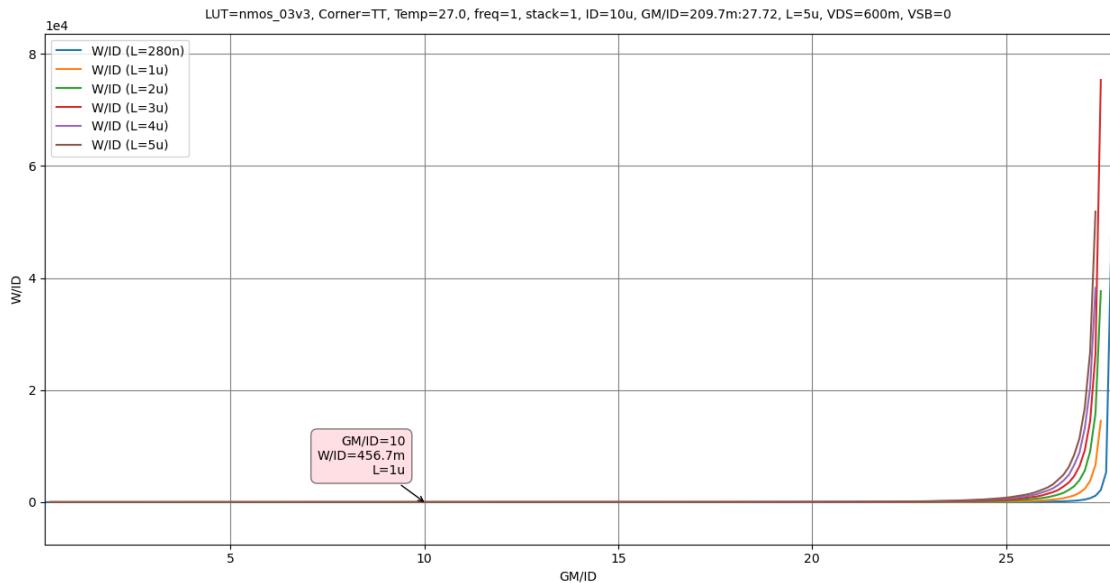
$$CMIR_{LOW} = -|V_{GS1}| + V_1^* + V_{2max}^* \rightarrow V_{2max}^* = CMIR_{LOW} + |V_{GS1}| - V_1^*$$

$$V_{2max}^* = 0 + 834mV - 111mV = 723mV \rightarrow \frac{g_m}{I_D} > 2.77$$

- For the current source transistors use relatively long L and bias them in SI, e.g.,  $L = 1\mu m$  and  $\frac{g_m}{I_D} = 10$ . These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the offset and noise.



- $g_{ds} = \frac{200\mu S}{250.4} = 800nS$



- Using unit transistor carry  $I_D = 5\mu A$
- $W = .457 * 5\mu A = 2.29\mu m$  and  $L = 1\mu m$

## Design of NMOS Common Gate

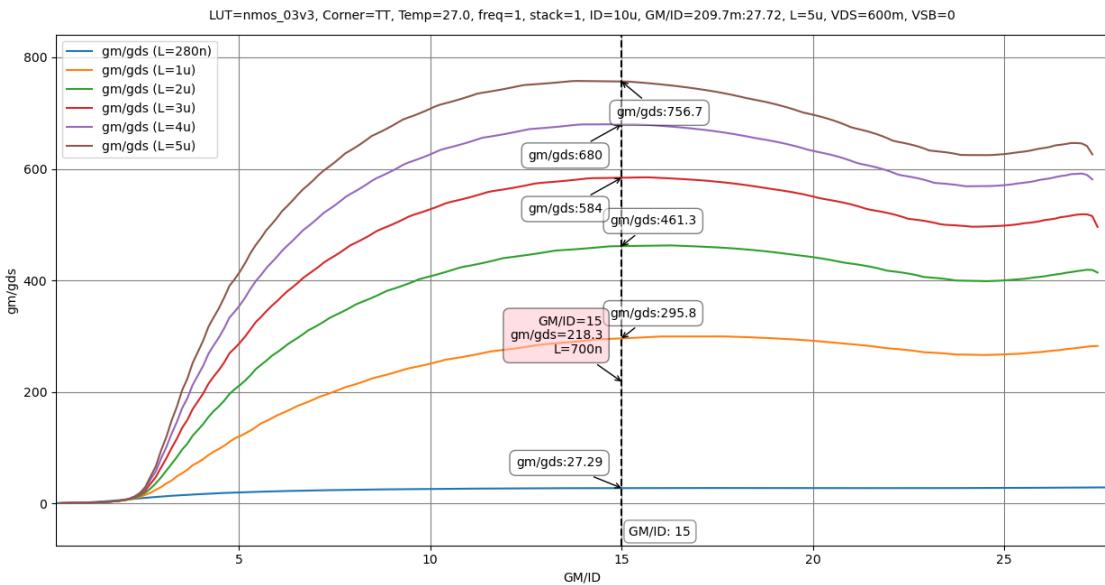
$$A_{OL} \geq 3000 = g_{m1} * R_{out} \rightarrow R_{out} = 16.7M\Omega$$

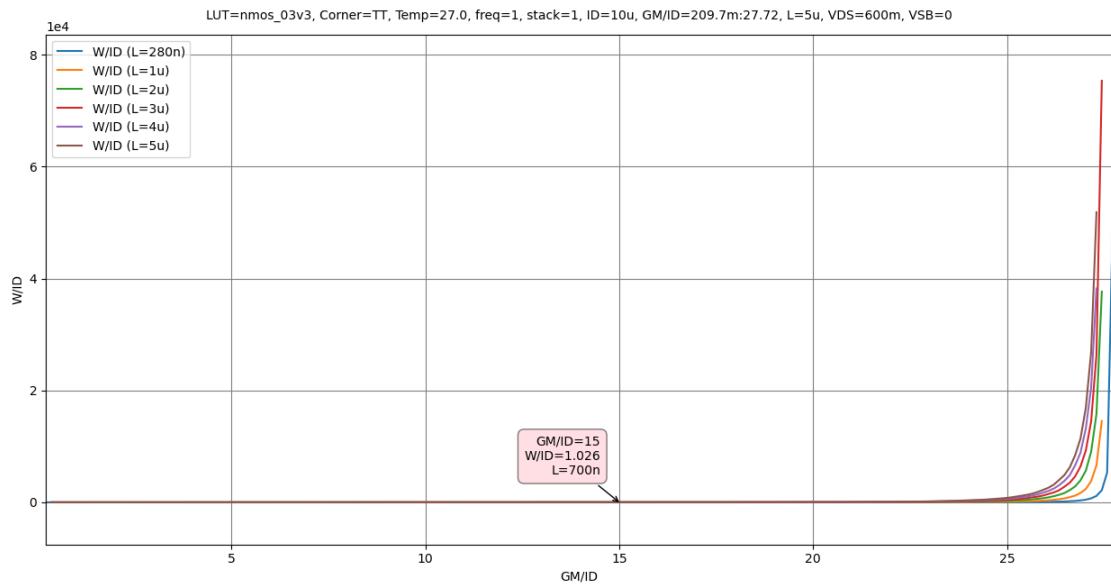
- By make the above resistance equal to the below resistance then  $R_{out}$  for CG NMOS  $R_{out1} = 16.7M\Omega * 2 = 33.4M\Omega$
- As we need maximum swing equal  $1.2V_{PK-to-PK}$  then we need  $.6V_{PK-to-PK}$  From one side then we need  $.3V_{PK}$  to get high swing we design

$$V_{OCM} = \frac{V_{DD}}{2} = 1.25 \text{ then for swing } .3V_{PK}$$

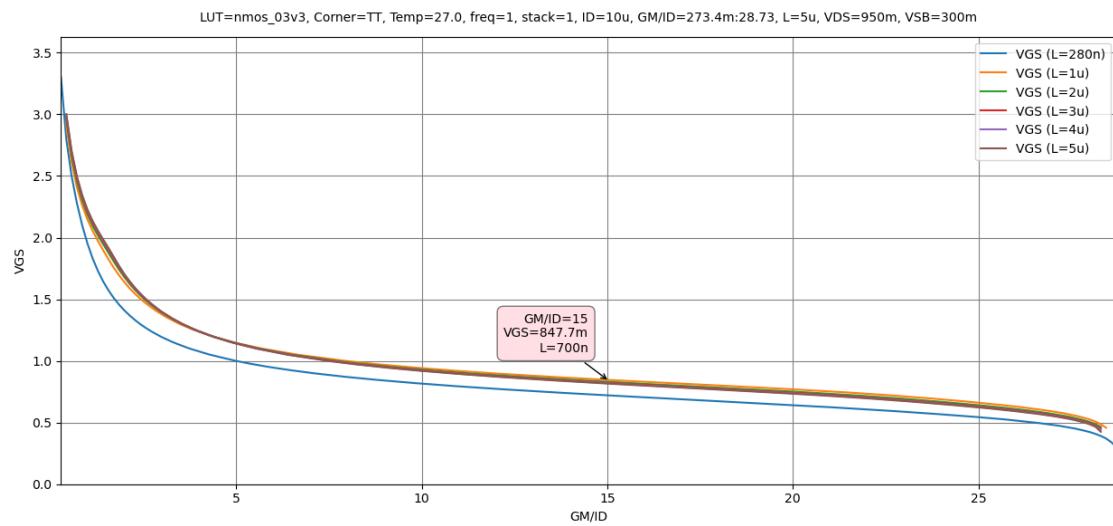
$$1.25V - .3V = V_{3max}^* + V_2^* \rightarrow V_{3max}^* = .95V - .2V = .75V \rightarrow \frac{g_m}{I_D} > 2.67$$

$$R_{out1} = \frac{g_{m3}}{g_{ds3}} * (r_{o1} || r_{o2}) = \frac{g_{m3}}{g_{ds3}} * \left( \frac{1}{5.02\mu S} || \frac{1}{800ns} \right) = 33.4M\Omega \rightarrow \frac{g_{m2}}{g_{ds}} = 206$$





- $W = 1.026 * 10\mu A = 10.3\mu m$  and  $L = 700nm$

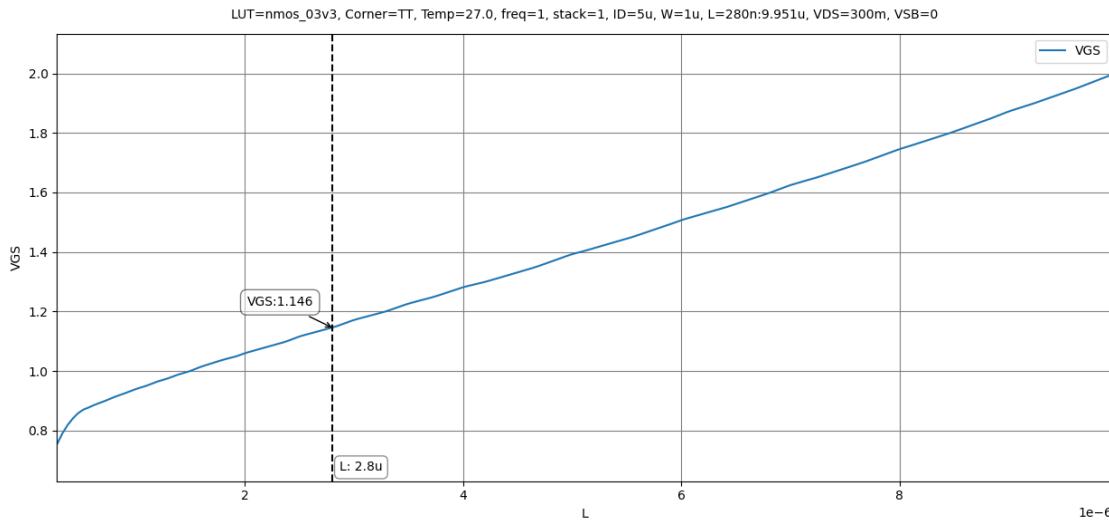


- For biasing NMOS CG and the NOMS tail current source by get current source .3V to biasing it deep in saturation

$$V_{CASCN} = V_{GS3} + .3V \approx 850mV + 300mV = 1.15V$$

### **Design of biasing circuit for NMOS Common Gate**

- We need to generate 1.15V by using NMOS with  $W = 1\mu m$  and using  $I_B = 5\mu A$  then we sweep L to generate required voltage



- $L = 2.8\mu m$  and  $W = 1\mu m$

### **Design of PMOS Common Gate**

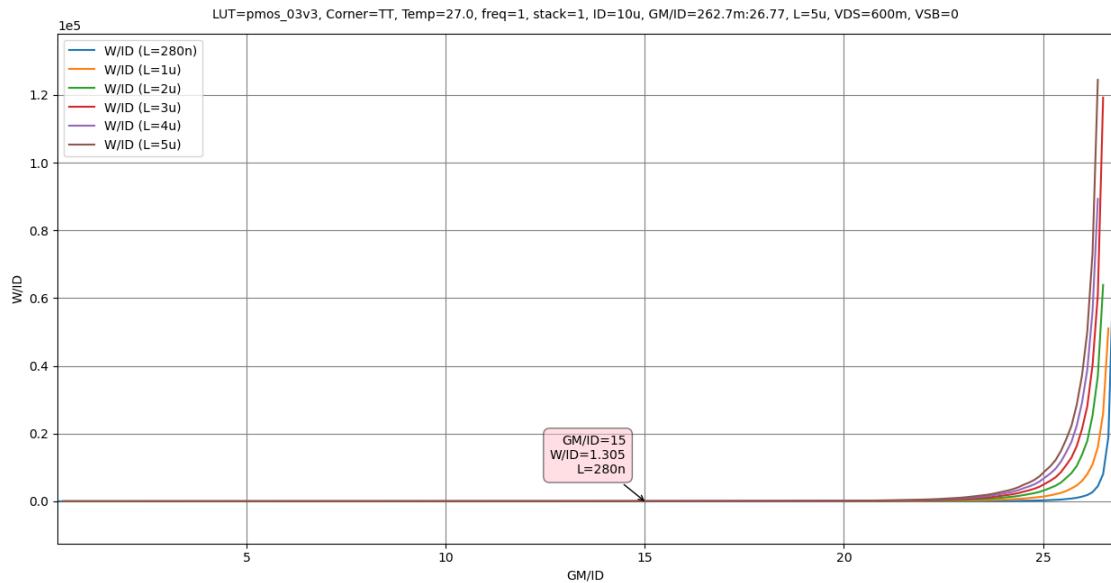
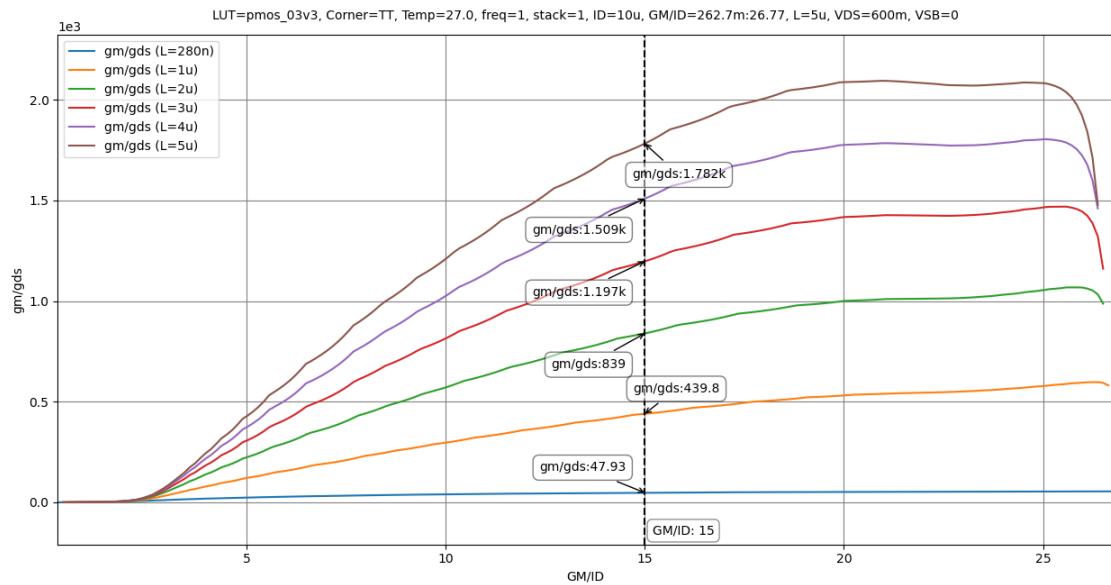
- For PMOS CG we need  $R_{out2} = 33.4M\Omega$
- As we need maximum swing equal  $1.2V_{PK-to-PK}$  then we need  $.6V_{PK-to-PK}$  From one side then we need  $.3V_{PK}$  to get high swing we design

$$V_{OCM} = \frac{V_{DD}}{2} = 1.25 \text{ then for swing } .3V_{PK}$$

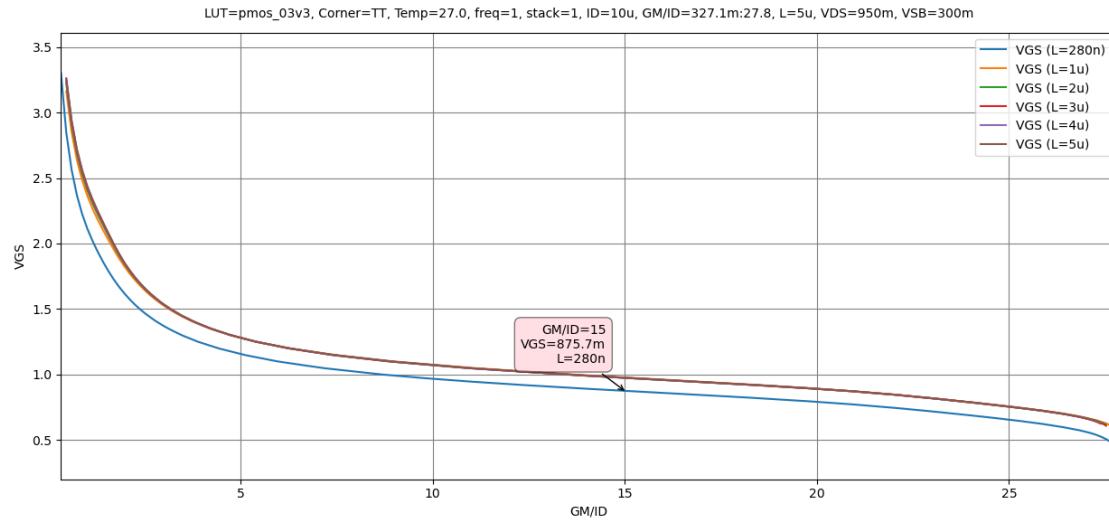
$$1.25V + .3V = V_{DD} - V_{4max}^* - V_5^* \rightarrow V_{4max}^* = V_{DD} - 1.55V - V_5^*$$

$$V_{4max}^* = 2.5 - 1.55V - .2V = .75V \rightarrow \frac{g_m}{I_D} > 2.7$$

$$R_{out2} = \frac{g_{m4}}{g_{ds4}} * r_{o5} = \frac{g_{m4}}{g_{ds4}} * \frac{1}{.8\mu S} = 33.4M\Omega = \frac{g_{m3}}{g_{ds3}} = 27$$



- $W = 1.305 * 10\mu S = 13.05\mu m$  and  $L = 280nm$

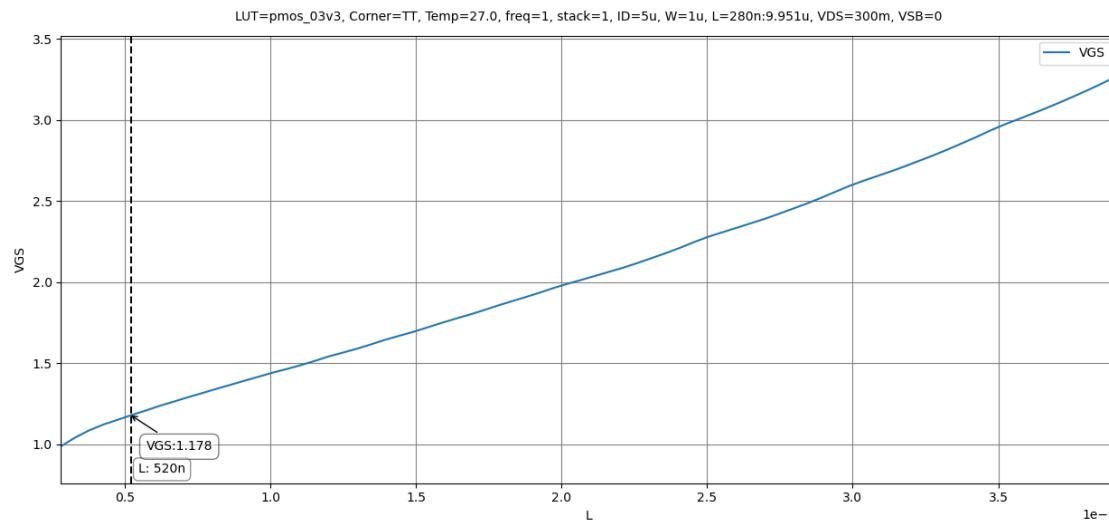


- For biasing PMOS CG and the POMS tail current source by get current source .3V to biasing it deep in saturation

$$V_{CASCSP} = V_{DD} - .3V - |V_{GS4}| = 2.5V - .3V - .88V \approx 1.32$$

### ***Design of biasing circuit for PMOS Common Gate***

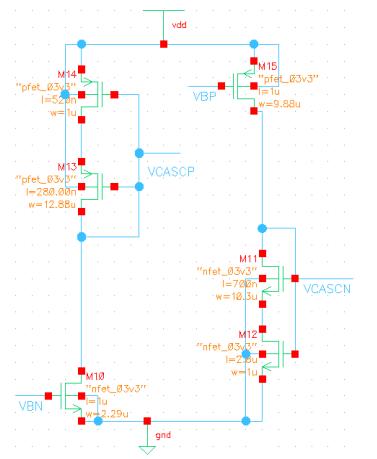
- We need to generate  $V_{DD} - 1.32V = 1.18$  by using NMOS with  $W = 1\mu m$  and using  $I_B = 5\mu A$  and sweep L to generate required voltage



- $L = 520nm$  and  $W = 1\mu m$

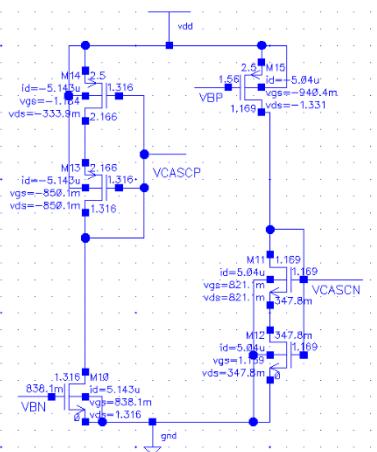
## The Biasing Circuit

- The biasing circuit for NMOS CG and PMOS CG
- M10&M15 are current source for biasing the branch with  $I_B = 5\mu A$
- M11 are typical to M3 this to match the change in  $V_{TH}$  and  $\mu_e$  in M3 and cancel it
- M13 are typical to M4 this to match the change in  $V_{TH}$  and  $\mu_h$  in M4 and cancel it



## TestBench for Biasing Circuit

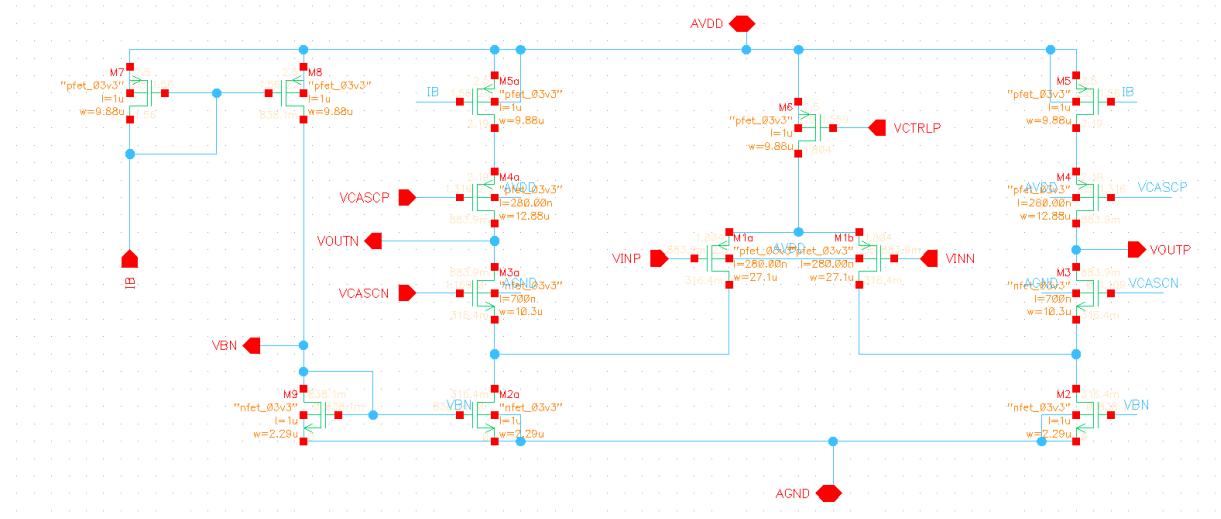
- We see that the  $V_{CASCP} = 1.316V$  and  $V_{CASCN} = 1.169V$



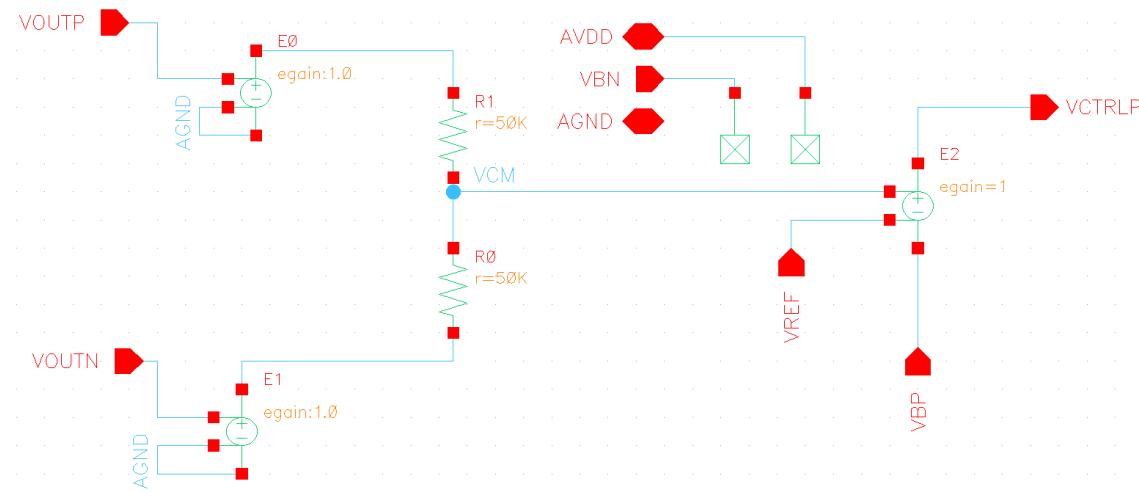
transistor	$L$	$W$	$g_m/I_D$	$I_D$	$g_m$	$V_{dsat}$	$V_{ov}$	$V^*$
M1&M1a	280nm	27.1 $\mu m$	18S/A	10 $\mu A$	180 $\mu S$	87.2mV	11.3mV	111mV
M2&M2a	1 $\mu m$	2.29 $\mu m \times 4$	10S/A	20 $\mu A$	200 $\mu S$	172mV	149mV	200mV
M3&M3a	700nm	10.3 $\mu m$	15S/A	10 $\mu A$	150 $\mu S$	110mV	49.7mV	133mV
M4&M4a	280nm	12.88 $\mu m$	15S/A	10 $\mu A$	150 $\mu S$	116mV	60.4mV	133mV
M5&M5a	1 $\mu m$	9.88 $\mu m \times 2$	10S/A	10 $\mu A$	100 $\mu S$	156mV	160mV	200mV
M6	1 $\mu m$	9.88 $\mu m \times 4$	10S/A	20 $\mu A$	200 $\mu S$	156mV	160mV	200mV

## PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- Schematic of Fully-Differential Folded Cascode OTA

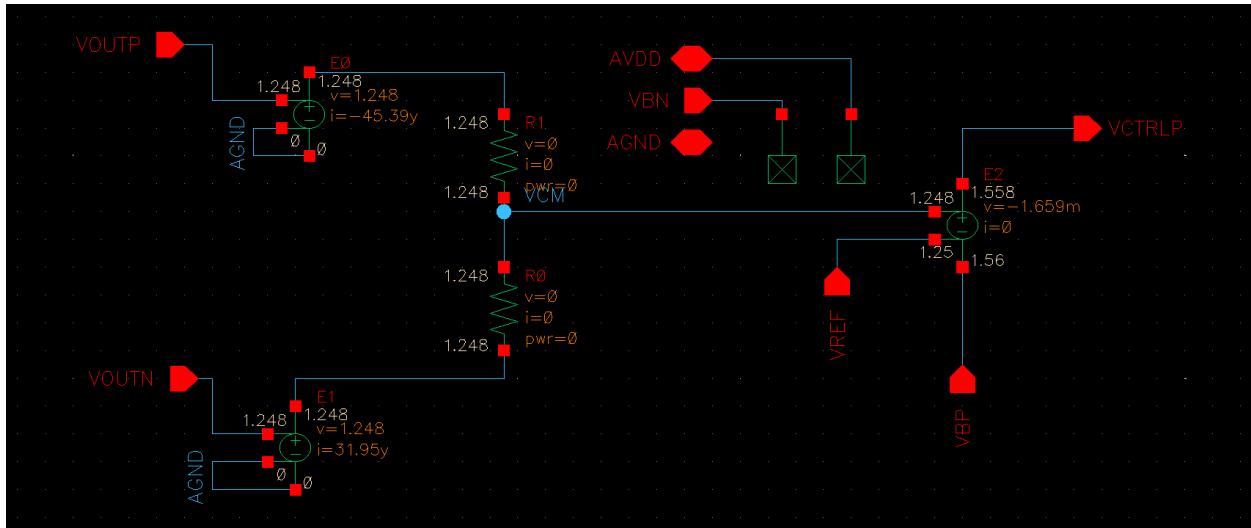
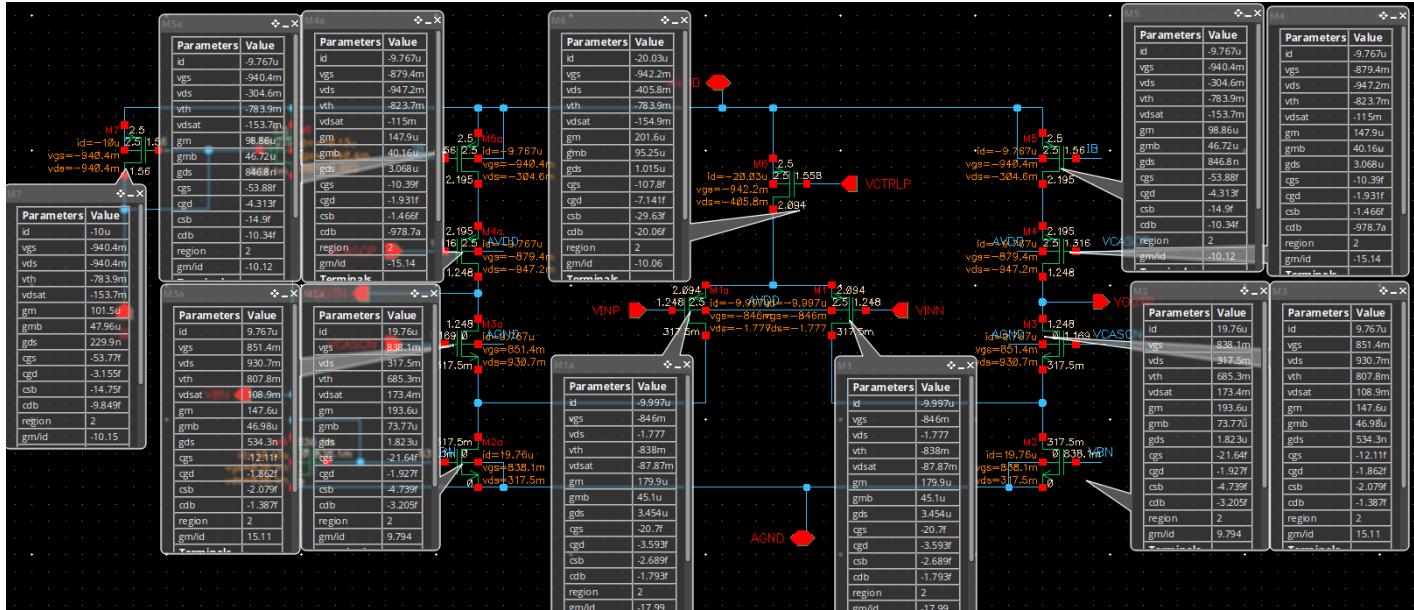


- Schematic of behavioral model of Common Mode FeedBack



# 1. OP (Operating Point) Analysis

## 1. Schematic of the OTA with DC node voltages and transistors OP parameters



2. The CM level at the OTA output  $V_{DS3} + V_{DS2} = 930.7mV + 317.5mV = 1.248V$   
And this approximately equal to the  $V_{REF} = 1.25V$  we apply to set the CM output voltage

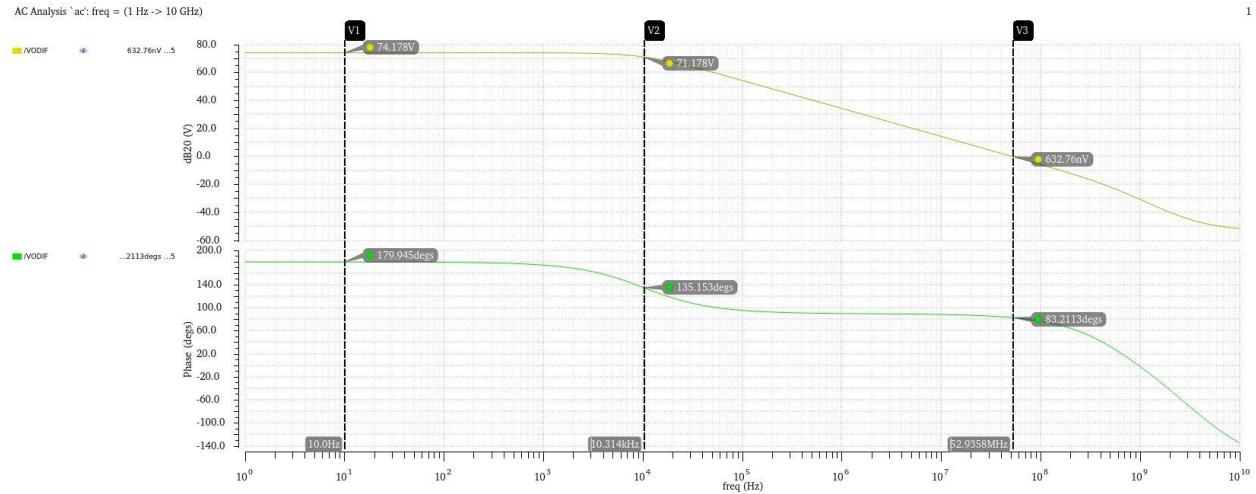
3. For error amplifier

$$V_{in_{dif}} = 1.248 - 1.25 = -2mV \text{ & } V_{out_{dif}} = 1.558 - 1.56 = -2mV \rightarrow \frac{V_{out_{dif}}}{V_{in_{dif}}} = 1$$

- We see that the relation between  $V_{in_{dif}} = V_{out_{dif}}$

## 2. Diff small signal ccs

### 1. Plot diff gain (magnitude in dB and phase) vs frequency



### 2. The result from simulation

ITI2024Su:Lab11_tb:1	AOL	5.116k
ITI2024Su:Lab11_tb:1	AOL_dB	74.18
ITI2024Su:Lab11_tb:1	BW	10.33k
ITI2024Su:Lab11_tb:1	GBW	52.85M
ITI2024Su:Lab11_tb:1	UGF	53.2M
ITI2024Su:Lab11_tb:1	PM	83.24

### 3. Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

$$A_{OL} = g_{m1} * \left( \frac{g_{m4}}{g_{ds4}} * r_{o5} \parallel \frac{g_{m3}}{g_{ds3}} * (r_{o2} + r_{o1}) \right) = \\ 179.9\mu S * \left( \frac{147.9\mu S}{3.068\mu S} * \frac{1}{846.8nS} \parallel \frac{147.6\mu S}{534.3nS} * \left( \frac{1}{1.823\mu S} \parallel \frac{1}{3.454\mu S} \right) \right) = 4910 = 73.8dB$$

$$BW = \frac{1}{2\pi * R_{out} * C_{out}} = \frac{1}{2\pi * \left( \frac{g_{m4}}{g_{ds4}} * r_{o5} \parallel \frac{g_{m3}}{g_{ds3}} * (r_{o2} + r_{o1}) \right) * C_L} = \\ \frac{1}{2\pi \left( \frac{147.9\mu S}{3.068\mu S} * \frac{1}{846.8nS} \parallel \frac{147.6\mu S}{534.3nS} * \left( \frac{1}{1.823\mu S} \parallel \frac{1}{3.454\mu S} \right) * 500fF \right)} = 11.5kHz$$

$$UGF = GBW = A_{OL} * BW = 4910 * 11.5kHz = 56.5MHz$$

$$f_{p2} = \frac{1}{2\pi * C_{folded} * R_{folded}} = \frac{1}{2\pi * 24.7fF * 17.3k\Omega} = 372.5MHz$$

$$PM = 90 - \tan^{-1} \left( \frac{f_u}{f_{p2}} \right) = 81.4$$

	Simulation	Analysis
<b>Gain</b>	74.18dB	73.8dB
<b>Bandwidth</b>	10.33kHz	11.5kHz
<b>GBW</b>	52.85MHz	56.5MHz
<b>UGF</b>	53.2MHz	56.5MHz
<b>PM</b>	83.24	81.4

## PART 4: Open-Loop OTA Simulation (Actual CMFB)

- You may assume  $L = 1\mu m$  and  $\frac{g_m}{I_D} = 15$  for all transistors with unknown  $L$  or  $\frac{g_m}{I_D}$  for simplicity and the other transistor used as current source or current load we will use  $L = 1\mu m$  and  $\frac{g_m}{I_D} = 10$  as we use in Fully-Differential Folded Cascode OTA
- We need CD (source followers) to buffer the OTA output. This avoids loading the OTA with the sensing resistors

PMOS

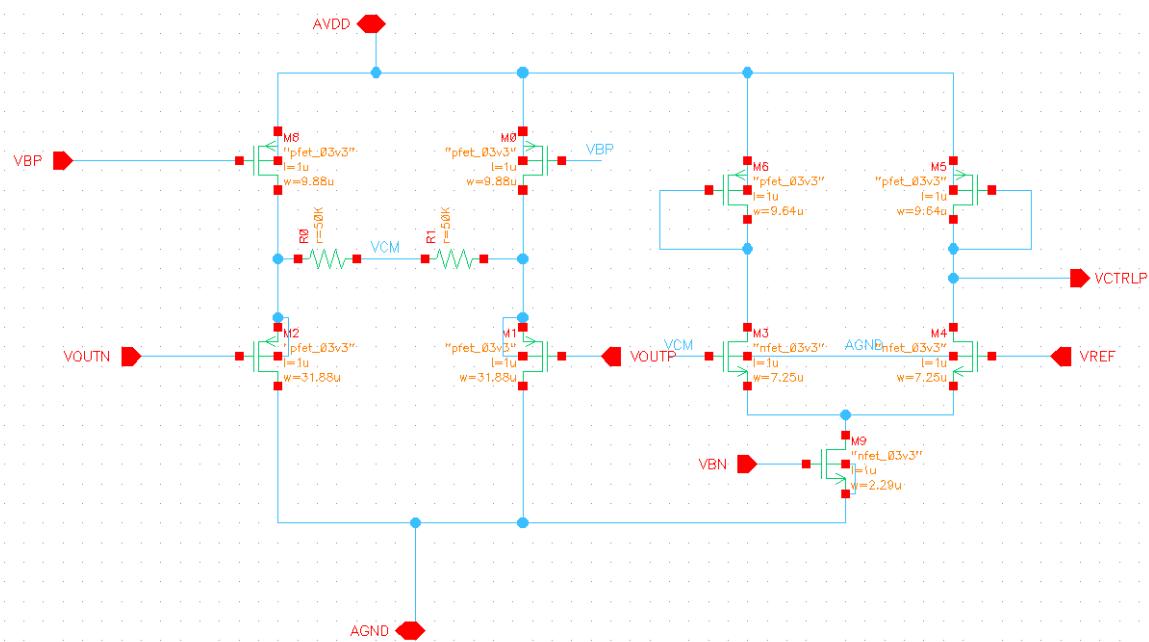
TT-27.0		
	Name	
4	W	31.88u
5	VGS	846.2m
6	VDS	1.25
7	VSB	0
8	gm/ID	14.85
9	Vstar	134.7m
10	fT	112.7MEG
11	gm/gds	697.2
12	VA	46.95
13	ID/W	156.8m

NMOS

TT-27.0		
	Name	
4	W	7.25u
5	VGS	830.7m
6	VDS	1
7	VSB	250m
8	gm/ID	14.8
9	Vstar	135.1m
10	fT	662.8MEG
11	gm/gds	358.4
12	VA	24.22
13	ID/W	689.7m

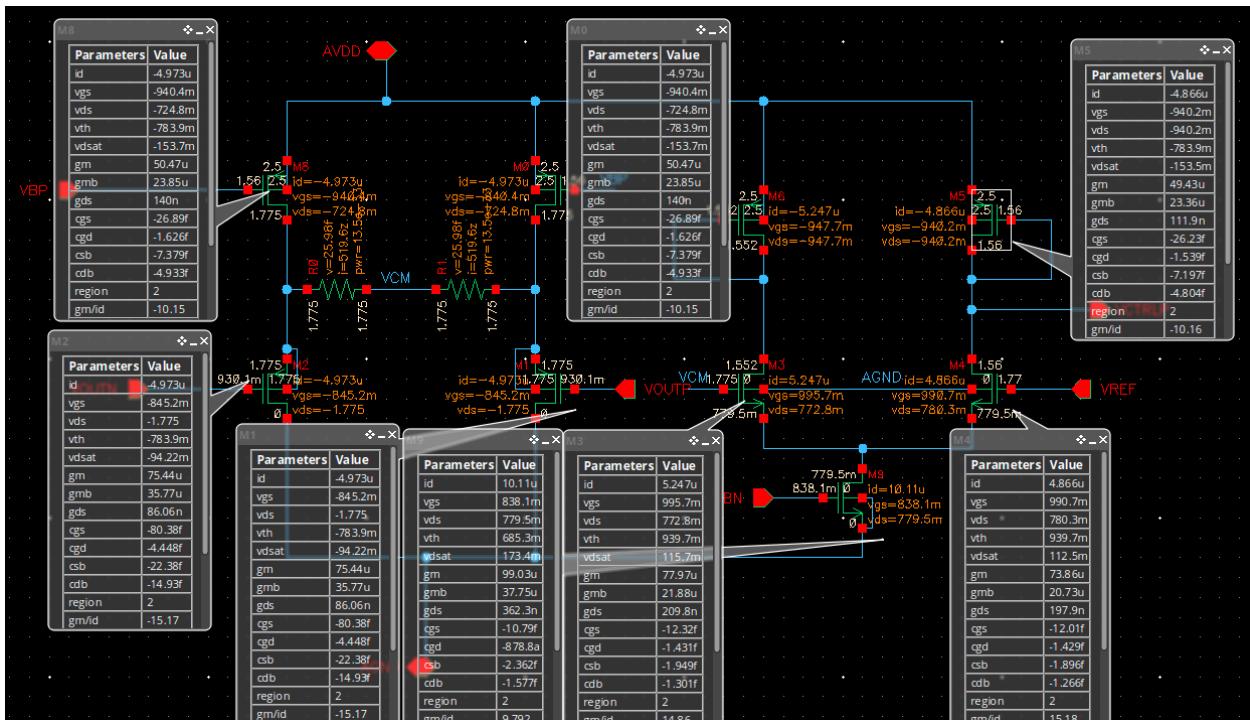
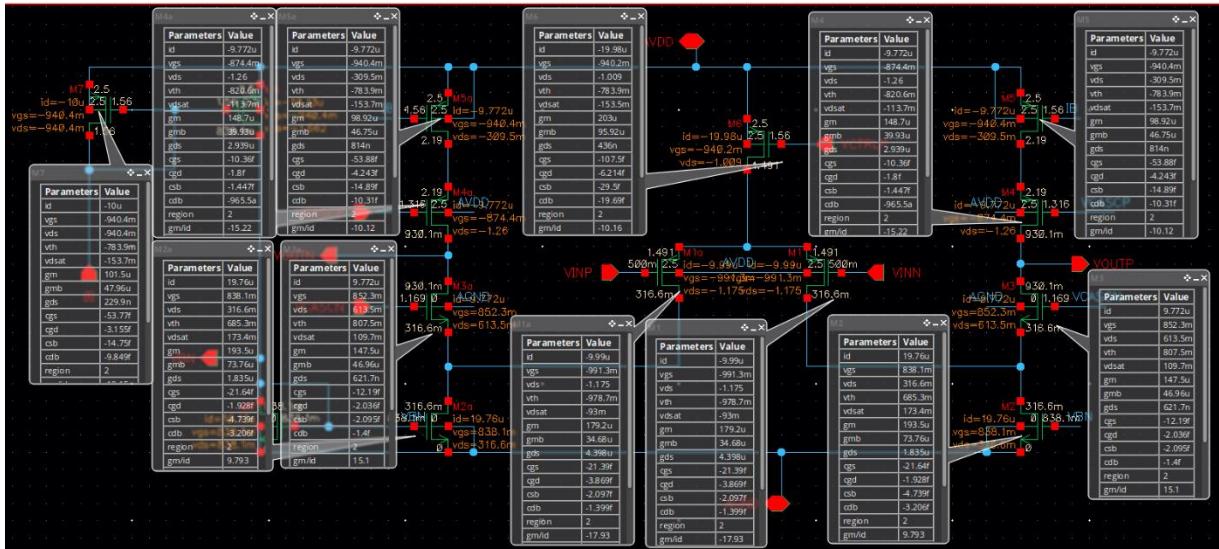
- The CMFB limits the output swing. Max  $V_{out}$  is  $V_{DD} - V^* - |VGSP|$ . One reason why we selected PMOS CD is to avoid increasing  $V_{TH}$  by body effect (increasing  $V_{TH}$  will limit output swing even more).
- The output range now is from  $2V^* = 400mV$  to  $V_{DD} - V^* - |VGSP| = 2.5 - .2 - .846 \approx 1.45V \rightarrow V_{OCM} = \frac{1.45+.4}{2} = .92$
- The output of the CD buffer is close to VDD; thus, we select NMOS input for the error amplifier.
- The error amplifier is a simple differential amplifier with diode connected loads. We don't need high gain from the error amplifier, but we need low impedance nodes to avoid deteriorating the stability of the CMFB loop.
- The bias point output of the error amplifier is equal to  $VDD - |VGSP|$ . That's why we use the error amplifier output to control the PMOS current source in the folded OTA rather than the NMOS current source.

- The schematic of Common Mode FeedBack



## 1. OP (Operating Point) Analysis

### 1. Schematic of the OTA with DC node voltages and transistors OP parameters



- The CM level at the OTA output  $V_{DS3} + V_{DS2} = 613.5mV + 316.6mV = 930.1mV$  And this approximately equal to the  $V_{REF} = 925mV$  we apply to set the CM output voltage

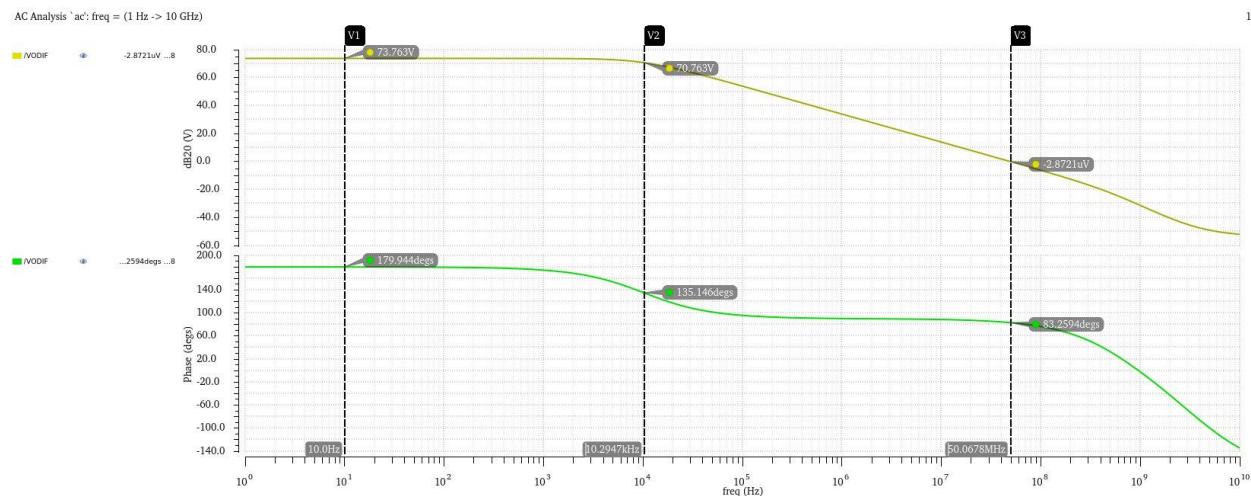
### 3. For error amplifier

$$V_{in_{dif}} = 1.775 - 1.77 = 5mV \text{ & } V_{out_{dif}} = 1.56 - 1.552 = 8mV \rightarrow \frac{V_{out_{dif}}}{V_{in_{dif}}} = 1.6$$

4. We see that the relation between  $V_{out_{dif}} = 1.6V_{in_{dif}}$  as we design the error amplifier with low gain

## 2. Diff small signal ccs

1. Plot diff gain (magnitude in dB and phase) vs frequency



### 2. The result from simulation

ITI2024Su:Lab11_tb:1	AOL	4.877k
ITI2024Su:Lab11_tb:1	AOL_dB	73.76
ITI2024Su:Lab11_tb:1	BW	10.31k
ITI2024Su:Lab11_tb:1	GBW	50.29M
ITI2024Su:Lab11_tb:1	UGF	50.07M
ITI2024Su:Lab11_tb:1	PM	83.26

3. Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

$$A_{OL} = g_{m1} * \left( \frac{g_{m4}}{g_{ds4}} * r_{o5} \parallel \frac{g_{m3}}{g_{ds3}} * (r_{o2} + r_{o1}) \right) = \\ 179.2\mu S * \left( \frac{148.7\mu S}{2.393\mu S} * \frac{1}{814nS} \parallel \frac{147.5\mu S}{621.7nS} * \left( \frac{1}{1.835\mu S} \parallel \frac{1}{4.398\mu S} \right) \right) = 4552 = 73.16dB$$

$$BW = \frac{1}{2\pi * R_{out} * C_{out}} = \frac{1}{2\pi * \left( \frac{g_{m4}}{g_{ds4}} * r_{o5} \parallel \frac{g_{m3}}{g_{ds3}} * (r_{o2} + r_{o1}) \right) * C_L} =$$

$$\frac{1}{2\pi(\frac{148.7\mu S}{2.393\mu S} * \frac{1}{814nS} || \frac{147.5\mu S}{621.7nS} * (\frac{1}{1.835\mu S} || \frac{1}{4.398\mu S})) * 500fF} = 12.3kHz$$

$$UGF = GBW = A_{OL} * BW = 4552 * 12.3kHz = 56MHz$$

$$f_{p2} = \frac{1}{2\pi * C_{folded} * R_{folded}} = \frac{1}{2\pi * 24.7fF * 17.3k\Omega} = 372.5MHz$$

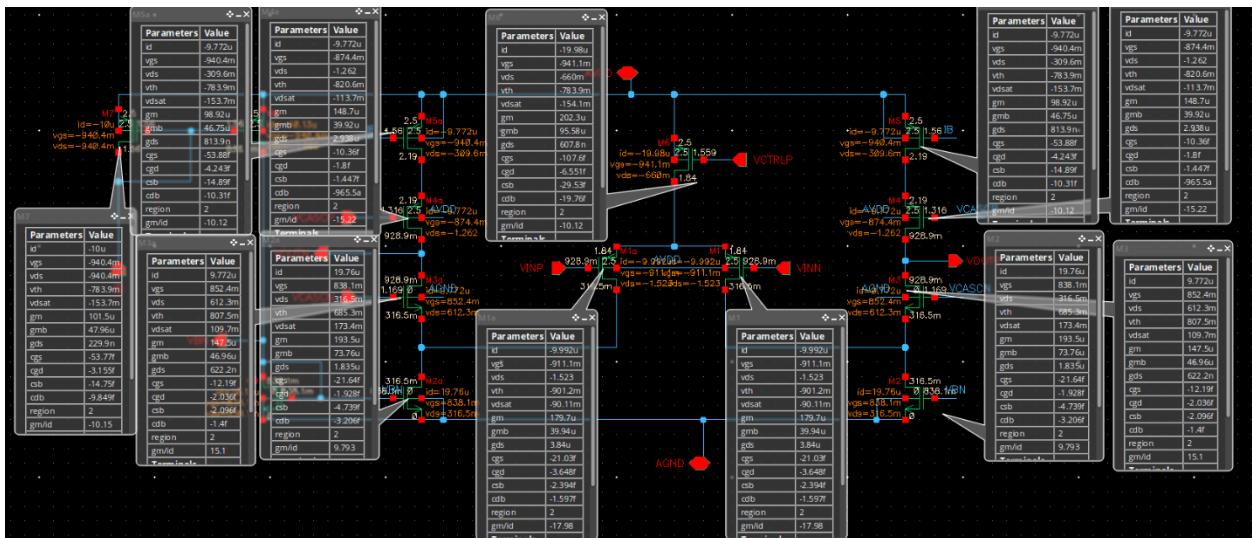
$$PM = 90 - \tan^{-1} \left( \frac{f_u}{f_{p2}} \right) = 81.4$$

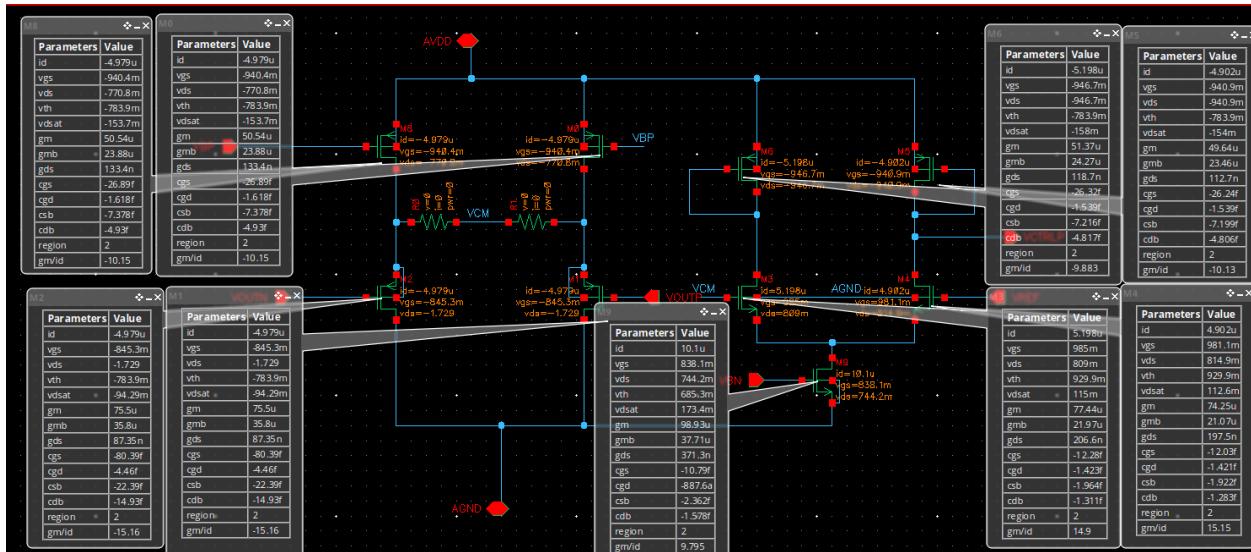
	Simulation	Analysis
<b>Gain</b>	73.76dB	73.8dB
<b>Bandwidth</b>	10.31kHz	12.3kHz
<b>GBW</b>	50.29MHz	56MHz
<b>UGF</b>	50.07MHz	56MHz
<b>PM</b>	83.24	81.4

## PART 5: Closed Loop Simulation (AC and STB Analysis)

### 1. OP (Operating Point) Analysis

- Schematic of the OTA with DC node voltages and transistors OP parameters

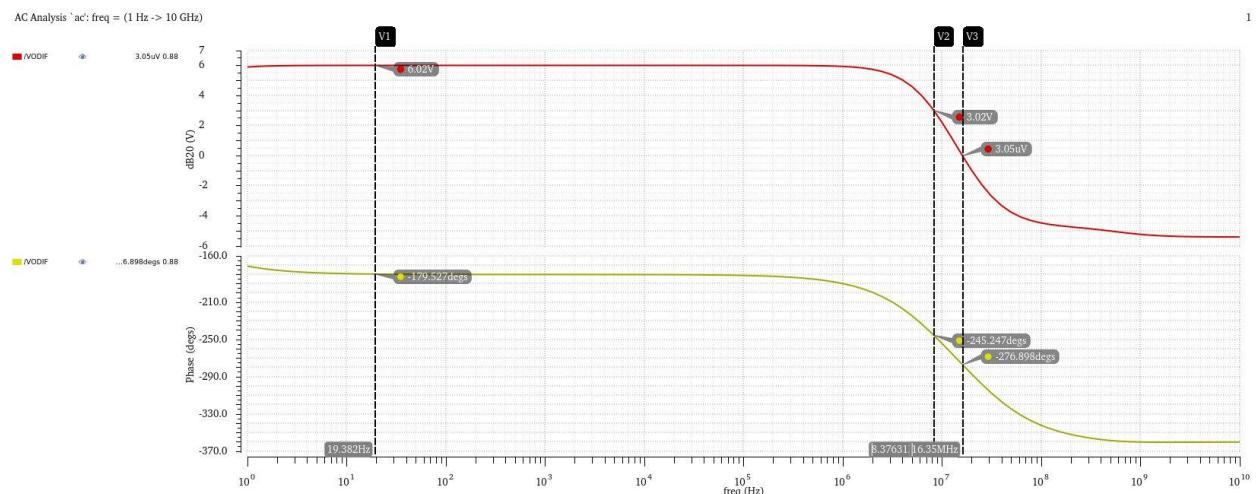




2. the CM level at the OTA output is  $928.9\text{mV}$  and it's approximately equal to  $V_{REF} = 925\text{mV}$  as the CMFB make the output around  $V_{REF}$
3. the CM level at the OTA input  $928.9\text{mV}$  and it's approximately equal to  $V_{REF} = 925\text{mV}$  as capacitors are open circuit in dc so the connection is  $1T\Omega$  resistance connect between the output and the input and as OTA don't allow the current to pass in dc so the input will by same as output

## 2. Differential closed-loop response:

1. Plot VODIFF vs frequency

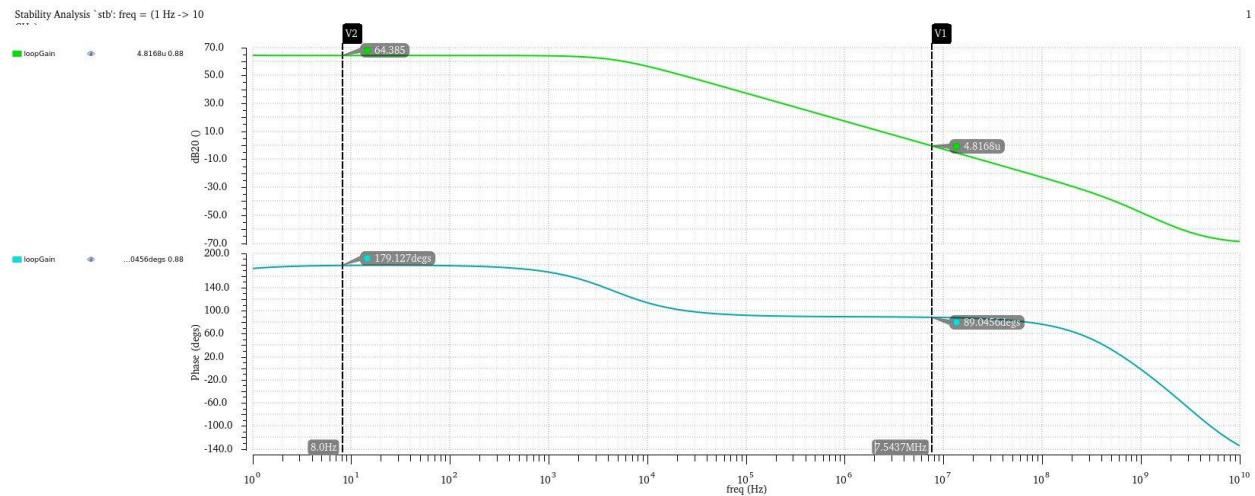


## 2. Result from simulation

ITI2024Su:Lab11_tb:1	ACL	1.999
ITI2024Su:Lab11_tb:1	ACL_dB	6.016
ITI2024Su:Lab11_tb:1	BW	8.652M
ITI2024Su:Lab11_tb:1	GBW	17.3M
ITI2024Su:Lab11_tb:1	UGF	16.39M

## 3. Differential and CMFB loops stability (STB analysis):

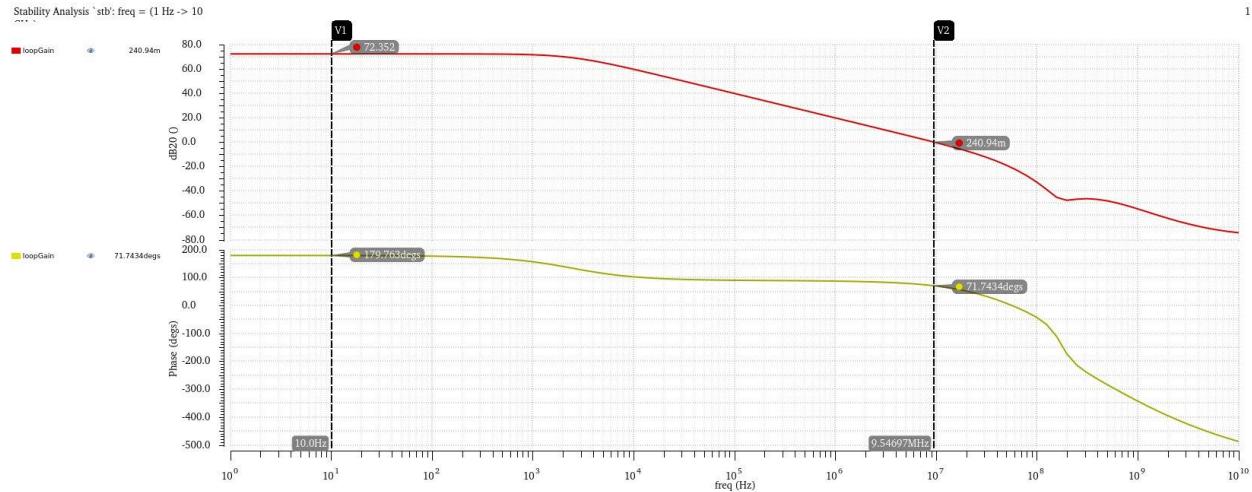
- Plot loop gain in dB and phase vs frequency for the two simulations
- Loop gain of differential path



- Result from simulation

ITI2024Su:Lab11_tb:1	ACL	1.999
ITI2024Su:Lab11_tb:1	ACL_dB	6.016
ITI2024Su:Lab11_tb:1	LG	1.897k
ITI2024Su:Lab11_tb:1	LG_dB	65.56
ITI2024Su:Lab11_tb:1	BW_LG	3.909k
ITI2024Su:Lab11_tb:1	UGF_LG	7.582M
ITI2024Su:Lab11_tb:1	GBW_LG	7.416M
ITI2024Su:Lab11_tb:1	PM.	89.05

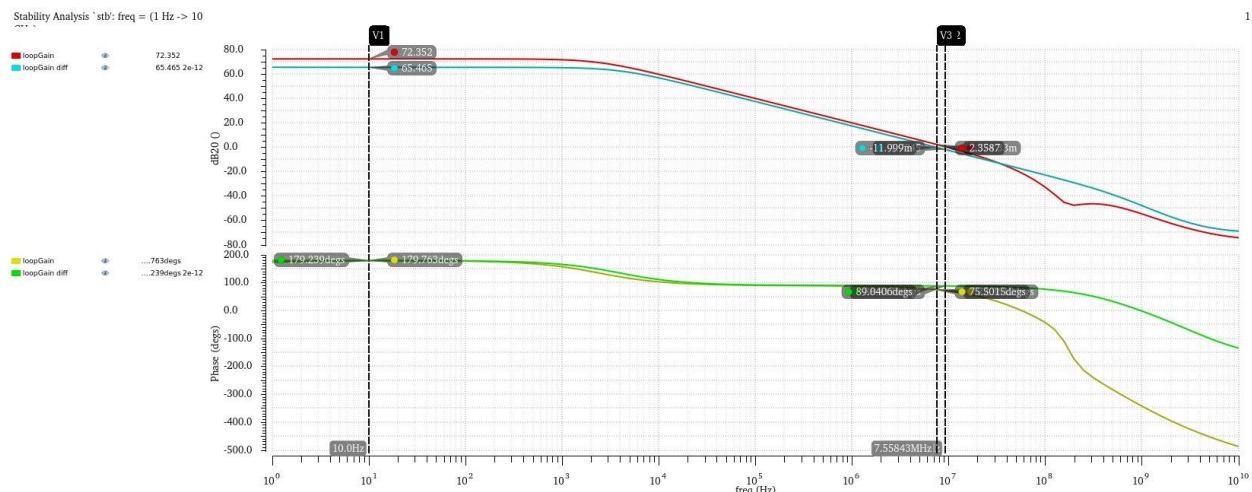
- Loop gain of Common Mode path



- Result from simulation

ITI2024Su:Lab11_tb:1	ACL	909.9f
ITI2024Su:Lab11_tb:1	ACL_dB	-240.8
ITI2024Su:Lab11_tb:1	LG	4.146k
ITI2024Su:Lab11_tb:1	LG_dB	72.35
ITI2024Su:Lab11_tb:1	BW_LG	2.42k
ITI2024Su:Lab11_tb:1	UGF_LG	9.806M
ITI2024Su:Lab11_tb:1	GBW_LG	10.03M
ITI2024Su:Lab11_tb:1	PM.	71.33

- Plot loop gain in dB and phase vs frequency for the two simulations overlaid.



## 2. Compare GBW and PM of diff and CM loops

	Differential	Common Mode
GBW	7.4MHz	10.3MHz
PM	89.05	71.33

- The GBW of CM is higher than diff and as the CM has another pole in the output of the error amplifier is less than the pole of folded node and this make the PM of the CM Loop is less than PM of diff Loop

## 3. Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation

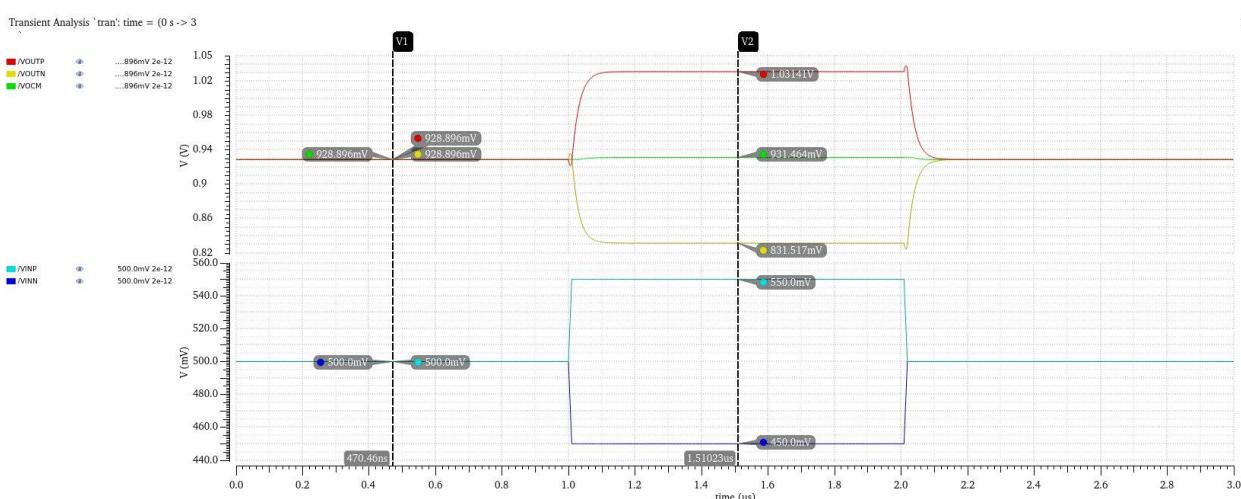
	STB analysis	Open LOOP
DC LG	65.56dB	74.18dB
BW	3.9kHz	10.33kHz
GBW	7.4MHz	52.85MHz

- As open loop is an LG with  $\beta = 1$  and as in closed loop  $\beta \approx \frac{1}{3}$  that mean decrease about 9.5dB than the open loop simulation and the result make sense in the bandwidth as the load cap increase from .5pF to 1.17pF the bandwidth divide by 2.4 as the output resistance remain constant so the GBW of STB analysis is less than open loop analysis by factor 7.2

## PART 6: Closed Loop Simulation (Transient Analy)

### 1. Differential and CMFB loops stability (STB analysis):

1. Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure



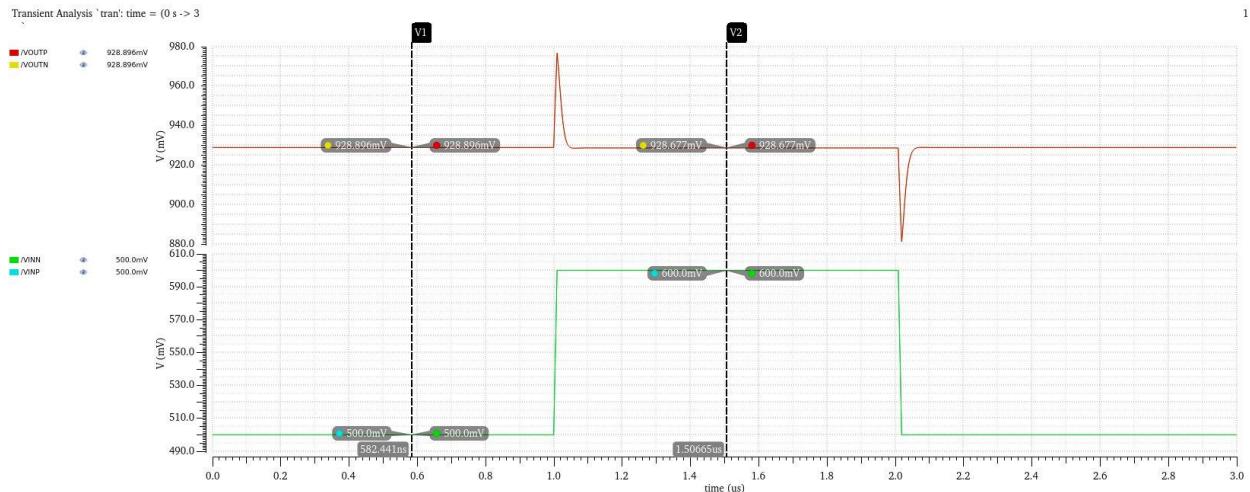
2. There is a little spark due to the change at the voltage on the capacitance as there are small rise and fall time but there are no ringing and peaking the response of the output show that diff and CM has a stable response as there are no ringing or oscillation behavior
3. The Settling time from simulation

ITI2024Su:Lab11\_tb:1 | ST | 96.44 n

- To increase the settling time, we can decrease the PM of diff loop as the second order system faster than first order we can decrease PM by increase the capacitance or resistance of folded node by using higher  $\frac{g_m}{I_D}$  or longer L for M3 (NMOS CG) and another solution is has a bigger UGF in closed loop by increasing  $\frac{g_m}{I_D}$  of input pair or increasing the current consumption in input pair and we can use the two of them together

## 2. Differential and CMFB loops stability (transient analysis): CM input pulse

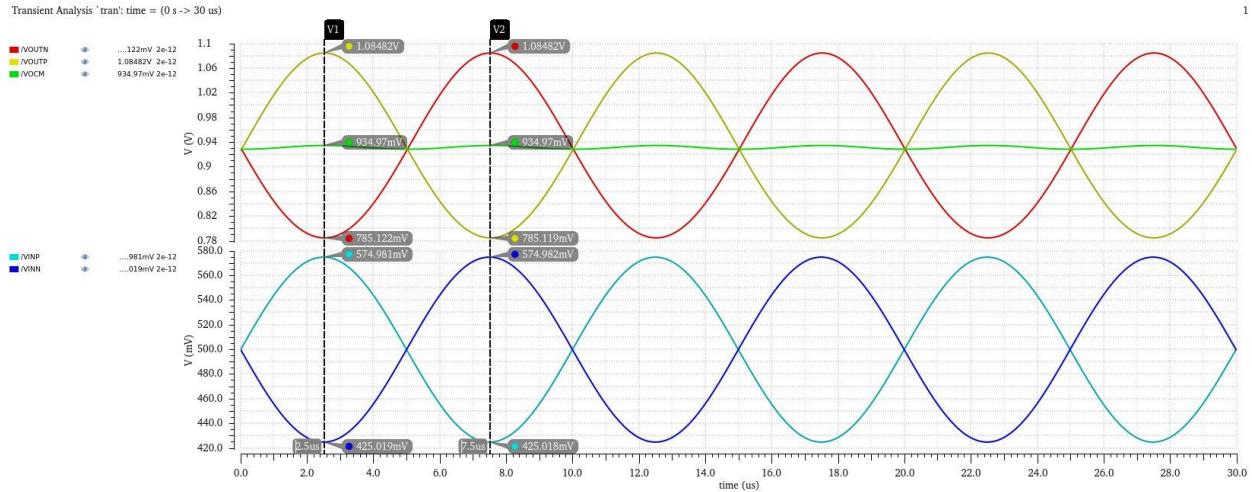
1. Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



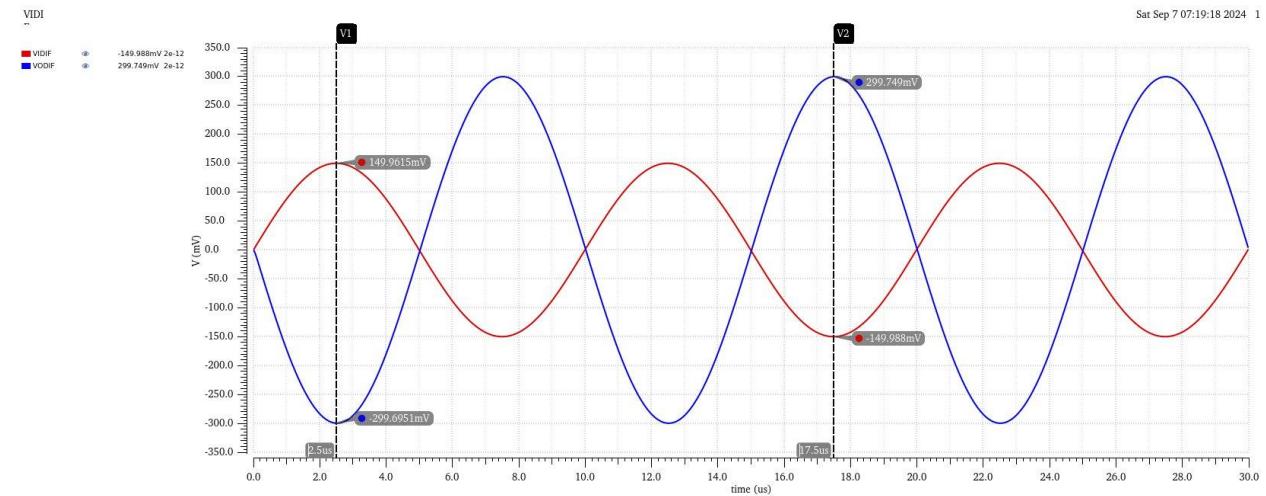
- There is no ringing in the response, so the CM and diff loop are stable with adequate PM this spark due to fast change of voltage on the feedback capacitance

### 3. Output swing:

- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure



- Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



- Calculate the diff input and output peak-to-peak swings and the closed loop gain.

ITI2024Su:Lab11_tb:1	Vin_Dif	300m
ITI2024Su:Lab11_tb:1	Vout_Dif	599.6m
ITI2024Su:Lab11_tb:1	ACL.	1.999