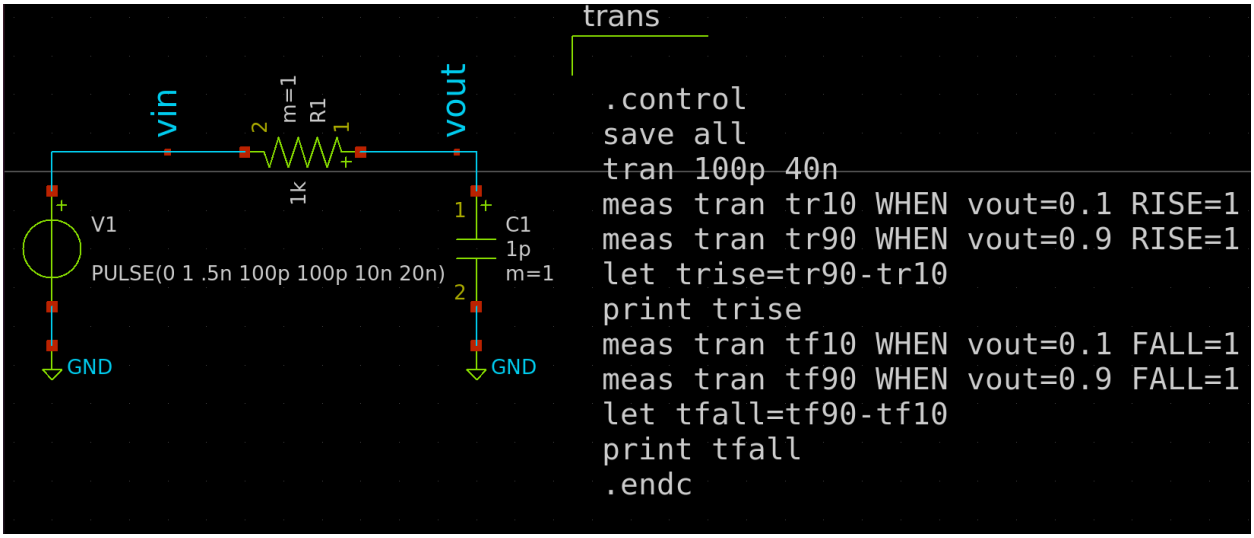
ITI CMOS Analog IC Design 2024
Lab 01
LPF Simulation and MOSFET Characteristics

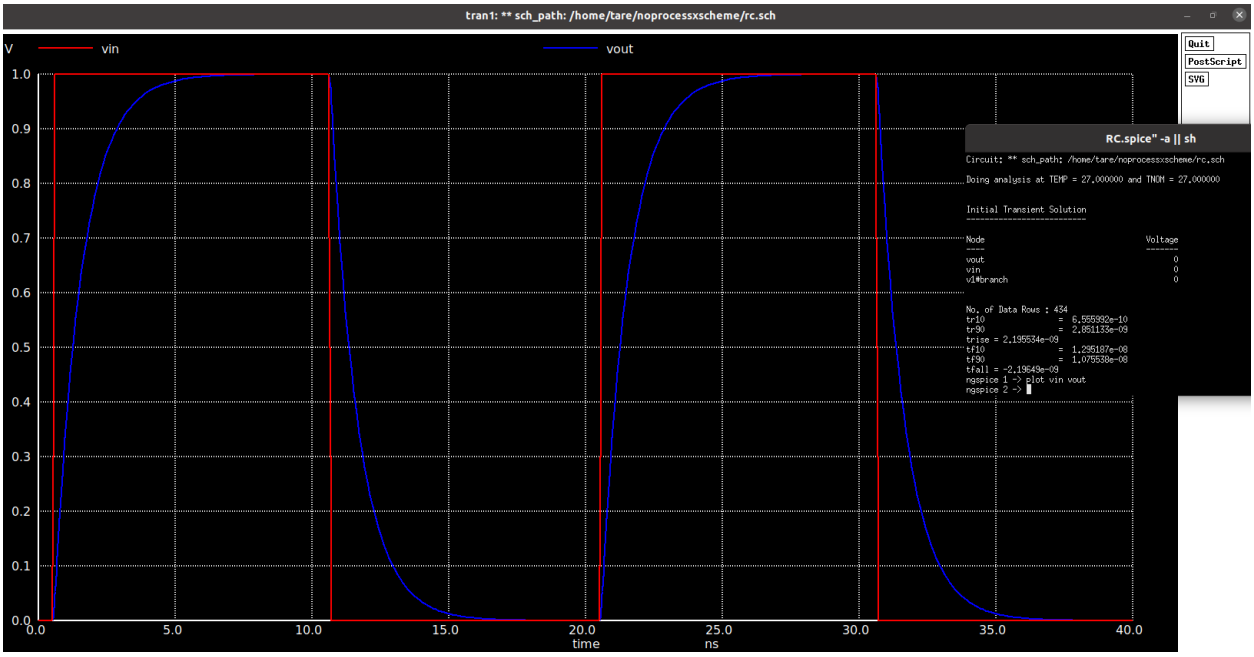
Part 1: Low Pass Filter Simulation (LPF)

1. Transient Analysis

1. The design of a first order low pass filter that has $R = 1k\Omega$ and 1ns time constant.



2. Applying a square wave input with $Thigh = Pulse\ Width = 10ns$, $Tclk = Period = 20ns$, and $Trise = Tfall = 100ps$.
3. Transient analysis results for two periods.

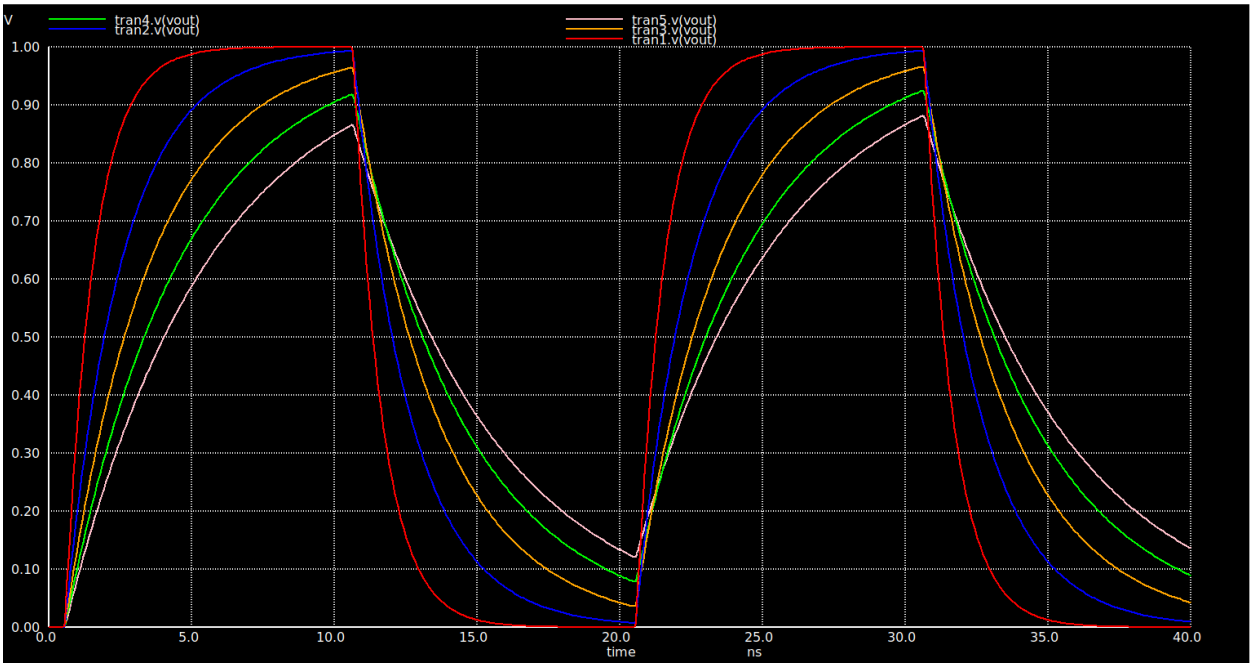


- As we see the capacitor take a time to recharge and the voltage follow the equation $Vout=Vin*(1-e^{-t/\tau})$ and time to discharge and follow the equation $Vout=Vin*e^{-t/\tau}$. ($\tau=R*C$) in this circuit τ= 1KΩ * 1pF =1ns

4. Rise and fall time (10% to 90%). From the last image we notice that Trise=2.196ns and Tfall= 2.196ns
5. Comparison between simulation and analytical results.
   Analytical results: $T_{fall} = T_{rise} = 2.2*RC = 2.2 * 1k * 1p = 2.2$ ns

	Rise time	Fall time
Analytical	2.2 ns	2.2 ns
Simulation	2.196 ns	2.196 ns

6. Parametric sweep for $R = 1{:}\ 1{:}\ 5k\Omega$.



Trise @R=1K=2.196ns

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vout                                         0
vin                                          0
v1#branch                                    0


No. of Data Rows : 434
tr10                =  6.555992e-10
tr90                =  2.851133e-09
trise = 2.195534e-09
```

Trise @R=2K =4.393ns

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vout                                         0
vin                                          0
v1#branch                                    0


No. of Data Rows : 434
tr10                =  7.605891e-10
tr90                =  5.154053e-09
trise = 4.393464e-09
```

Trise @R=3K=6.591ns

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vout                                         0
vin                                          0
v1#branch                                    0


No. of Data Rows : 433
tr10                =  8.658120e-10
tr90                =  7.456885e-09
trise = 6.591073e-09
```

Trise @R=4K =8.789ns

```
Initial Transient Solution
--------------------------

Node                                    Voltage
----                                    -------
vout                                          0
vin                                           0
v1#branch                                     0


No. of Data Rows : 433
tr10                =  9.712214e-10
tr90                =  9.759747e-09
trise = 8.788526e-09
```

Trise @R=5K

```
Initial Transient Solution
--------------------------

Node                                    Voltage
----                                    -------
vout                                          0
vin                                           0
v1#branch                                     0


No. of Data Rows : 432
tr10                =  1.076581e-09

Error: measure  tr90  when(WHEN) : out of interval
 meas tran tr90 when vout=0.9 rise=1 failed!
```

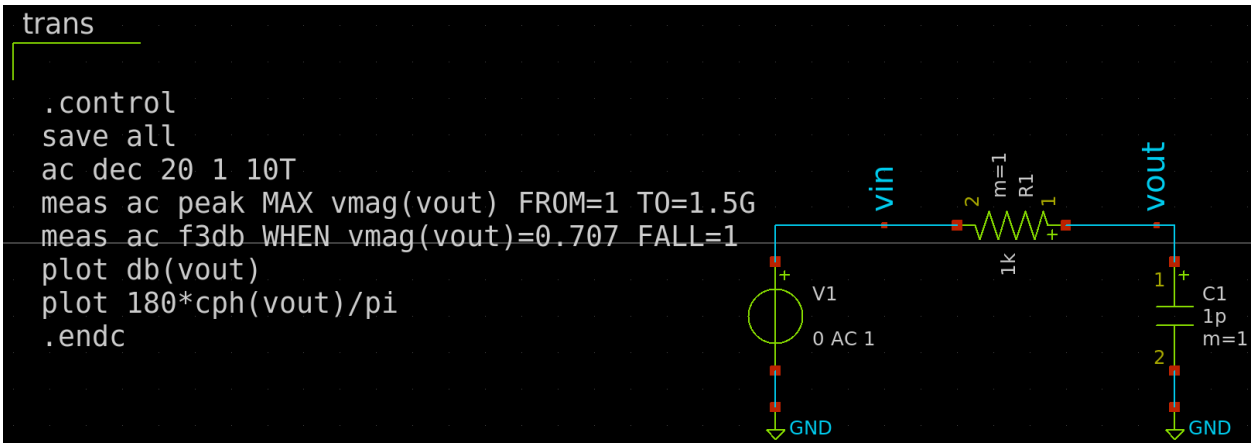
- We see that the rise time increase with increasing of RL and after the rise time exceed the pulse width of input there are no fall time and rise time
- At R=5KΩ Vout doesn't reach 90% of Vin Value
- Analytical the fall time and constant time in RL=5KΩ equal 2.2*RC = 2.2 * 5KΩ * 1pF= **11 ns** and this exceed the pulse width (10 ns)
- As the time constant increase, the voltage can't reach its final value.
- Time constant increasing with increasing of RL but the voltage can't reach 90% of its value as RL exceed 4KΩ so there are no fall time and rise time after RL=4KΩ

2. AC Analysis

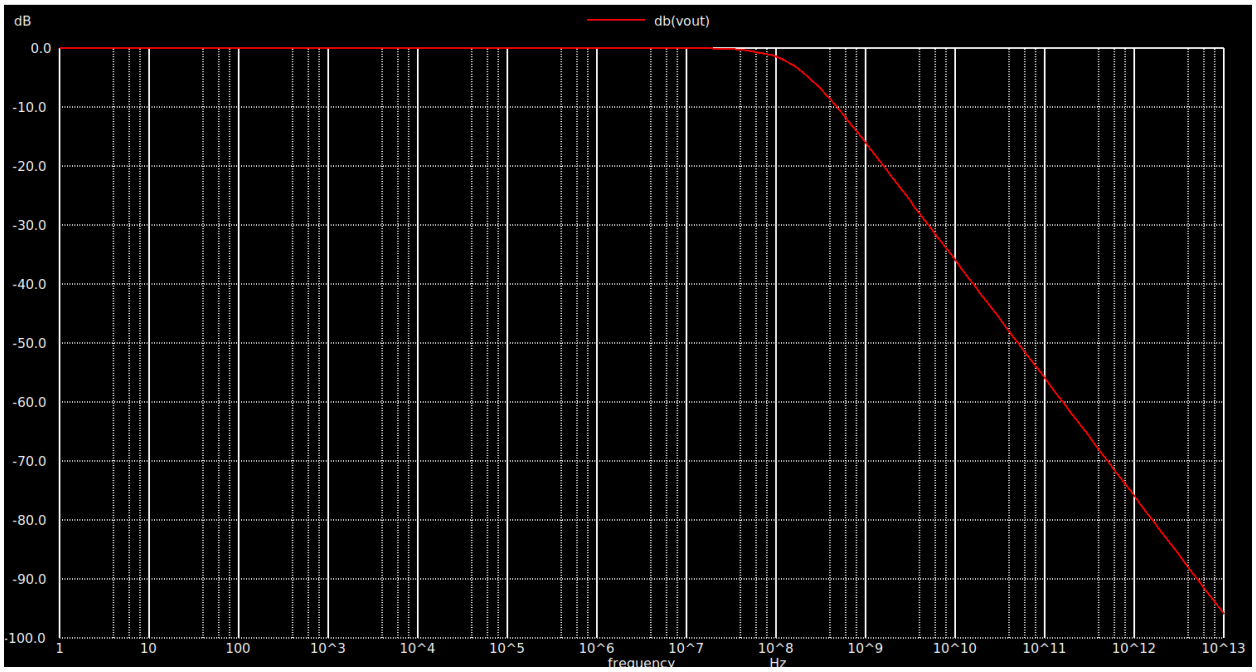
To perform AC analysis, we use Vsource With ac magnitude equal 1V amplitude so that the output voltage be the transfer function.

1. Bode Plot (magnitude and phase)

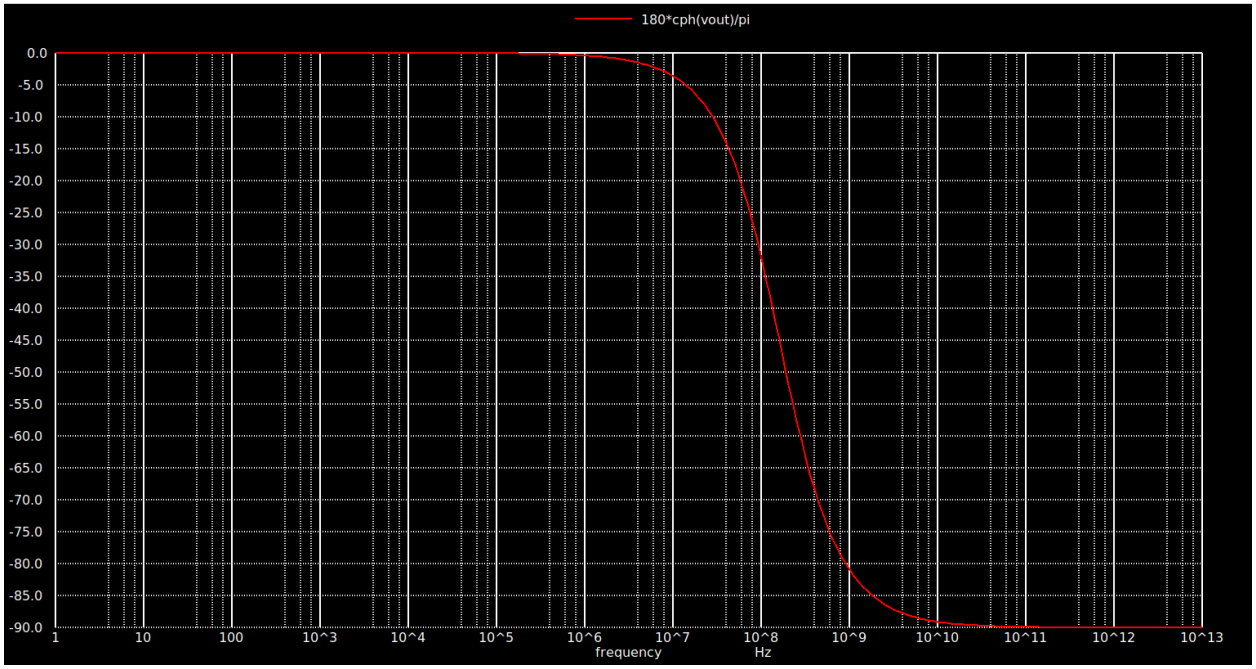
   1.1.Schematic



1.2.Magnitude



1.3.Phase



- The circuit cut the high frequency and pass low frequency, and the phase of the voltage transport from 0 to -90 degree in the cut-off frequency the phase =-45

2. DC gain and 3dB bandwidth.

```
Circuit: ** sch_path: /home/tare/noprocessxscheme/rc.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 261
peak                =  1.000000e+00 at=  1.584893e+00
f3db                =  1.592255e+08
```

3. Compare simulation with analytical results.

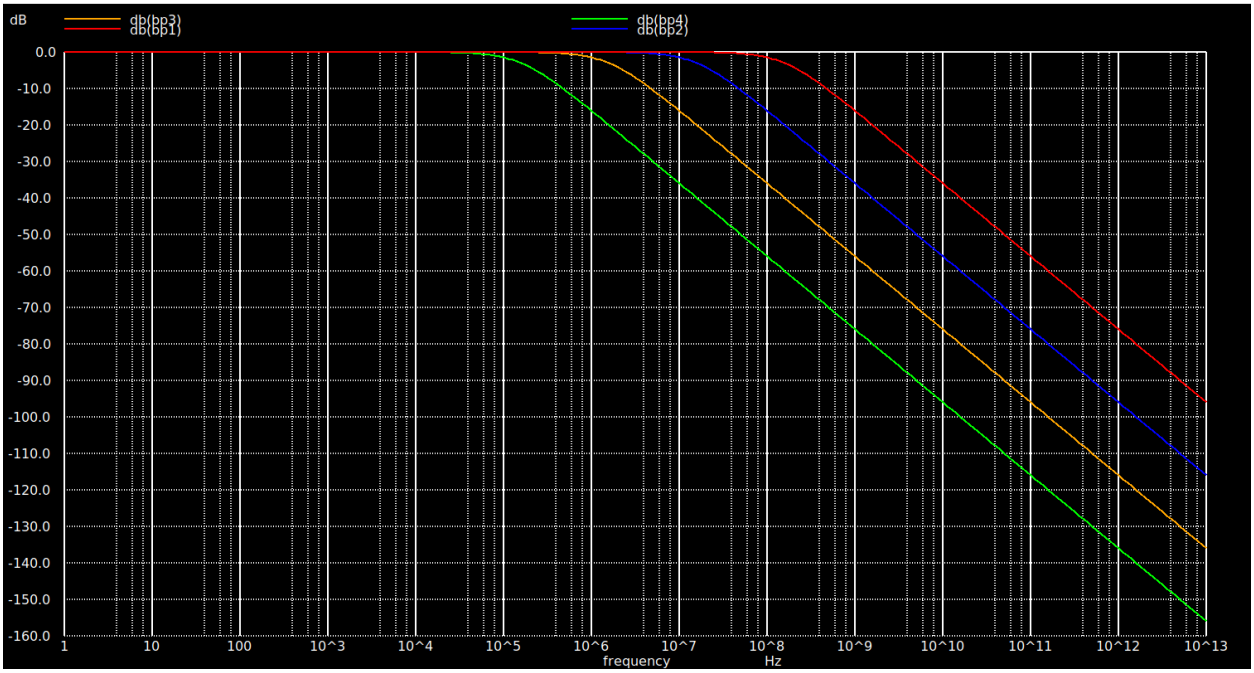
$Fc = 1/(2\pi RC) = \frac{1}{2\pi*1000*1*10^{-12}} = 159.155$ MHz

$DC\_Gain = \frac{1}{\sqrt{1+(RC*12\pi f)^2}}$ @ f = 0 Hz, DC_Gain = 1

	DC Gain	3dB_BW
Analytical	1	159.155 MHz
Simulation	1	159.226 MHz

4. Parametric sweep for R = 1,10,100,1000$k\Omega$.

- The gain remains constant and the bandwidth decreasing with increasing of RL, BW α 1/RL



```
No. of Data Rows : 261
peak                =  1.000000e+00 at=  1.584893e+00
f3db                =  1.592255e+08
Reset re-loads circuit ** sch_path: /home/tare/noprocessxscheme/rc.sch

Circuit: ** sch_path: /home/tare/noprocessxscheme/rc.sch

binary raw file "RC.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

@R=1K
Dc gain =1
BW=159.226 MHz

```
No. of Data Rows : 261
peak                =  1.000000e+00 at=  1.000000e+00
f3db                =  1.592255e+07
Reset re-loads circuit ** sch_path: /home/tare/noprocessxscheme/rc.sch

Circuit: ** sch_path: /home/tare/noprocessxscheme/rc.sch

binary raw file "RC.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

@R=10K
Dc gain =1
BW=15.923 MHz

```
No. of Data Rows : 261
peak                =  1.000000e+00 at=  1.000000e+00
f3db                =  1.592255e+06
Reset re-loads circuit ** sch_path: /home/tare/noprocessxscheme/rc.sch

Circuit: ** sch_path: /home/tare/noprocessxscheme/rc.sch

binary raw file "RC.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

@R=100K
Dc gain =1
BW=1.59226 MHz

```
No. of Data Rows : 261
peak                =  1.000000e+00 at=  1.000000e+00
f3db                =  1.592255e+05
Reset re-loads circuit ** sch_path: /home/tare/noprocessxscheme/rc.sch
```

@R=1M
Dc gain =1
BW=159.226 KHz

- We see that the cut off frequency decrease as RL increase.

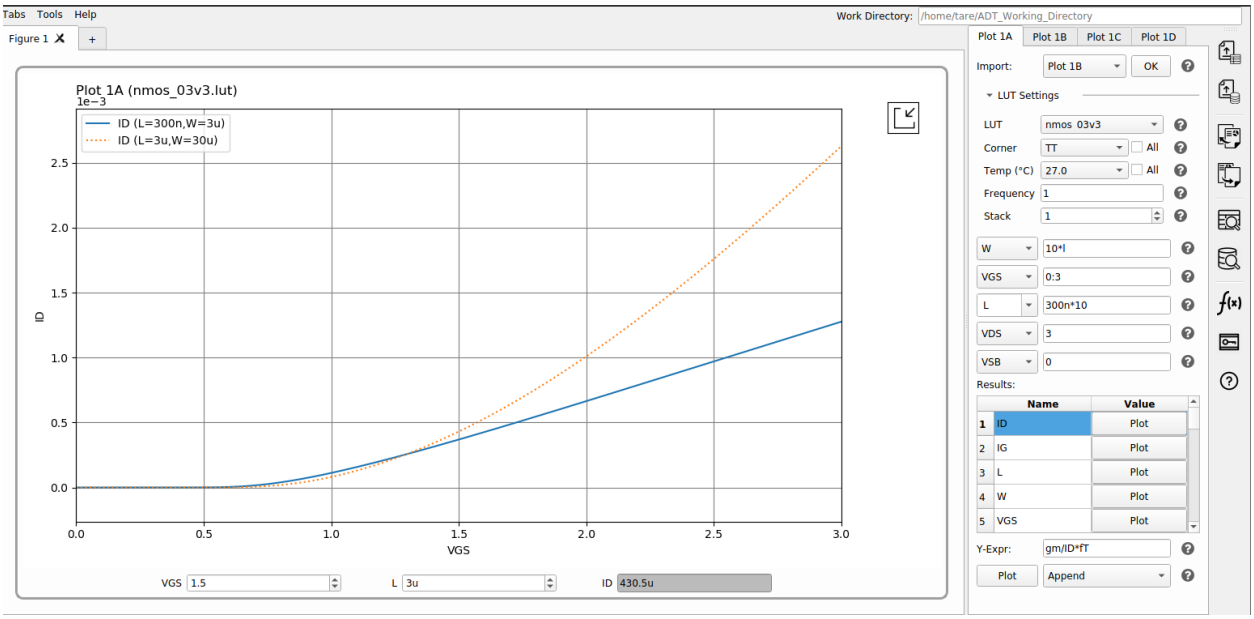
Part 2: MOSFET Characteristics

1. ID vs VGS

1. $I_D - VGS$ characteristics for NMOS and PMOS devices. Set $VDS = VDD$, and $VGS =$ 0: VDD. Use $VDD = 3V$ Plot the results overlaid for the following:

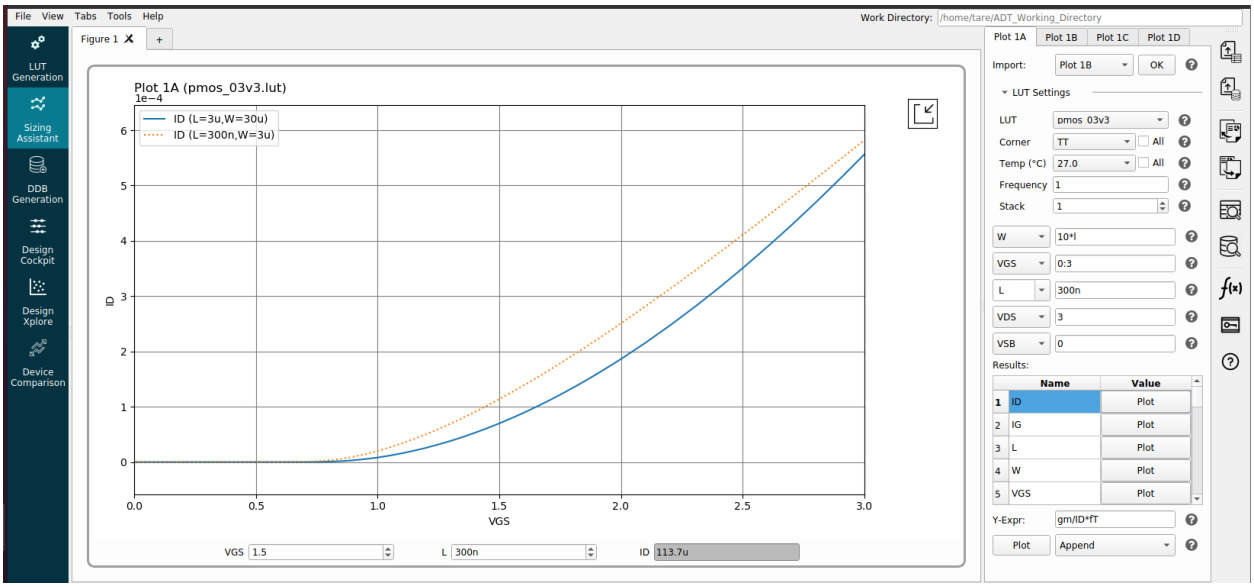
• Short channel device: $W = 3\mu m$ and $L = 300nm$

• Long channel device: $W = 30\mu m$ and $L = 3\mu m$.



2. We notice that long channel NMOS has higher current than short channel NMOS. Because of short channel NMOS affected by velocity saturation and mobility degradation

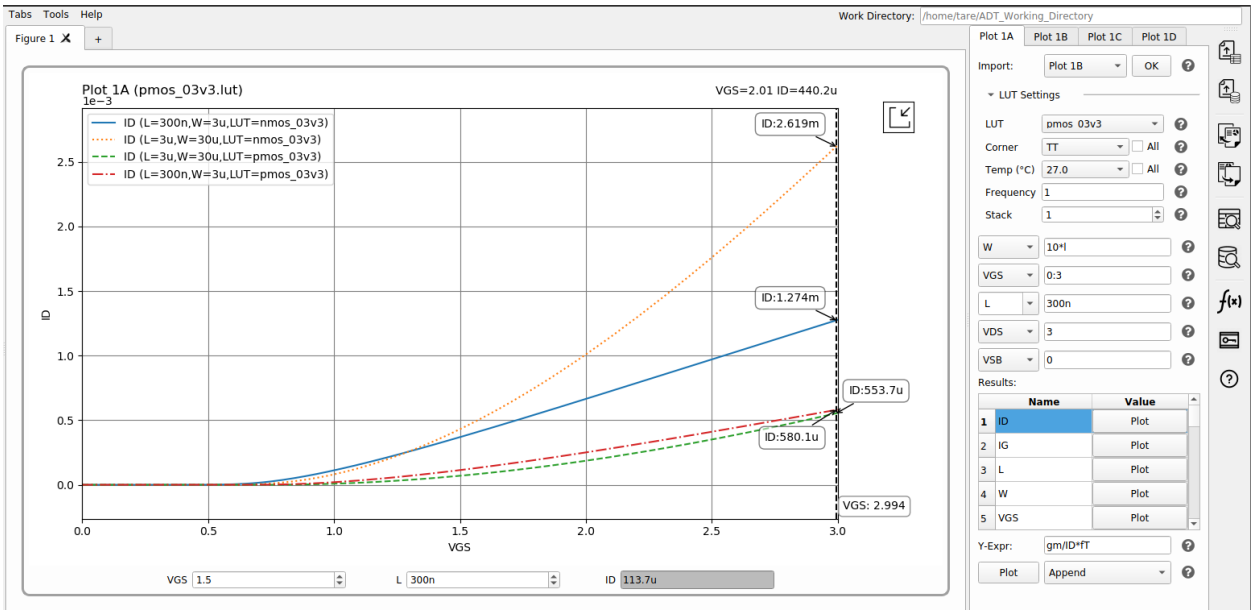
- Approximately, Long Channel has a quadratic relation however short channel has linear.
- Velocity saturation and mobility degradation have great effect on short channel NMOS



- In PMOS the drain current in long channel and short channel approximately the same.
- PMOS has less effected by velocity saturation and mobility degradation.

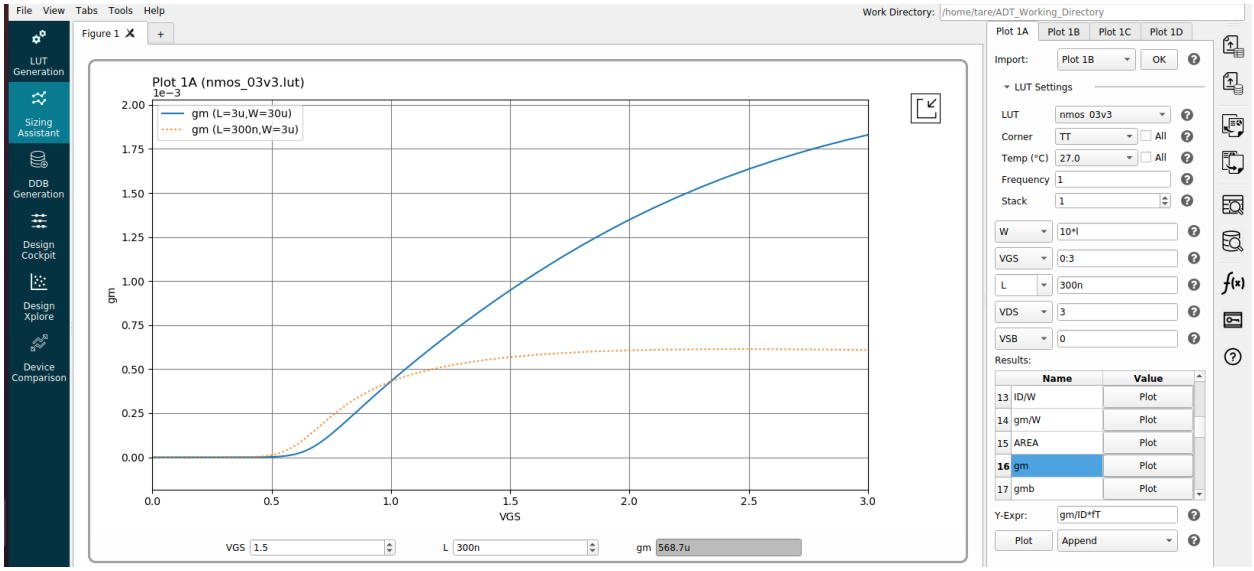
3. NMOS has higher current than PMOS and Short channel NMOS has higher current than short and long channel PMOS because NMOS has higher mobility than PMOS

- The ratio between NMOS and PMOS current at VGS=VDD for short channel is: NMOS current =1.274 mA, PMOS current=.58 mA so the ratio is equal to 2.2
  For Long channel is: NMOS current =2.62 mA, PMOS current =.553 mA so the ratio is equal to 4.74



- Long channel has higher ratio because short channel NMOS has velocity saturation and mobility degradation

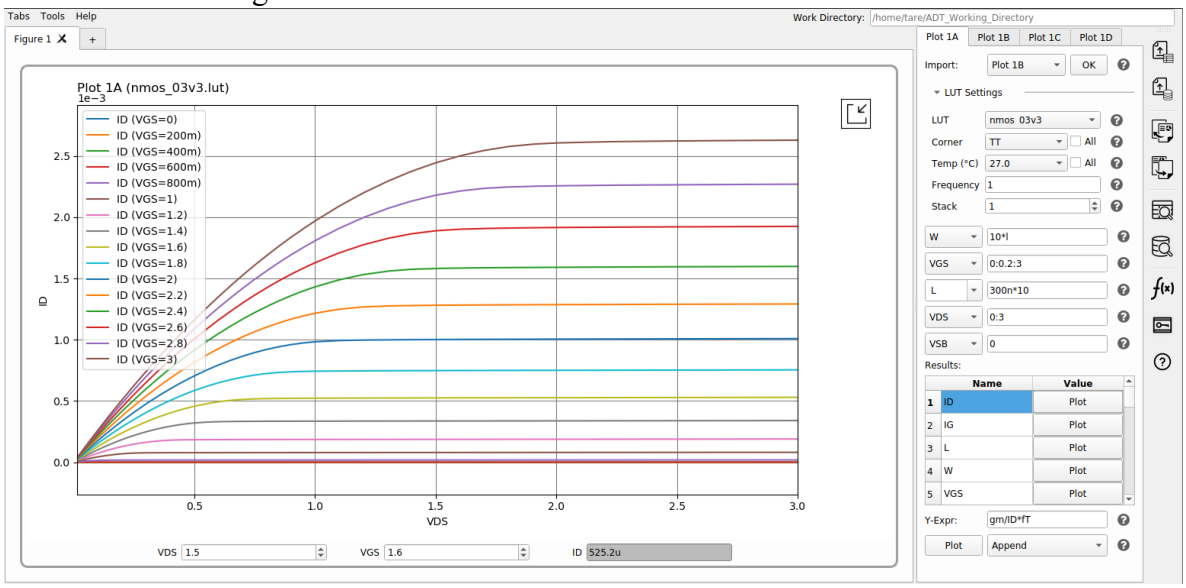
2. gm vs VGS



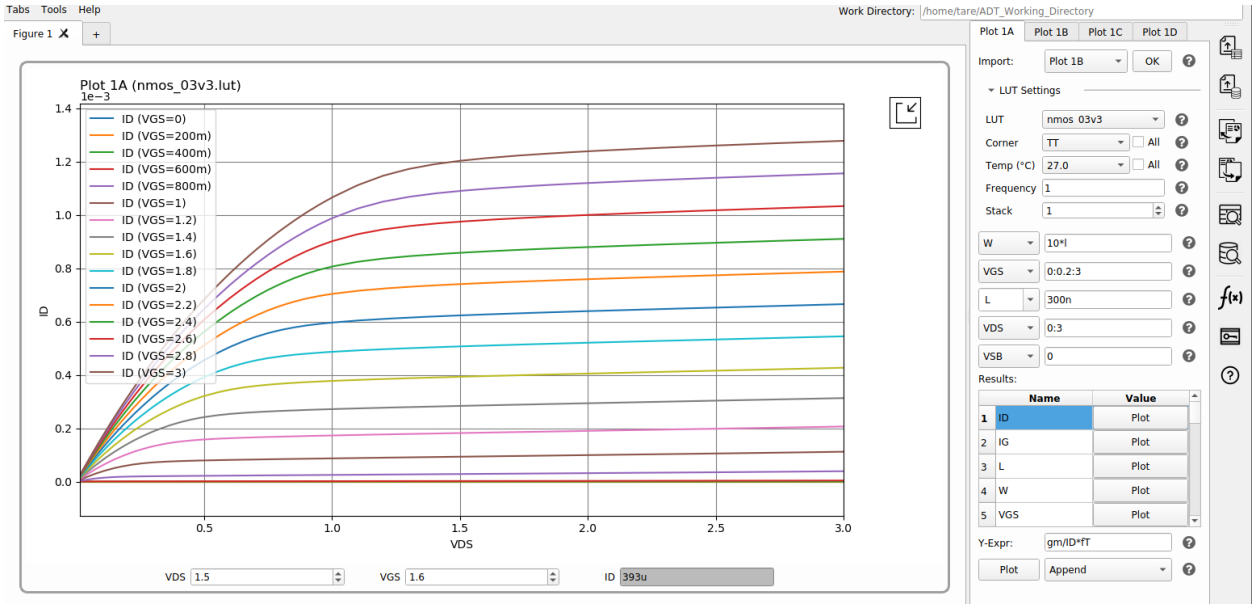
- Long Channel has higher gm than short channel.
- Approximately, gm is linear in long channel. Because gm is the derivative of the current and long channel current has quadratic characteristic.
- Short channel in the beginning is linear, approximately. Then start saturating. As gm is the derivative of the current and short channel current in the beginning is quadratic and then become linear because of velocity saturation and mobility degradation.

3. ID vs VDS

3.1. NMOS Long Channel



3.2. NMOS Short channel



- We see that long channel NMOS has higher current than short channel NMOS, because short channel effected by velocity saturation and mobility degradation.
- In saturation, short channel NMOS has higher slope than long channel NMOS, because $r_o \propto L$ so long channel NMOS has higher r_o and r_o is the reciprocal of the slope so long channel has lower slope than short channel
- Approximately, long channel has quadratic step between one curve to the curve that is above the first, however short channel has linear step