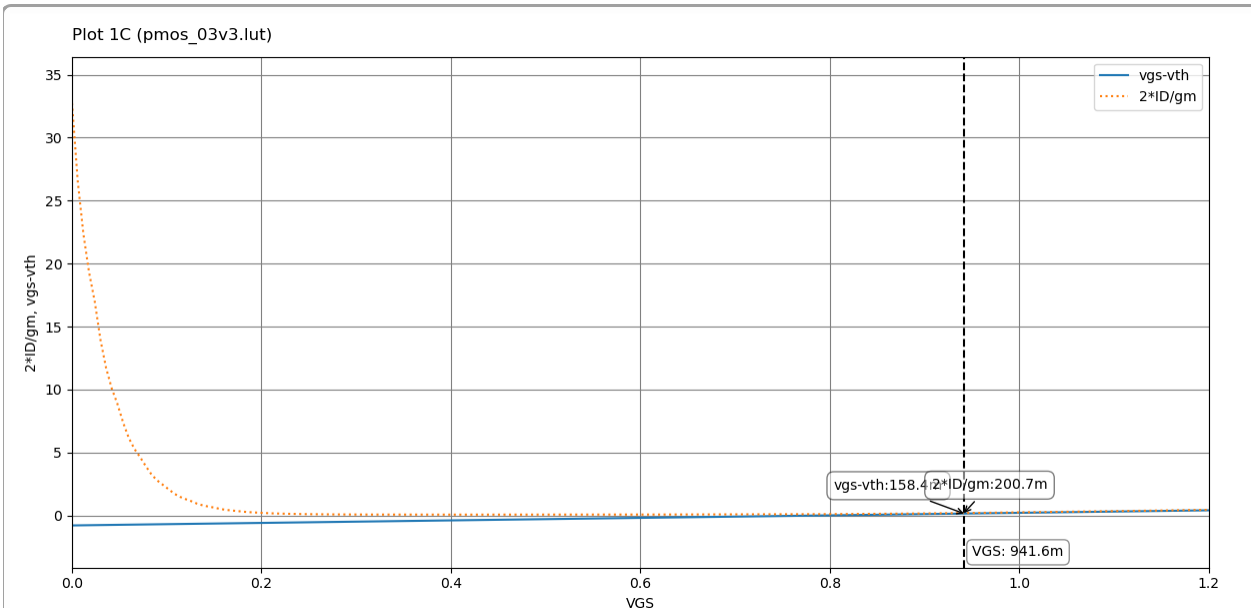
ITI CMOS Analog IC Design 2024
Lab 04
Common Drain Frequency Response

Part 1: Sizing Chart Using ADT SA

- We want to design a CD amplifier with the parameters below

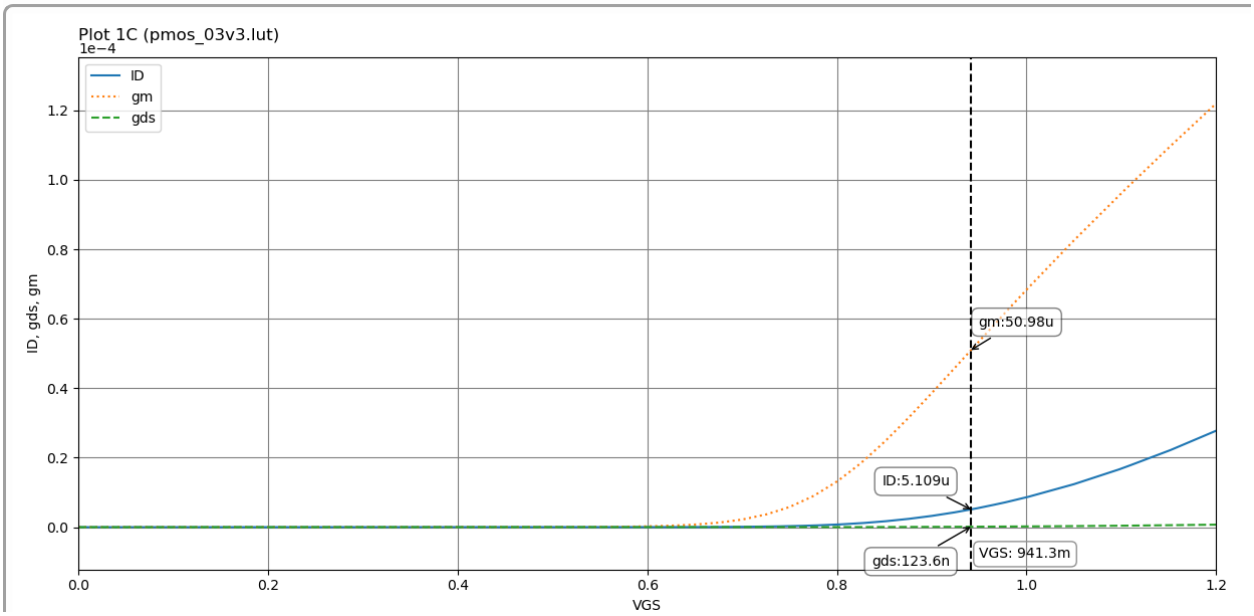
spec	Value
Input Transistor	**PMOS**
L	**1 µm**
V*	**200 mV**
Supply	**1.8 V**
Current consumption	**10µA**

- The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from ADT.
- Using ADT Sizing Assistant, plot the following design charts vs Vgs for PMOS. Set $\boldsymbol{VDS} = \boldsymbol{VDD/2}$, $\boldsymbol{L} = \boldsymbol{1\mu m}$, and $\boldsymbol{w} = \boldsymbol{10\mu m}$. Sweep Vgs from 0 to $\approx \boldsymbol{VTH} + \boldsymbol{0.4V}$,($\boldsymbol{VTH} \approx \boldsymbol{780\ mV}$) , $\boldsymbol{VTH} + \boldsymbol{0.4V} \approx \boldsymbol{1.2V}$
- Plot $V*$ and Vov overlaid vs V_{GS}



- We see that V_{GSQ}=941.6 mV and Vov =158.4 mV

- Plot ID, gm, and gds vs VGS. Find their values at V_{GSQ}



@ V_{GSQ}=941.3 mV and $W = 10\ \mu m$		
I_{DX}	gmx	gdsx
5.109 µA	50.98 µS	123.6 nS

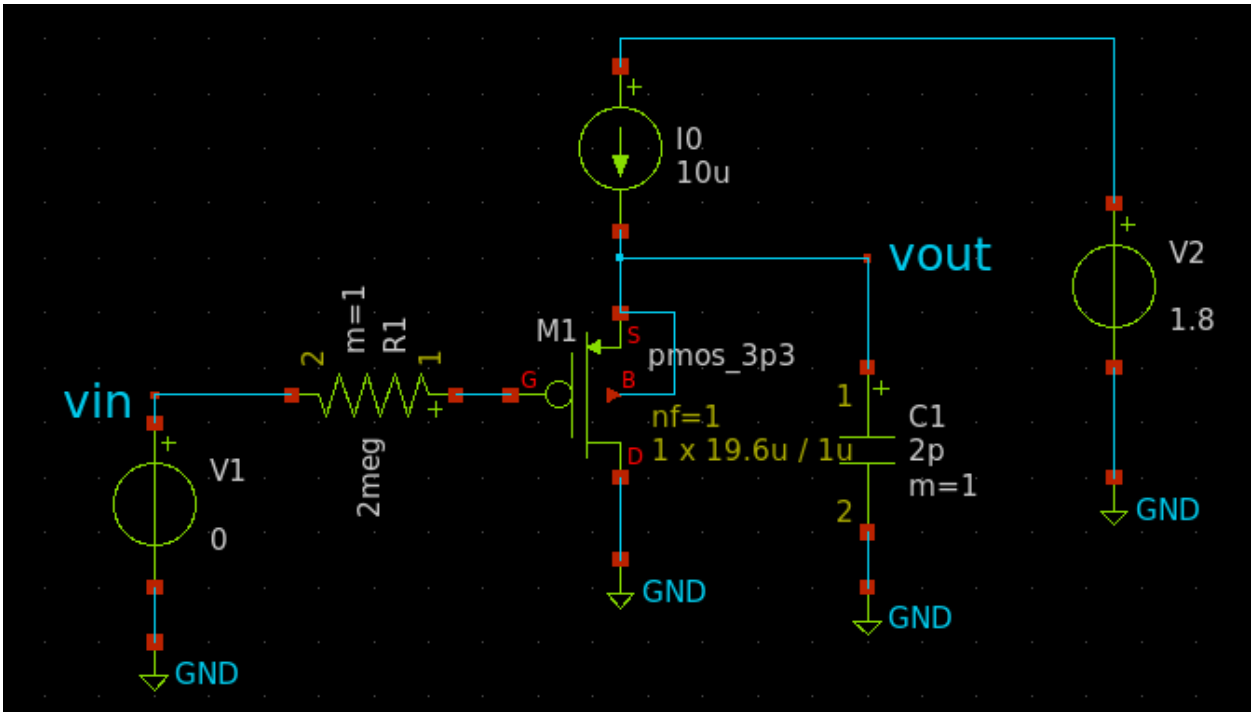
- So, to achieve I_D = 10 µA so we need W= 19.6 µm

@ V_{GSQ}=941.3 mV and $W = 19.6\ \mu m$			
I_{DQ}	gmQ	gdsQ	r_o =1/gds
10 µA	100 µS	242.256 nS	4.128 MΩ

Part 2: CD Amplifier

1. OP (Operating Point) Analysis

1. Create a new schematic for the CD amplifier



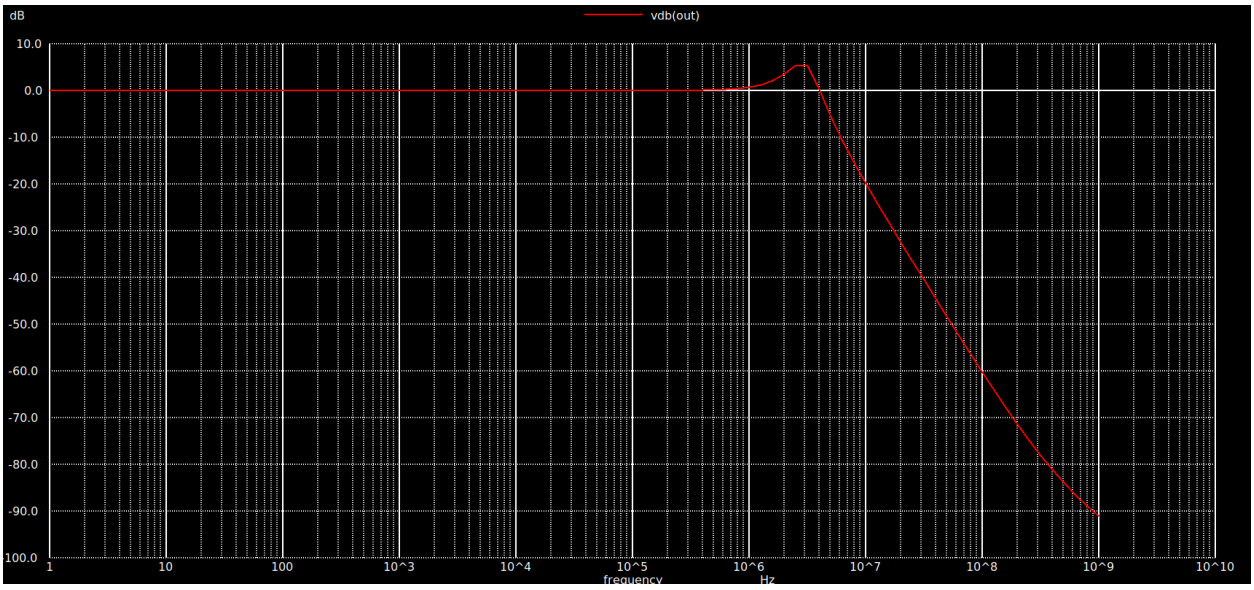
2. Simulate the OP point. Report a snapshot

device	m.xm1.m0
model	pmos_3p3.13
gm	0.000101116
gds	2.29619e-07
id	1e-05
vgs	0.941212
vth	0.783839
vds	0.941211
vdsat	0.154288
gmbs	4.77816e-05
cdb	-9.7757e-15
cgd	-1.40387e-17
cgs	-5.01454e-14
csb	-1.46395e-14

3. As Vds= .941 V and Vdsat =.154 V so Vds>1.2*Vdsat so the PMOS works in saturation

2. AC Analysis

1. Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz)




```
No. of Data Rows : 91
peak1                =  5.444827e+00 at=  2.511886e+06
```

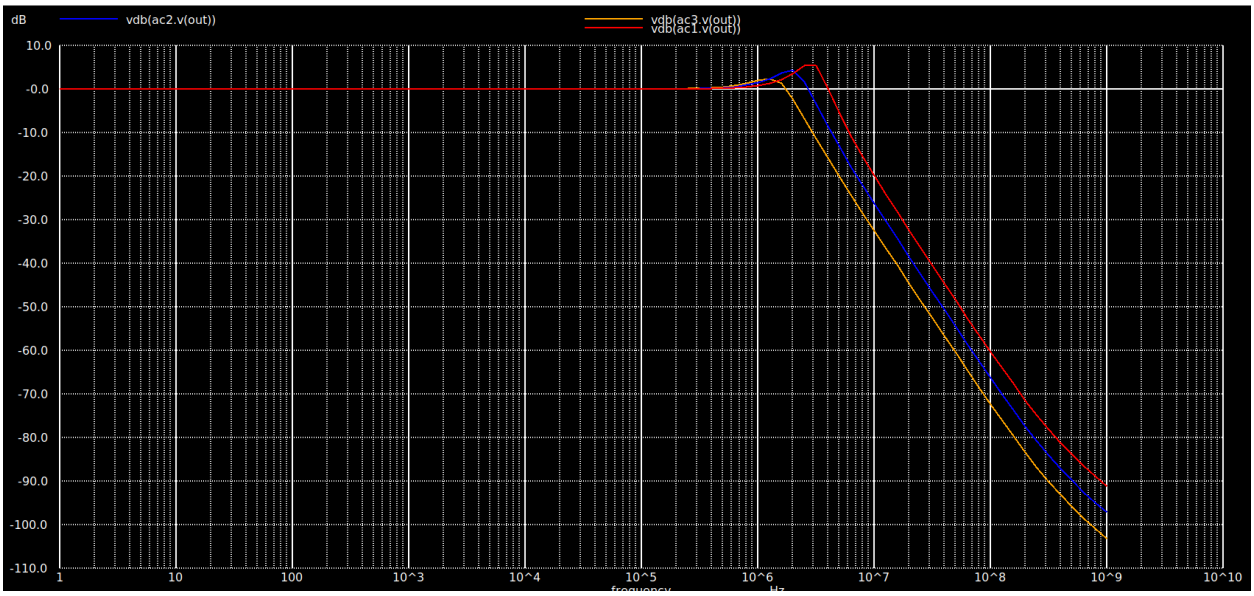
2. From the figure above we notice there are frequency domain peaking= 5.4db at frequency 2.51 MHz
3. calculate quality factor (use approximate expressions)

$$Q \approx \sqrt{\frac{gm(\,Cgs + Cgd\,)Rsig}{Cl}} = \sqrt{\frac{101*10^{-6}*(50.15+.014)*10^{-15}*2*10^{6}}{2*10^{-12}}} = 2.25$$

- as Q >.5 this system is underdamped system and as Q>.707 there are peaking in the system

4. (Optional) Perform parametric sweep: CL = 2p, 4p, 8p

- Report Bode plot magnitude overlaid on same plot.



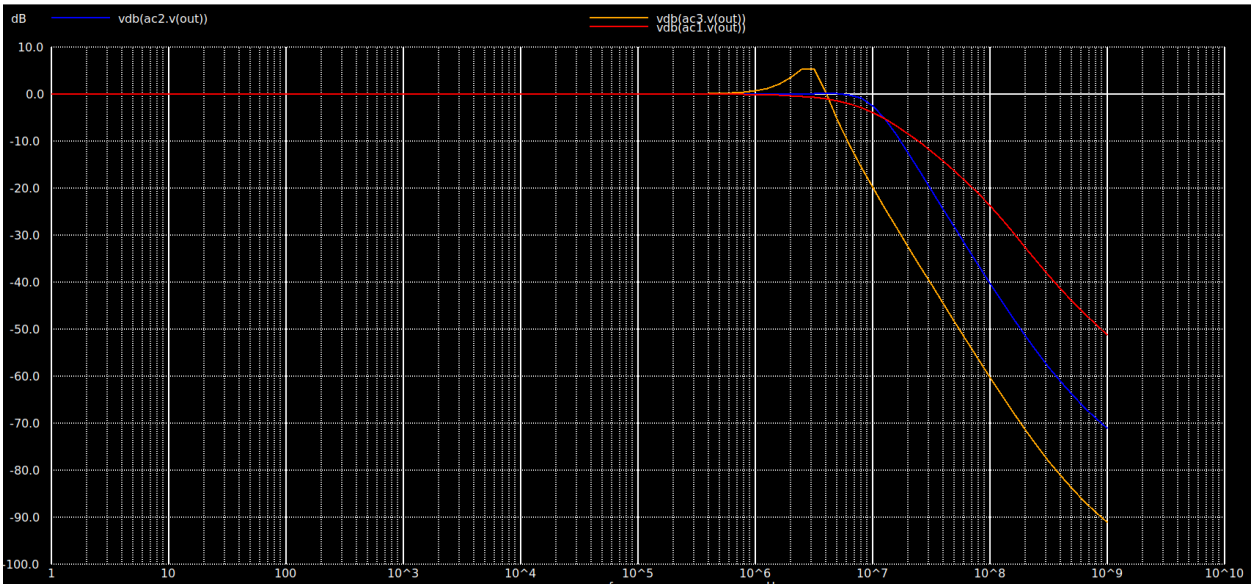
- Report the peaking vs CL.

```
binary raw file "lab4_ac.raw"
-------------------------------------------

ac1.cap = 2.000000e-12
ac1.peak1 = 5.445564e+00
ac1.f3db1 = 4.555775e+06
-------------------------------------------

ac2.cap = 4.000000e-12
ac2.peak1 = 4.375586e+00
ac2.f3db1 = 3.118289e+06
-------------------------------------------

ac3.cap = 8.000000e-12
ac3.peak1 = 2.434549e+00
ac3.f3db1 = 2.086024e+06
-------------------------------------------
```

- As we increase CL the output pole decreases and the difference between input and output pole increase, and this solve the peaking and make it less but it decreases the BW of the system
- As CL increase Q (quality factor) decrease as Q decrease the system go to overdamped system when CL exceed 41 pf as
  $Q = .5\ (criticaldamped)\ at\ CL \approx 40.5$ pf

5. (Optional) Perform parametric sweep: Rsig = 20k, 200k, 2M.

- Report Bode plot magnitude overlaid on same plot



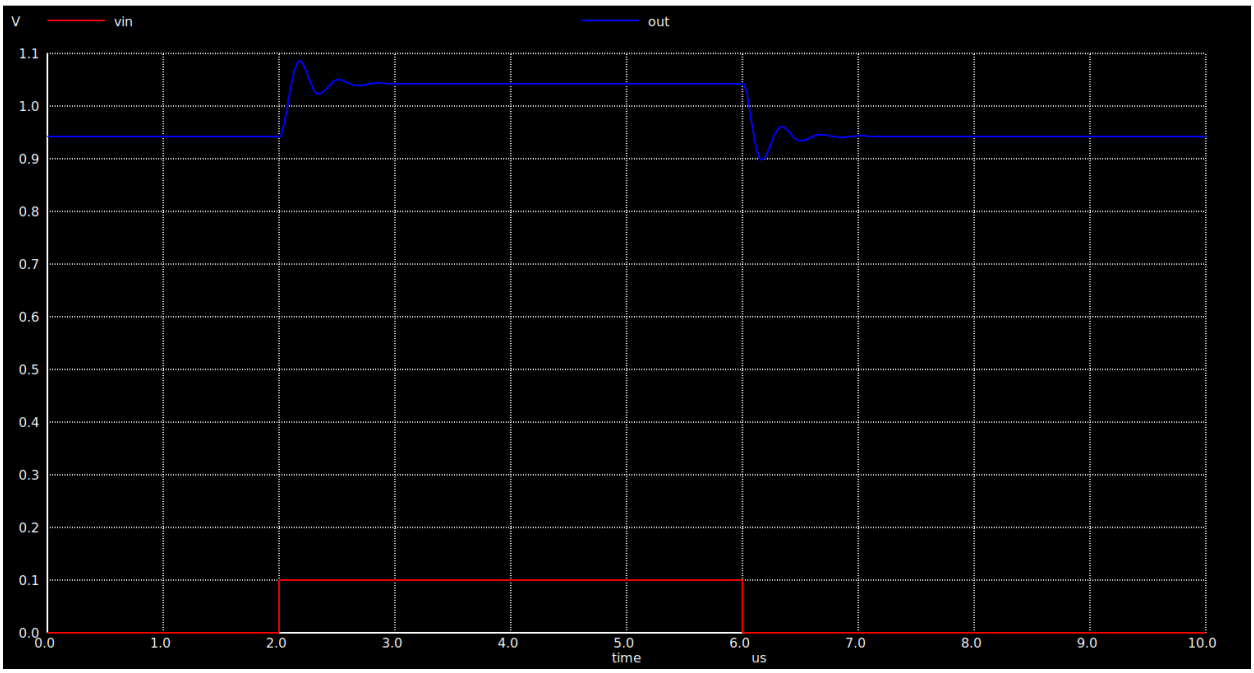
- Report the peaking vs Rsig.

```
binary raw file "lab4_ac.raw"
--------------------------------------------

ac1.res = 2.000000e+04
ac1.peak1 = -1.97226e-02
ac1.f3db1 = 8.304922e+06
--------------------------------------------

ac2.res = 2.000000e+05
ac2.peak1 = 1.407192e-01
ac2.f3db1 = 1.055359e+07
--------------------------------------------

ac3.res = 2.000000e+06
ac3.peak1 = 5.445261e+00
ac3.f3db1 = 4.555978e+06
--------------------------------------------
```

- As Rsig increase input pole decrease and as Q @ Rsig =20 kΩ ≈.225 that means the system is overdamped and as Rsig increase Q increase the system goes to underdamped and @Rsig= 200KΩ ,Q ≈.71 which achieve the maximum flat response as we see in graphs

3. Transient Analysis

1. Use a pulse source as your transient stimulus and set it as follows (delay = 2us, initial = 0V, period = 8us, pulse_value = 100mV, t_fall = 1ns, t_rise = 1ns, width = 4us). Run transient analysis for 10us to investigate the time domain ringing. Report Vin and Vout overlaid vs time.



2. Calculate the DC voltage difference (DC shift) between Vin and Vout.

```
peak1 = 1.084572e+00
vgs = 9.417292e-01
dcshift = 9.417299e-01
overshoot = 4.315403e+01
```

- DC shift =941.73 mV

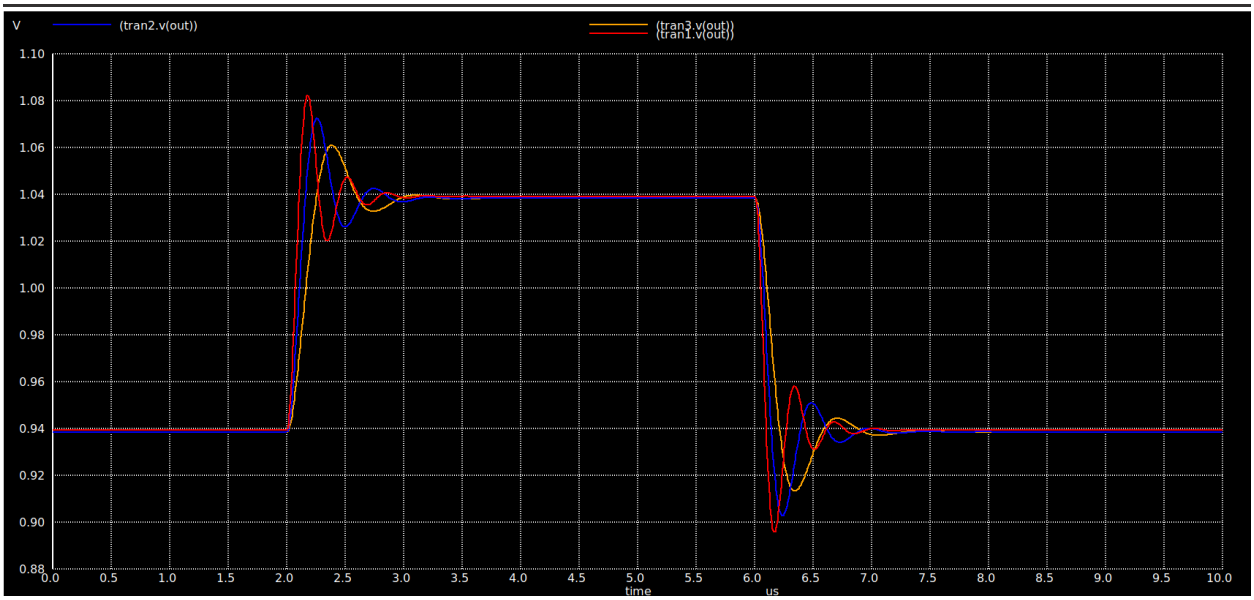
- the relation between the DC shift and VGS of the transistor is they are equal
- to shift the signal down we can use NMOS

3. there are ringing when the input signal change from one value to another

- we can notice from the figure above that the overshoot equal 43.15 and by hand analysis is equal 48.87

4. [Optional] Perform parametric sweep: CL = 2p, 4p, 8p

- Report Vout vs time overlaid on same plot.



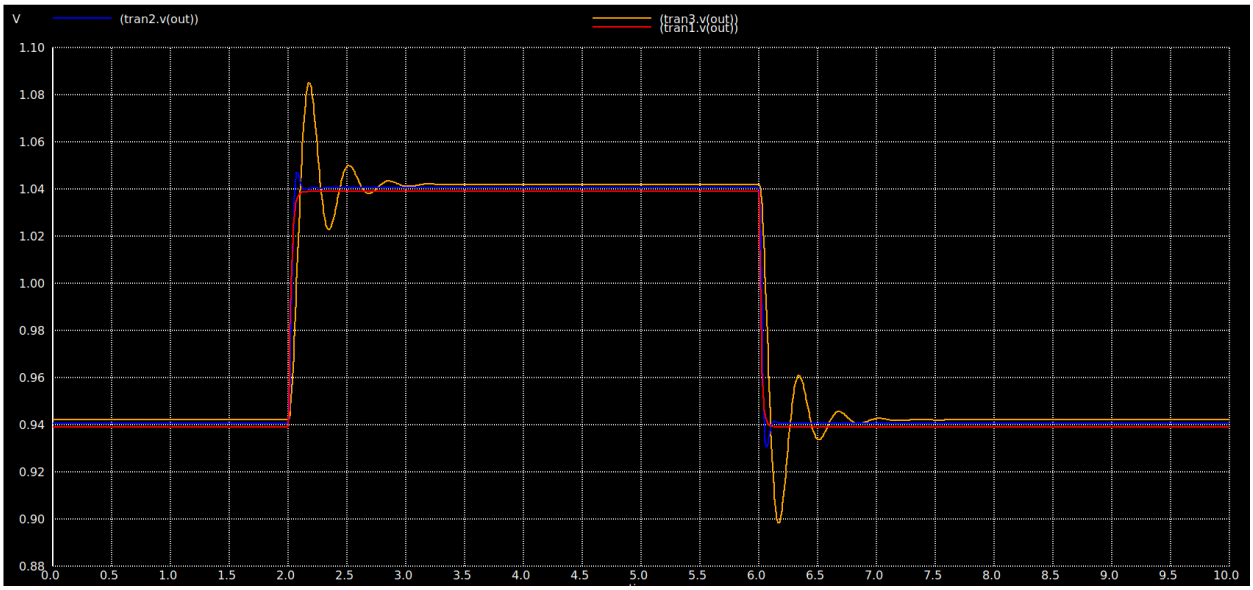
- • Report the overshoot vs CL

```
------------------------

tran1.cap = 2.000000e-12
tran1.peak1 = 1.082452e+00
tran1.dcshift = 9.396069e-01
tran1.overshoot = 4.315704e+01

------------------------

tran2.cap = 4.000000e-12
tran2.peak1 = 1.074648e+00
tran2.dcshift = 9.405993e-01
tran2.overshoot = 3.434197e+01

------------------------

tran3.cap = 8.000000e-12
tran3.peak1 = 1.063999e+00
tran3.dcshift = 9.415524e-01
tran3.overshoot = 2.271461e+01
```

- As we increase CL the peak value and overshoot decrease the dc shift remain constant

5. [Optional] Perform parametric sweep: Rsig = 20k, 200k, 2M

- Report Vout vs time overlaid on same plot.



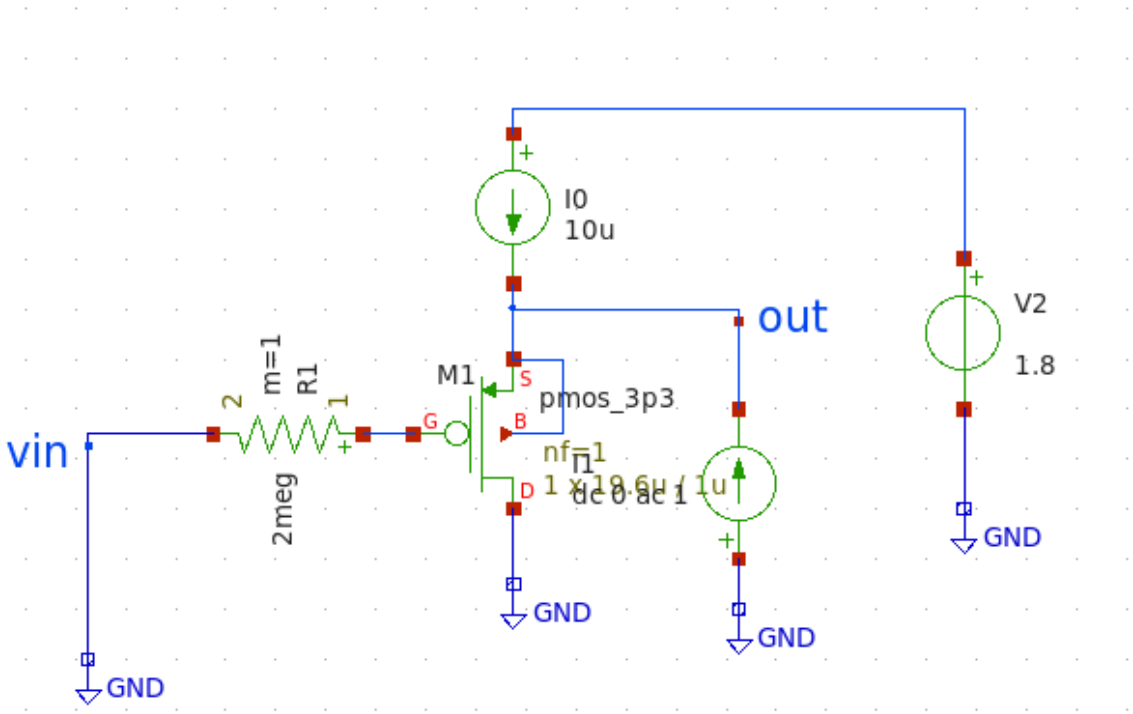
- Report the overshoot vs Rsig.

```
-------------------------

tran1.res = 2.000000e+04
tran1.peak1 = 1.041616e+00
tran1.dcshift = 9.418337e-01
tran1.overshoot = 0.000000e+00

-------------------------

tran2.res = 2.000000e+05
tran2.peak1 = 1.048555e+00
tran2.dcshift = 9.419617e-01
tran2.overshoot = 6.825860e+00

-------------------------

tran3.res = 2.000000e+06
tran3.peak1 = 1.083028e+00
tran3.dcshift = 9.401836e-01
tran3.overshoot = 4.315734e+01

-------------------------
```

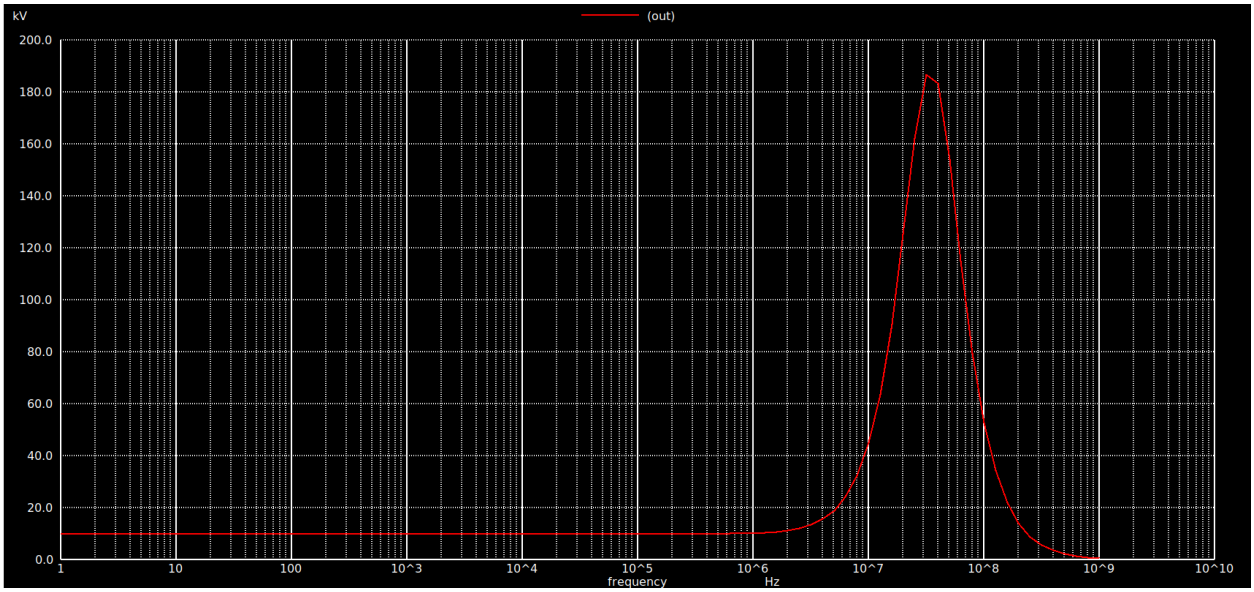
- As Rsig increase the overshoot and peak value increase

4. [Optional] *Zout* (Inductive Rise)

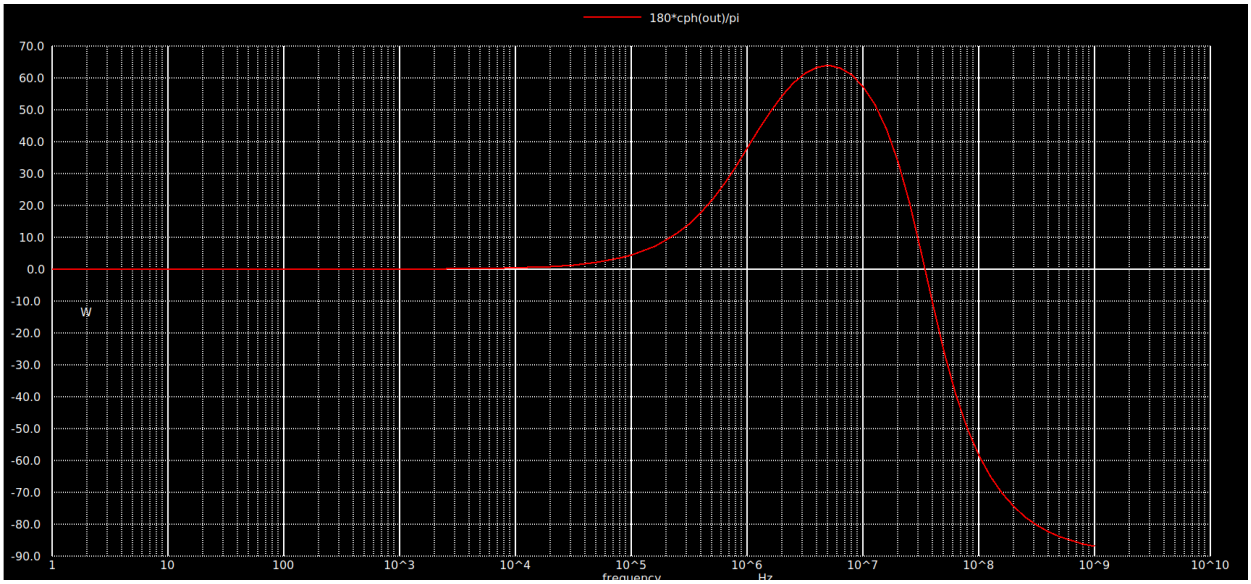
1. Schematic



2. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade).
3. Plot the output impedance vs frequency.
   3.1. Magnitude



3.2. phase



3.3. there are inductive rise in the high frequency as cgs become a short circuit in high frequency and the output impedance rise to reach Rsig

4. at high frequency after output impedance increases Cgd take over and shunt Rsig to the ground
5. Analytically calculate the zeros, poles, and magnitude at low/high frequency for $Zout$. Compare with simulation results in a table.

```
No. of Data Rows : 1
zero(1) = -9.68799e+14,0.000000e+00
zero(2) = -4.21579e+14,0.000000e+00
zero(3) = -7.31739e+06,0.000000e+00
Doing analysis at TEMP = 27.000000 a

No. of Data Rows : 31
Doing analysis at TEMP = 27.000000 a

No. of Data Rows : 1
pole(1) = -3.99840e+14,0.000000e+00
pole(2) = -1.73557e+08,1.362622e+08
pole(3) = -1.73557e+08,-1.36262e+08
```

22	cgg	67.45f
23	cgs	52.73f
24	cgd	3.083f
25	cgb	11.64f
26	cdb	18.65f
27	csb	26.46f
28	cdd	12.08f

- For analytical solution $Zout \approx \frac{1}{gm}\left(\frac{1+sRsigCgs}{1+\frac{sCgs}{gm}}\right)$ so there are zero at $\frac{1}{RsigCgs} = 9.48\ Mrad/s$ and pole at $\frac{gm}{Cgs} = 1.9\ Grad/s$ the actual pole come before this pole because of Cgd take over and make the Zout =0

- Zout at Low frequency equal 1/gm as we can ignore terminal has s and the equation will reduce to Zout=1/gm
- Zout at High Frequency equal Rsig as Cgs become like Short Circuit and the impedance seen equal Rsig but Cgd take over and shunt Rsig to the ground before the impedance equal Rsig