

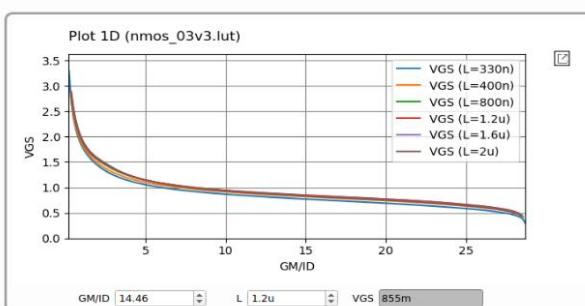
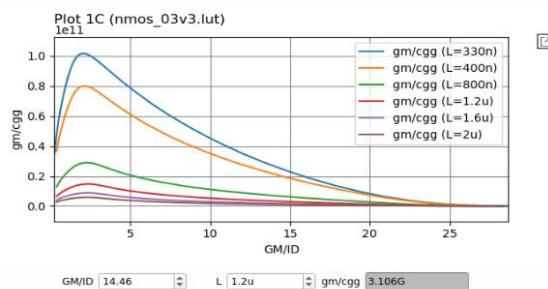
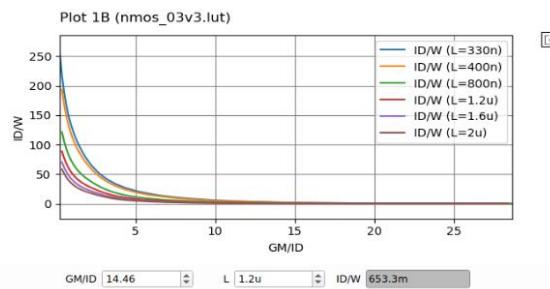
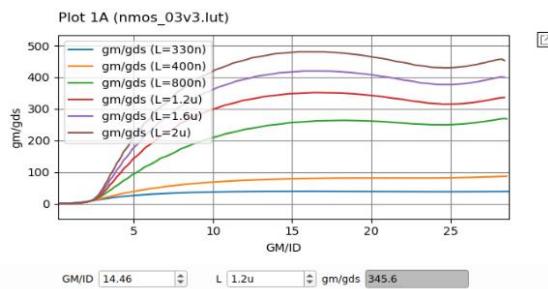
ITI CMOS Analog IC Design 2024  
Lab 07  
Gm/ID Design Methodology

## Part 1: gm/ID design charts

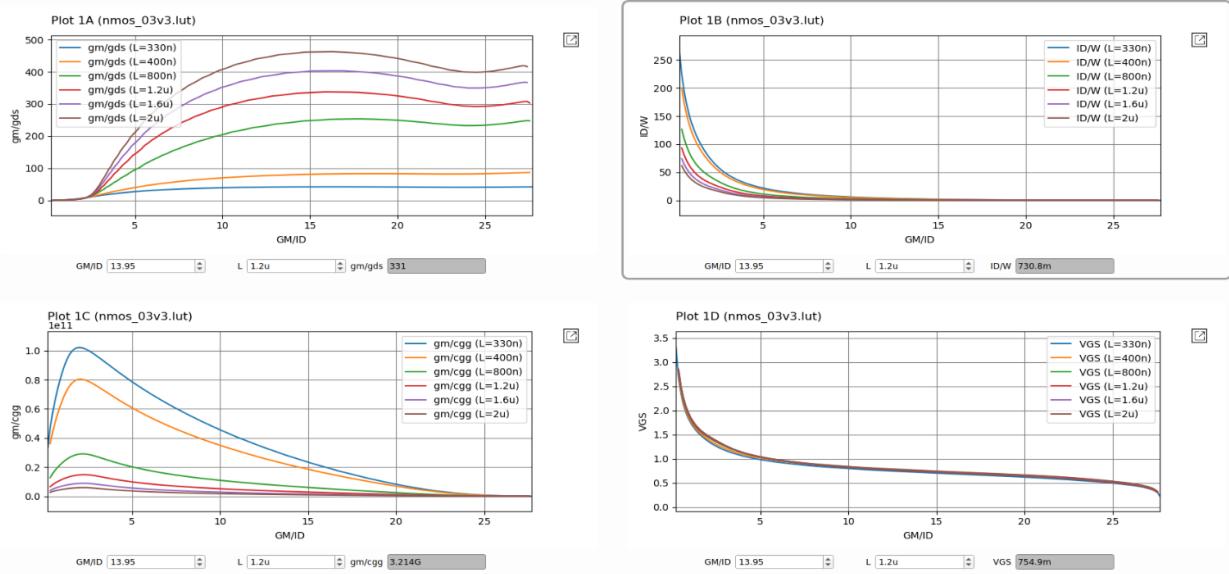
- Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.33u,0.4u:0.4u:2u:  
And from the specs below we need will choose ID=20  $\mu$ A to get  
 $gm/ID = 16$  for input pair

### 1. Design chart for input pair

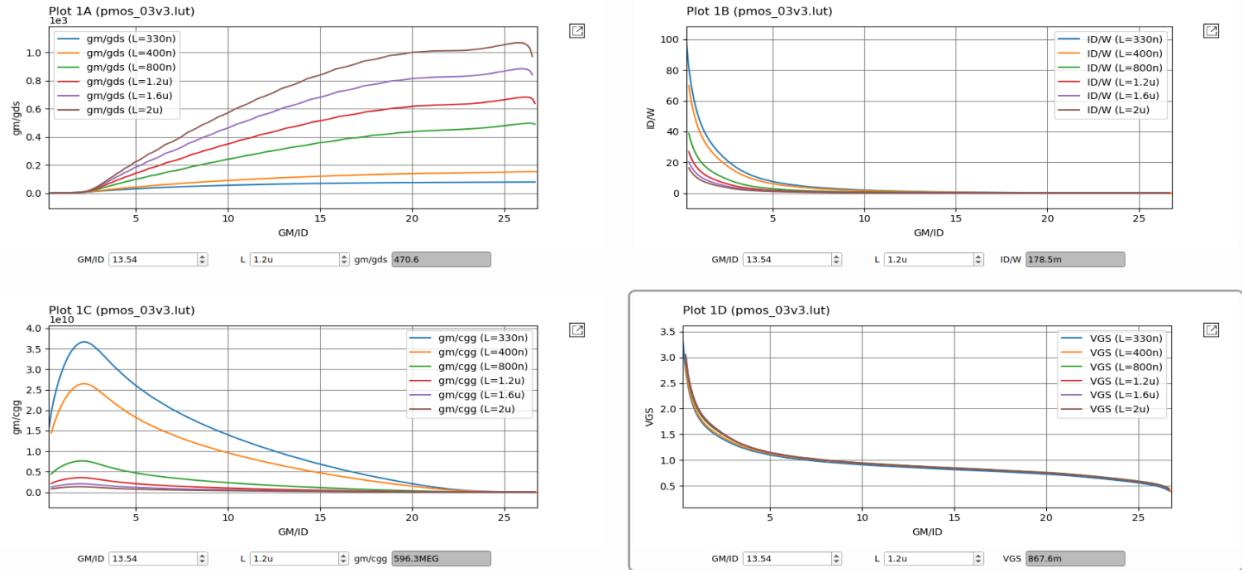
- As the specs below CMIR is near to the VDD so I will choose NMOS as input pair and the tail current has  $V_{ds} \neq 0$  so it make  $V_{sb} \neq 0$  for input pair and I choose it .3 V as it's the average of  $VDD/6$  for  $V_{ds}$  we choose to design for tail current source



## 2. Design Chart for tail current source



## 3. Design Chart For load current mirror



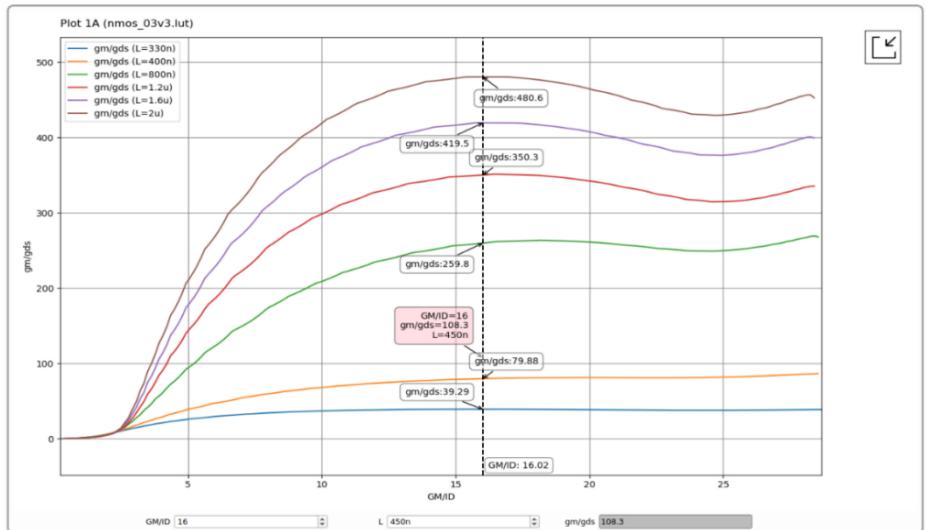
## Part 2: OTA Design

- Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs
- The required gain is not high (only 32 dB = 40) so it can be achieved by a simple single stage OTA

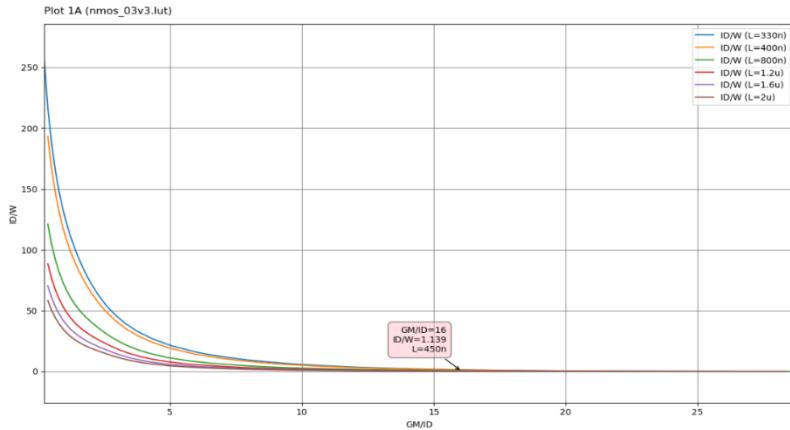
Technology	0.18 $\mu$ m CMOS
Supply Voltage	1.8V
Load	5pF
Open Loop DC Voltage Gain	$\geq 34\text{dB}$
CMRR @ DC	$\geq 74\text{dB}$
Phase Margin	$\geq 70^\circ$
CM input range - low	$\leq 1\text{V}$
CM input range - high	$\geq 1.5\text{V}$
GBW	$\geq 10\text{MHz}$

### 1. Design steps for input pair

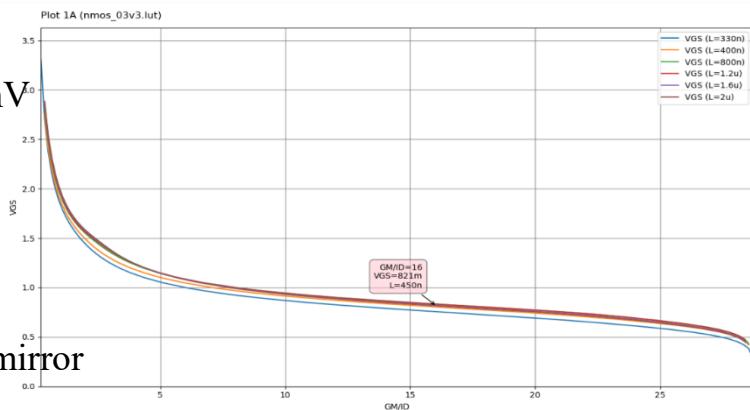
- For OTA the output pole is the dominant so  $GBW \approx gm * Rout * \frac{1}{2\pi * Rout * Cl} = \frac{gm}{2\pi * Cl}$  as  $Cl >> C_{dd}$  for the two transistor so  $\frac{gm}{2\pi * 5\text{pF}} \geq 10\text{MHz}$ , so  $gm \geq 314\mu\text{s}$  so I choose  $gm = 320\mu\text{s}$
- Then I need a reasonable value for  $gm/ID$  let's assume  $gm/ID = 16$  to decrease the power consumptions so we need  $ID = 20\mu\text{A}$  and this is the value I use above to draw the design chart for the device above
- we assume PMOS and NMOS has same  $r_o$  so gain =  $gm * r_o / 2$
- $50 = 320 * r_o / 2$  so  $r_o = 312.5\text{k}\Omega$  so from chart  $gm/gds$  we need  $gm/gds > 100$  at  $gm/ID = 16$  so we choose  $L = 450\text{nm}$



- For ID from chart ID/W at L=450nm and Gm/ID=16 ID/W=1.139
- So for ID=20 $\mu$ A we need W=17.57 $\mu$ m
- So for input pair we need NMOS with L=450nm and ID=20 $\mu$ A and W=17.57 $\mu$ m

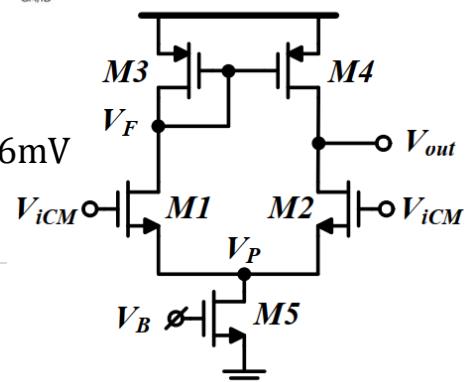
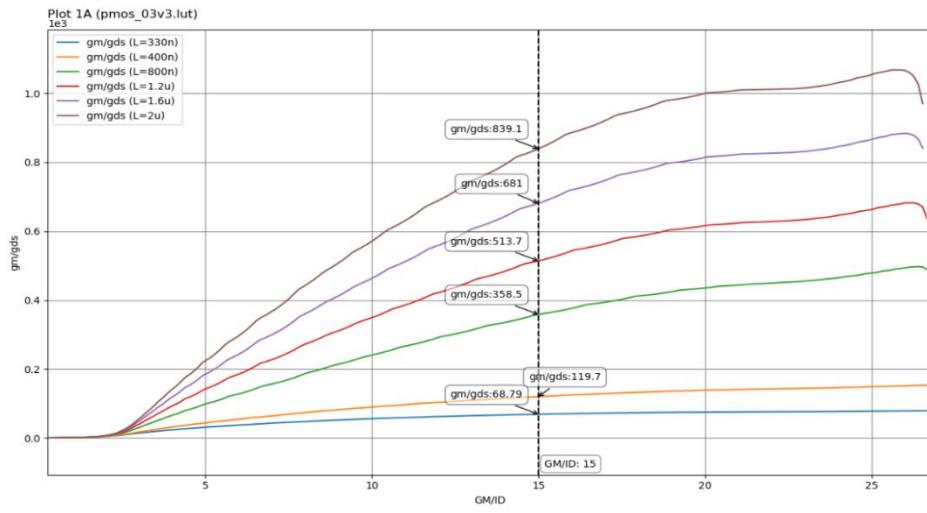


- from chart Vgs at L=450nm and gm/ID=16 then Vgs=821mV

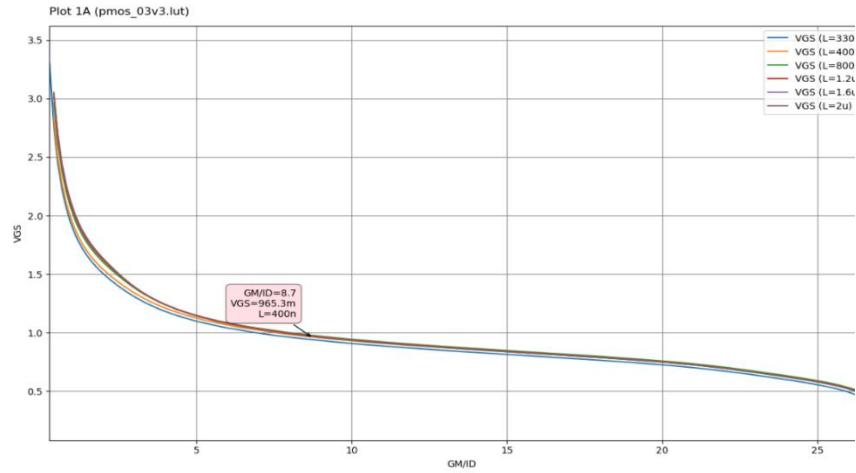


## 2. Design steps for Load current mirror

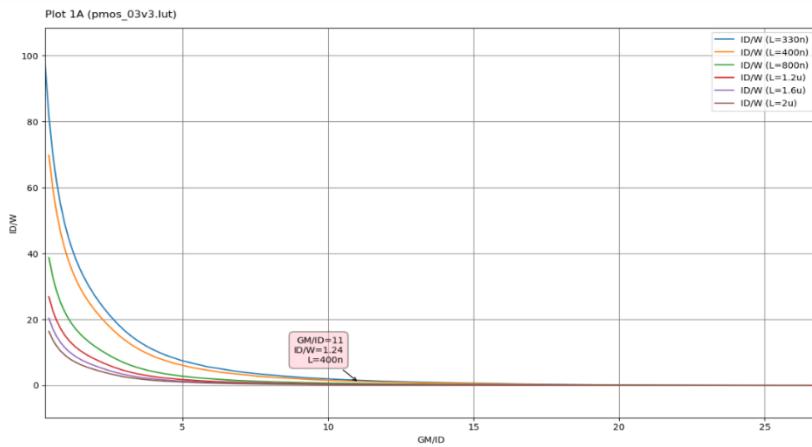
- Let's assume a reasonable gm/ID let's start with gm/ID = 15 and as we have ID=20 $\mu$ A so gm=300 $\mu$ S
- From the assumption of the gain, we need  $gm/gds > 93.75$  from gm/gds chart at gm/ID=15
- So we choose L=400nm
- As the Load current mirror near to the VDD it limits the maximum Common mode input range (CMIR)
- $ViCM_{Max} \leq VDD - |V_{gs3}| + V_{THN1}$
- $V_{gs3} \leq VDD + V_{gs1} - V^* - ViCM_{Max} = 1800 - 821 - 125 - 1500 = 966\text{mV}$
- So we need to check that  $V_{gs3} \leq 966\text{mV}$



- from Vgs chart at L=400nm we find that  $\left(\frac{g_m}{I_D}\right)_{Min} = 8.7$  so choosing  $g_m/I_D = 11$

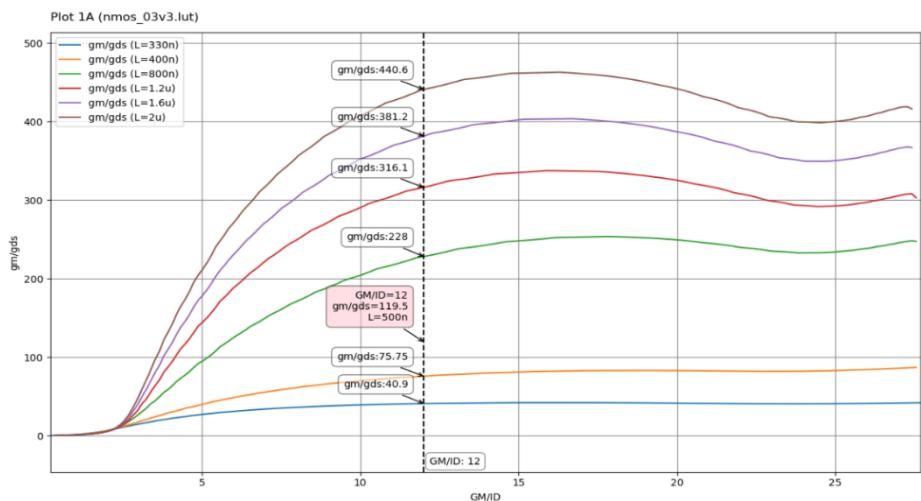


- From ID/W chart at gm/ID=11 and L=400nm we find  $ID/W = 1.24\mu A/\mu m$  for  $ID = 20\mu A$   
We need  $W = 16.13\mu m$
- So the sizing of the load current mirror L=400nm and W=16.13 $\mu m$  and ID=20 $\mu A$



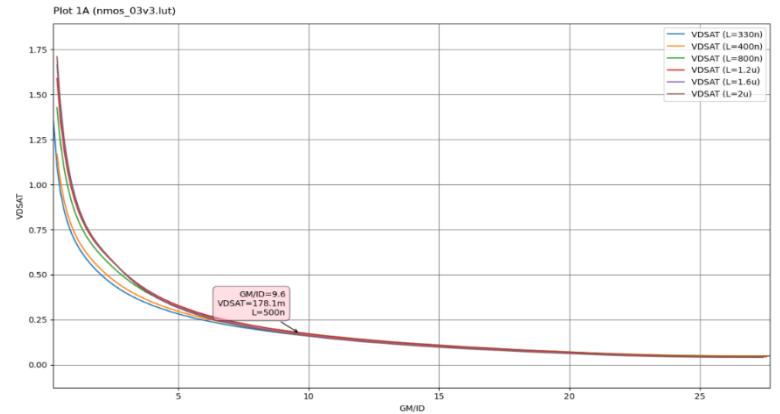
### 3. For tail current source

- $A_{cm} = -40db = .01 = A_{cm} = \frac{1}{2g_{m3}*R_{ss5}}$  then  $g_{ds5} = .01 * 2 * 220\mu S = 4.4\mu S$  we choose  $g_m/I_D = 12$  and  $I_D = 40$  so  $g_m = 480\mu S$  so  $\frac{g_m}{g_{ds}} > 109$
- from  $g_m/g_{ds}$  chart at  $g_m/I_D = 12$  then we need L=500nm for tail current source
- As the tail current source attach to the ground, it limits the CMIR<sub>Min</sub>



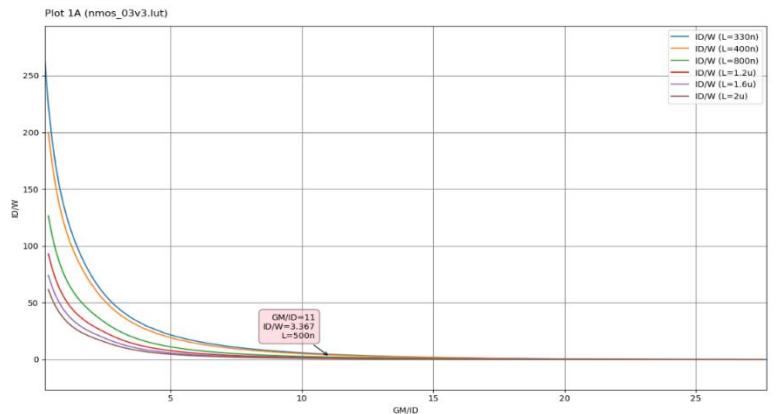
- $V_{iCM} \geq V_{THN} + V_{ov1} + V_{ov5} = V_{GS1} + V_{ov5}$  then  $V_{ov5} \leq V_{iCM} - V_{GS1} = 1000 - 821 = 179mV$  so  $V_{ov5} \leq 179 mV$  so  $\left(\frac{g_m}{I_D}\right)_{Min} = 9.6$

- choosing gm/ID greater to set margin I choose  $g_m/I_D = 11$



- From ID/W chart to achieve ID=40μA at gm/ID=12 and L=500nm ID/W=3.367 so W=11.88μm

So for tail current we need L=430nm and W=10.43μm and gm/ID=11

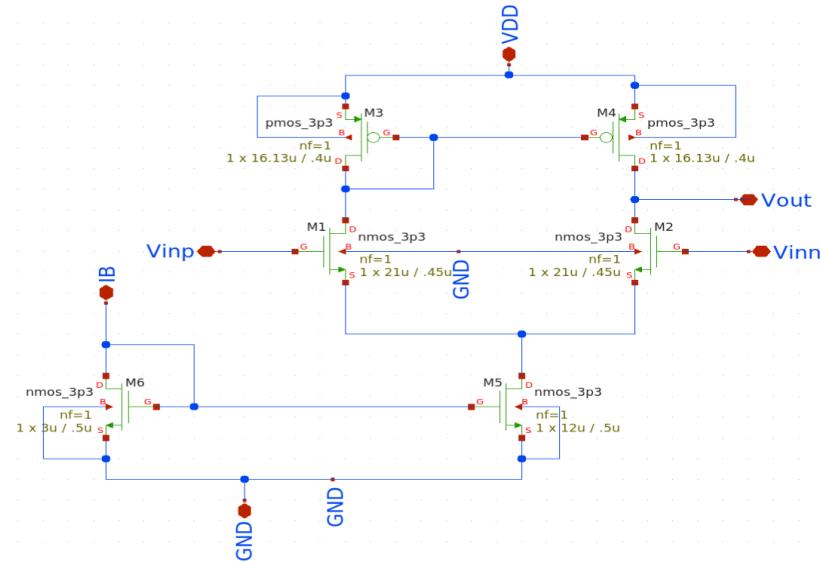


transistor	L	W	Gm/ID	ID	gm	Vdsat	Vov	V*
M1&M2	450nm	17.57μm	16	20μA	320μS	100.9mV	26.61mV	125mV
M3&M4	400nm	16.13μm	11	20μA	220μS	161.2mV	135mV	181.8mV
M5&M6	500nm	11.88μm&2.97μm	11	40μA&10μA	440μS&110μS	155.6mV	131.6mV	181.8mV

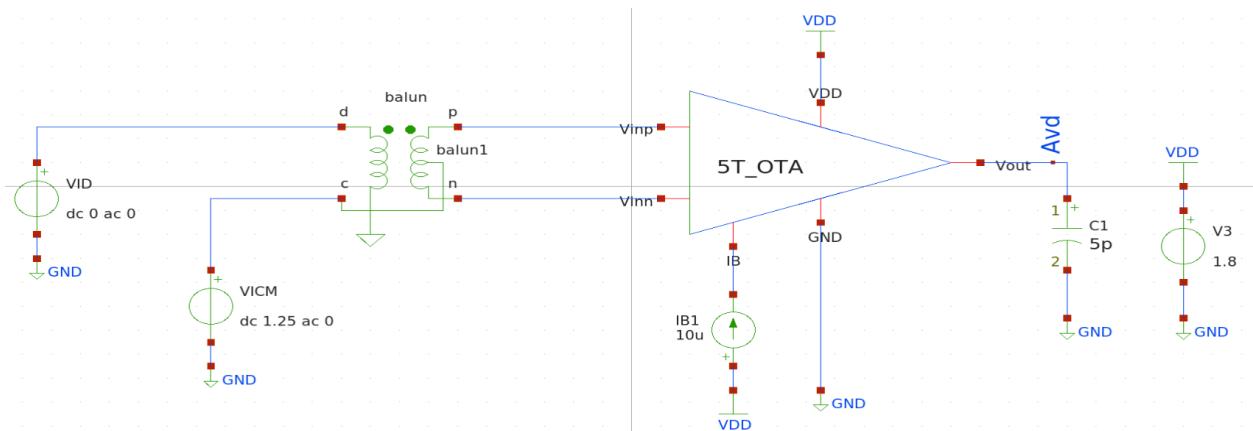
- As there are two pole in this topology the output node and mirror node and as the output pole has high impedance and mirror node has low impedance so output pole is the dominant and mirror node is so far so the phase margin for the system is >70

## Part 3: Open – loop OTA simulation

- The design of 5T\_OTA



- The Testbench



- I tune the sizing a bit to match the specs the new sizing as shown in the figure above

## 1. OP (Operating Point) Analysis

1. Use VCM at the middle of the CMIR and show the operating points.

BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x1.xm6.m0	m.x1.xm4.m0	m.x1.xm3.m0
model	nmos_3p3.8	pmos_3p3.12	pmos_3p3.12
gm	0.000110671	0.000216449	0.000216449
gmbs	3.97057e-05	8.94639e-05	8.94639e-05
gds	8.22248e-07	1.74899e-06	1.74899e-06
vds	0.820753	0.906142	0.906142
vdsat	0.154772	0.154319	0.154319
vgs	0.820757	0.906143	0.906143
vth	0.70807	0.77952	0.77952
id	1e-05	1.91475e-05	1.91475e-05

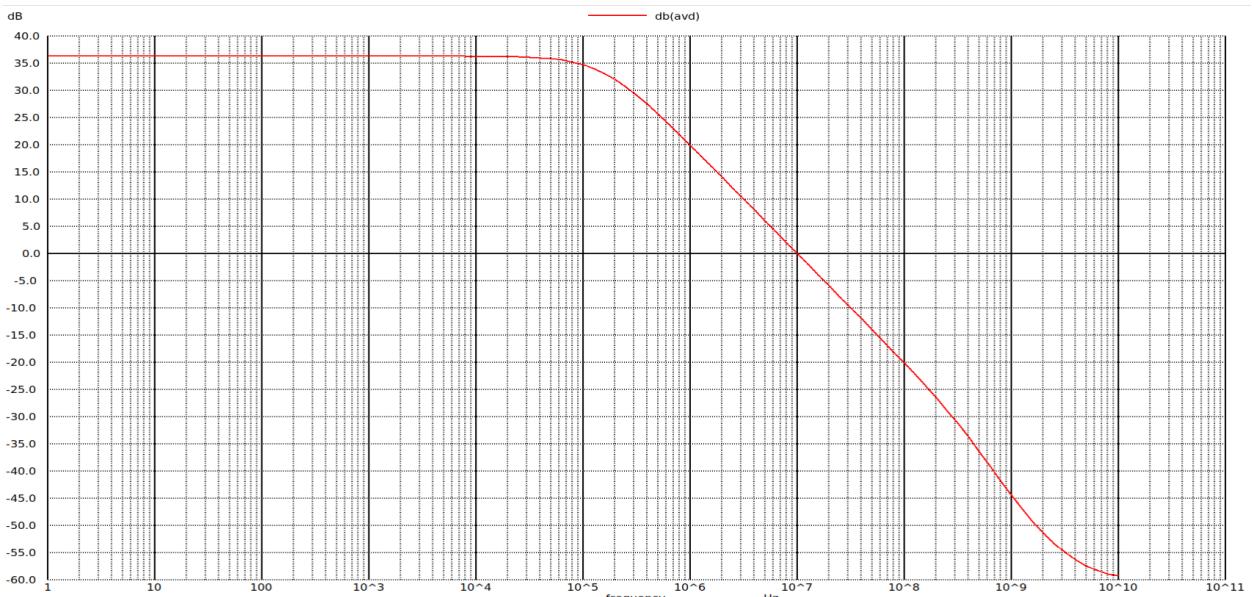
  

BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x1.xm5.m0	m.x1.xm2.m0	m.x1.xm1.m0
model	nmos_3p3.12	nmos_3p3.12	nmos_3p3.12
gm	0.000427813	0.00032025	0.00032025
gmbs	0.000152933	8.74289e-05	8.74289e-05
gds	4.90897e-06	3.13809e-06	3.13809e-06
vds	0.410631	0.483214	0.483214
vdsat	0.151287	0.0940938	0.0940938
vgs	0.820757	0.83936	0.83936
vth	0.713634	0.82917	0.82917
id	3.8295e-05	1.91475e-05	1.91475e-05

2. The current and the gm in the input pair are exactly the same
3. The dc voltage at the output node is  $V_{DD} - V_{ds4} = 1.8 - .906 = 894mV$  it's equal for the mirror node voltage this because the two current are equal and as the voltage at the gate of the two current mirror load transistors are equal so that means they have the same Vds

## 2. Diff small signal ccs:

1. Plotting diff gain (in dB) vs frequency.



```

peak = 6.526437e+01 at= 2.511886e+00
f2 = 1.534929e+05
peak = 6.526437e+01
gaindb = 3.629352e+01
f2 = 1.534929e+05
gbw = 1.001762e+07

```

2. To calculate the gain and Bandwidth and GBW

$$A_v = g_{m2} * (r_{o2} || r_{o4}) = 320.25 \mu S * \left( \frac{1}{3.14 \mu S} || \frac{1}{1.75 \mu S} \right) = 65.49$$

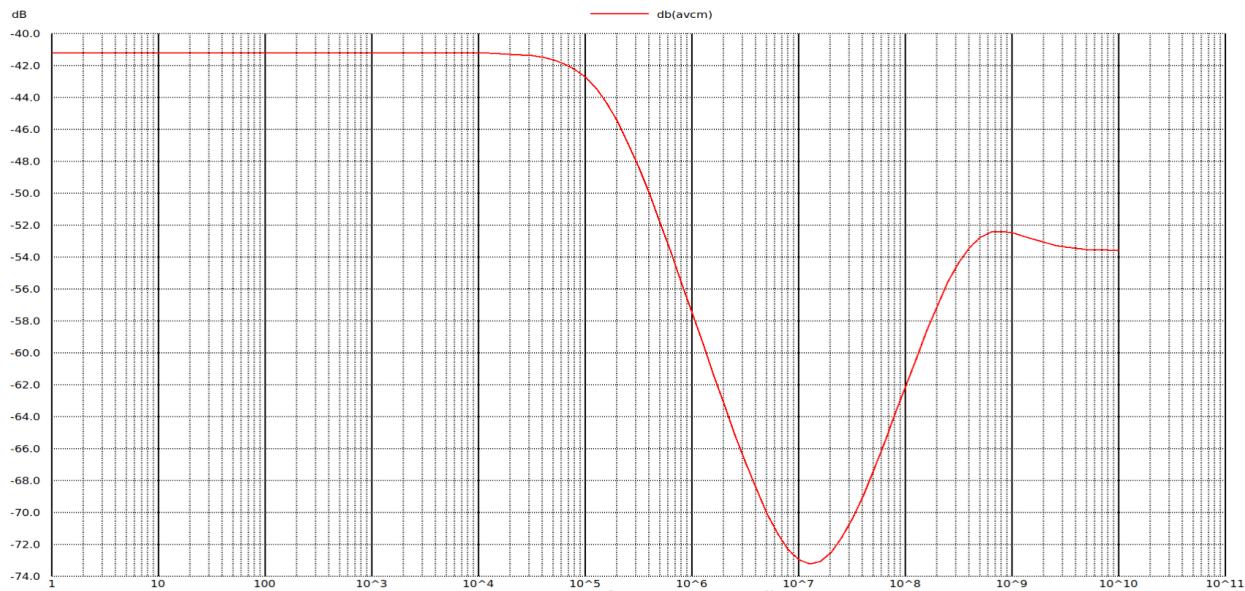
$$BW = \frac{1}{2\pi(r_{o2} || r_{o4}) * C_L} = \frac{1}{2\pi * \left( \frac{1}{3.14 \mu S} || \frac{1}{1.75 \mu S} \right) * 5 pF} = 155.66 \text{ kHz}$$

$$GBW = \frac{g_{m2}}{2\pi * C_L} = \frac{320.25 \mu S}{2\pi * 5 pF} = 10.19 \text{ MHz}$$

	Simulation	Analytical
DC gain	65.26	65.49
BandWidth	153.49 kHz	155.66 kHz
GBW	10.02 MHz	10.19 MHz

### 3. CM small signal ccs:

1. Plotting CM gain (in dB) vs frequency.



```

peak = 8.715843e-03
gaindb = -4.11938e+01
f2 = 1.535451e+05
gbw = 1.338275e+03

```

2. To calculate the gain and Bandwidth and GBW

$$A_v = \frac{g_{m2}}{1 + (g_{m2} + g_{mb2}) * 2R_{ss5}} * \frac{1}{g_{m4}}$$

$$= \frac{320.25\mu S}{1 + (320.25\mu S + 87.43\mu S) * \frac{2}{4.91\mu S}} * \frac{1}{216.45\mu S} = 8.86 * 10^{-3}$$

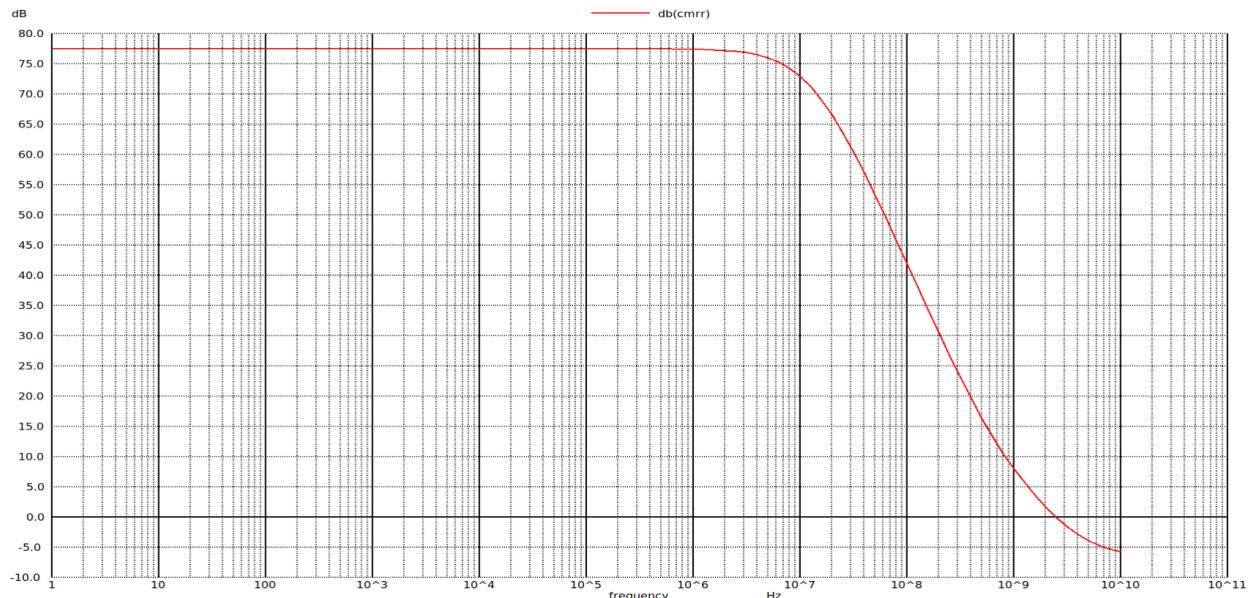
$$BW = \frac{1}{2\pi(r_{o2}||r_{o4}) * C_L} = \frac{1}{2\pi * (\frac{1}{3.14\mu S} || \frac{1}{1.75\mu S}) * 5pF} = 155.66 kHz$$

$$GBW = A_v * BW = 8.86 * 10^{-3} * 155.66kHz = 1.38 kHz$$

	Simulation	Analytical
DC gain	$8.72 * 10^{-3}$	$8.86 * 10^{-3}$
BandWidth	$153.54 kHz$	$155.66 kHz$
GBW	$1.34 kHz$	$1.38 kHz$

## 4. CMRR

1. Plotting CMRR (in dB) vs frequency



```
peak = 7.488016e+03
gaindb = 7.748734e+01
f2 = 7.673300e+06
gbw = 5.745779e+10
```

1. To calculate the gain and Bandwidth and GBW

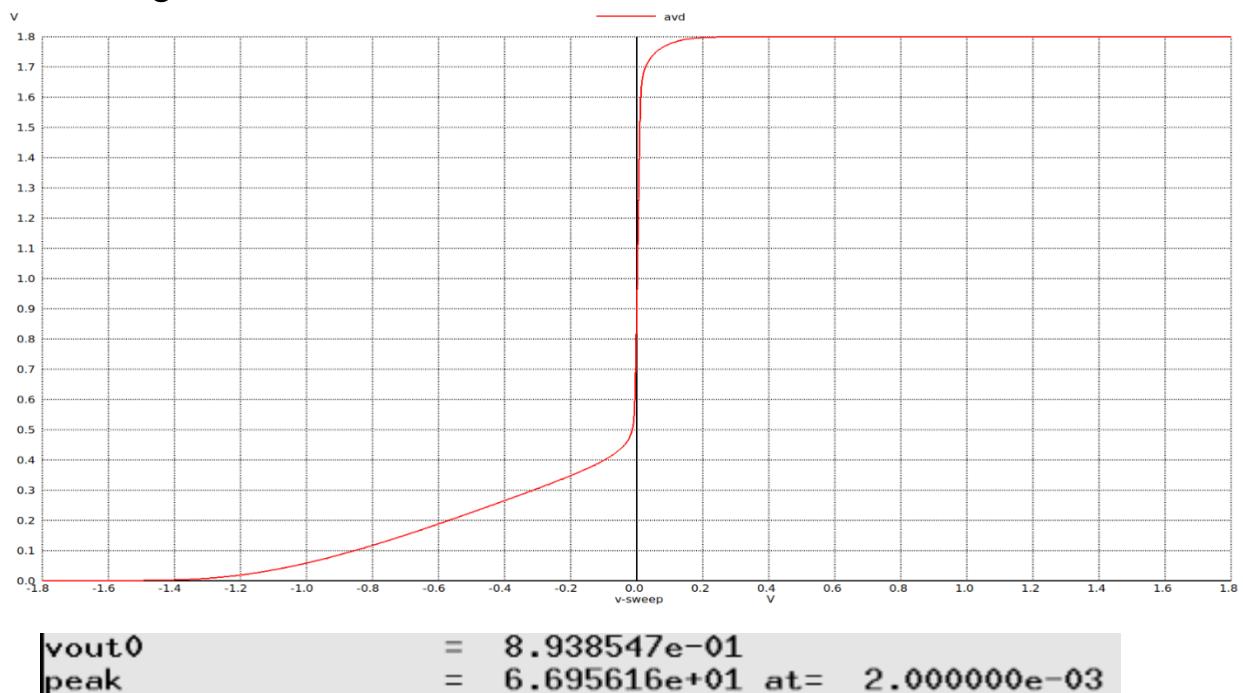
$$A_v = (r_{o2} || r_{o4}) * ((g_{m2} + g_{mb2}) * 2R_{ss5}) * g_{m4}$$

$$= \left( \frac{1}{3.14\mu S} || \frac{1}{1.75\mu S} \right) ((320.25\mu S + 87.43\mu S) * \frac{2}{4.91\mu S} * 216.45\mu S) = 7350$$

	Simulation	Analytical
DC gain	7488	7350

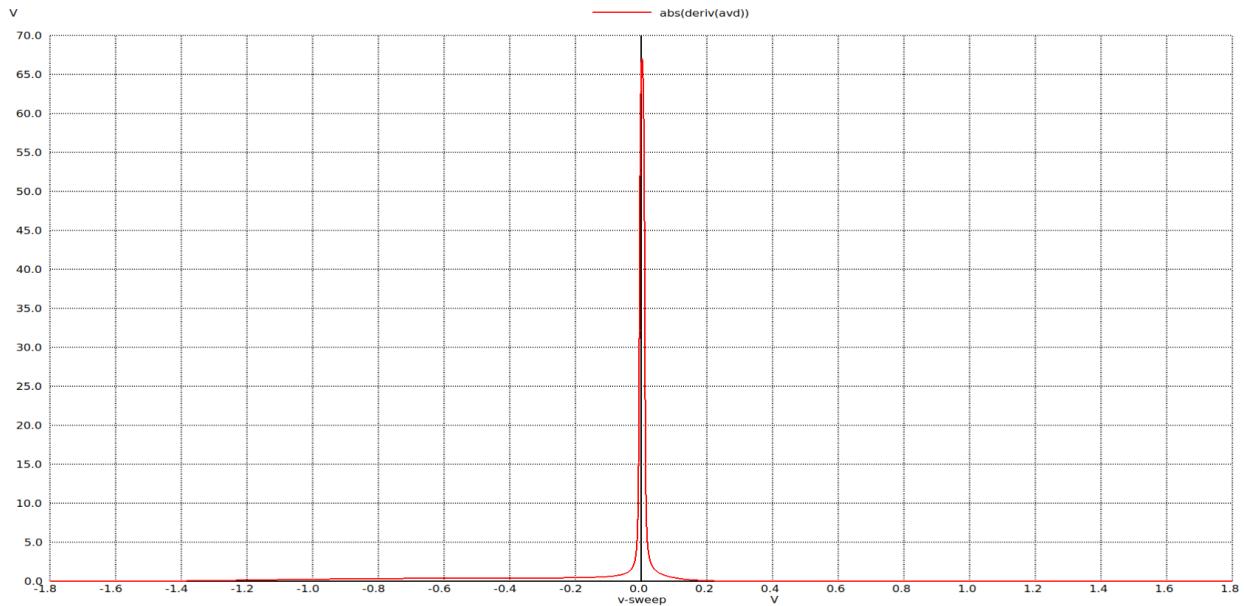
## 5. Diff large signal ccs:

1. Plotting Vout vs Vid

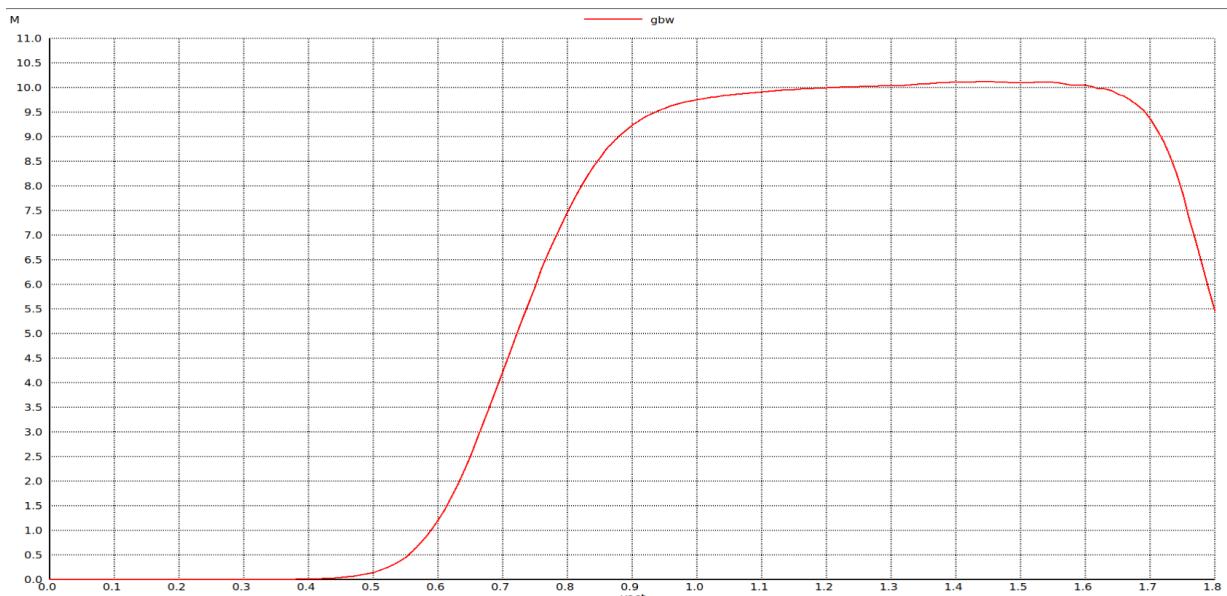


- Vout@Vid=0 is the same operating point as above so as the V<sub>GS</sub> for two input pair are equal so the two current are equal and as the voltage at the gate of the two current mirror load transistors are equal so that means they have the same V<sub>ds</sub> so output node voltage is  $V_{DD} - V_{ds4} = 1.8 - .906 = 894mV$  it's equal for the mirror node voltage
- As we see the peak of derivative =66.96 and it's approximately equal to the dc gain of the above analysis

## 2. Plotting the derivative of VOUT vs VID



## 6. (Optional) CM large signal ccs (GBW vs VICM):



```
vicmmax = 1.710000e+00  
vicmmin = 8.700000e-01
```

- As we see it meets the above specs of CMIR

## PART 4: Closed-Loop OTA Simulation

### 1. OP analysis

```

gm_mismatch = 3.475838e-06
id_mismatch = 2.720255e-07
BSIM4v5: Berkeley Short Channel IGFET Model-4
  device      m.x2.xm6.m0      m.x2.xm4.m0      m.x2.xm3.m0
  model       nmos_3p3.8      pmos_3p3.12      pmos_3p3.12
  gm          0.000110671     0.000211112     0.000213777
  gmb      3.97057e-05      8.73053e-05      8.83543e-05
  gds        8.22248e-07      1.86136e-06      1.72089e-06
  vds        0.820753         0.75216         0.904374
  vdsat      0.154772         0.152692        0.153011
  vgs        0.820757         0.904375        0.904375
  vth        0.70807          0.779959        0.779525
  id          1e-05           1.84921e-05     1.87641e-05

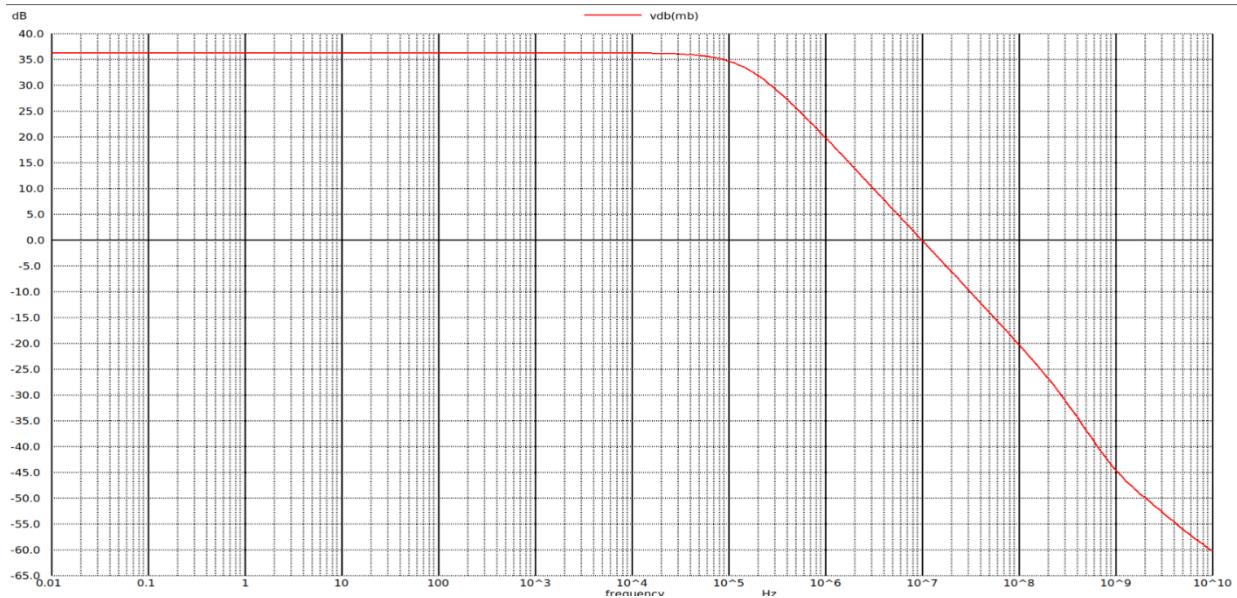
BSIM4v5: Berkeley Short Channel IGFET Model-4
  device      m.x2.xm5.m0      m.x2.xm2.m0      m.x2.xm1.m0
  model       nmos_3p3.12      nmos_3p3.12      nmos_3p3.12
  gm          0.00041391     0.000312311     0.000315787
  gmb      0.000148006      9.16579e-05      9.26912e-05
  gds        1.04327e-05      2.58691e-06      2.77652e-06
  vds        0.256807          0.79102         0.638806
  vdsat      0.151161          0.0912327        0.092099
  vgs        0.820758          0.791021        0.793184
  vth        0.713817          0.785556        0.785939
  id          3.72563e-05      1.84921e-05     1.87641e-05

```

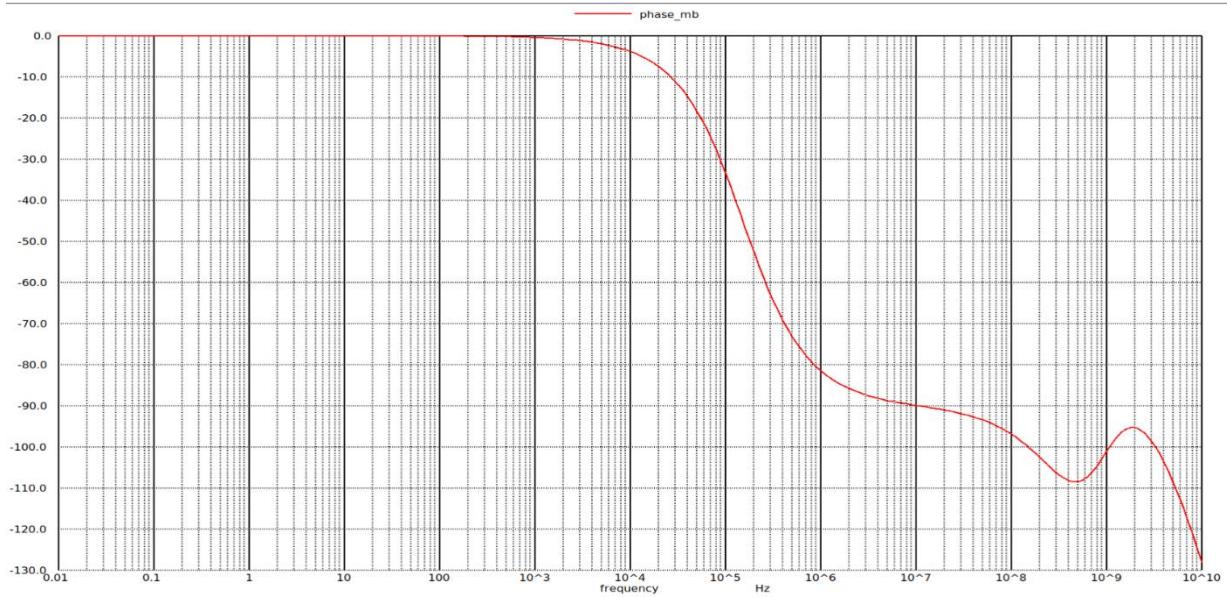
- We see that the current and gm aren't equal in the two input pair transistors (M1&M2) that because the 5T OTA doesn't have an infinite gain so there are  $V_{err} \neq 0$  difference between the two input and this make the current and the gm in the two transistors are different
- The mismatch in current from the above code equal =272nA
- The mismatch in gm from the above code equal = $3.48\mu S$

## 2. Loop Gain:

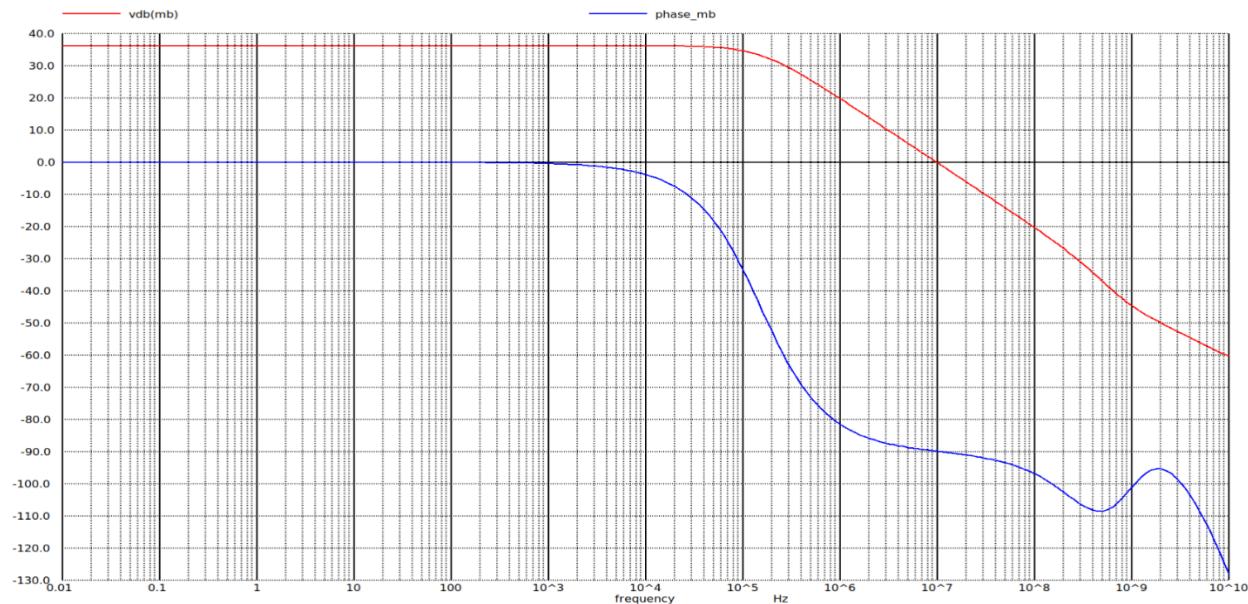
### 1. Plotting loop gain in dB vs frequency



### 2. Plotting phase vs frequency



### 3. Plotting loop gain in dB and phase vs frequency



### 4. Showing the operating point at VICM in the middle of the CMIR

```

peak           = 6.512221e+01 at= 4.466836e+00
bw             = 1.512356e+05
pm_deg         = -8.982445e+01
dominant_pole_f = 9.845405e+06
loop_gain      = 3.627458e+01
gbw = 9.848797e+06
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

```

No. of Data Rows : 1			
BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x2.xm6.m0	m.x2.xm4.m0	m.x2.xm3.m0
model	nmos_3p3.8	pmos_3p3.12	pmos_3p3.12
gm	0.000110671	0.000211963	0.000218822
gmbs	3.97057e-05	8.77328e-05	9.04492e-05
gds	8.22248e-07	2.22899e-06	1.77411e-06
vds	0.820753	0.555273	0.907711
vdsat	0.154772	0.154741	0.155484
vgs	0.820757	0.907713	0.907712
vth	0.70807	0.78052	0.779516
id	1e-05	1.8799e-05	1.94918e-05
BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x2.xm5.m0	m.x2.xm2.m0	m.x2.xm1.m0
model	nmos_3p3.12	nmos_3p3.12	nmos_3p3.12
gm	0.000427767	0.000316156	0.000324673
gmbs	0.000152917	8.63152e-05	8.86716e-05
gds	4.91947e-06	2.59682e-06	3.18684e-06
vds	0.409787	0.834928	0.482489
vdsat	0.151286	0.0924754	0.0946281
vgs	0.820757	0.834929	0.840204
vth	0.713635	0.828007	0.828945
id	3.82908e-05	1.8799e-05	1.94918e-05

5. Comparing DC gain and GBW with those obtained from open-loop simulation.

	Open loop	Closed loop
DC gain	65.26	65.12
BandWidth	153.54 kHz	151.24kHz
GBW	10.02MHz	9.85MHz

6. Comparing simulation results with hand calculations in table.

- Hand analysis for gain and bandwidth and GBW

$$A_v \approx g_{m2} * (r_{o2} || r_{o4}) = 320.25\mu S * \left( \frac{1}{3.14\mu S} || \frac{1}{1.75\mu S} \right) = 65.49$$

$$BW \approx \frac{1}{2\pi(r_{o2} || r_{o4}) * C_L} = \frac{1}{2\pi * \left( \frac{1}{3.14\mu S} || \frac{1}{1.75\mu S} \right) * 5pF} = 155.66 \text{ kHz}$$

$$GBW \approx \frac{g_{m2}}{2\pi * C_L} = \frac{320.25\mu S}{2\pi * 5pF} = 10.19 \text{ MHz}$$

	Analysis	Simulation
DC gain	65.49	65.12
BandWidth	155.66 kHz	151.24kHz
GBW	10.19MHz	9.85MHz

- We see that the phase margin =89.8 and meet the specs of phase margin above