ITI CMOS Analog IC Design 2024
Lab 03
Cascode Amplifier

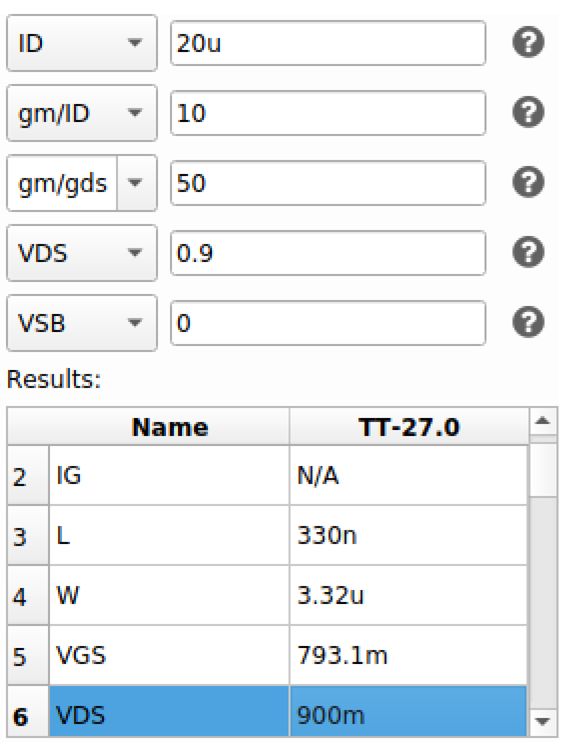
PART 1: Sizing Chart

1. $|Av| \approx gmro = 2I_D/V_{ov} \times V_A/I_D = 2V_A/V_{ov}$

- if we compute Vov and $2ID/gm$ they will not be equal. Let's define a new parameter called V-star ($V*$) which is calculated from actual simulation data using the formula $V* = 2ID/gm \leftrightarrow gm = 2ID/V*$

2. The specs we must achieve.

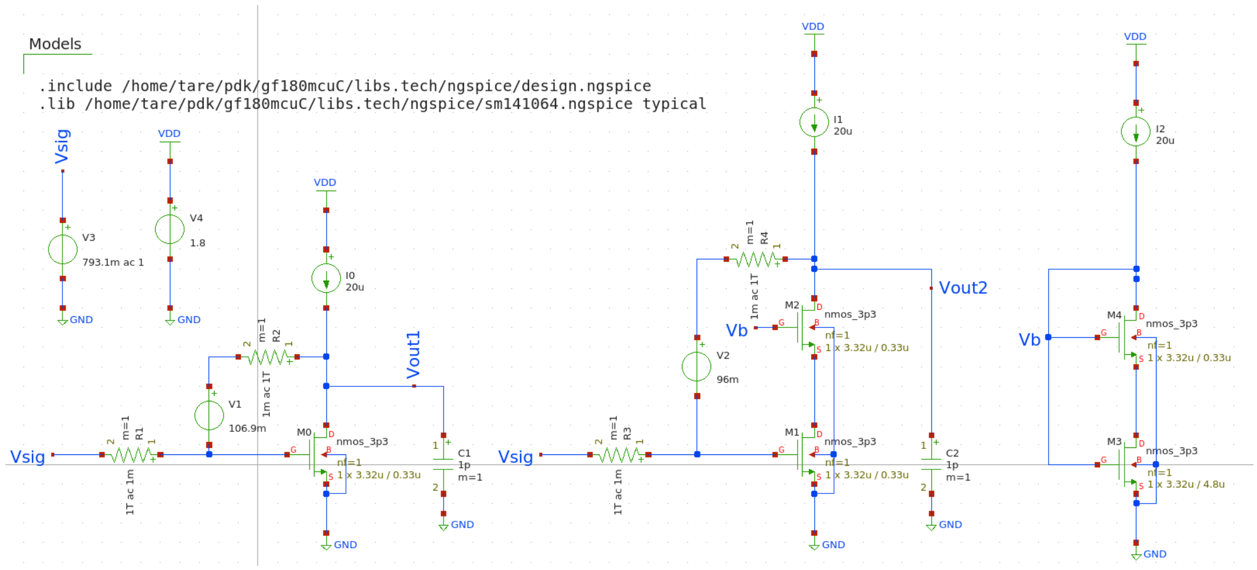
spec	Value
gm*ro	**50**
gm/Id	**10**
Supply	**1.8V**
Quiescent (DC) output voltage	**$V_{DD}/2$ =.9**
Current consumption	**20µA**



- From SA in ADT we need NMOS with L=330nm and W=3.32µm and the voltage in gate V_{GS} =793.1 mV to achieve the specs above

PART 2: Cascode for Gain

1. OP Analysis

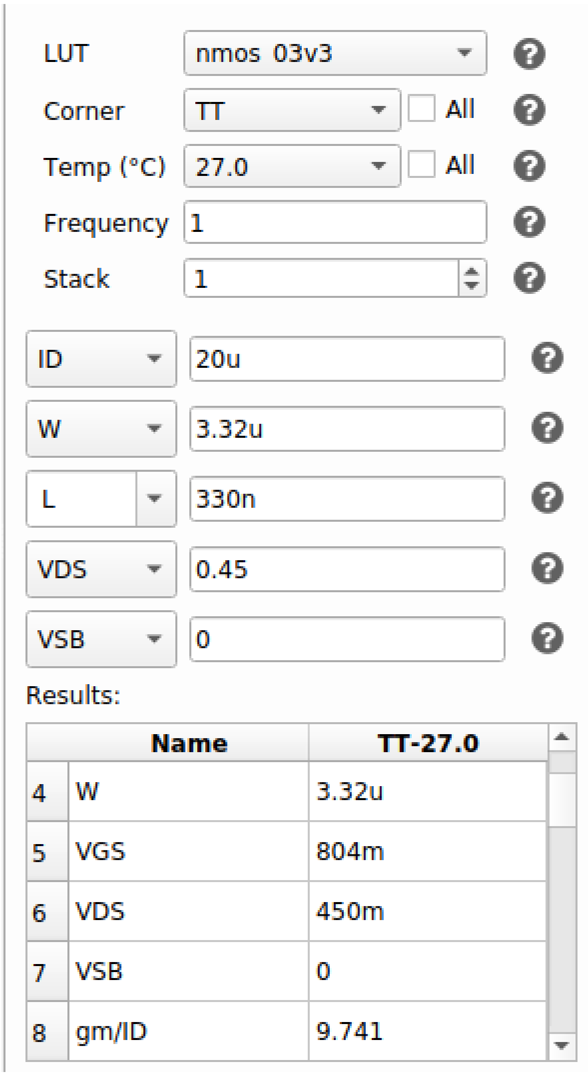


1. We need to bias transistors in saturation; however, the output node is a high impedance node (ideal DC Current source); thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations. The input transistor is diode connected for DC simulation, while in AC simulation the feedback is disconnected, and the AC input source is connected.

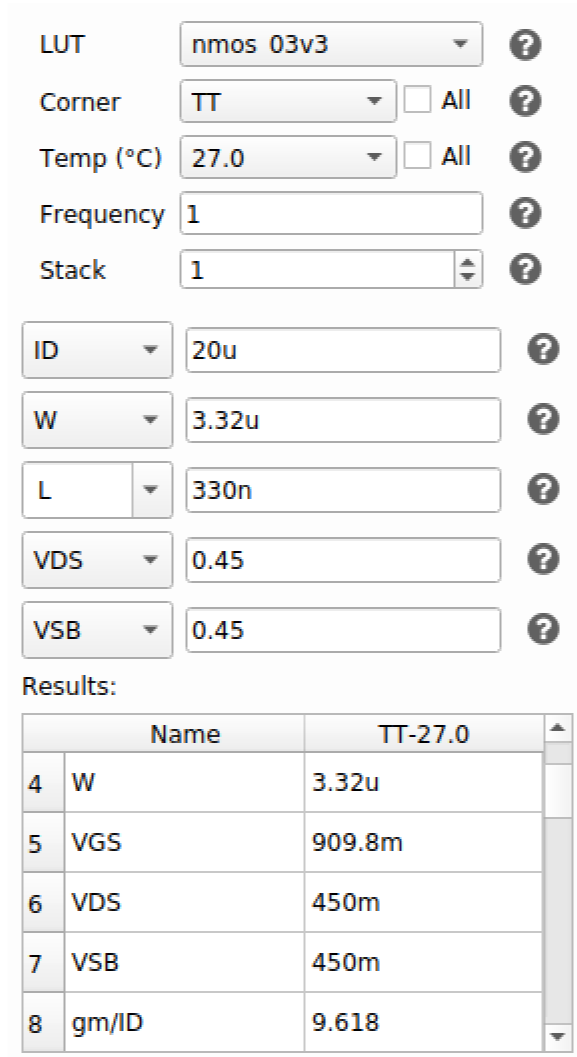
- V_{DC0} =900- V_{GS0}=900-793.1=106.9 mV
- V_{DC1} =900- V_{GS1}=900-804=96 mV

2. For the Cascode amplifier, we will design $\boldsymbol{V_B}$ **to set** $\boldsymbol{V_{DS1} \approx VDS2 \approx 0.45\ V}$ as shown below
3. to calculate V_B we need to find V_{GS2} because $\boldsymbol{V_B = V_{GS2} + V_{DS1}}$.

M1



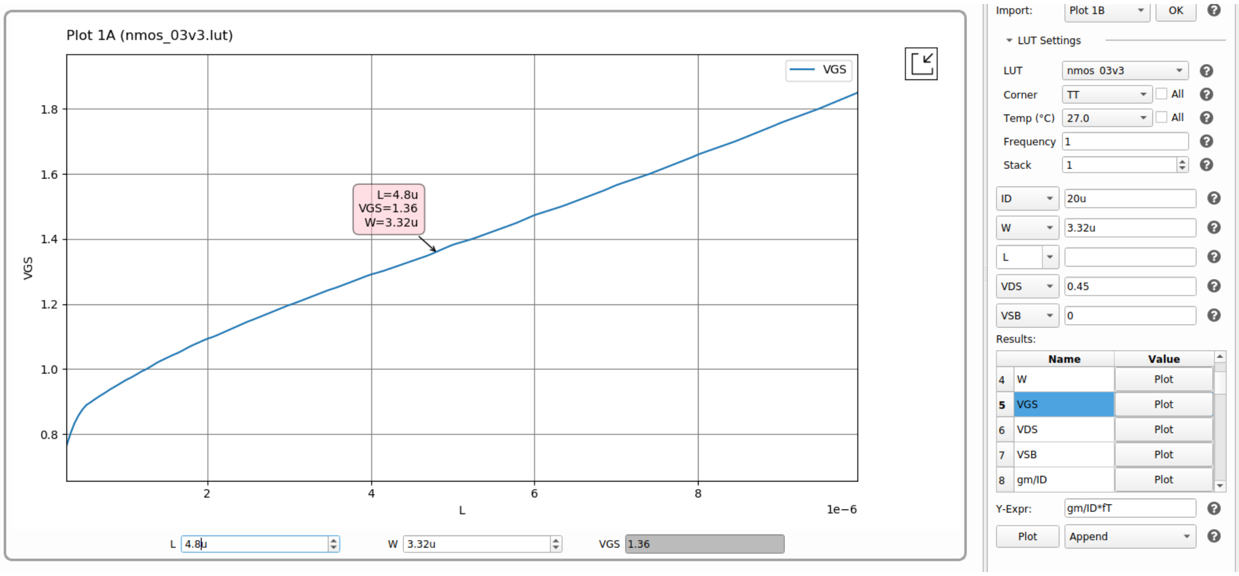
M2



- $V_B = V_{GS2} + V_{DS1}$ =909.8+450=1359 mV

4. M3 and M4 are used to generate the Cascode bias voltage.

- find L_3 at $\boldsymbol{V_{GS}} = \boldsymbol{V_B} = \boldsymbol{V_{GS2}} + \boldsymbol{V_{DS1}}$ using W_3, I_D.



- L_3=4.8µm

5. Simulate the DC OP point of the CS and cascode amplifiers.

```
igain0 = 4.707964e+01
igain1 = 1.445516e+03
binary raw file "lab3.raw"
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device            m.xm3.m0             m.xm4.m0             m.xm2.m0
      model        nmos_3p3.10           nmos_3p3.8           nmos_3p3.8
         id              2e-05                2e-05                2e-05
        vgs            1.36366             0.903809             0.912647
        vth            0.65495             0.774616             0.777992
        vds            0.45984             0.903801             0.450764
      vdsat           0.549665             0.164476             0.168102
         gm         4.5658e-05          0.000198379          0.000195411
        gds         1.2877e-05          4.55058e-06          5.83296e-06
       gmbs        1.77078e-05          4.09775e-05          4.08803e-05
        cdb       -8.21134e-15         -1.99345e-16         -2.05408e-16
        cgd       -4.55802e-15          2.52964e-17          2.00481e-17
        cgs         -4.493e-14         -2.36965e-15         -2.39635e-15
        csb       -1.08115e-14         -2.98619e-16         -3.05644e-16

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device            m.xm1.m0             m.xm0.m0
      model         nmos_3p3.8           nmos_3p3.8
         id              2e-05                2e-05
        vgs           0.805788             0.790787
        vth           0.673713             0.664441
        vds           0.451001              0.89768
      vdsat           0.164544             0.160739
         gm        0.000196097          0.000199096
        gds        5.49551e-06          4.22893e-06
       gmbs        5.35701e-05          5.40377e-05
        cdb       -2.67481e-16         -2.61376e-16
        cgd        1.43821e-17          1.94041e-17
        cgs       -2.34049e-15         -2.31133e-15
        csb       -3.98066e-16          -3.9154e-16
```

- PS. I change the code to make Vth before Vds to make Vds before Vdsat to make it easier to notice is that in saturation or not.

6. Putting the OP of all transistors in a table with the appropriate units

device	M0	M1	M2	M3	M4
id	*20 µA*	*20 µA*	*20 µA*	*20 µA*	*20 µA*
vgs	*796.84 mV*	*812.11 mV*	*908.43 mV*	*1361.08 mV*	*896.59 mV*
vth	*670.42 mV*	*679.97 mV*	*773.82 mV*	*653.73 mV*	*767.49 mV*
vds	*903.73 mV*	*455.52 mV*	*447.22 mV*	*464.47 mV*	*896.58 mV*
vdsat	*160.81 mV*	*164.62 mV*	*168.06 mV*	*548.63 mV*	*164.39 mV*
gm	*199.01 µS*	*196.05 µS*	*195.44 µS*	*46.13 µS*	*198.5 µS*
Gds	*4.22 µS*	*5.46 µS*	*5.86 µS*	*12.17 µS*	*4.56 µS*
Gmbs	*54.01 µS*	*53.56 µS*	*40.85 µS*	*17.85 µS*	*40.91 µS*
Cdb	*-261.37 aF*	*-267.42 aF*	*-205.29 aF*	*-8148.73 aF*	*-198.89 aF*
Cgd	*19.42 aF*	*14.58 aF*	*19.9 aF*	*-4302.41 aF*	*25.34 aF*
Cgs	*-2.31 fF*	*-2.34 fF*	*-2.4 fF*	*-44.98 fF*	*-2.37 fF*
Csb	*-391.54 aF*	*-398.05 aF*	*-304.88 aF*	*-10793.8 aF*	*-298.05 aF*
1.2*vdsat	*192.98 mV*	*197.54 mV*	*201.67 mV*	*658.36 mV*	*197.27mV*

7. Check that all transistors operate in saturation. **Check $V_{DS} > V_{dsat}*1.2$**
- For M0: ***903.73 mV > 192.98 mV*** then it's in **Saturation**
- For M1: ***455.52 mV > 197.54 mV*** then it's in **Saturation**
- For M2: ***447.22 mV > 201.67 mV*** then it's in **Saturation**
- For M3: ***464.47 mV < 658.36 mV*** then it's in **Triode**
- For M4: ***896.58 mV > 197.27 mV*** then it's in **Saturation**
  - M3 works in triode: as M3 has low aspect ratio than any other NMOS it has higher V_{GS} =*1361.08 mV* than anyone, so it has higher $V_{ov} \approx V_{dsat}$*1.2=658.36 mV* too and as M4 is diode connected and suffer from body effect, so it has high $V_{th,}$ so it consumes *896.59 mV* from V_{GSQ3} and let *1361.08-896.59=464.49mV* and it's less than V_{ov} to make M3 work in saturation

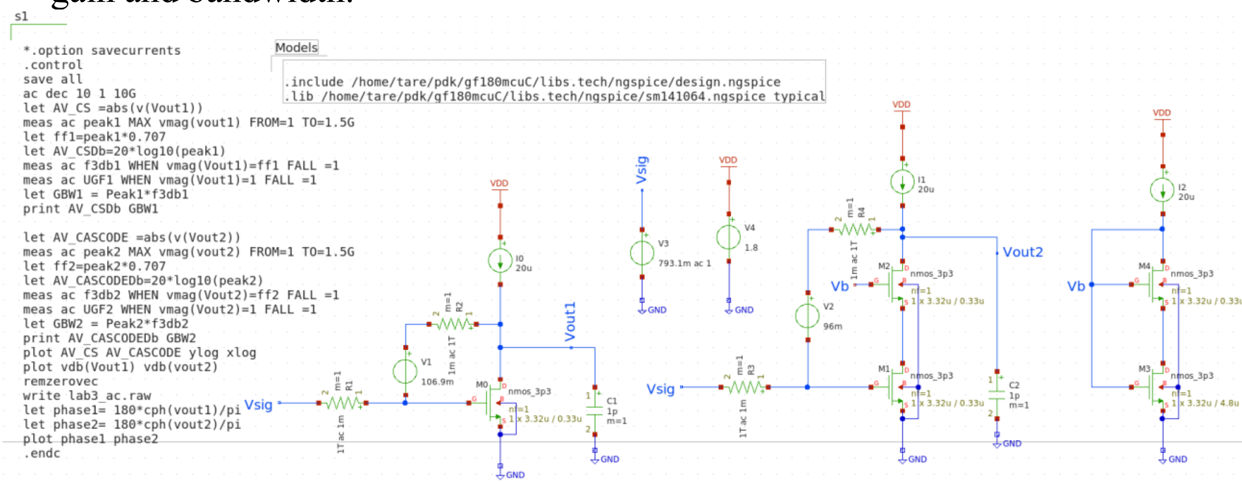
8. Approximately, M0, M1 and M3 has the same V_{th} but M4 and M2 has higher V_{th} because they suffer from body effect as there are a voltage difference between their source and body terminal.
- As M0 and M1 has the same V_{th} and has the same I_D and aspect ratio they have the same V_{GS}

9. In all transistor gm≫gds. But for M3:gm> gds because it is on triode and has low ro and then high gds

10. In all transistor gm>gmb as gmb/gm ≈ .3-.4
11. In all transistor |cgs|≫|cgd| as
12. In all transistor |csb| > |cdb| as |cdb|/ |csb| ≈ .67

2. AC Analysis

1. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.

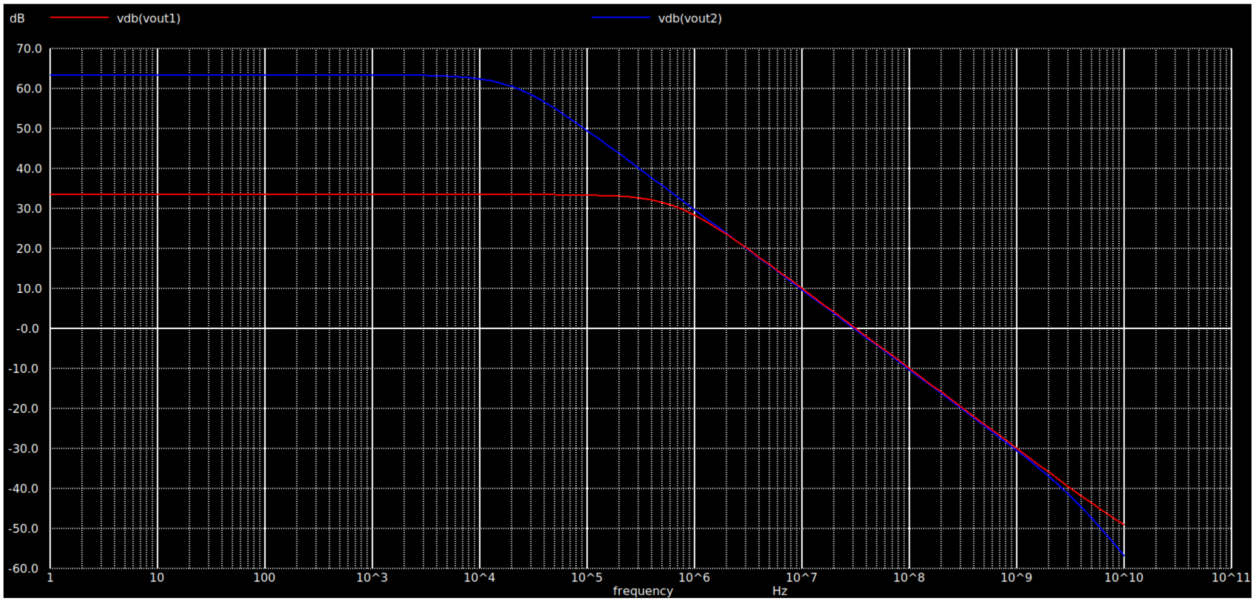


2. expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to interactive.

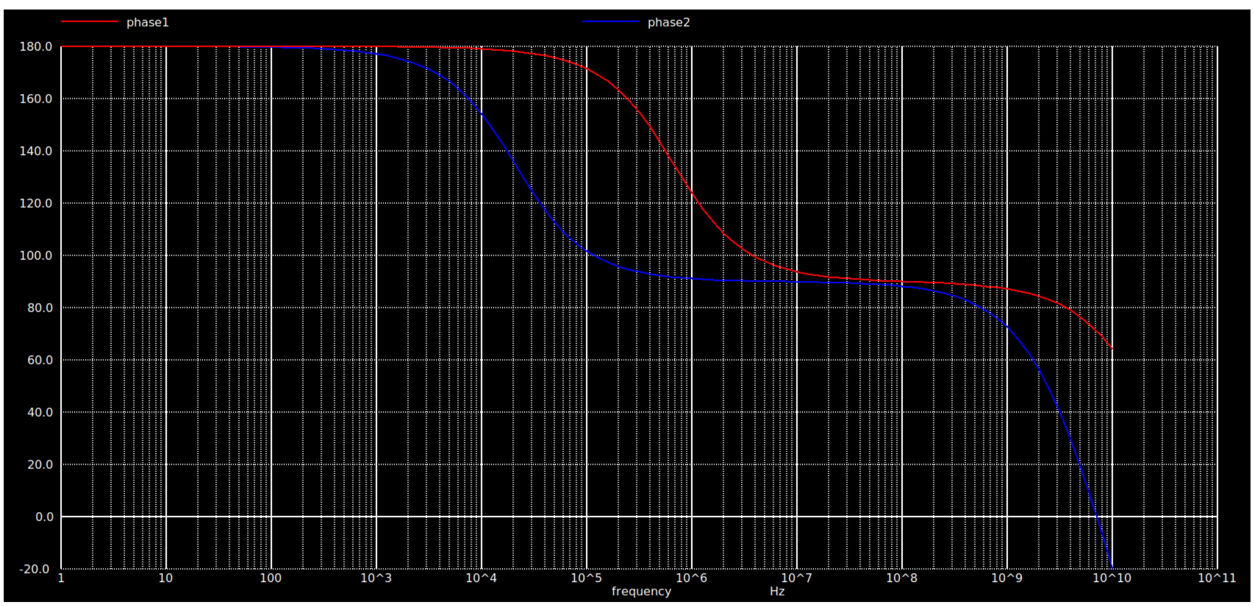
```
peak1                   =  4.723033e+01 at=  1.000000e+00
f3db1                   =  6.701949e+05
ugf1                    =  3.156219e+07
av_csdb = 3.348442e+01
gbw1 = 3.165353e+07
peak2                   =  1.507056e+03 at=  1.000000e+00
f3db2                   =  2.016317e+04
ugf2                    =  3.057482e+07
av_cascodedb = 6.356259e+01
gbw2 = 3.038703e+07
```

3. Bode plot (magnitude) of CS and cascode appended on the same plot.

3.1. Magnitude



3.2. Phase



4. Dc gain for Common source(M0) amplifier = $-\frac{gm}{1+(gm+gmb)Rs} * ro = -\frac{gm}{gds}$

=*-199.01 µS/ 4.22 µS* =-47.16

- Dc gain for Cascode amplifier == $-\frac{gm1}{1+(gm1+gmb1)Rs2} * ro1 *$

$(gm2 + gmb2)ro2 = -\frac{gm1}{gds1} * \frac{gm2+gmb2}{gds2} = -1481.3$

- Bandwidth for CS Amplifier as from the bode plot we can notice that the output pole is the dominant $fc = \frac{1}{2\pi Rout(CL+Cdb+Cgd)} = \frac{1}{2\pi(263.97e3(1e-12+19.42e-18+261.37e-18))} = 603\ Khz$
- For Cascode Amplifier the output pole is the dominant
- $fc = \frac{1}{2\pi Rout(CL+Cdb+Cgd)} = \frac{1}{2\pi(7.56e6(1e-12+19.9e-18+205.29e-18))} = 21khz$
- GainBandWidth Product for CS, $GBW = fc * Av = 603 * 10^3 * 47.16 = 28.44 * 10^6$
- GainBandWidth Product for Cascode, $GBW = fc * Av = 21 * 10^3 * 1481 = 28.44 * 10^6 = 31 * 10^6$
- Unity gain frequency $UGF = GBW$

5. table comparing the DC gain, BW, UGF, and GBW of CS Amplifier.

CS Amplifier	DC gain	BW	UGF	GBW
Simulation	47.23	670.19 kHz	31.56 MHz	31.65 MHz
Analytical	47.16	603 kHz	28.44 MHz	28.44 MHz

- table comparing the DC gain, BW, UGF, and GBW of Cascode Amplifier

Cascode Amplifier	DC gain	BW	UGF	GBW
Simulation	1507	21.16 kHz	30.57 MHz	30.39 MHz
Analytical	1481	21 kHz	31 MHz	31 MHz

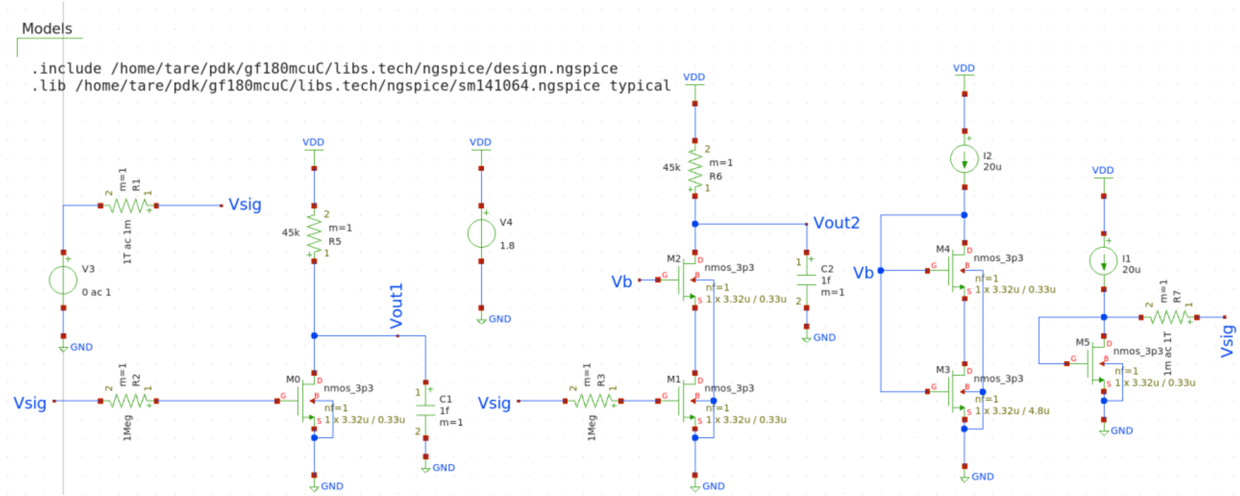
6. we notice that GBW for CS and Cascode are approximately the same as Cascode amplify the Rout but reduce the Bandwidth

- we see that cascode amplifier has very high gain but less bandwidth
- the cascode has less swing for output and must bias V_B to has value bigger than $V_{ov1} + V_{ov2} + V_{th2}$

Part 3: "Optional" Cascode for BW

1. OP Analysis

1. Create new schematic



2. Calculate R_D analytically such that the voltage drop on it is $\approx VDD/2$ (the current remains roughly the same as in Part 2 because we are using the VGS generated by M5)

3. Simulate the DC OP point of the new CS and cascode amplifiers.

```
igain0 = 4.403117e+01
igain1 = 1.580814e+03
binary raw file "lab3.raw"
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device            m.xm3.m0             m.xm5.m0             m.xm4.m0
      model        nmos_3p3.10          nmos_3p3.8           nmos_3p3.8
         id              2e-05                2e-05                2e-05
        vgs            1.36366             0.803448             0.899981
        vds           0.463659             0.803441             0.899974
        vth           0.655911             0.675868             0.770838
      vdsat           0.548938             0.161599             0.164434
         gm          4.602e-05          0.000198559          0.000198448
        gds        1.23028e-05          4.33626e-06          4.55847e-06
       gmbs        1.78233e-05          5.39715e-05          4.09126e-05
        cdb       -8.16058e-15         -2.62358e-16         -1.98966e-16
        cdg       -2.00346e-14         -9.48214e-16         -9.57814e-16
        cgs         -4.497e-14         -2.31725e-15         -2.36981e-15
        csb       -1.07937e-14         -3.92847e-16         -2.98047e-16

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device            m.xm2.m0             m.xm1.m0             m.xm0.m0
      model         nmos_3p3.8           nmos_3p3.8           nmos_3p3.8
         id        1.88613e-05          1.88613e-05          2.34426e-05
        vgs           0.903329             0.803449             0.803447
        vds           0.490903             0.460312             0.745066
        vth           0.775275             0.677347             0.659037
      vdsat            0.16365             0.160586             0.172757
         gm        0.000189593          0.000189808          0.000216885
        gds         5.3144e-06          5.17462e-06          4.92571e-06
       gmbs        3.94414e-05          5.18304e-05          5.90354e-05
        cdb       -2.02031e-16         -2.65133e-16         -2.68353e-16
        cdg       -9.61542e-16         -9.52201e-16         -9.71288e-16
        cgs       -2.37211e-15          -2.3181e-15         -2.37788e-15
        csb       -3.01172e-16         -3.94816e-16          -4.0164e-16
```

- PS) I change the order and make Vth before Vds and vdsat

4. From figure above we can notice that vds>vdsat for all transistor but M3 which has vds<vdsat so all transistor work in saturation but M3 works in triode

- M3 works in triode: as M3 has low aspect ratio than any other NMOS it has higher V_{GS} than anyone, so it has higher $V_{ov} \approx V_{dsat}*1.2=658.78\ mV$ too and as M4 is diode connected and suffer from body effect, so it has high $V_{th,}$ so it consumes $900.76\ mV$ from V_{GSQ3} and let $1364.44-900.76=463.68mV$ and it's less than V_{ov} to make M3 work in saturation

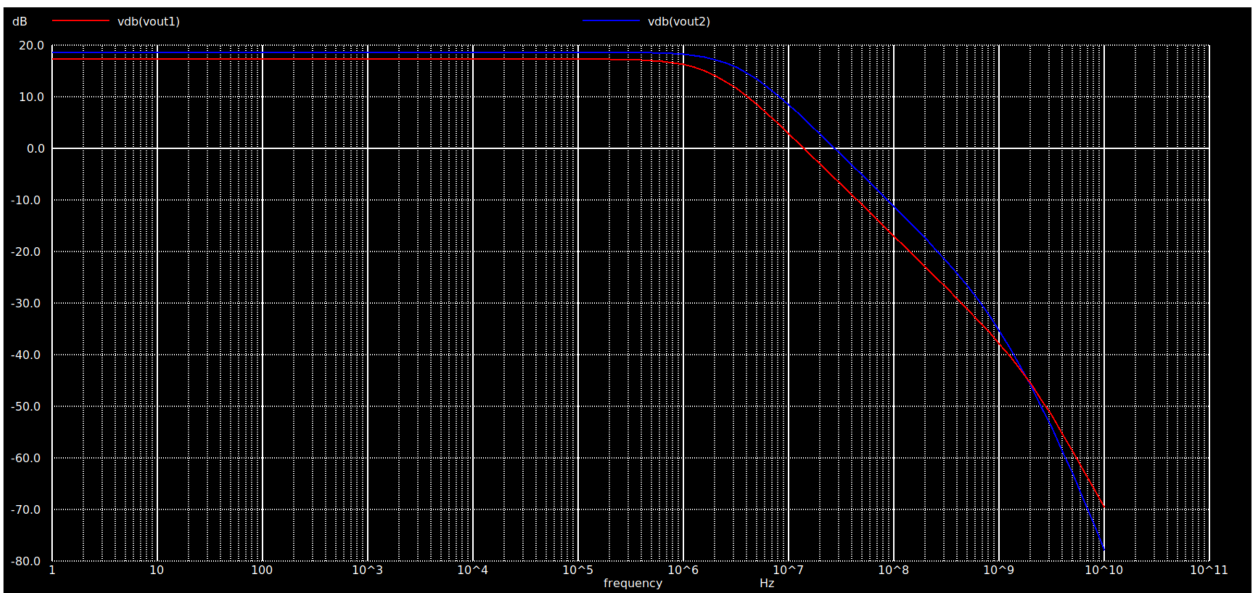
2. AC Analysis

1. Performing AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth

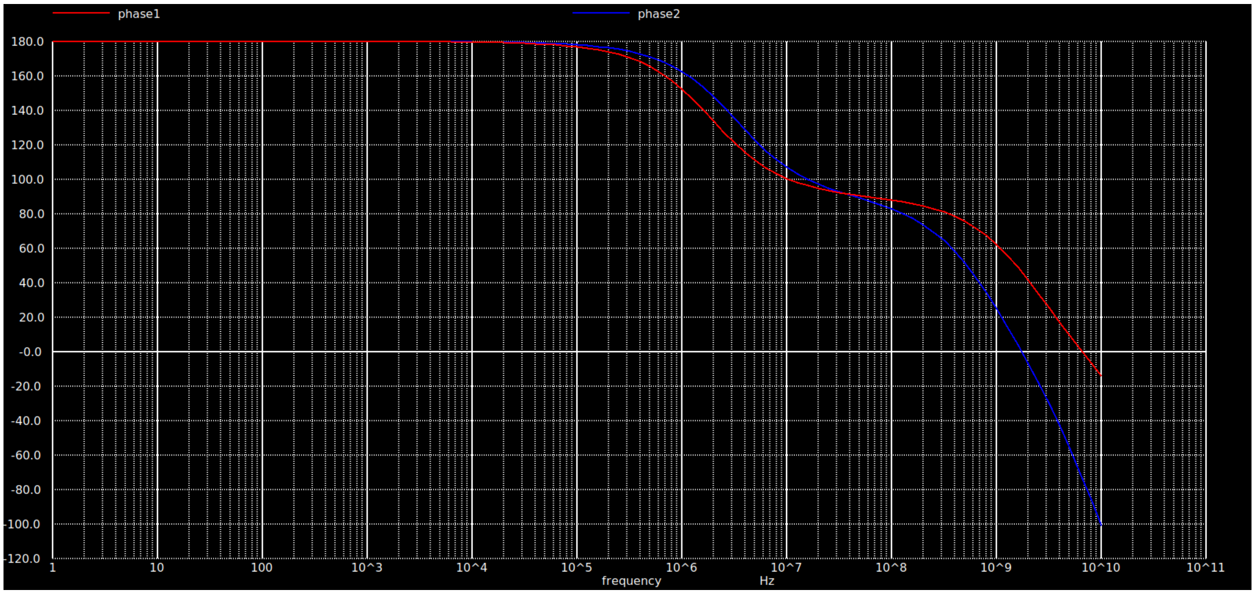
2. create expressions for circuit parameters (DC gain, BW, GBW, and UGF)

```
peak1                    =  7.341043e+00 at=  1.000000e+00
f3db1                    =  1.928633e+06
ugf1                     =  1.418322e+07
av_csdb = 1.731516e+01
gbw1 = 1.415818e+07
peak2                    =  8.551252e+00 at=  1.000000e+00
f3db2                    =  3.243251e+06
ugf2                     =  2.781260e+07
av_cascodedb = 1.864059e+01
gbw2 = 2.773386e+07
```

3. Bode plot (magnitude) of CS and cascode **appended on the same plot**.
   3.1. magnitude



3.2. phase



4. Dc gain for Common source(M0) amplifier = -gm/(1+(gm+gmb)Rs)*(ro||R_D) =-gm*(R_D||1/gds) =-7.77

- Dc gain for Cascode amplifier = $gm1 * (ro2 * (1 + (gm2 + gmb2)ro1)||RD \approx -gm1 * RD = -8.67$
- Bandwidth for CS Amplifier as from the bode plot we can notice that the input pole is the dominant $fc = \frac{1}{2\pi Rin((1+Av)cdg+cgs)} = 1.46MHz$
- For Cascode Amplifier the output pole is the dominant

$$fc = \frac{1}{2\pi Rin(2cdg1 + cgs1)} = 3.77\ MHz$$

- GainBandWidth Product for CS, $GBW = fc * Av = 11.34\ MHz$
- GainBandWidth Product for Cascode, $GBW = fc * Av = 32.69\ MHz$
- Unity gain frequency $UGF = GBW$

5. table comparing the DC gain, BW, UGF, and GBW of CS Amplifier.

CS Amplifier	DC gain	BW	UGF	GBW
Simulation	7.34	1.93 MHz	14.18 MHz	14.16 MHz
Analytical	7.77	1.46 MHz	11.34 MHz	11.34MHz

- table comparing the DC gain, BW, UGF, and GBW of Cascode Amplifier.

Cascode Amplifier	DC gain	BW	UGF	GBW
Simulation	8.55	3.24 MHz	27.81 MHz	27.73 MHz
Analytical	8.67	3.77 MHz	32.69 MHz	32.69MHz

6. we notice that GBW for Cascode bigger than CS amplifier when input pole is dominant, and they are equal when the output pole is dominant

- we see that cascode amplifier has slightly higher gain than CS because of the high increase in Rout and high Bandwidth because of the cascode decrease miller effect in the input capacitance
- as the input pole has lower value than the output pole in part 2 the bandwidth in part 3 is less than the bandwidth in part 2