ITI CMOS Analog IC Design 2024
Lab 02
Common Source Amplifier

PART 1: Sizing Chart

1. The specs we want to achieve for common source amplifier.

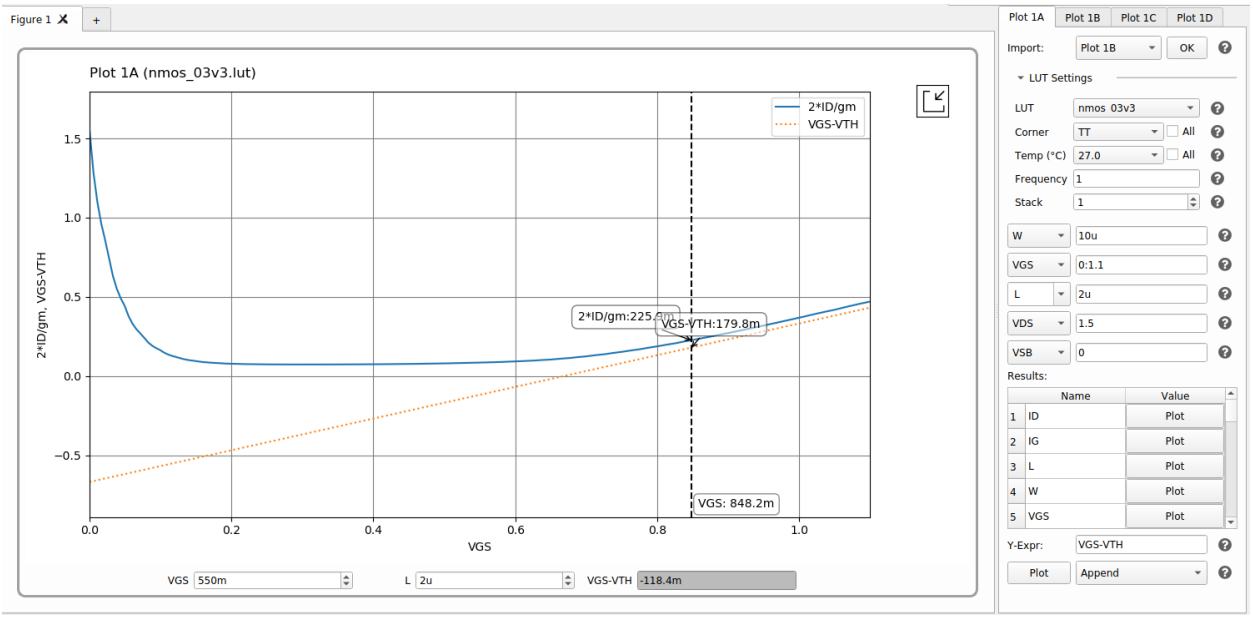
spec	Value
DC gain	**-8**
Supply	**1.8 V**
Current consumption	**100µA**

2. we will assume that L=2 µm for get high r_o and avoid short channel effect
3. $|A_v| \approx gm*R_D = 2I_D*R_D/V_{ov} = 2V_{RD}/V_{ov}$

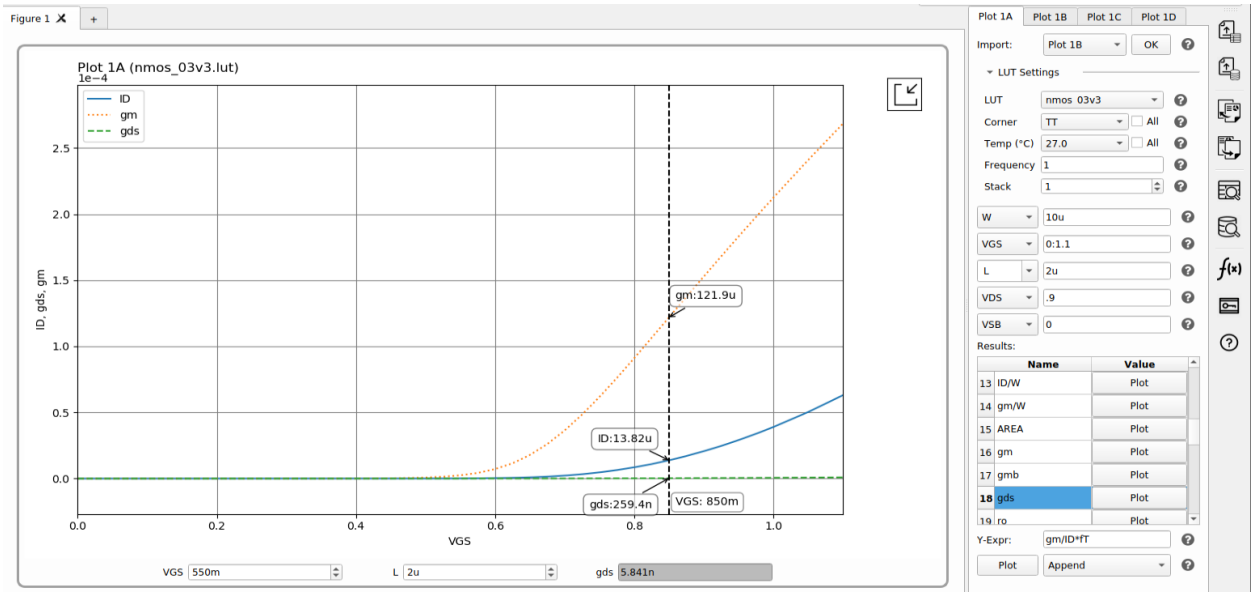
- As $V_{ov} \neq 2I_D/gm$ in real MOSFET so we define $V^* = 2I_D/gm$

4. We make V_{RD}= VDD/2 to get the high swing so V_{RD} =1.8/2=.9 V
   I_D*R_D =.9 V and I_D=100 µA then R_D = 9 KΩ
5. then 2 V_{RD}/V_Q^* =8 then V_Q^*= 225mV
6. We use W=10 µm
7. As $V_{th} \approx 670\ mV$, so V_{th} +.4 ≈ 1.1V, so we sweep V_{GS} from *0mV to 1.1V*

8. Plot V_{ov} and V^* Vs V_{GS}



9. As we see that at $V_Q^* = 225.9\ mV$ that $V_{ovQ} = 179.8\ mV$ and $V_{GSQ} = 848.2\ mV$
10. Plot gm and I_D and gds



11.

@ W=10 μm and V_{GS} 850 mV and L=2 μm		
I_{DX}	*gmx*	*gdsx*
13.82μA	*121.9μS*	*259.4nS*

12. to get I_D = 100 *μA* we need W=72.35 *μm*

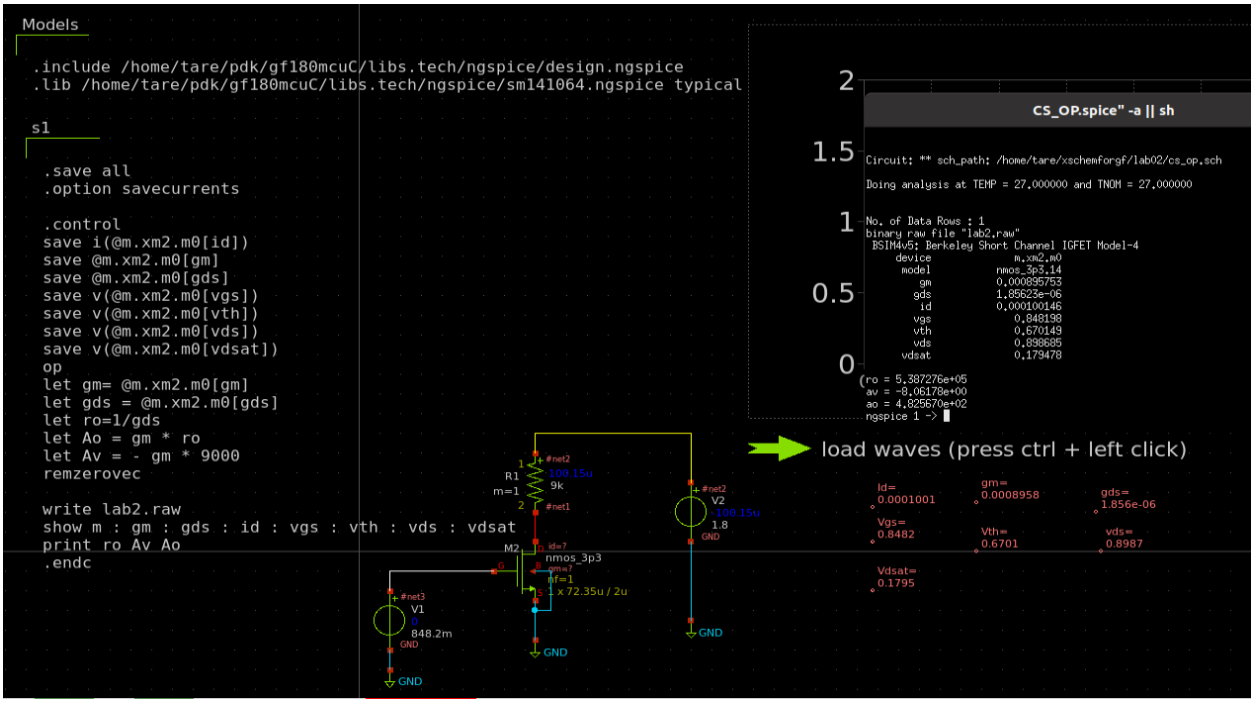
@ W=72.35 µm and V_{GS} = 850 mV and L=2 µm		
I_D	*gm*	*gds*
100µA	*881.95µS*	*1876.76nS*

13. then we have r_o =1/gds=532.83 kΩ

- so, A_V=-gm $R_D||r_o$ =-881.95*10^{-6}*(532.83 kΩ||9 kΩ)= -7.81
  so we meet the specs mentioned above

PART 2: CS Amplifier

1. **OP and AC Analysis**
   1. Createing a testbench for the resistive loaded CS amplifier



   2. Simulating the DC OP.

parameter	I_D	gm	gds
Simulation	*100.1µA*	*895.8 µS*	*1.856 µS*
Sizing Chart	*100 µA*	*881.95µS*	*1876.76 nS*

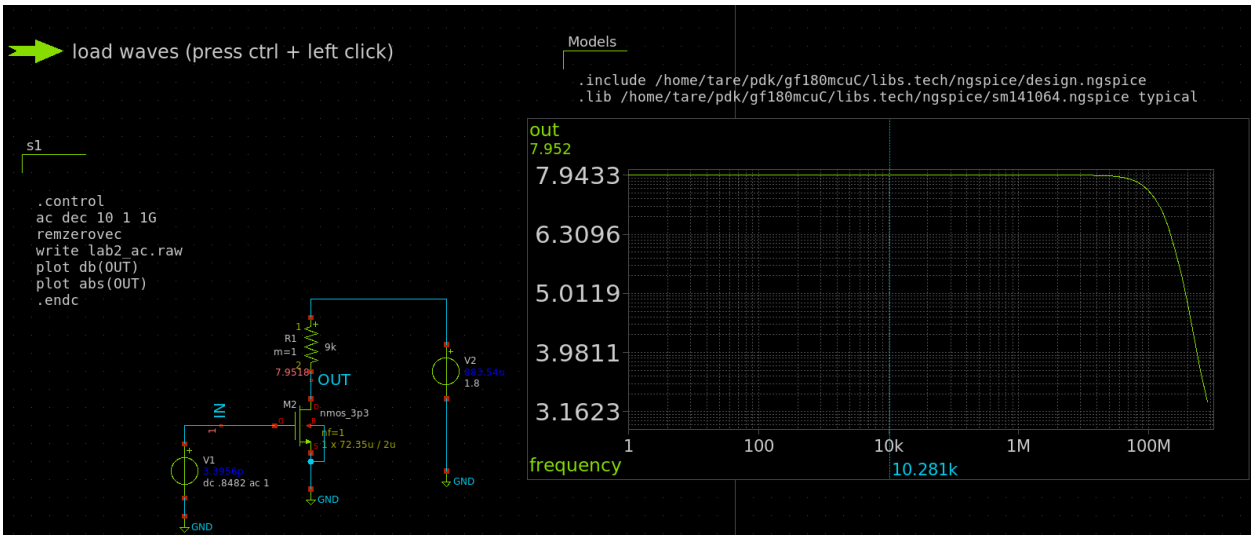
- The two value are approximately equal.

3. r_o = 538.8kΩ, so r_o/R_D = 59.87 then $r_o \gg R_D$ so $r_o||R_D \approx R_D$

- we can ignore r_o in our case
- $r_o \propto$ L so as L decrease r_o decrease and this will affect the gain of the circuit.

4. intrinsic gain equal gm*r_o =gm/gds =895.8µS/1.856 µS =482.65
5. the gain of this circuit equal $-\frac{gm}{1+(gm+gmb)Rs} * ro||R_D$

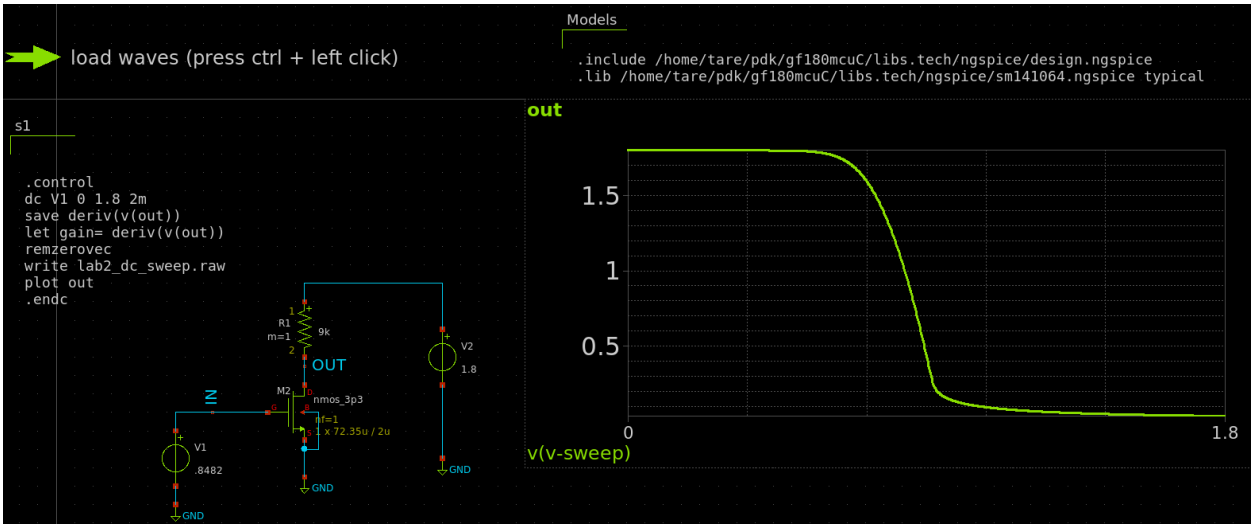
- there are no body effect and no Rs then gain equal -gm*r_o||R_D
  = -*895.8* µS *(538.8kΩ ||9 kΩ) =-7.93
- we notice that gm*r_o≫ gm*r_o||R_D



6. when applying ac voltage =1 V we get output voltage =7.952V this mean we have dc gain equal 7.952

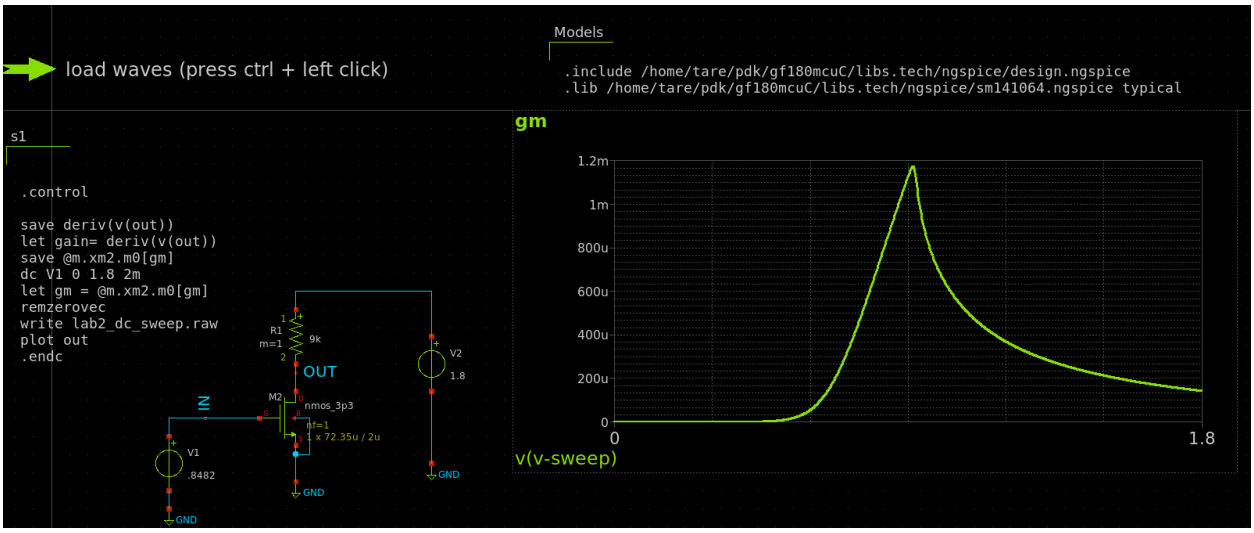
2. Gain Non-Linearity

1. Performing a DC sweep for the input voltage from 0 to VDD with 2mV step.
2. V_{OUT} vs V_{IN}

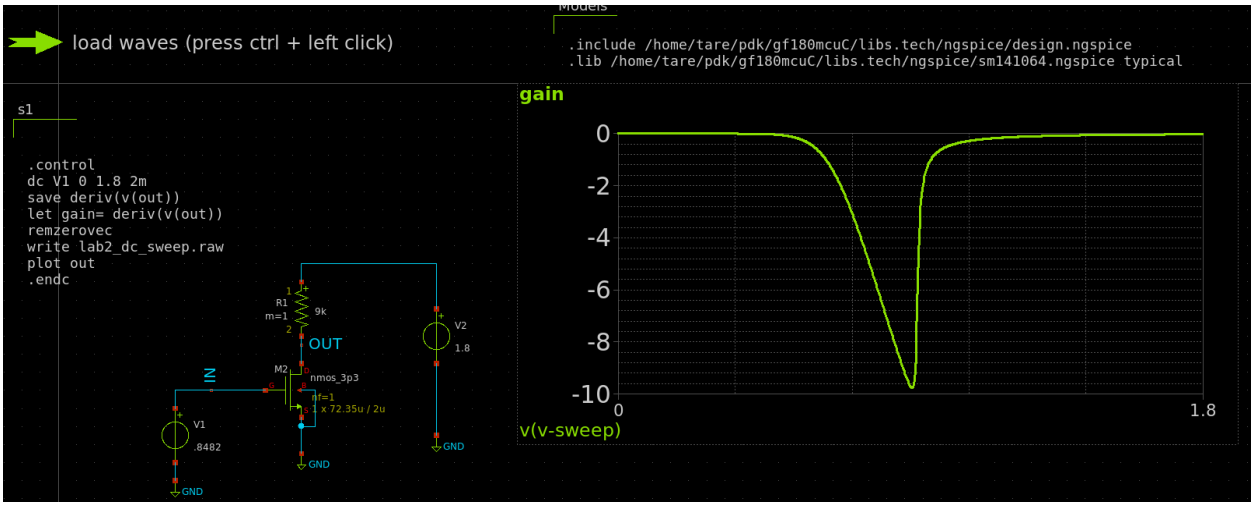


- We see that the relation is not linear there are three region

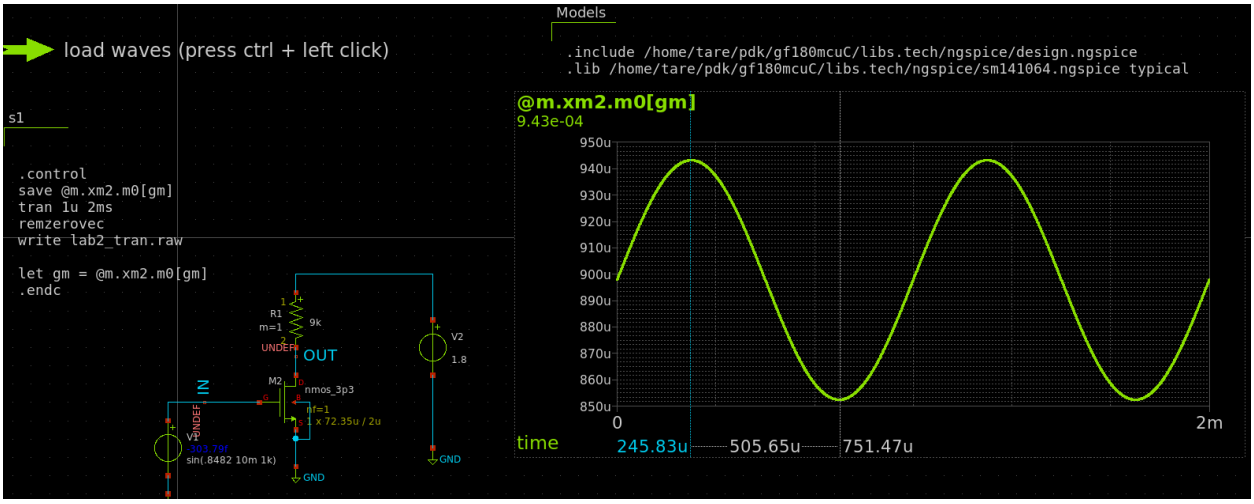
- first one the transistor is still off so V_{out} is constant and equal VDD =1.8V



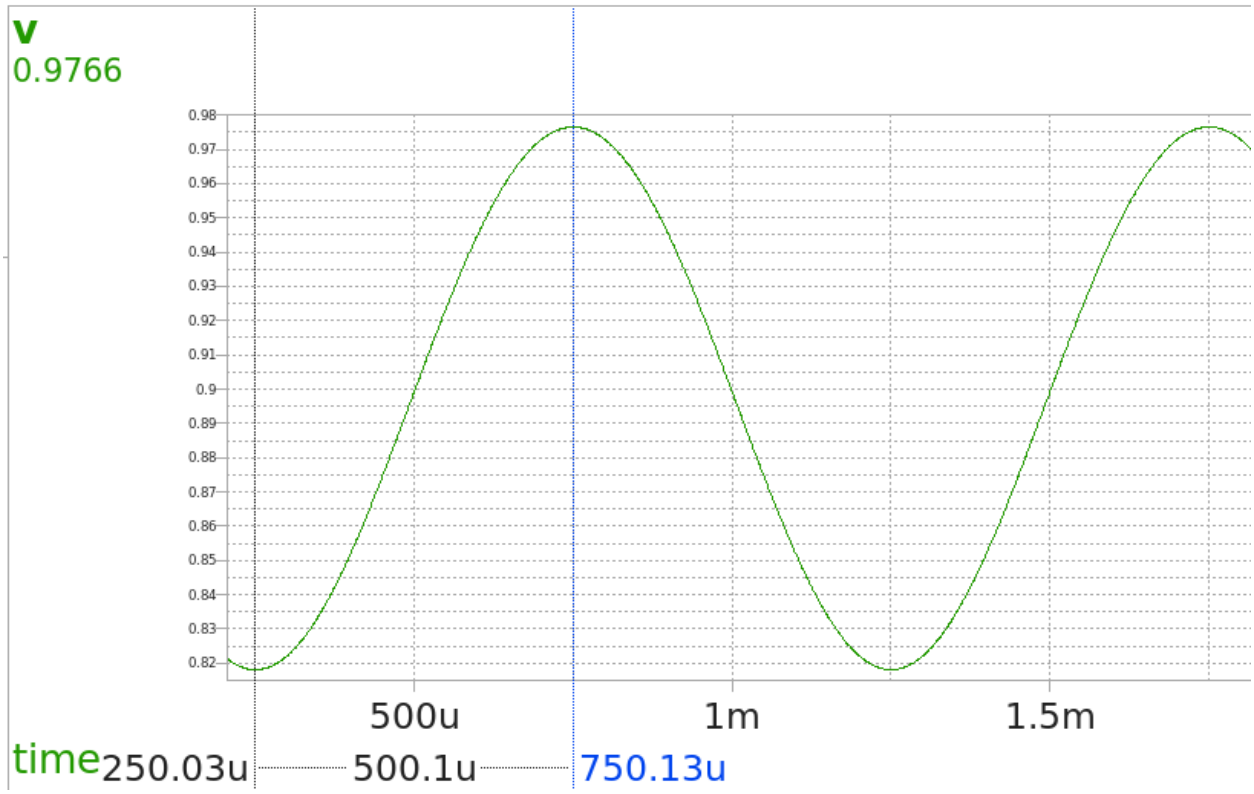
- second one is the satouration region and the MOSFET amplify the signal and it is not linear because gm changing with changing of the input voltage.
- third one is the the triode region and the V_{out} equal aprroximately 0



3. gain isn't linear because it depend on gm and gm∝V_{in} as W/L is constant. From the gm Vs Vin grap $\Delta gm = 943 - 851 = 92\ \mu S$



4. the peak to peak V_{out} =976.6-818.1= 158.5mV and peak to peak V_{in}= 20mV so dc gain =158.5/20=7.925



5. gm vary with the input signal as gm∝V_{in} that mean the gain isn't linear but it varying slightly with the input voltage.
6. The amplifier isn't typicaly linear but it vary with the input signal.

- From Vout Vs time figure above we can think it idle sine wave but its down peak bigger than the up peak because down peak from the output come from the up peak of the imput and up peak has bigger gm and bigger amplification
- Biasing Vds voltage =1.8-100.1µA*9kΩ=899.1 mV
- Down peak =899.1-818.1 =81 mV
- Up peak =976.6 -889.1=77.5mV