

SPARTAN-6 FPGA DSP48A1 SLICE

**UNDER SUPERVISION OF:
KAREEM_WASEEM**

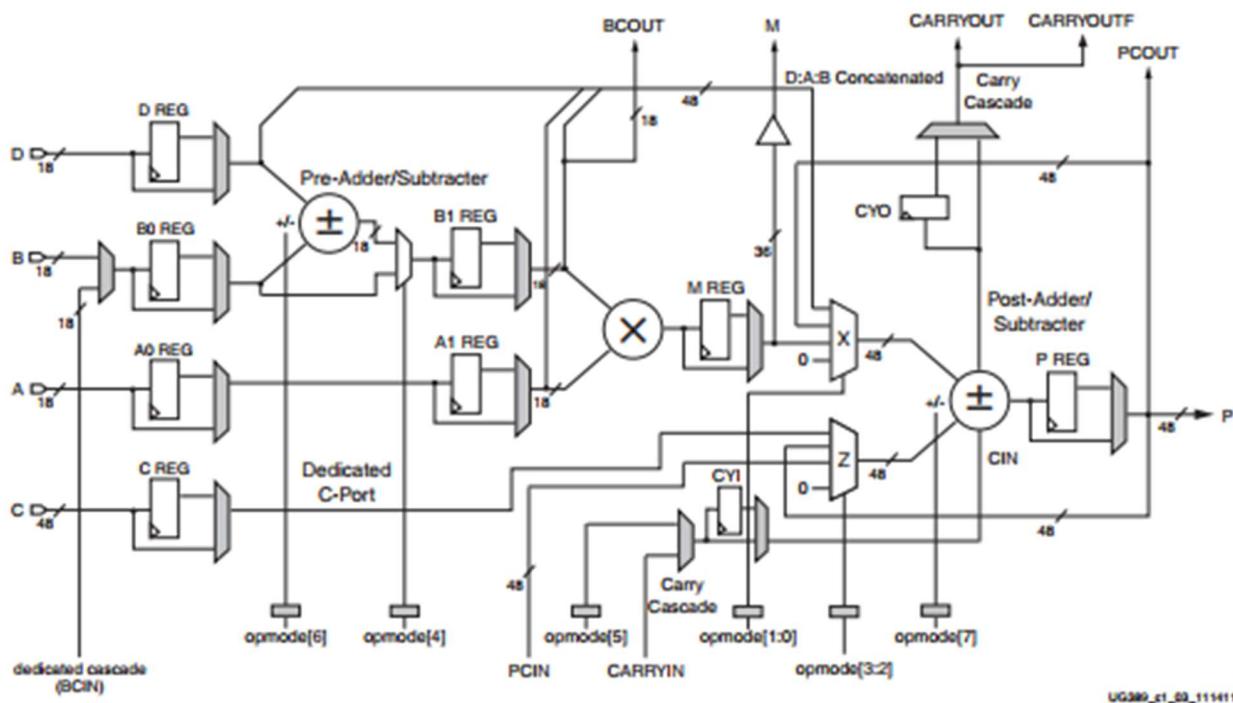
 **Mostafa Ahmed Productions**

**PREPARED BY:
MOSTAFA_AHMED_ESSA**

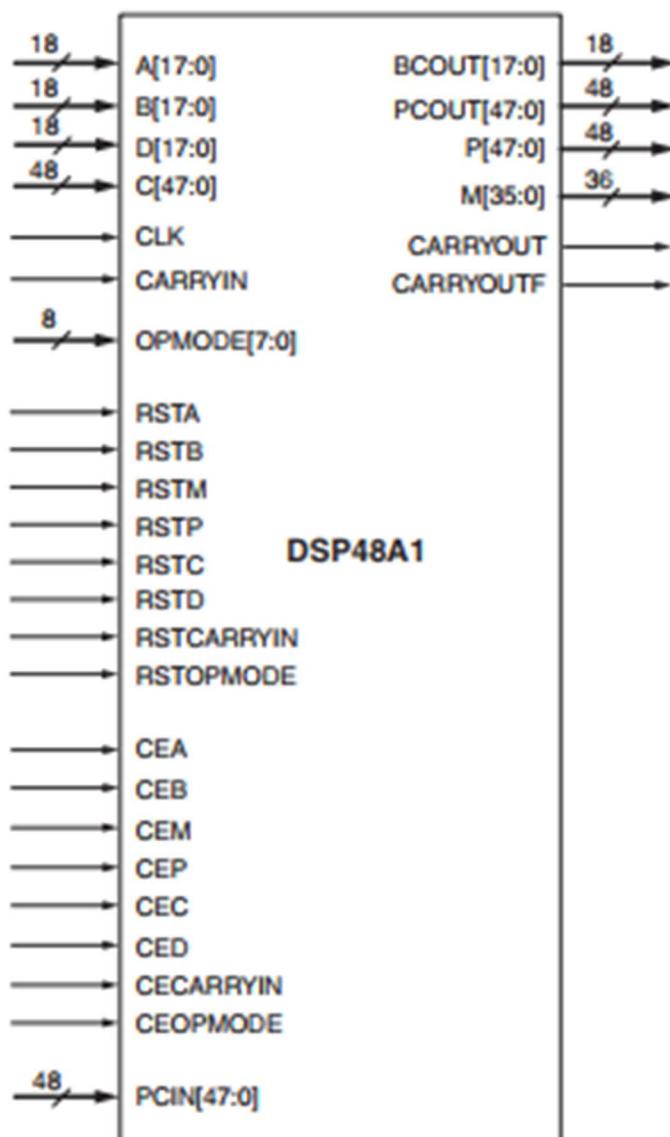
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UG389_c1_03_111411



RTL:

REG_MUX

```
● ● ●

1 module reg_mux(data,enable,rst,CLK,data_reg,REG);
2 parameter WIDTH=18;
3 parameter RST="SYNC";
4
5
6 input [WIDTH-1:0]data;
7 input CLK,rst,enable;
8 input REG;
9 output [WIDTH-1:0]data_reg;
10 reg [WIDTH-1:0]internal;
11
12 assign data_reg=(REG)?internal:data;
13
14 generate
15     if(RST=="ASYNC")begin
16         always@(posedge CLK or posedge rst)begin
17             if(rst) internal<=0;
18             else internal<=data;
19         end
20     end
21
22     if(RST=="SYNC") begin
23         always@(posedge CLK )begin
24             if(rst) internal<=0;
25             else internal<=data;
26         end
27     end
28 endgenerate
29
30
31 endmodule
32
```

DSP

```
 1 module DSP(A,B,C,D,CARRYIN,CLK,OPMODE,
 2 CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,
 3 RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP
 4 ,PCIN,CARRYOUT,CARRYOUTF,M,P,BCOUT,BCIN,PCOUT);
 5
 6 parameter A0REG=0;
 7 parameter B0REG=0;
 8 parameter A1REG=1;
 9 parameter B1REG=1;
10 parameter CREG=1;
11 parameter DREG=1;
12 parameter MREG=1;
13 parameter PREG=1;
14 parameter CARRYINREG=1;
15 parameter OPMODEREG=1;
16 parameter CARRYOUTREG=1;
17
18 parameter CARRYINSEL="OPMODE5";
19
20 parameter B_INPUT="DIRECT";
21
22 parameter RSTTYPE="SYNC";
23
24 input [17:0] A,B,D;
25 input [47:0]C,PCIN;
26 input [7:0]OPMODE;
27 input CLK,CARRYIN;
28 input [17:0] BCIN;
29 input RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
30 input CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP;
31 output [35:0]M;
32 output [47:0]P,PCOUT;
33 output [17:0]BCOUT;
34 output CARRYOUT,CARRYOUTF;
35
36
37 wire [17:0]A0_reg,B0_reg,D0_reg,A1_reg;
38 wire [17:0] B_Selected;
39 wire [47:0]C0_reg;
40 wire [7:0] opmode_reg;
41
42 wire [17:0]first_adder_reg;
43 reg [17:0] first_adder;
44
45 wire [35:0]multibly_reg;
46 reg [35:0]multibly;
47
48 wire carryin_reg;
49 reg carryin;
50
51 wire carryout_reg;
52 reg carryout;
53
54 wire [47:0] second_adder_reg;
55 reg [47:0] second_adder;
56
57 reg [47:0]x,z;
58
```

```

1 assign B_selected=(B_INPUT=="DIRECT")?B:(B_INPUT=="CASCADE")?BCOUT:0;
2 reg_mux #(.WIDTH(18),.RST(RSTTYPE)) A0 (.data(A),.enable(CEA),.rst(RSTA),.CLK(CLK),.REG(A0REG),.data_reg(A0_reg));
3 reg_mux #(.WIDTH(18),.RST(RSTTYPE)) B0 (.data(B_selected),.enable(CEB),.rst(RSTB),.CLK(CLK),.REG(B0REG),.data_reg(B0_reg));
4 reg_mux #(.WIDTH(48),.RST(RSTTYPE)) C0 (.data(C),.enable(CEC),.rst(RSTC),.CLK(CLK),.REG(C0REG),.data_reg(C0_reg));
5 reg_mux #(.WIDTH(18),.RST(RSTTYPE)) D0 (.data(D),.enable(CED),.rst(RSTD),.CLK(CLK),.REG(D0REG),.data_reg(D0_reg));
6 reg_mux #(.WIDTH(8),.RST(RSTTYPE)) opmode(.data(OPMODE),.enable(CEOPMODE),.rst(RSTOPMODE),.CLK(CLK),.REG(OPMODEREG),.data_reg(opmode_reg));
7
8
9 always@(*)begin
10    case(opmode_reg[4])
11        0: first_adder=B0_reg;
12        1:begin
13            if(opmode_reg[6]) first_adder=D0_reg-B0_reg;
14            else first_adder=D0_reg+B0_reg;
15        end
16    endcase
17 end
18
19 reg_mux #(.WIDTH(18),.RST(RSTTYPE)) B1 (.data(first_adder),.enable(CEB),.rst(RSTB),.CLK(CLK),.REG(B1REG),.data_reg(first_adder_reg));
20 reg_mux #(.WIDTH(18),.RST(RSTTYPE)) A1 (.data(A0_reg),.enable(CEA),.rst(RSTA),.CLK(CLK),.REG(A1REG),.data_reg(A1_reg));
21
22 assign BCOUT=first_adder_reg;
23
24 always@(*)begin
25    multibily=first_adder_reg*A1_reg;
26 end
27 reg_mux #(.WIDTH(36),.RST(RSTTYPE)) multiblication (.data(multibily),.enable(CEM),.rst(RSTM),.CLK(CLK),.REG(MREG),.data_reg(multibily_reg));
28 assign M=multibily_reg;
29
30 always@(*)begin
31    case(CARRYINSEL)
32        "OPMDES":carryin=opmode_reg[5];
33        "CARRYIN":carryin=CARRYIN;
34        default :carryin=0;
35    endcase
36 end
37 reg_mux #(.WIDTH(1),.RST(RSTTYPE)) carry_in (.data(carryin),.enable(CECARRYIN),.rst(RSTCARRYIN),.CLK(CLK),.REG(CARRYINREG),.data_reg(carryin_reg));
38
39
40 always@(*)begin
41    case(opmode_reg[1:0])
42        2'b00:x=0;
43        2'b01:x=multibily_reg;
44        2'b10:x=PCOUT;
45        2'b11:x={D0_reg[11:0],A1_reg,first_adder_reg};
46    endcase
47 end
48
49 always@(*)begin
50    case(opmode_reg[3:2])
51        2'b00:z=0;
52        2'b01:z=PCIN;
53        2'b10:z=PCOUT;
54        2'b11:z=C0_reg;
55    endcase
56 end
57
58 always@(*)begin
59    case(opmode_reg[7])
60        1:{carryout,second_adder}=z-(x+carryin_reg);
61        0:{carryout,second_adder}=z+x+carryin_reg;
62    endcase
63 end
64
65 assign PCOUT=P;
66 assign CARRYOUTF=CARRYOUT;
67
68 reg_mux #(.WIDTH(48),.RST(RSTTYPE)) secondadder (.data(second_adder),.enable(CEP),.rst(RSTP),.CLK(CLK),.REG(PREG),.data_reg(second_adder_reg));
69 reg_mux #(.WIDTH(1),.RST(RSTTYPE)) carryingout (.data(carryout),.enable(CECARRYIN),.rst(RSTCARRYIN),.CLK(CLK),.REG(CARRYOUTREG),.data_reg(carryout_reg));
70
71 assign P=second_adder_reg;
72 assign CARRYOUT=carryout_reg;
73
74 endmodule

```

TEST_BENCH:

```
1 module DSP_tb();
2
3 parameter A0REG=0;
4 parameter B0REG=0;
5 parameter A1REG=1;
6 parameter B1REG=1;
7 parameter CREG=1;
8 parameter DREG=1;
9 parameter MREG=1;
10 parameter PREG=1;
11 parameter CARRYINREG=1;
12 parameter OPMODEREG=1;
13 parameter CARRYOUTREG=1;
14
15 parameter CARRYINSEL="OPMODE5";
16
17 parameter B_INPUT="DIRECT";
18
19 parameter RSTTYPE="SYNC";
20
21 reg [17:0] A,B,D;
22 reg [47:0]C,PCIN;
23 reg [7:0]OPMODE;
24 reg CLK,CARRYIN;
25 reg [17:0] BCIN;
26 reg RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
27 reg CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP;
28
29 reg past_value_1_pcout ;
30 reg past_value_1_p ;
31 reg past_value_1_carryout ;
32 reg past_value_1_carryoutf ;
33
34 wire [35:0]M;
35 wire [47:0]P,PCOUT;
36 wire [17:0]BCOUT;
37 wire CARRYOUT,CARRYOUTF;
38
39 DSP #(A0REG(0),B0REG(0),A1REG(1),B1REG(1),CREG(1),DREG(1),MREG(1),PREG(1),CARRYINREG(1),OPMODEREG(1),CARRYOUTREG(1),
40 .CARRYINSEL("OPMODE5"),.B_INPUT("DIRECT"),.RSTTYPE("SYNC"))
41 DUT (A,B,C,D,CARRYIN,CLK,OPMODE,CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP,RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,
42 RSTOPMODE,RSTP,PCIN,CARRYOUT,CARRYOUTF,M,P,BCOUT,BCIN,PCOUT);
43
```

```

1 initial begin
2   CLK=0;
3   forever begin
4     #1 CLK=~CLK;
5   end
6 end
7
8 initial begin
9   $display("=====Test_RST=====");
10 RSTA=1;RSTB=1;RSTC=1;RSTCARRYIN=1;
11 RSTD=1;RSTM=1;RSTOPMODE=1;RSTP=1;
12 repeat(2)begin
13   A=$random;B=$random;C=$random;
14   D=$random;CARRYIN=$random;
15   CEA=$random;CEB=$random;CEC=$random;
16   CECARRYIN=$random;CED=$random;CEM=$random;
17   CEOPMODE=$random;CEP=$random;
18   OPMODE=$random;
19   @(negedge CLK);
20   if (P !== 0 || PCOUT !== 0 || CARRYOUT !== 0 || BCOUT !== 0 || M !== 0) $display("Error at -----(TEST_RESET)---- at time : %0t", $time);
21   else $display("CORRECT at -----(TEST_RESET)---- ");
22   #1;
23 end
24 $display("=====Test_RST=====");
25 separator();
26
27
28 $display("=====PATH____1=====");
29 RSTA=0;RSTB=0;RSTC=0;RSTCARRYIN=0;
30 RSTD=0;RSTM=0;RSTOPMODE=0;RSTP=0;
31 CEA=1;CEB=1;CEC=1;
32 CECARRYIN=1;CED=1;CEM=1;
33 CEOPMODE=1;CEP=1;
34 OPMODE=8 b1011101;
35 repeat(1)begin
36   A=18'd20;B=18'd10;C=48'd350;
37   D=18'd25;CARRYIN=$random;
38   PCIN=$random;BCIN=$random;
39   @(negedge CLK);
40   @(negedge CLK);
41   @(negedge CLK);
42   if (P !== 48'd50 || PCOUT !== 48'd50 || CARRYOUT !== 0 || CARRYOUTF !== 0 || BCOUT !== 18'd15 || M !== 36'd300) $display("Error at -----(PATH____1)---- at time : %0t", $time);
43   else $display("CORRECT at -----(PATH____1)---- ");
44   #1;
45 end
46 $display("=====PATH____1=====");
47 separator();
48
49
50 $display("=====PATH____2=====");
51 RSTA=0;RSTB=0;RSTC=0;RSTCARRYIN=0;
52 RSTD=0;RSTM=0;RSTOPMODE=0;RSTP=0;
53 CEA=1;CEB=1;CEC=1;
54 CECARRYIN=1;CED=1;CEM=1;
55 CEOPMODE=1;CEP=1;
56 OPMODE=8 b00010000;
57 repeat(1)begin
58   A=18'd20;B=18'd10;C=48'd350;
59   D=18'd25;CARRYIN=$random;
60   PCIN=$random;BCIN=$random;
61   @(negedge CLK);
62   @(negedge CLK);
63   @(negedge CLK);
64
65   assign past_value_1_p=P;
66   assign past_value_1_pcout=PCOUT;
67   assign past_value_1_carryout=CARRYOUT;
68   assign past_value_1_carryoutf=CARRYOUTF;
69
70   if (P !== 0 || PCOUT !== 0 || CARRYOUT !== 0 || CARRYOUTF !== 0 || BCOUT !== 18'd35 || M !== 36'd700) $display("Error at -----(PATH____2)---- at time : %0t", $time);
71   else $display("CORRECT at -----(PATH____2)---- ");
72   #1;
73 end
74 $display("=====PATH____2=====");
75 separator();
76
77 $display("=====PATH____3=====");
78 RSTA=0;RSTB=0;RSTC=0;RSTCARRYIN=0;
79 RSTD=0;RSTM=0;RSTOPMODE=0;RSTP=0;
80 CEA=1;CEB=1;CEC=1;
81 CECARRYIN=1;CED=1;CEM=1;
82 CEOPMODE=1;CEP=1;
83 OPMODE=8 b00001010;
84 repeat(1)begin
85   A=18'd20;B=18'd10;C=48'd350;
86   D=18'd25;CARRYIN=$random;
87   PCIN=$random;BCIN=$random;
88   @(negedge CLK);
89   @(negedge CLK);
90   @(negedge CLK);
91   if (P != past_value_1_p || PCOUT != past_value_1_pcout || CARRYOUT != past_value_1_carryout || CARRYOUTF != past_value_1_carryoutf || BCOUT != 18'd10 || M != 36'd200)
92   $display("Error at -----(PATH____3)---- at time : %0t", $time);
93   else $display("CORRECT at -----(PATH____3)---- ");
94   #1;
95 end
96 $display("=====PATH____3=====");
97 separator();

```

```

1 $display("=====PATH____2=====");
2 RSTA=0;RSTB=0;RSTC=0;RSTCARRYIN=0;
3 RSTD=0;RSTM=0;RSTOPMODE=0;RSTP=0;
4 CEA=1;CEB=1;CEC=1;
5 CECARRYIN=1;CED=1;CEM=1;
6 CEOPMODE=1;CEP=1;
7 OPMODE=8'b00010000;
8 repeat(1)begin
9 A=18'd20;B=18'd10;C=48'd350;
10 D=18'd25;CARRYIN=$random;
11 PCIN=$random;BCIN=$random;
12 @(posedge CLK);
13 @(posedge CLK);
14 @(posedge CLK);

15 assign past_value_1_p=P;
16 assign past_value_1_pcout=PCOUT;
17 assign past_value_1_carryout=CARRYOUT;
18 assign past_value_1_carryoutf=CARRYOUTF;
19
20 if (P !== 0 || PCOUT !== 0 || CARRYOUT !== 0 || CARRYOUTF !== 0 || BCOUT !== 18'd35 || M !== 36'd700) $display("Error at -----(PATH____2)---- at time : %0t", $time);
21 else $display("CORRECT at -----(PATH____2)---- ");
22 #1;
23 end
24 $display("=====PATH____2=====");
25 separator();
26

27 $display("=====PATH____3=====");
28 RSTA=0;RSTB=0;RSTC=0;RSTCARRYIN=0;
29 RSTD=0;RSTM=0;RSTOPMODE=0;RSTP=0;
30 CEA=1;CEB=1;CEC=1;
31 CECARRYIN=1;CED=1;CEM=1;
32 CEOPMODE=1;CEP=1;
33 OPMODE=8'b00001010;
34 repeat(1)begin
35 A=18'd20;B=18'd10;C=48'd350;
36 D=18'd25;CARRYIN=$random;
37 PCIN=$random;BCIN=$random;
38 @(posedge CLK);
39 @(posedge CLK);
40 @(posedge CLK);
41 if (P !== past_value_1_p || PCOUT !== past_value_1_pcout || CARRYOUT !== past_value_1_carryout || CARRYOUTF !== past_value_1_carryoutf || BCOUT !== 18'd10 || M !== 36'd200)
42 $display("Error at -----(PATH____3)---- at time : %0t", $time);
43 else $display("CORRECT at -----(PATH____3)---- ");
44 #1;
45 end
46 $display("=====PATH____3=====");
47 separator();
48

49 $display("=====PATH____4=====");
50 RSTA=0;RSTB=0;RSTC=0;RSTCARRYIN=0;
51 RSTD=0;RSTM=0;RSTOPMODE=0;RSTP=0;
52 CEA=1;CEB=1;CEC=1;
53 CECARRYIN=1;CED=1;CEM=1;
54 CEOPMODE=1;CEP=1;
55 OPMODE=8'b10100111;
56 repeat(1)begin
57 A=18'd5;B=18'd6;C=48'd350;
58 D=18'd25;CARRYIN=$random;
59 PCIN=3000;BCIN=$random;
60 @(posedge CLK);
61 @(posedge CLK);
62 @(posedge CLK);
63 if (P !== 48'hfe6fffec0bb1 || PCOUT !== 48'hfe6fffec0bb1 || CARRYOUT !== 1 || CARRYOUTF !== 1 || BCOUT !== 18'd6 || M !== 36'd30)
64 $display("Error at -----(PATH____4)---- at time : %0t", $time);
65 else $display("CORRECT at -----(PATH____4)---- ");
66 #1;
67 end
68 $display("=====PATH____4=====");
69 separator();
70
71 $stop;
72 end
73
74 task separator();begin
75 $display("=====-----=====");
76 end
77 endtask
78
79 endmodule

```

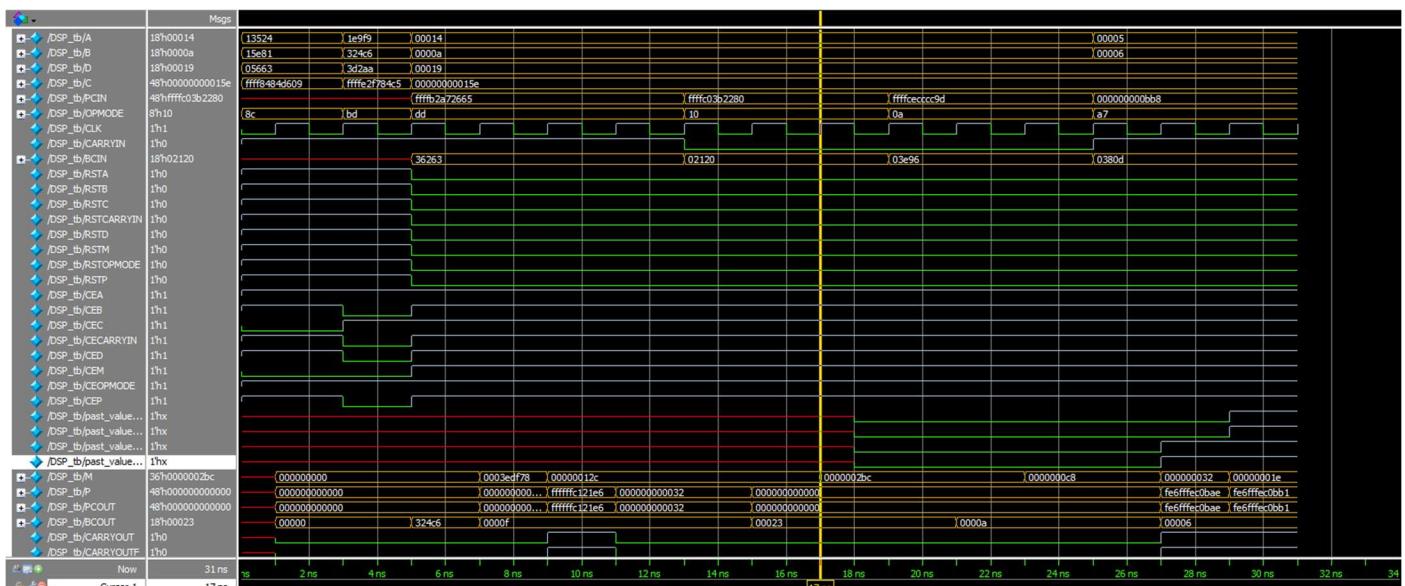
DOFILE:

```
1 vlib work
2 vlog reg_mux.v DSP_tb.v DSP.v
3 vsim -voptargs+=acc work.DSP_tb
4 add wave *
5 run -all
6 #quit -sim
```

TRANSCRIPT:

```
1 # =====Test_RST=====
2 # CORRECT at ----(TEST_RESET)-----
3 # CORRECT at ----(TEST_RESET)-----
4 # =====Test_RST=====
5 #
6 # =====PATH____1=====
7 # CORRECT at ----(PATH____1)-----
8 # =====PATH____1=====
9 #
10 # =====PATH____2=====
11 # CORRECT at ----(PATH____2)-----
12 # =====PATH____2=====
13 #
14 # =====PATH____3=====
15 # CORRECT at ----(PATH____3)-----
16 # =====PATH____3=====
17 #
18 # =====PATH____4=====
19 # CORRECT at ----(PATH____4)-----
20 # =====PATH____4=====
21 # =====
```

QUESTA_WAVE:



CONSTRAIN:

```

● ● ●

1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 ## Clock signal
7 set_property -dict { PACKAGE_PIN W5 IOSTANDARD LVCMOS33 } [get_ports CLK]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
9
10 ## Configuration options, can be used for all designs
11 set_property CONFIG_VOLTAGE 3.3 [current_design]
12 set_property CFGBVS VCCO [current_design]
13
14 ## SPI configuration mode options for QSPI boot, can be used for all designs
15 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
16 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
17 set_property CONFIG_MODE SPIx4 [current_design]

```

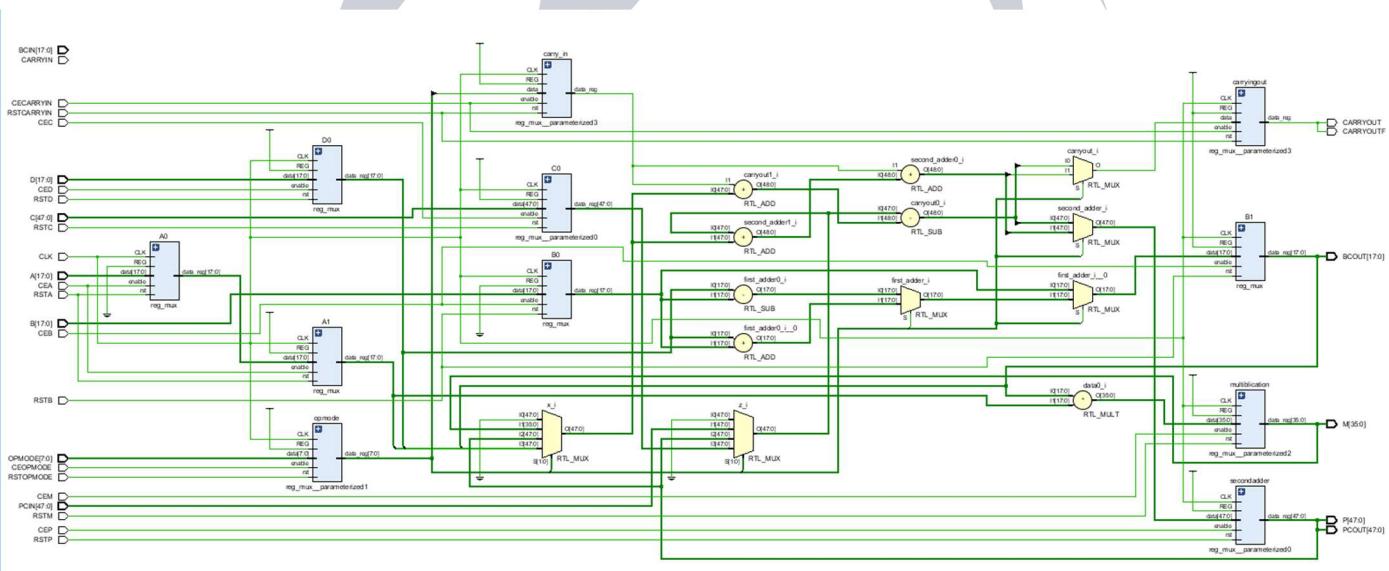
ELABORATION:

MESSAGES

✓ Elaborated Design (25 warnings, 31 infos)

- General Messages (25 warnings, 31 infos)
 - [Synth 8-6157] synthesizing module 'DSP' [DSP.v1] (5 more like this)
 - [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [reg_mux.v1] (5 more like this)
 - [Synth 8-3331] design reg_mux_parameterized3 has unconnected port enable (23 more like this)
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - [IP_Flow 19-1839] IP Catalog is up to date. (15 more like this)
 - [Filemgmt 56-12] File 'D:/Courses/K.Waseem/Projects/Project_1/questa/reg_mux.v' cannot be added to the project because it already exists in the project, skipping this file

SCHEMATIC



SYNTHESIS:

MESSAGES

- ✓ Synthesized Design (10 infos)
 - ✓ General Messages (10 infos)
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - > ⓘ [Timing 38-35] Done setting XDC timing constraints. (3 more like this)
 - ⓘ [DRC 23-133] Running Methodology with 2 threads
 - ⓘ [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max, Timing Stage: Requireds.
 - ⓘ [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs
 - ⓘ [Timing 38-480] Writing timing data to binary archive.

- ✓ Synthesis (70 warnings, 44 infos)
 - ⓘ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
 - > ⓘ [Synth 8-6157] synthesizing module 'DSP' [DSP.v:1] (5 more like this)
 - > ⓘ [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [reg_mux.v:1] (5 more like this)
 - > ⓘ [Synth 8-3331] design reg_mux_parameterized3 has unconnected port enable (50 more like this)
 - ⓘ [Device 21-403] Loading part xc7a200tfg1156-3
 - ⓘ [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP.v:71]
 - > ⓘ [Synth 8-3886] merging instance 'A0/internal_reg[0]' (FDR) to 'A1/internal_reg[0]' (17 more like this)
 - > ⓘ [Synth 8-3332] Sequential element (B0/internal_reg[17]) is unused and will be removed from module DSP. (17 more like this)
 - ⓘ [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [DSP.v:83]
 - ⓘ [Project 1-571] Translating synthesized netlist
 - ⓘ [Netlist 29-17] Analyzing 212 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

UTILIZATION_REPORT

Utilization Tcl Console Messages Log Reports Design Runs Methodology Timing

Hierarchy Summary Slice Logic Memory DSP IO and GT Specific

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP	255	160	1	319	1
A1 (reg_mux)	0	18	0	0	0
B1 (reg_mux_0)	1	18	0	0	0
C0 (reg_mux_param...)	0	48	0	0	0
carry_in (reg_mux_pa...)	0	1	0	0	0
carryingout (reg_mux_...)	0	1	0	0	0
D0 (reg_mux_1)	18	18	0	0	0
opmode (reg_mux_p...)	236	8	0	0	0
secondadder (reg_mu...)	0	48	0	0	0

utilization_1 utilization_2 utilization_3

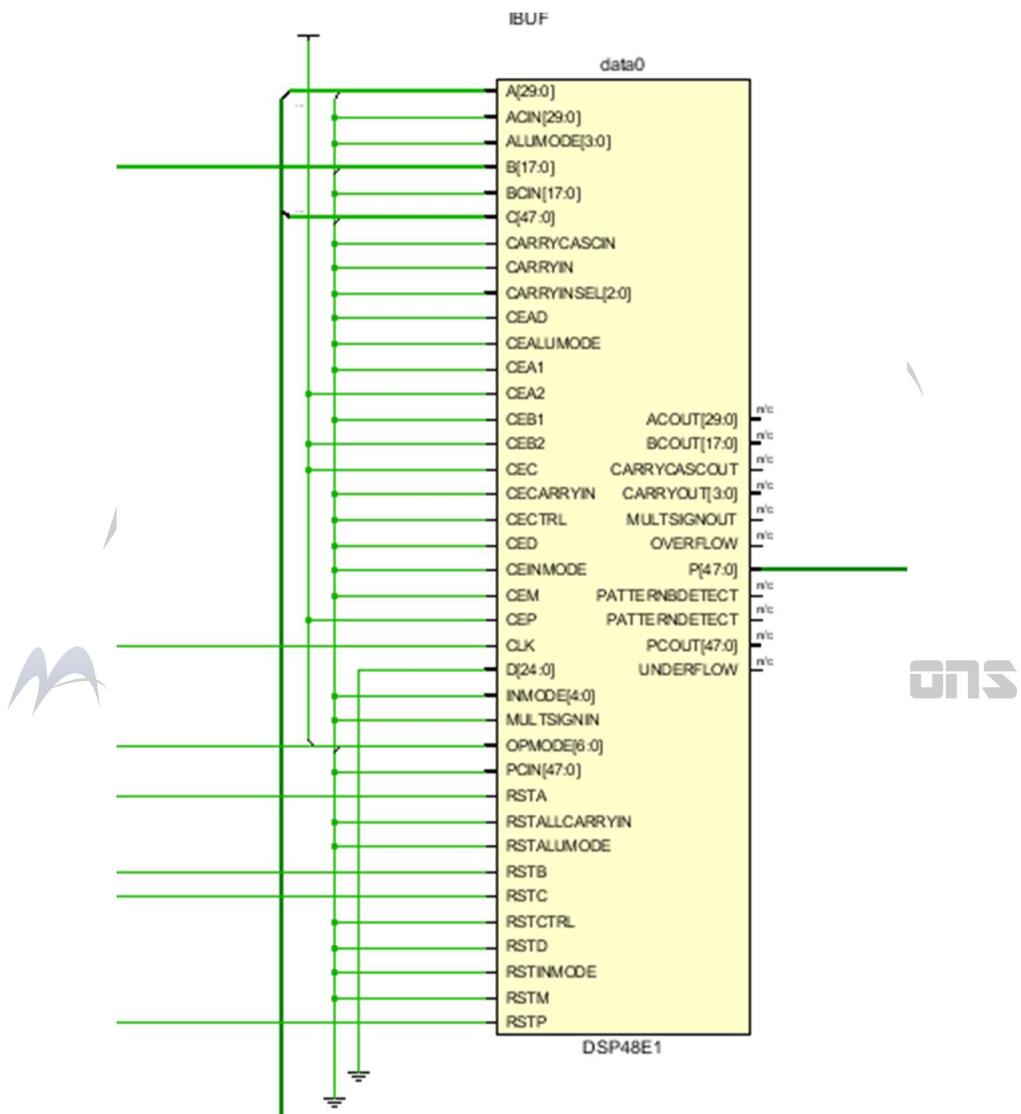
TIMING

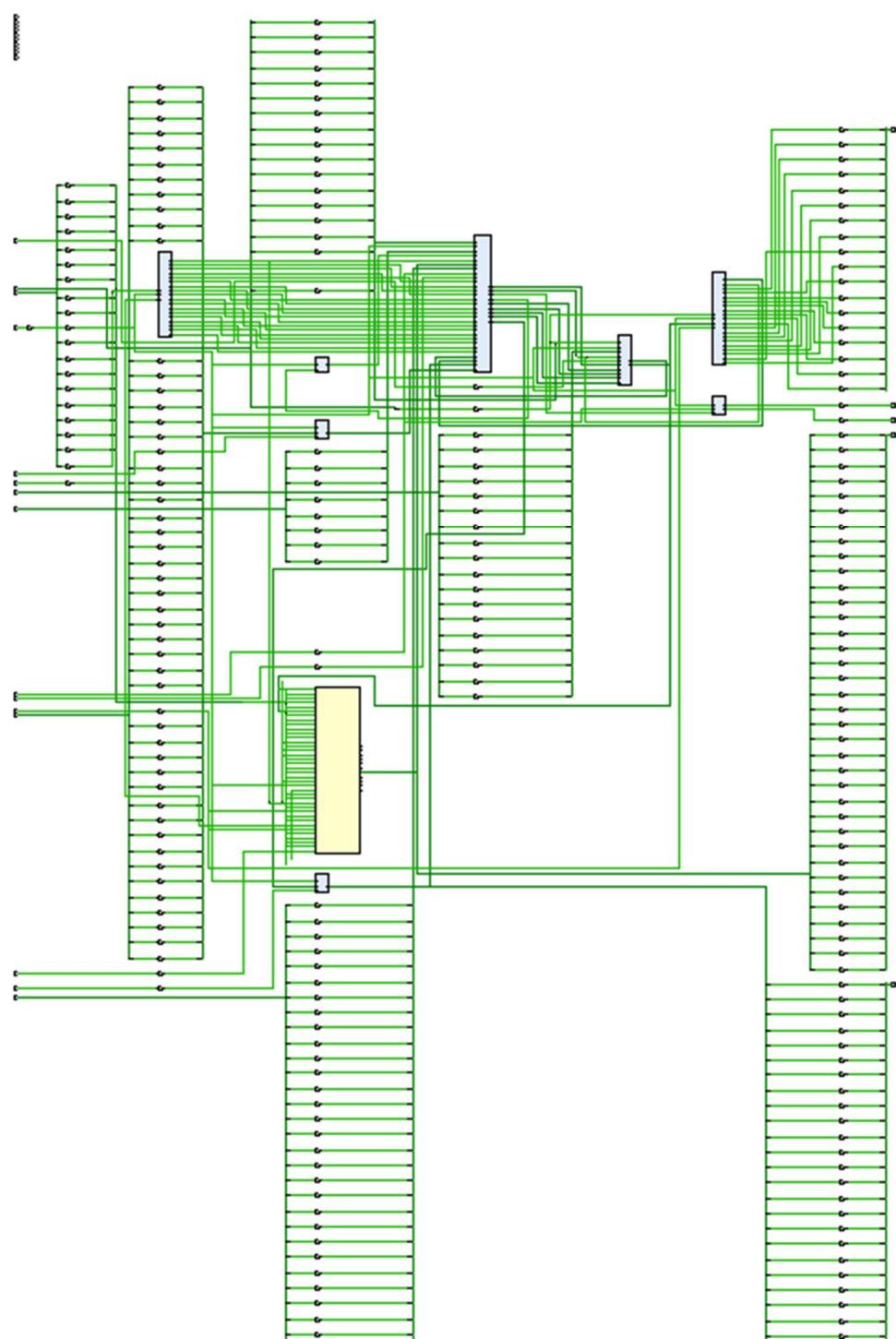
Design Timing Summary

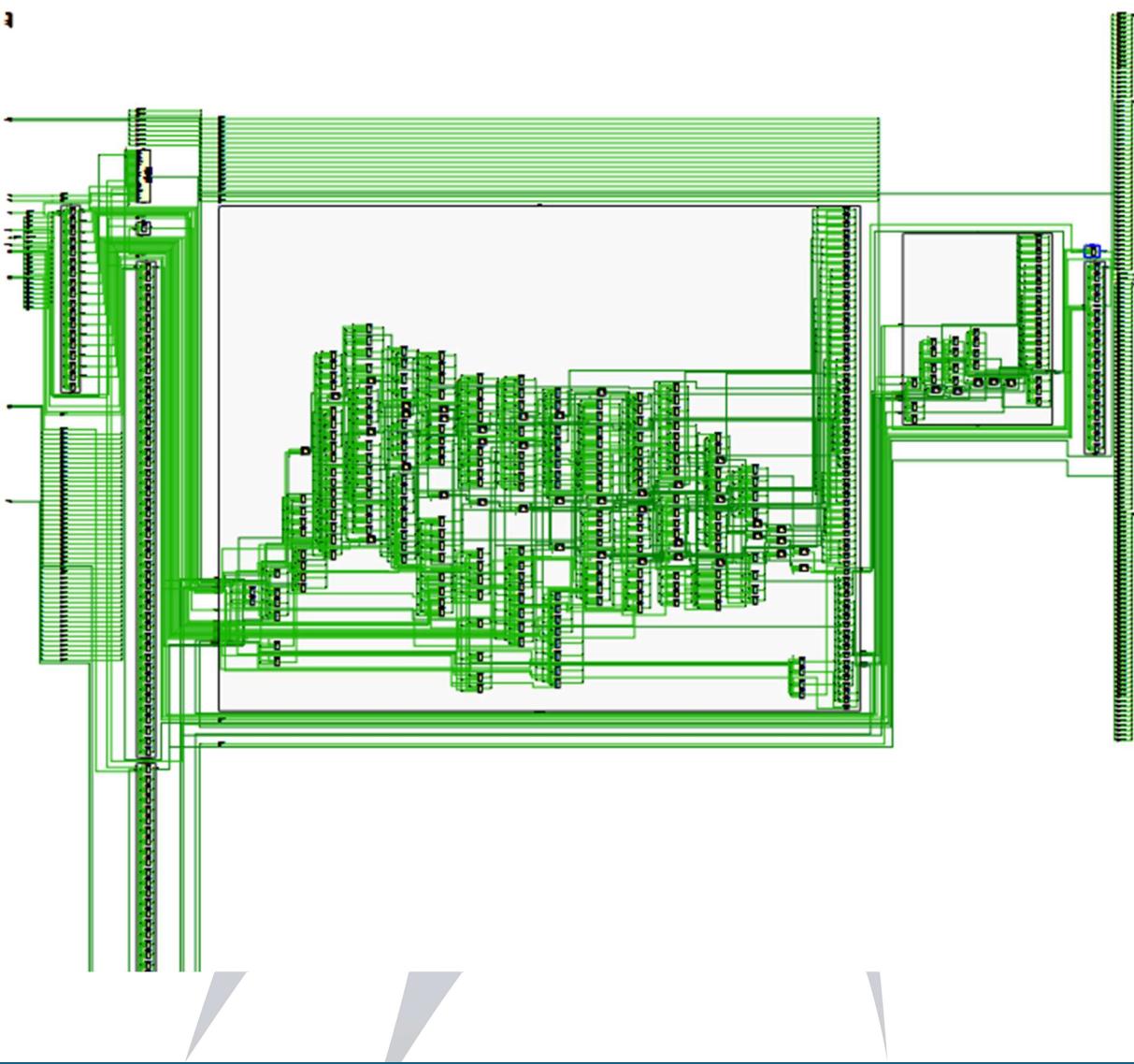
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.224 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 106	Total Number of Endpoints: 106	Total Number of Endpoints: 162

All user specified timing constraints are met.

SCHEMATIC







IMPLEMENTATION:

MESSAGES

- ✓ Implementation (1 warning, 91 infos)
 - ✓ Design Initialization (11 infos)
 - ⓘ [Netlist 29-17] Analyzing 212 Unisim elements for replacement
 - ⓘ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - ⓘ [Project 1-479] Netlist was created with Vivado 2018.2
 - ⓘ [Device 21-403] Loading part xc7a200tffg1156-3
 - ⓘ [Project 1-570] Preparing netlist for logic optimization
 - ⓘ [Timing 38-478] Restoring timing data from binary archive.
 - ⓘ [Timing 38-479] Binary timing data restore complete.
 - ⓘ [Project 1-856] Restoring constraints from binary archive.
 - ⓘ [Project 1-853] Binary constraint restore complete.
 - ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - ⓘ [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

UTILIZATION_REPORT

Tcl Console | Messages | Log | Reports | Design Runs | Power | Methodology | DRC | Timing | Utilization | ? | - | □ |

Hierarchy

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP	254	179	109	254	28	1	319	1
A1 (reg_mux)	0	18	8	0	0	0	0	0
B1 (reg_mux_0)	0	36	13	0	0	0	0	0
C0 (reg_mux_param...	0	48	20	0	0	0	0	0
carry_in (reg_mux_pa...	0	1	1	0	0	0	0	0
carryingout (reg_mux_...	0	2	1	0	0	0	0	0
D0 (reg_mux_1)	18	18	21	18	0	0	0	0
opmode (reg_mux_p...	236	8	79	236	0	0	0	0
secondadder (reg_mu...	0	48	11	0	0	0	0	0

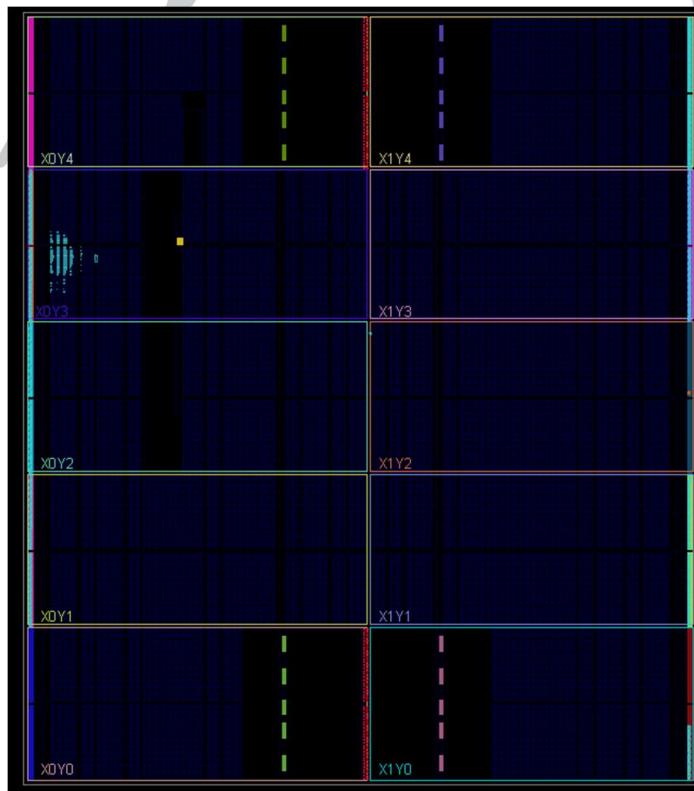
TIMING

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.368 ns	Worst Hold Slack (WHS): 0.295 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 125	Total Number of Endpoints: 125	Total Number of Endpoints: 181

All user specified timing constraints are met.

DEVICE



QUESTA_LINT:

MESSAGES

Flow Navigator Design 1

Message Viewer

Filter: Type here Waived Fixed Pending Uninspected Bug Verified

Severity-Type	Phase	Message	Comment	Status	Owner	Reviewer	File	Line
Warning (11)								

Lint Checks

Filter: Type here Waived Fixed Pending Uninspected Bug Verified Total: 16 Selected: 1

Severity	Status	Check	Alias	Message	Module	Category	State	Owner	ARC
?	?	mux_select_const		Constant value drives mux select pin. Signal C0.data_reg, Module re...	reg_mux	Connectivity	open	unassigned	
?	?	mux_select_const		Constant value drives mux select pin. Signal C0.data_reg, Module re...	reg_mux	Connectivity	open	unassigned	
?	?	mux_select_const		Constant value drives mux select pin. Signal carry_in.data_reg, Modu...	reg_mux	Connectivity	open	unassigned	
?	?	mux_select_const		Constant value drives mux select pin. Signal multiplication.data_re...	reg_mux	Connectivity	open	unassigned	
?	?	mux_select_const		Constant value drives mux select pin. Signal opmode.data_reg, Mod...	reg_mux	Connectivity	open	unassigned	
?	?	condition_const		Condition expression is a constant. Module DSP, File D:/Courses/K...	DSP	Rtl Design Style	open	unassigned	
?	?	line_char_large		Line has more characters than the specified limit. Current Count 120, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 127, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 116, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 111, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 124, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 134, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 125, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	line_char_large		Line has more characters than the specified limit. Current Count 139, ...	none	Rtl Design Style	open	unassigned	3.1.4
?	?	multi_ports_in_single_line		Multiple ports are declared in one line. Module DSP, File D:/Courses/...	DSP	Rtl Design Style	open	unassigned	3.5.6
?	?	multi_ports_in_single_line		Multiple ports are declared in one line. Module reg_mux, File D:/Cour...	reg_mux	Rtl Design Style	open	unassigned	3.5.6

SCHEMATIC

