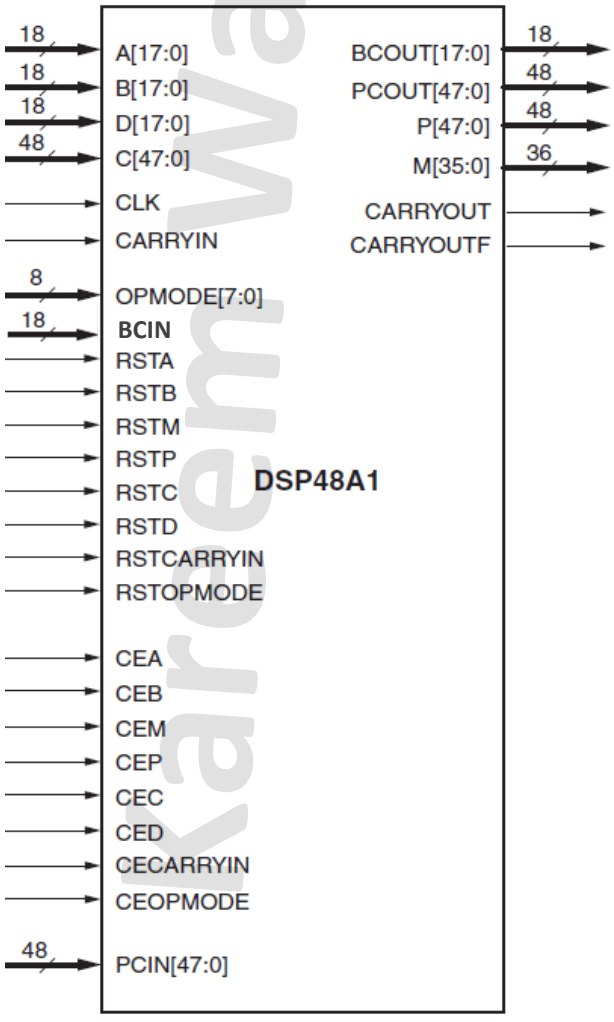
Spartan6 - DSP48A1

The Spartan-6 family offers a high ratio of DSP48A1 slices to logic, making it ideal for math-intensive applications. Design DSP48A1 slice of the spartan6 FPGAs. The testbench for this design can be challenging so use directed test patterns whenever needed to verify the design and either have expected value to compare with in the testbench or check the result from the waveforms. Use do file to run the Questasim flow.

Use **Vivado** to go through the **design flow** running elaboration, synthesis, implementation making sure that there are no design check errors during the design flow. Source of the requirements: Link



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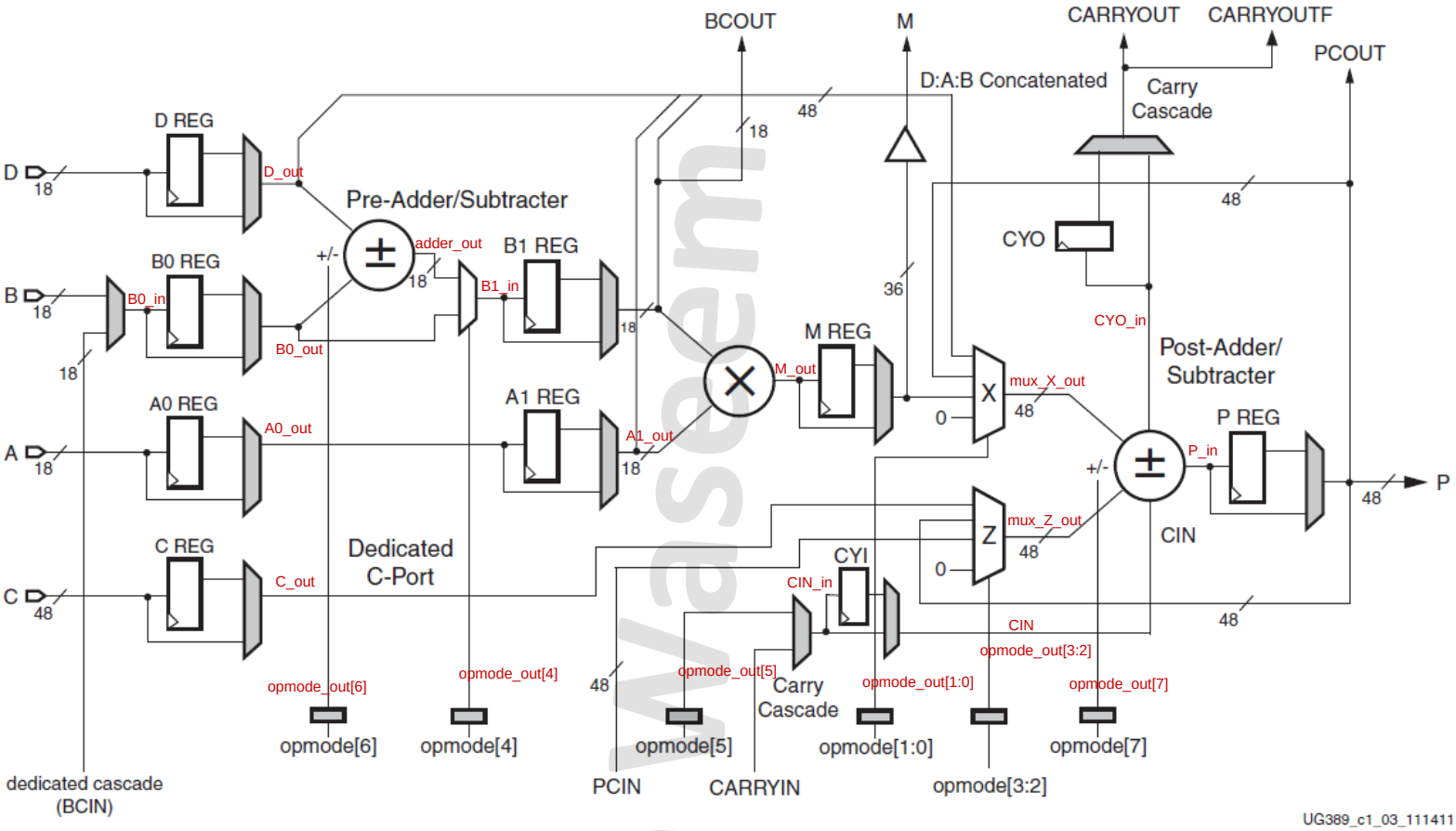

Note: opmode input has a register and mux pair in the design entry the same way as the input A, D, or C

Parameter (Attributes):

Parameter	Function
A0REG, A1REG, B0REG, and B1REG	The A0REG, A1REG, B0REG, and B1REG attributes can take values of 0 or 1. these values define the number of pipeline registers in the A and B input paths. A0REG defaults to 0 (no register). A1REG defaults to 1 (register). B0REG defaults to 0 (no register) B1REG defaults to 1 (register). A0 and B0 are the first stages of the pipelines. A1 and B1 are the second stages of the pipelines
CREG, DREG, MREG, PREG, CARRYINREG, CARRYOUTREG, and OPMODEREG	These attributes can take a value of 0 or 1. The number defines the number of pipeline stages. Default: 1 (registered)

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CARRYINSEL	The CARRYINSEL attribute is used in the carry cascade input, either the CARRYIN input will be considered or the value of opcode[5]. This attribute can be set to the string CARRYIN or OPMODE5. Default: OPMODE5. Tie the output of the mux to 0 if none of these string values exist.
B_INPUT	The B_INPUT attribute defines whether the input to the B port is routed from the B input (attribute = DIRECT) or the cascaded input (BCIN) from the previous DSP48A1 slice (attribute = CASCADE). Default: DIRECT. Tie the output of the mux to 0 if none of these string values exist.
RSTTYPE	The RSTTYPE attribute selects whether all resets for the DSP48A1 slice should have a synchronous or asynchronous reset capability. This attribute can be set to ASYNC or SYNC. Default: SYNC.

Data Ports:

Signal Name	Function
A	18-bit data input to multiplier, and optionally to post-adder/subtracter depending on the value of OPMODE[1:0].
B	18-bit data input to pre-adder/subtracter, to multiplier depending on OPMODE[4], or to post-adder/subtracter depending on OPMODE[1:0].
C	48-bit data input to post-adder/subtracter.
D	18-bit data input to pre-adder/subtracter. D[11:0] are concatenated with A and B and optionally sent to post-adder/subtracter depending on the value of OPMODE[1:0].
CARRYIN	carry input to the post-adder/subtracter
M	36-bit buffered multiplier data output, routable to the FPGA logic. It is either the output of the M register (MREG = 1) or the direct output of the multiplier (MREG = 0).
P	Primary data output from the post-adder/subtracter. It is either the output of the P register (PREG = 1) or the direct output of the post-adder/subtracter (PREG = 0).
CARRYOUT	Cascade carry out signal from post-adder/subtracter. It can be registered in (CARRYOUTREG = 1) or unregistered (CARRYOUTREG = 0). This output is to be connected only to CARRYIN of adjacent DSP48A1 if multiple DSP blocks are used.
CARRYOUTF	Carry out signal from post-adder/subtracter for use in the FPGA logic. It is a copy of the CARRYOUT signal that can be routed to the user logic.

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Control Input Ports:

Signal Name	Function
CLK	DSP clock
OPMODE	Control input to select the arithmetic operations of the DSP48A1 slice.

Clock Enable Input Ports:

Signal Name	Function
CEA	Clock enable for the A port registers: (A0REG & A1REG).
CEB	Clock enable for the B port registers: (B0REG & B1REG).
CEC	Clock enable for the C port registers (CREG).
CECARRYIN	Clock enable for the carry-in register (CYI) and the carry-out register (CYO).
CED	Clock enable for the D port register (DREG).
CEM	Clock enable for the multiplier register (MREG).
CEOPMODE	Clock enable for the opmode register (OPMODEREG).
CEP	Clock enable for the P output port registers (PREG = 1).

Reset Input Ports: All the resets are active high reset. They are either sync or async depending on the parameter RSTTYPE.

Signal Name	Function
RSTA	Reset for the A registers: (A0REG & A1REG).
RSTB	Reset for the B registers: (B0REG & B1REG).
RSTC	Reset for the C registers (CREG).
RSTCARRYIN	Reset for the carry-in register (CYI) and the carry-out register (CYO).
RSTD	Reset for the D register (DREG).
RSTM	Reset for the multiplier register (MREG).
RSTOPMODE	Reset for the opmode register (OPMODEREG).
RSTP	Reset for the P output registers (PREG = 1).

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Cascade Ports:

Signal Name	Function
BCOUT	Cascade output for Port B.
PCIN	Cascade input for Port P.
PCOUT	Cascade output for Port P.

OPMODE Pin Descriptions:

Port Name	Function
OPMODE[1:0]	**Specifies the source of the X input to the post-adder/subtracter**
	0 – Specifies to place all zeros (disable the post-adder/subtracter and propagate the Z result to P) 1 – Use the multiplier product 2 – Use the P output signal (accumulator) 3 – Use the concatenated D:A:B input signals
OPMODE[3:2]	**Specifies the source of the Z input to the post-adder/subtracter**
	0 – Specifies to place all zeros (disable the post-adder/subtracter and propagate the multiplier product or other X result to P) 1 – Use the PCIN 2 – Use the P output signal (accumulator) 3 – Use the C port
OPMODE[4]	**Specifies the use of the pre-adder/subtracter**
	0 – Bypass the pre-adder supplying the data on port B directly to the multiplier 1 – Selects to use the pre-adder adding or subtracting the values on the B and D ports prior to the multiplier
OPMODE[5]	**Forces a value on the carry input of the carry-in register (CYI) or direct to the CIN to the post-adder. Only applicable when CARRYINSEL = OPMODE5**
OPMODE[6]	**Specifies whether the pre-adder/subtracter is an adder or subtracter**
	0 – Specifies pre-adder/subtracter to perform an addition operation 1 – Specifies pre-adder/subtracter to perform a subtraction operation (D-B)
OPMODE[7]	**Specifies whether the post-adder/subtracter is an adder or subtracter**
	0 – Specifies post-adder/subtracter to perform an addition operation 1 – Specifies post-adder/subtracter to perform a subtraction operation (Z-(X+CIN))

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General Notes:

1. The 18-bit A, B, and D buses are concatenated in the following order: D[11:0], A[17:0], B[17:0].
2. The X and Z multiplexers are 48-bit designs. Multiplexer inputs less than 48-bits should be extended with zeros.
3. The multiply-accumulate path for P is through the Z multiplexer. The P feedback through the X multiplexer enables accumulation of P cascade when the multiplier is not used.
4. The gray-colored multiplexers are programmed at configuration time using parameters. The clear multiplexers are controlled by OPMODE inputs, allowing dynamic changes to functionality.
5. The C register supports multiply-add or wide addition operations.
6. Enabling SUBTRACT implements Z – (X + CIN) at the output of the post-adder/ subtracter.
7. B input can be added or subtracted from the D input using the pre-adder/subtracter. Enabling SUBTRACT implements D – B at the output of the pre-adder/subtracter.
8. CARRYOUTF is a copy of CARRYOUT but dedicated to applications in the FPGA logic, whereas CARRYOUT is the dedicated route to the adjacent DSP48A1 slice.
9. The registered output of the multiplier or its direct output can be routed to the FPGA logic through a 36-bit vector called M.
10. The BCIN input is the direct cascade from the adjacent DSP48A1 BCOUT.

Deliverables:

1) The assignment should be submitted as a PDF file with this format <your_name>_Project1 for example Kareem_Waseem_Project1.
2) Snippets from the waveforms captured from QuestaSim for the design with inputs assigned values and output values visible.
3) Run vivado and add a constraint file that has only timing constraint which defines the clock frequency to 100 MHz to pin W5 as usual. Since the design has I/O ports more than the Basys 3 FPGA board, choose the FPGA part xc7a200tffg1156-3 to accommodate for the large I/O ports.
4) Snippets from the schematic after the elaboration & synthesis (DSP block with other cells from the FPGA should be in the synthesized schematic)
5) Snippet from the utilization & timing report after the synthesis and implementation.
6) Snippet of the “Messages” tab showing no critical warnings or errors after running elaboration, synthesis, and implementation.
7) Run linting and make sure there are no errors reported by the linting tool keeping the default methodology and goals.

Note that your document should be organized as 8 sections as follows:

1. RTL code
2. Testbench code
3. Do file

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4. QuestaSim Snippets
5. Constraint File
6. Elaboration (“Messages” tab & Schematic snippets)
7. Synthesis (“Messages” tab, Utilization report, timing report & Schematic snippets)
8. Implementation (“Messages” tab, Utilization report, timing report & device snippets)
9. Linting (snippets showing no errors)