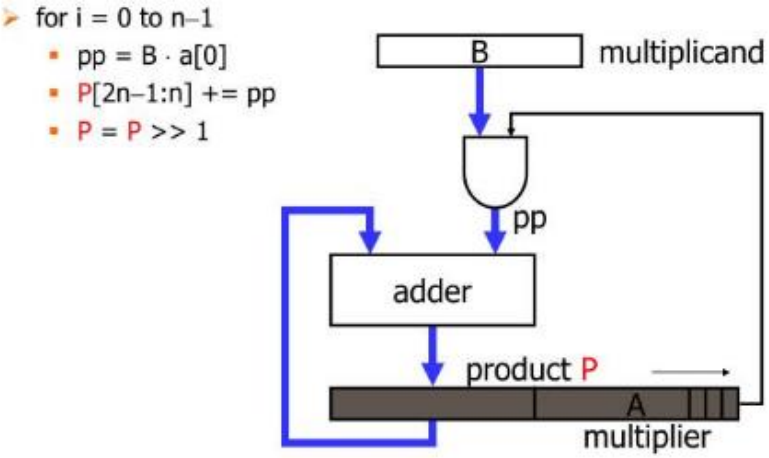
Lab 3 Requirement

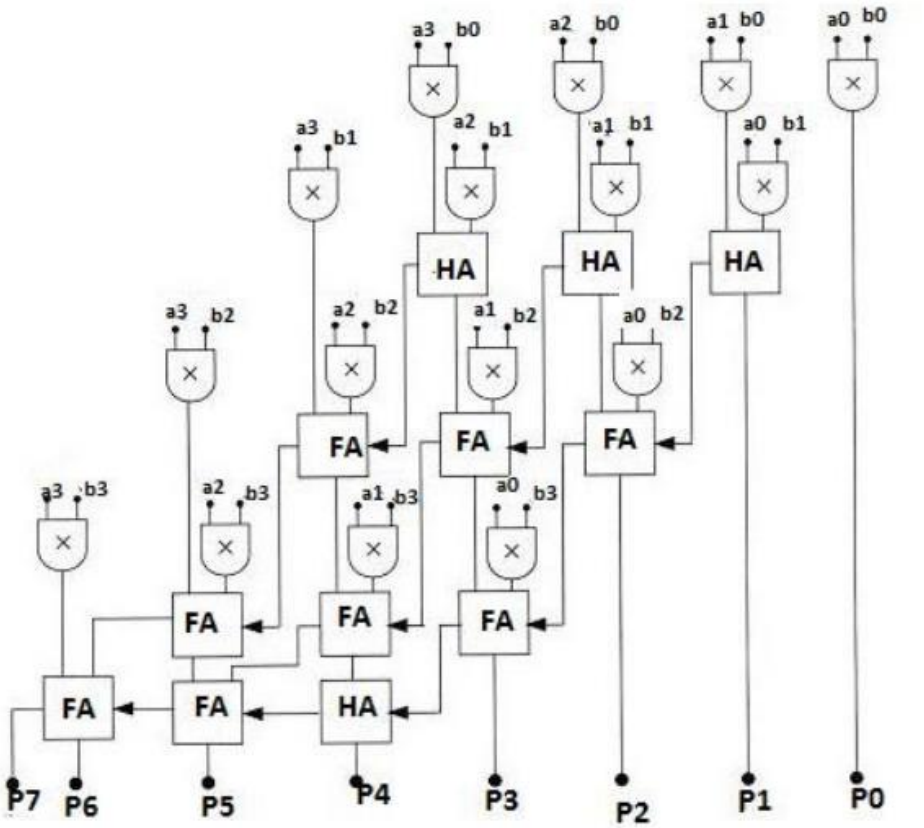
Requirement

A] Design generic **n-bit** multipliers using **two** different methods. Implement your designs using Verilog or VHDL (use **16 bits** as the default value for n):

1. Shift-And-Add Multiplier



2. Array Multiplier



B] Synthesize both multipliers using “oasys”.
Compare between the two multipliers w.r.t. Area, Time and Power. Justify your answers.

Submission

In all the submissions use the default n value.

1. All Verilog/VHDL code file(s).
2. **Two** do files one for each multiplier.
3. **Two** Screenshots one for each multiplier’s simulation results in **decimal**.
   Make sure to include at least **5 testcases** in each do file and consequently in the screenshots
4. For each multiplier submit the following reports generated from oasys:
   design.rpt, path.rpt and power.rpt.
5. **One** document containing your analysis/justification for the obtained metrics
   e.g. design X is faster than design Y because …..
   design X has less area than design Y because……
6. Include all the required deliverables in **ONE** zip/rar folder named with the team members’ names e.g.StudentName1_StudentName2.zip
7. Due date is **Monday 15 Oct. 2021 at 11:59 p.m**. via blackboard (“Lab3_Requirement_Submission”).
8. Make sure to follow all the submission guidelines not to lose any grades.