Lab 6

Requirement

A] Write a VHDL/Verilog code for a 16-bit multiplier which works along a **three stages clocked** pipeline. The multiplier should be able to multiply signed numbers where these numbers are represented as sign and 2's complement.

- In the first stage, each operand is converted to the 2's complement if it is negative; otherwise, it remains the same during this stage.
- In the second stage, the two operands after modifications are multiplied.
- In the last stage, the result of the multiplication is converted to the 2's complement if the signs of the two operands are different; otherwise, the result remains the same during this stage, where the result of this stage is the final output.

Hints:

- A and B are 16 bits, the output C should be 31 bits (multiplication of 15 bits of both A and B results in 30 bits + the sign bit)
- You can use "`y <= -x;`" to calculate the 2's complement, and "`z <= x * y;`" to multiply two operands (note that the size of z is the sum of sizes of x and y). You need to include another library for those operations, so add:

```
use ieee.std_logic_signed.all;
```

Test cases:

A = 2 (0002 hex) and B = 3 (0003 hex) => C=A*B= 6 (00000006 hex)

A = -3 (FFFD hex) and B = 3 (0003 hex) => C=A*B= -9 (7FFFFFF7 hex)

A = -3 (FFFD hex) and B = -3 (FFFD hex) => C=A*B= 9 (00000009 hex)

B] Simulate the code.
C] Perform synthesis.
D] Perform post-synthesis simulation.

Submission

1. **One** Verilog/VHDL code file for the problem above.
2. **One** do file or testbench containing the test cases above.
3. **One** Screenshot for the simulation results **before synthesis** showing the test cases above in **HEX**.
4. The generated Netlist file from the synthesis.
5. **One** Screenshot for the simulation results **after synthesis** showing the test cases above in **HEX**.

6. **One** document containing clear screenshots for design.rpt, path.rpt and power.rpt reports generated from oasys. In this document indicate if the simulation results before and after synthesis are not the same and what changes you made to make them identical.
7. Include all the required deliverables in **ONE** zip/rar folder named with the team members' names e.g.StudentName1_StudentName2.zip
8. Due date is **Monday 20 Dec. 2021 at 11:59 p.m**. via blackboard ("Lab6_Requirement_Submission").
9. Make sure to follow all the submission guidelines not to lose any grades.