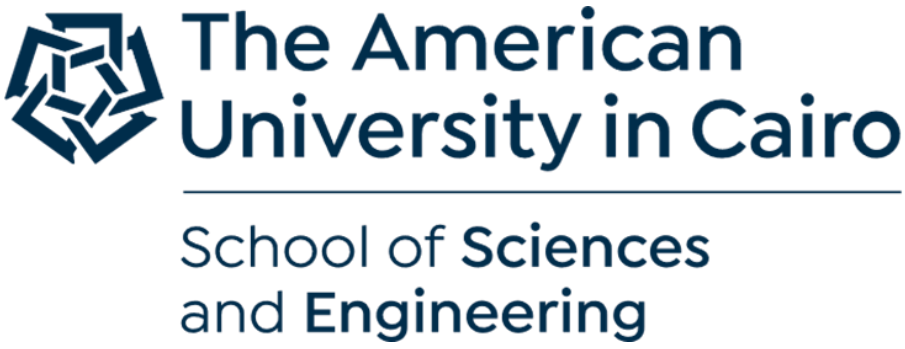

Digital Design II

Project 1 Milestone 2 Report

Spring 2022

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Contents

Contributions

All group members worked together to be able to obtain consistent results. However, the responsibilities were divided as follows:

Mohammed Farag: NOT, NAND, NOR

Mostafa Ibrahim: AOI22, Cell 5

Abdulrahman Said: Cell 6 and 7

Cell Heights

To determine the cell heights, we first drew a stick diagram that was optimized using Euler's path, we calculated estimates of the heights based on the DRC rules provided, then, we implemented the layout on Electric VLSI. To determine the minimum cell height we abided by the rules that specify the dimensions of the components and the distances between them. Then, we designed the largest cell, determined its height, and designed the rest of the cells accordingly. In addition, we designed the layouts to have widths that were multiples of 4**λ** and that were the smallest possible.

The **standard cell height** that was used for all the cells was the height of **cell 7 size 2** which turned out to be **300λ**. The estimated cell height for cell 7 of size 2 was 292**λ**; however, due to some constraints in the layout designing process.

Determining t_{pdf} and t_{pdr}

To determine tpdf and tpdr for each cell with the different loads, we connect the circuit with an inverter - size 1 for Cinv, size 2 for 2Cinv, and size 4 for 4Cinv - then we indicate the transition time in the spice deck and we simulate.

Cell Design

Each required component had a schematic design, layout design, and simulation schematic. Size 1 and 2 of each cell were grouped in separated cell groups.

Schematic Design

For each cell we had to create two schematics one of size 1 and the other of size 2. The only difference between both schematics is that the transistors were seized accordingly. In our library, the exported inputs in the library were named A, B, C, D and the output was exported as OUT. The power and the ground were exported as VDD and GND respectively.

Layout Design

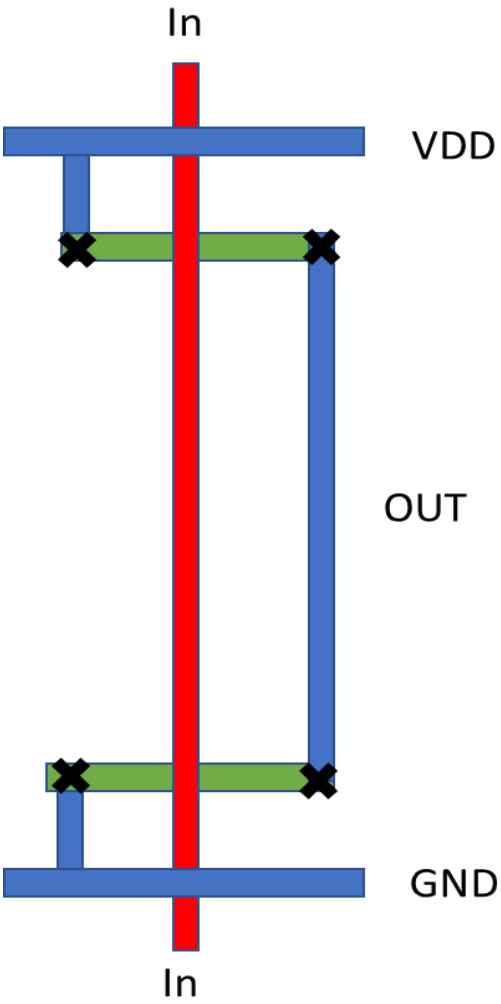
The layouts were designed according to the stick diagrams that we drew. In a size 2 cell we just multiply the size of the size 1 diffusion areas by 2. Eventually, all the cells were modified to have the cell height of the largest cell which is cell 7. The width of each cell was tailored to be a multiple of 4**λ** in all cells.

Simulation Schematic

In order to simulate the cells, we made a simulation schematic for each cell where we drag the icon of the cell to be simulated in it and connect it to inverters of size 1, 2, 4 in order to simulate the load capacitance of Cinv, 2Cinv, 4Cinv respectively. After that, we write spice code that includes a pulsating input which controls the output of the cell. Then we measure the Tpdf and Tpdf. We run the simulation and get the values of the delays from the log of the simulation.

Inverter

Stick Diagram



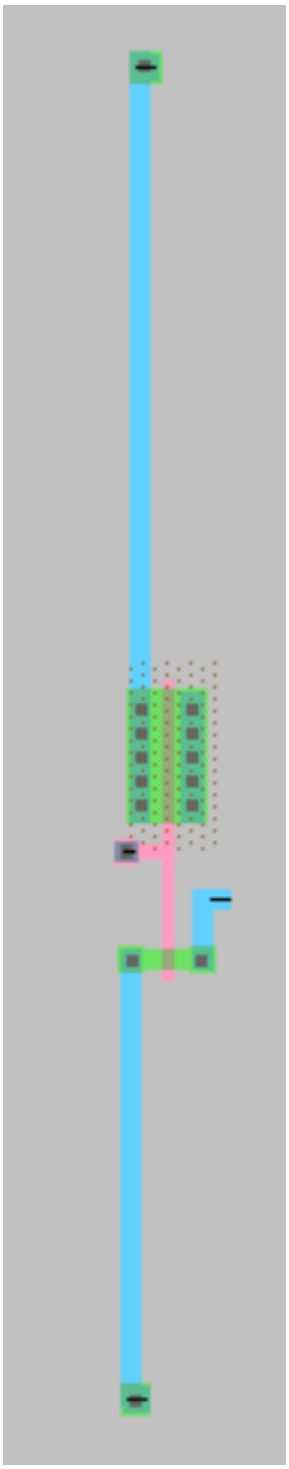
To calculate the inverter cell Height: GND wire height + Minimum Distance Between 2 metals + (Diffusion Area Wmin*nmos transistor size) + Minimum Distance Between 2 diffusion areas + (Diffusion Area Wmin*pmos transistor size) + VDD wire height + Minimum Distance Between 2 metals.

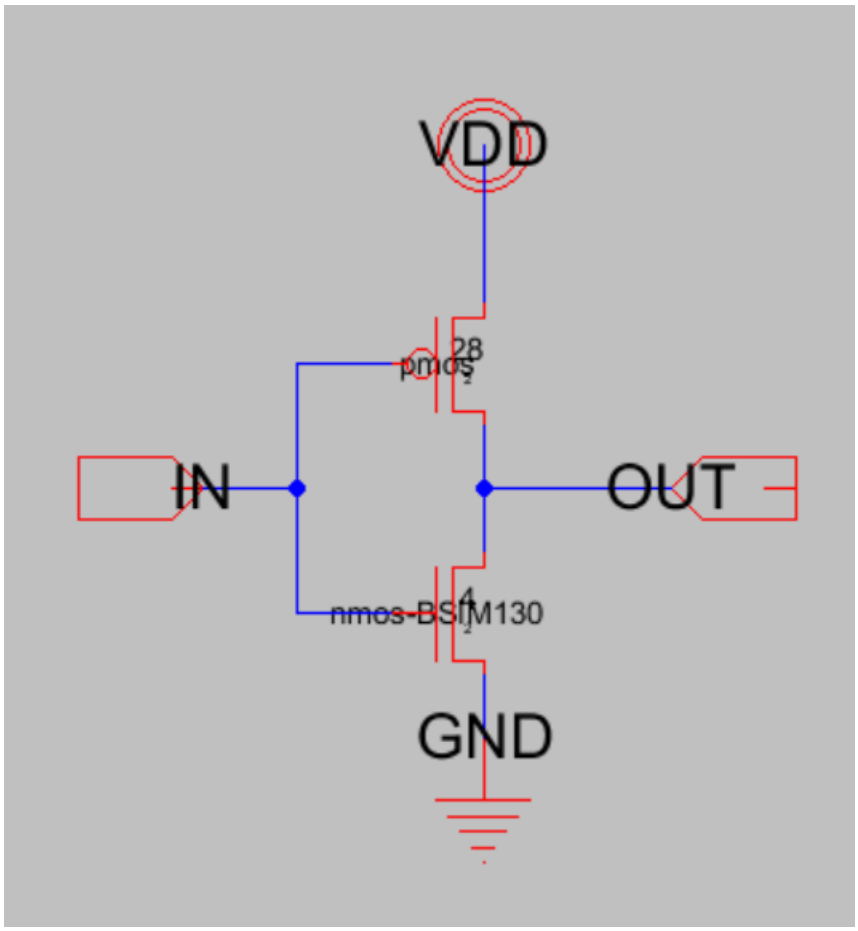
- Height (size 1) = 60λ
- Height (size 2) = 92λ
- Height (size 4) = 156λ

Actual cell size used = 300λ

Inverter {size 1}

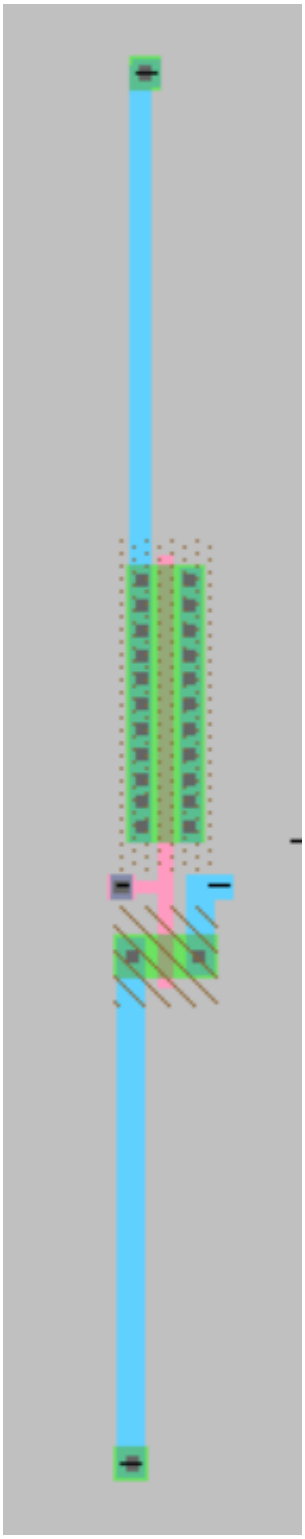
Layout & Schematic:

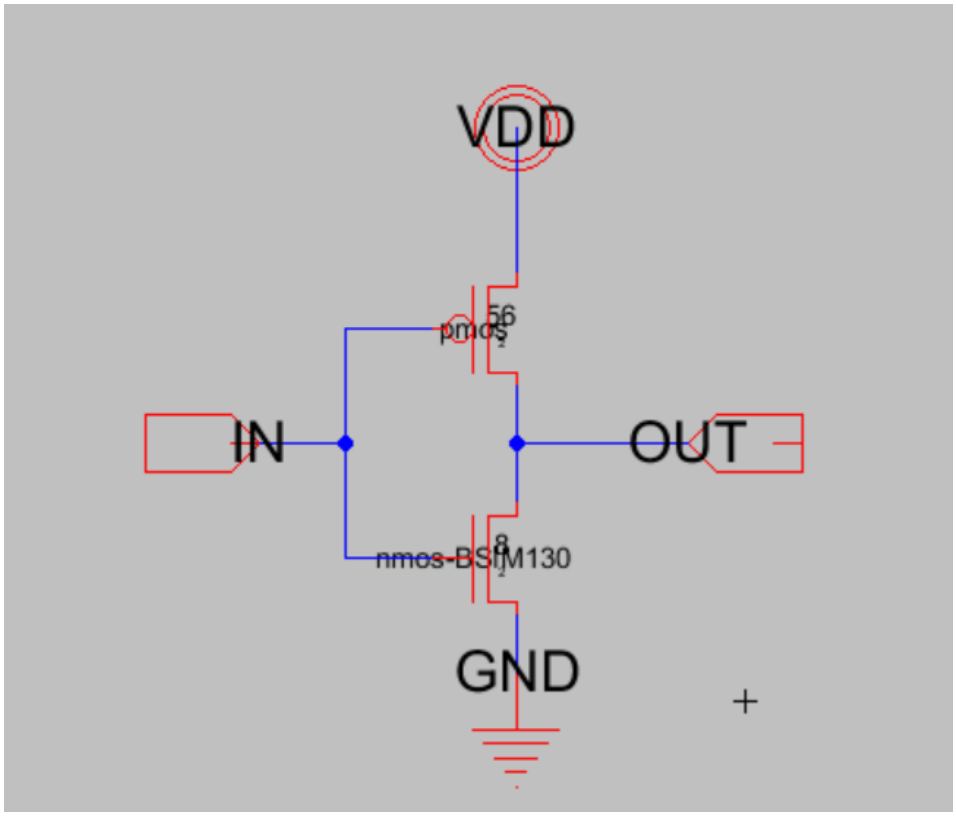




Inverter {size 2}

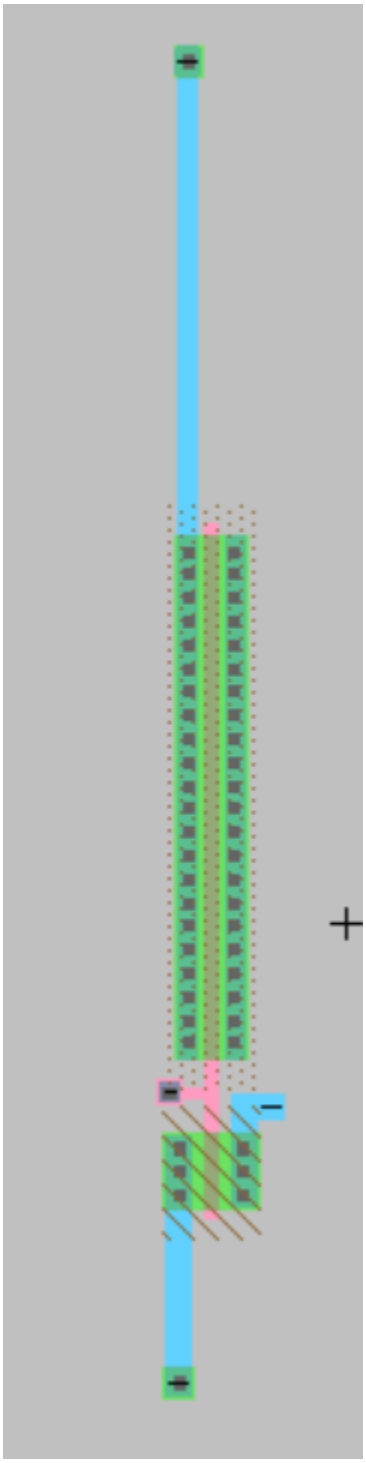
Layout & Schematic:

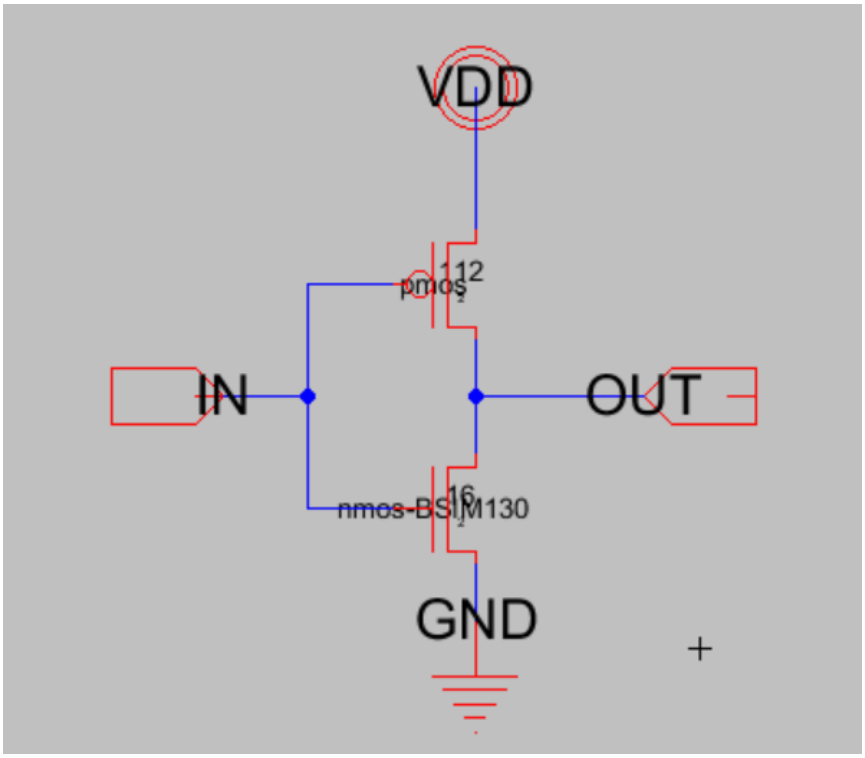




Inverter {size 4}

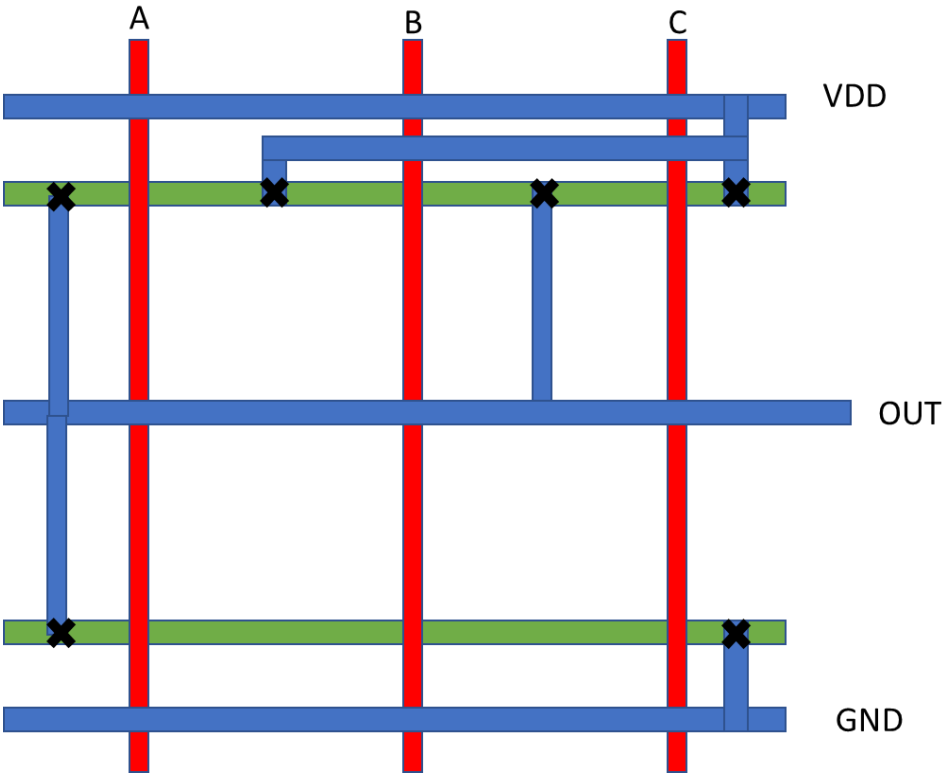
Layout & Schematic:





3 input NAND

Stick Diagram



Cell height = GND wire height + Minimum Distance Between 2 metals + (Diffusion Area Wmin*nmos transistor size) + Minimum Distance Between 2 diffusion areas + (Diffusion Area Wmin*pmos transistor size) + Minimum Distance Between 2 metals + VDD wire height.

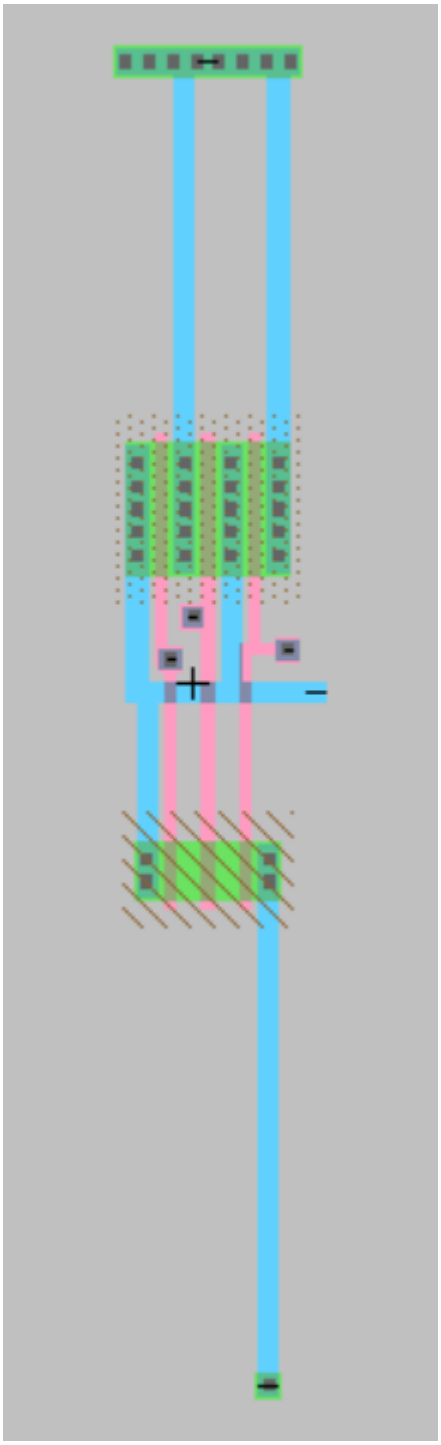
Height (size 1) = 4 + 4 + 4*3 + 12 + 4* 7 + 4 + 4 = 68λ

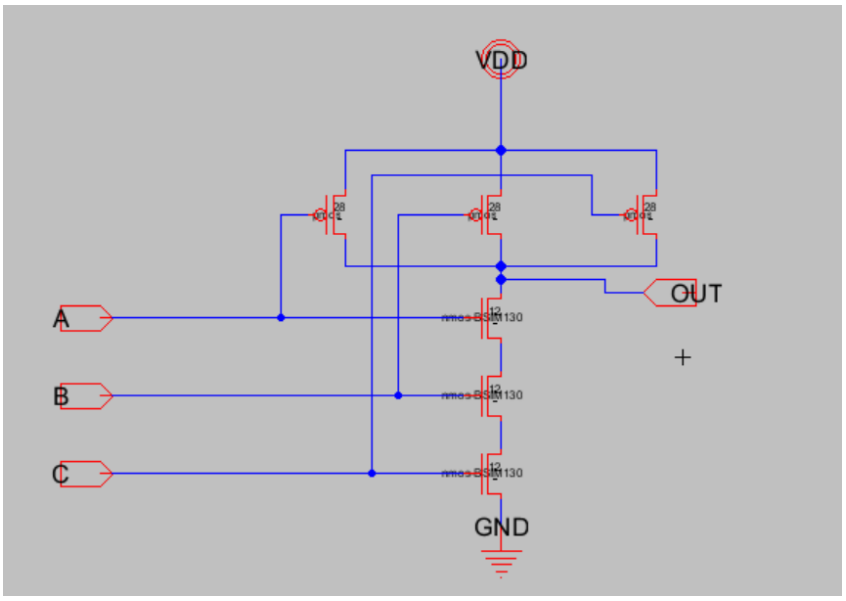
Height (size 2) = 4 + 4 + 4*(2*3) + 12 + 4* (2*7) + 4 + 4 + 4 + 4 = 116λ

Actual Size Used = 300λ

NAND {size 1}

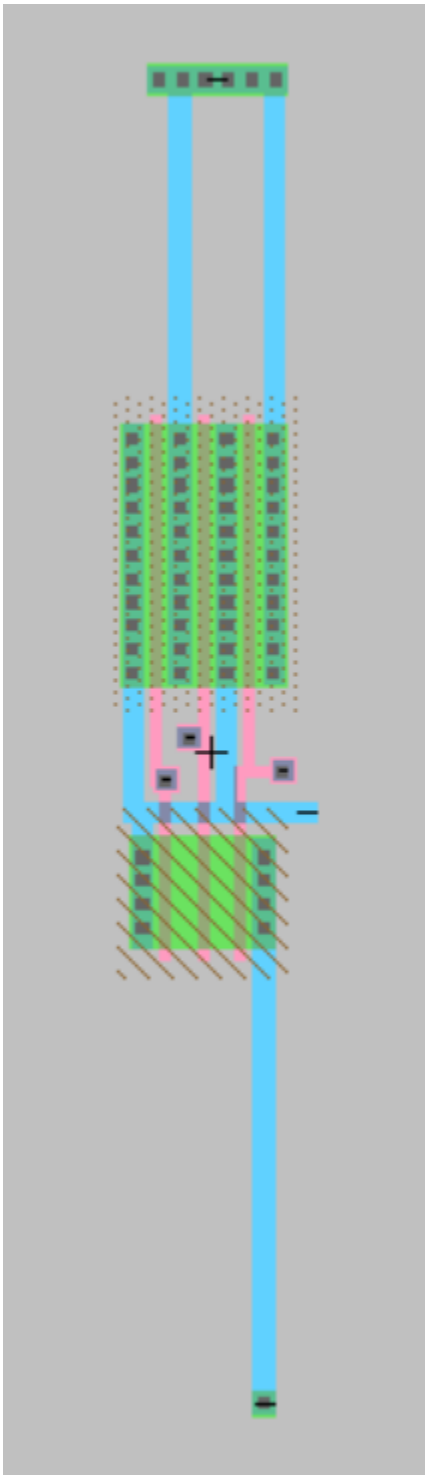
Layout & Schematic:

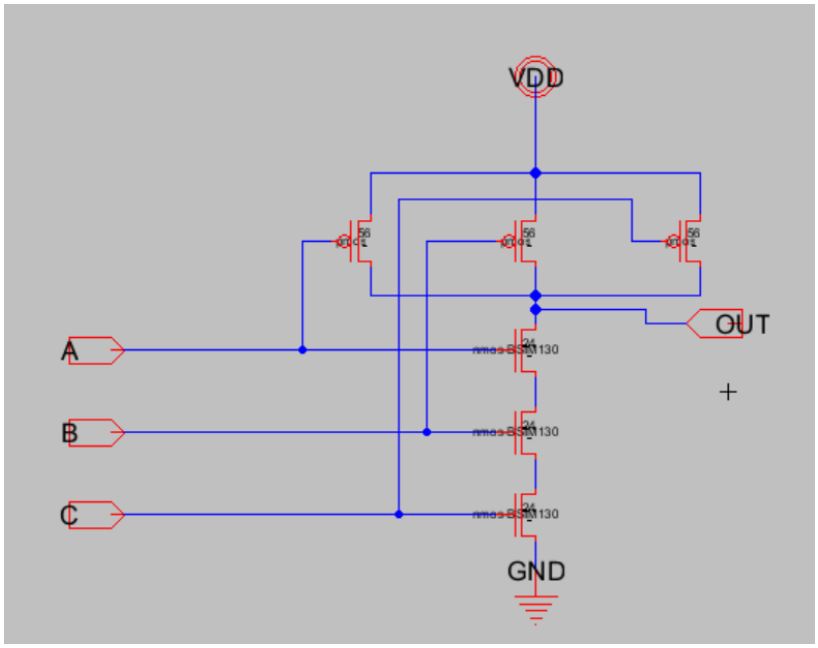




NAND {size 2}

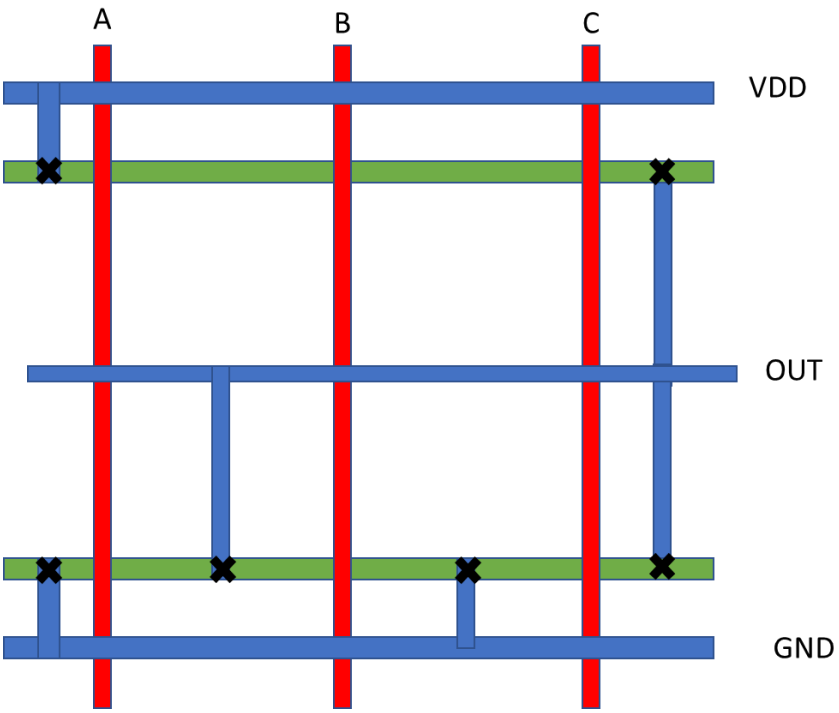
Layout & Schematic:





3 input NOR

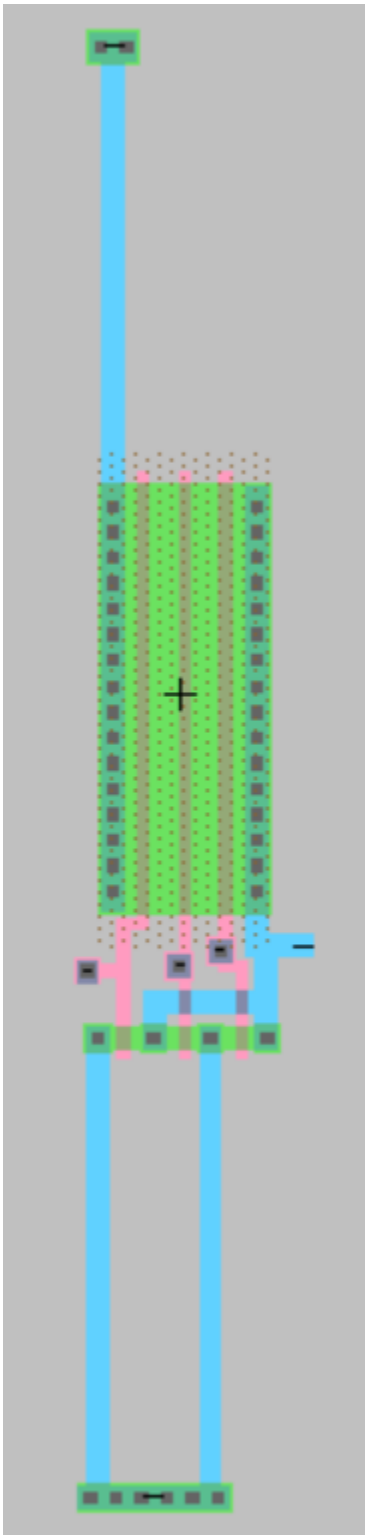
Stick Diagram

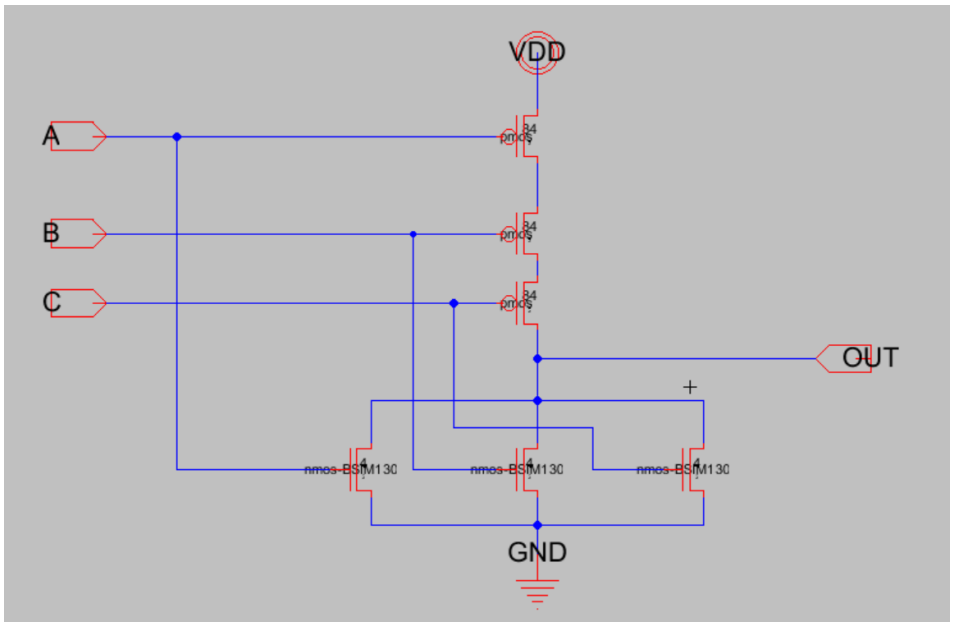


Height (size 1) =116λ
Height (size 2) = 204λ

NOR {size 1}

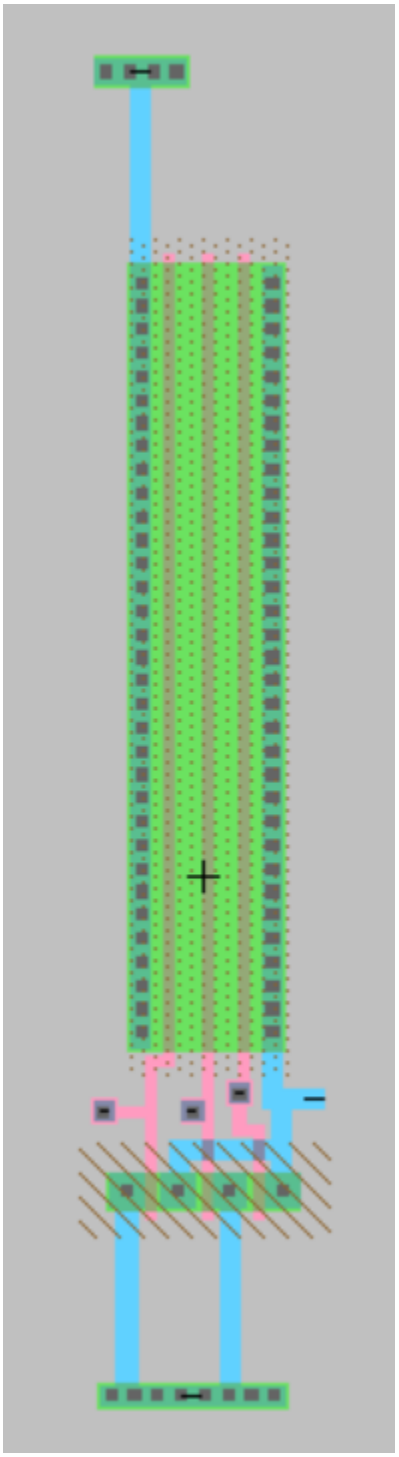
Layout & Schematic:

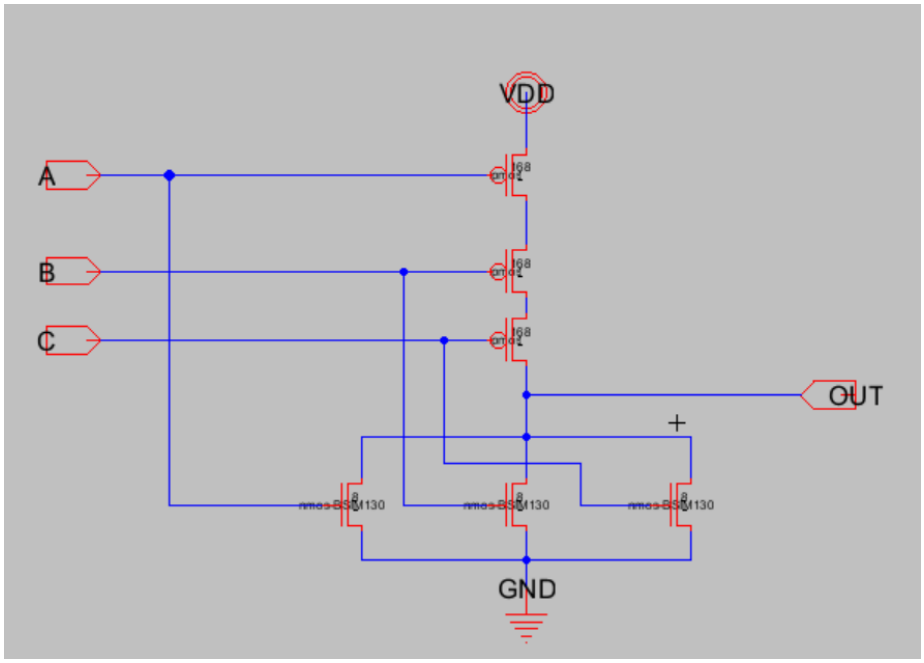




NOR {size 2}

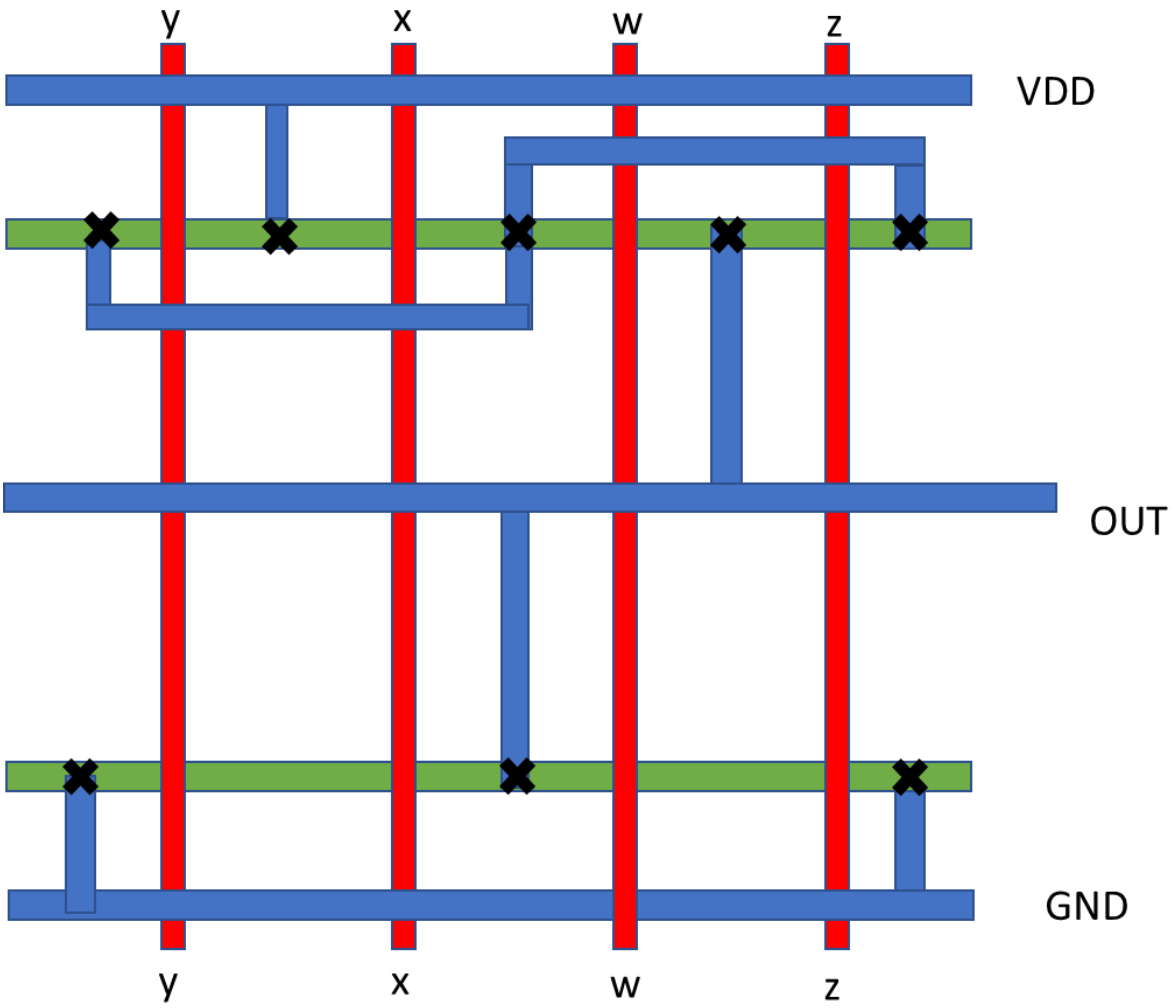
Layout & Schematic:





AOI22

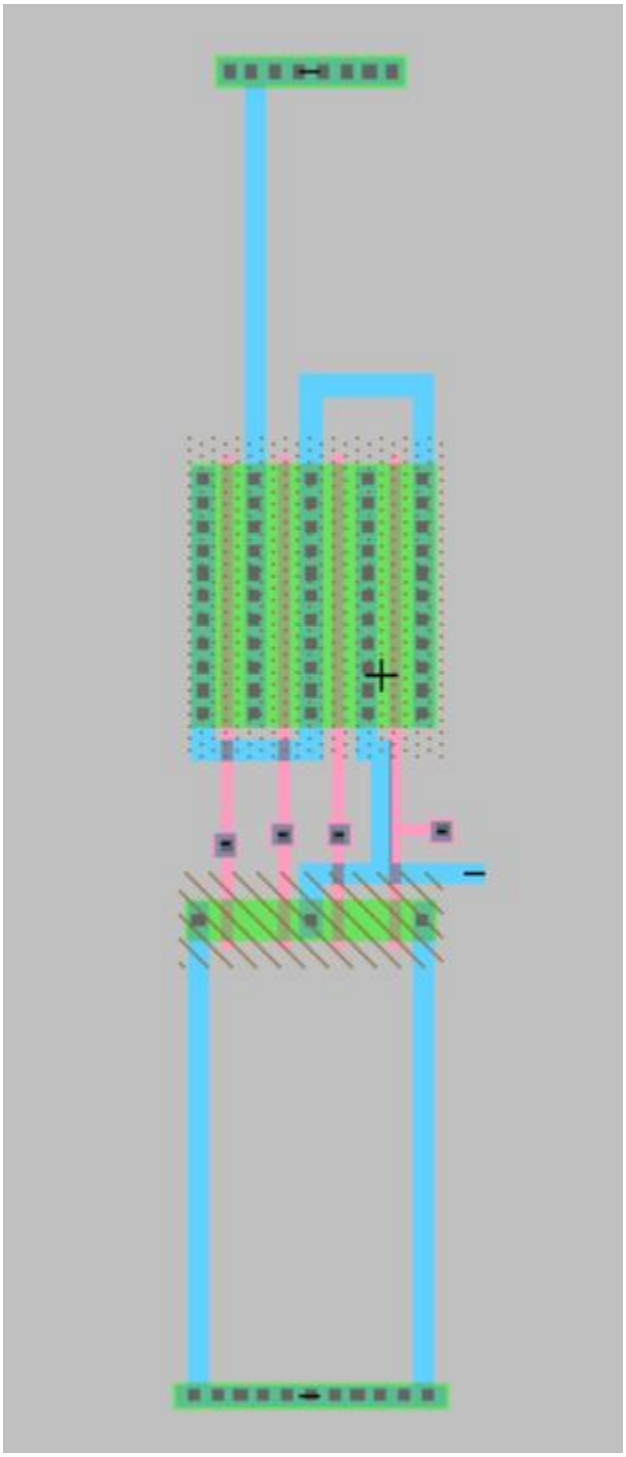
Stick Diagram



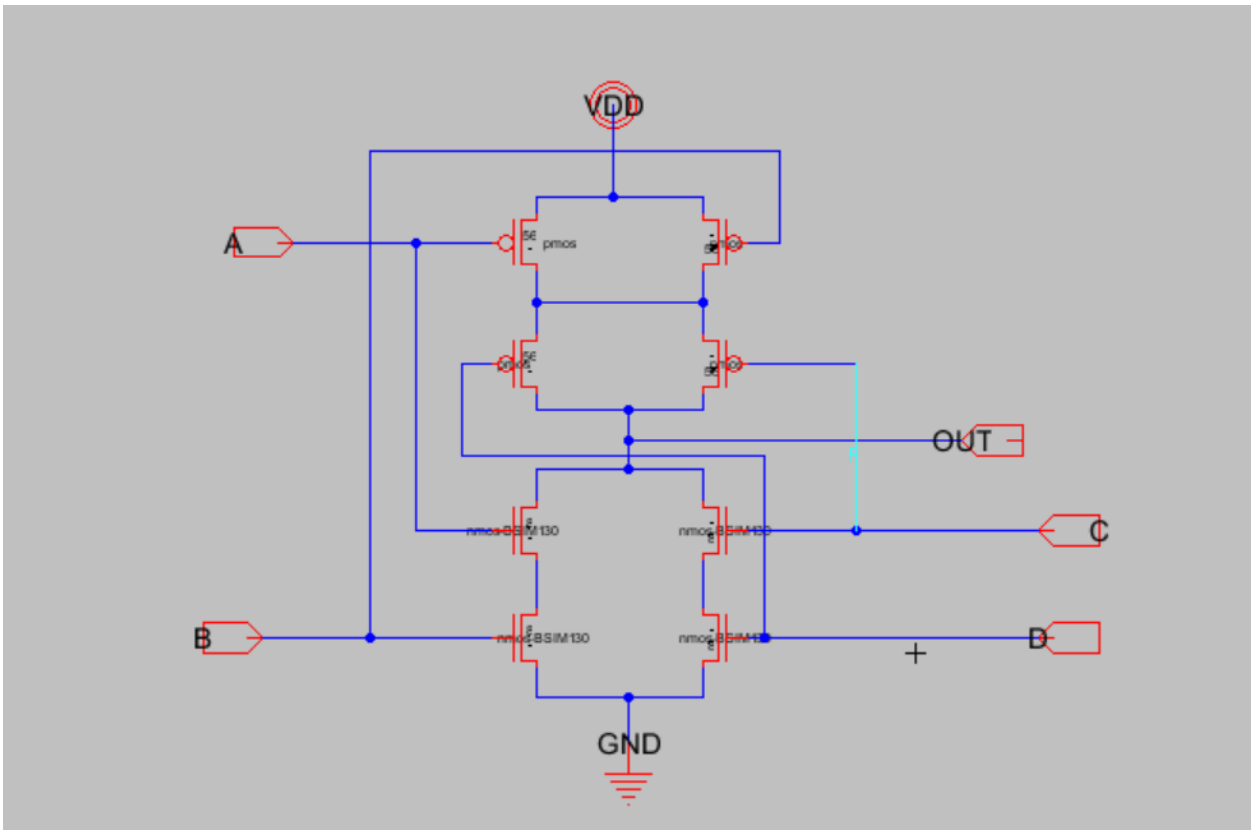
Height (size 1) = 108λ
Height (size 2) = 172λ

AOI22 {size 1}

Layout:

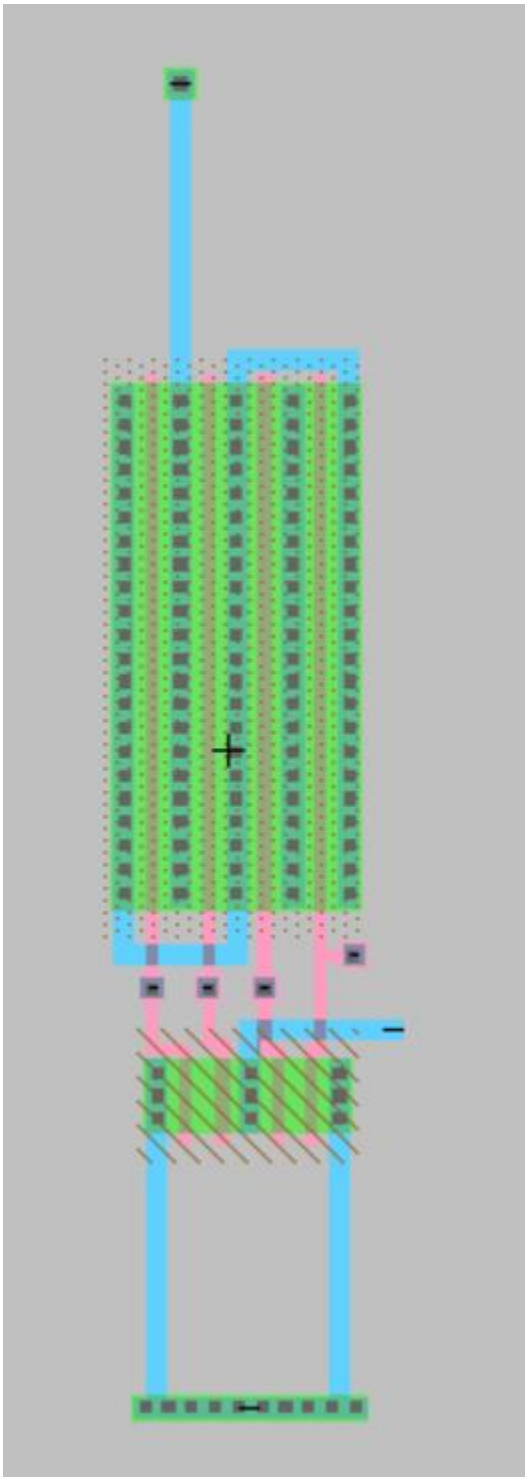


Schematic:

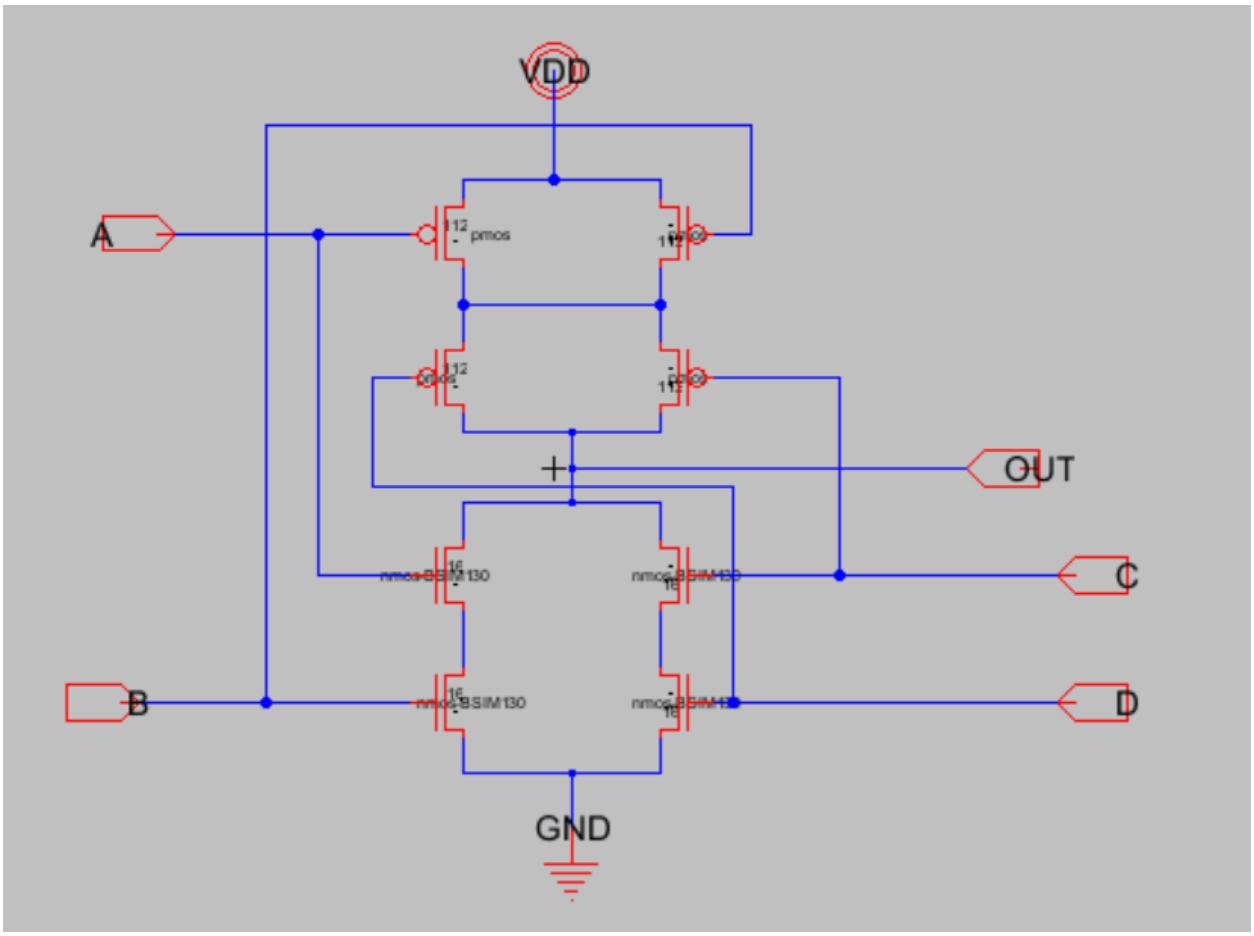


AOI22 {size 2}

Layout:



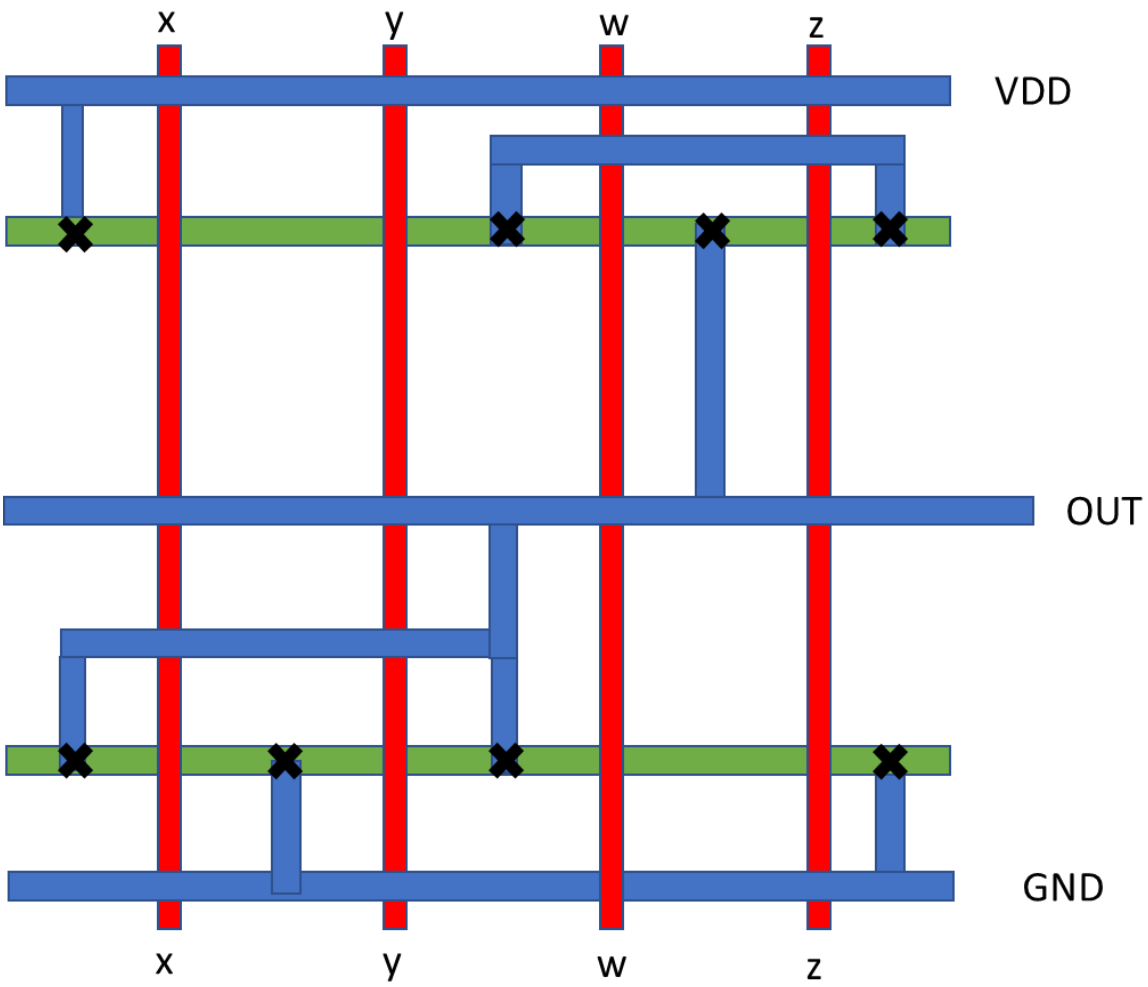
Schematic:



Cell 5

Stick Diagram

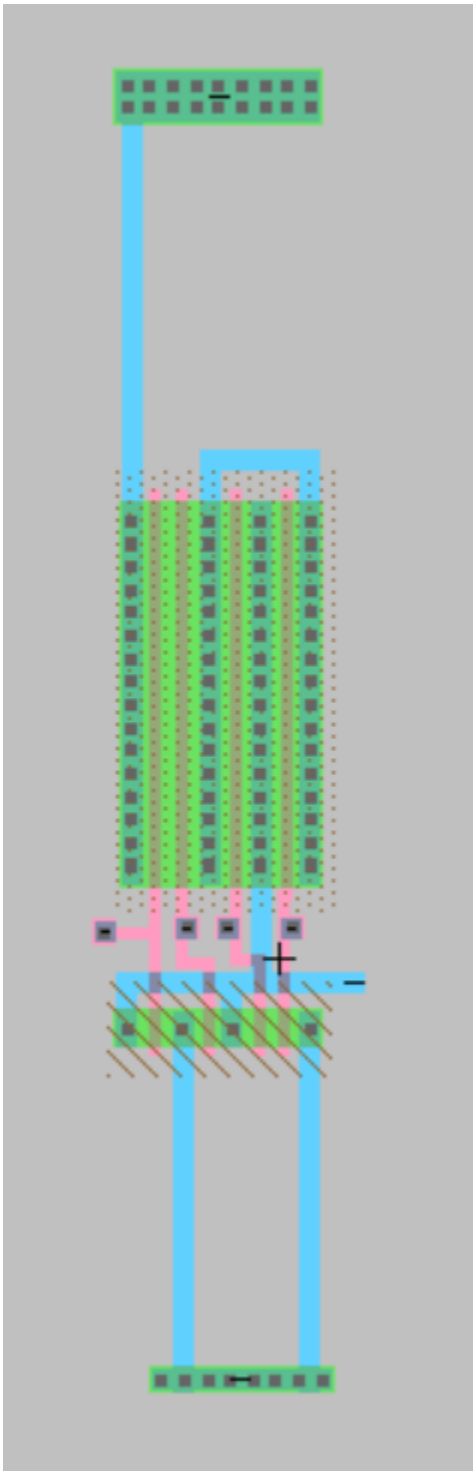
f(x,y,z,w) = (x+y+wz)'



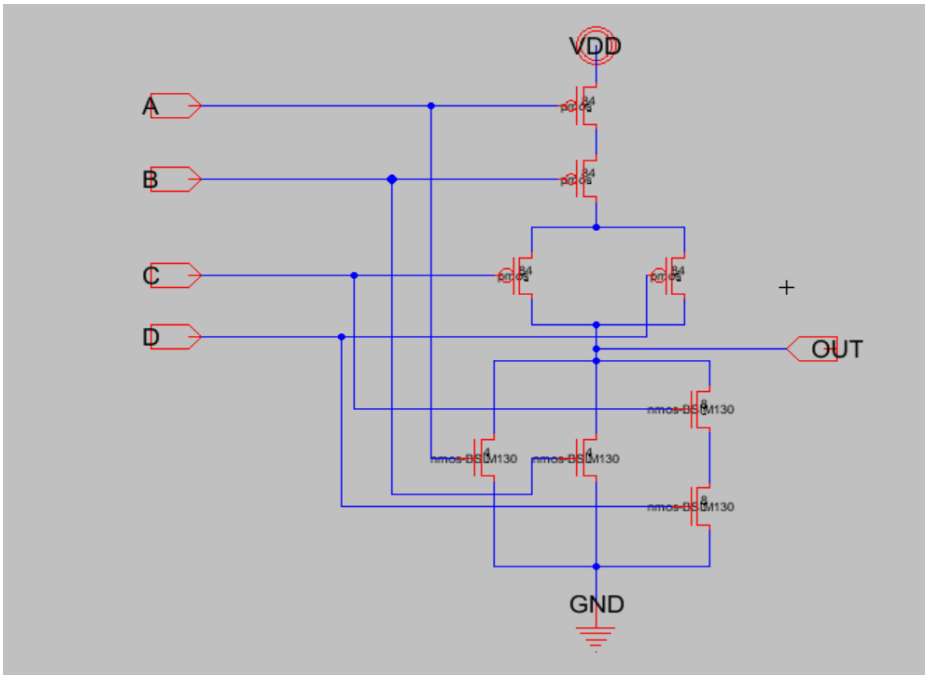
Height (size 1) = 136λ
Height (size 2) = 228λ

Cell 5 {size 1} - f(x,y,z,w) = (x+y+wz)’

Layout:

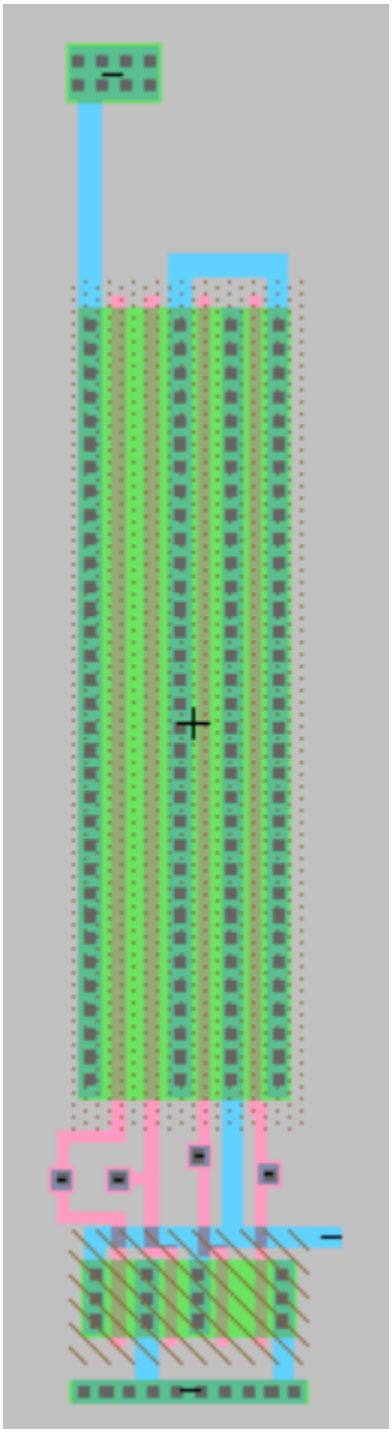


Schematic:

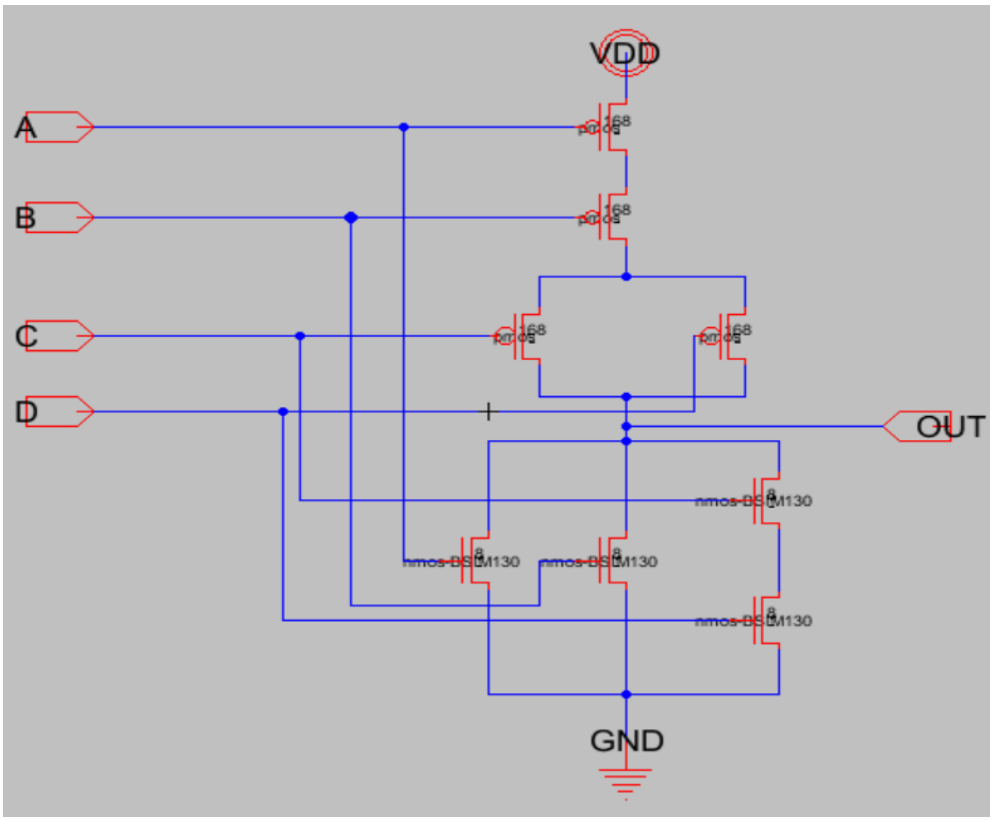


Cell 5 {size 2} - f(x,y,z,w) = (x+y+wz)’

Layout:



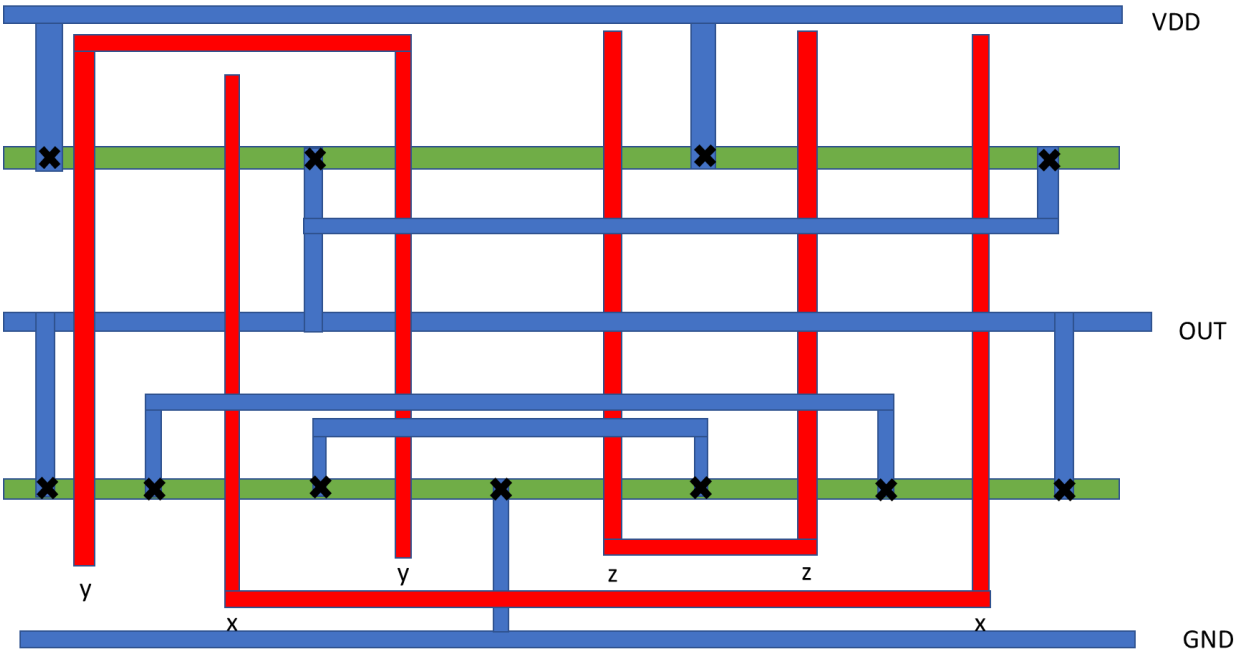
Schematic:



Cell 6

Stick Diagram

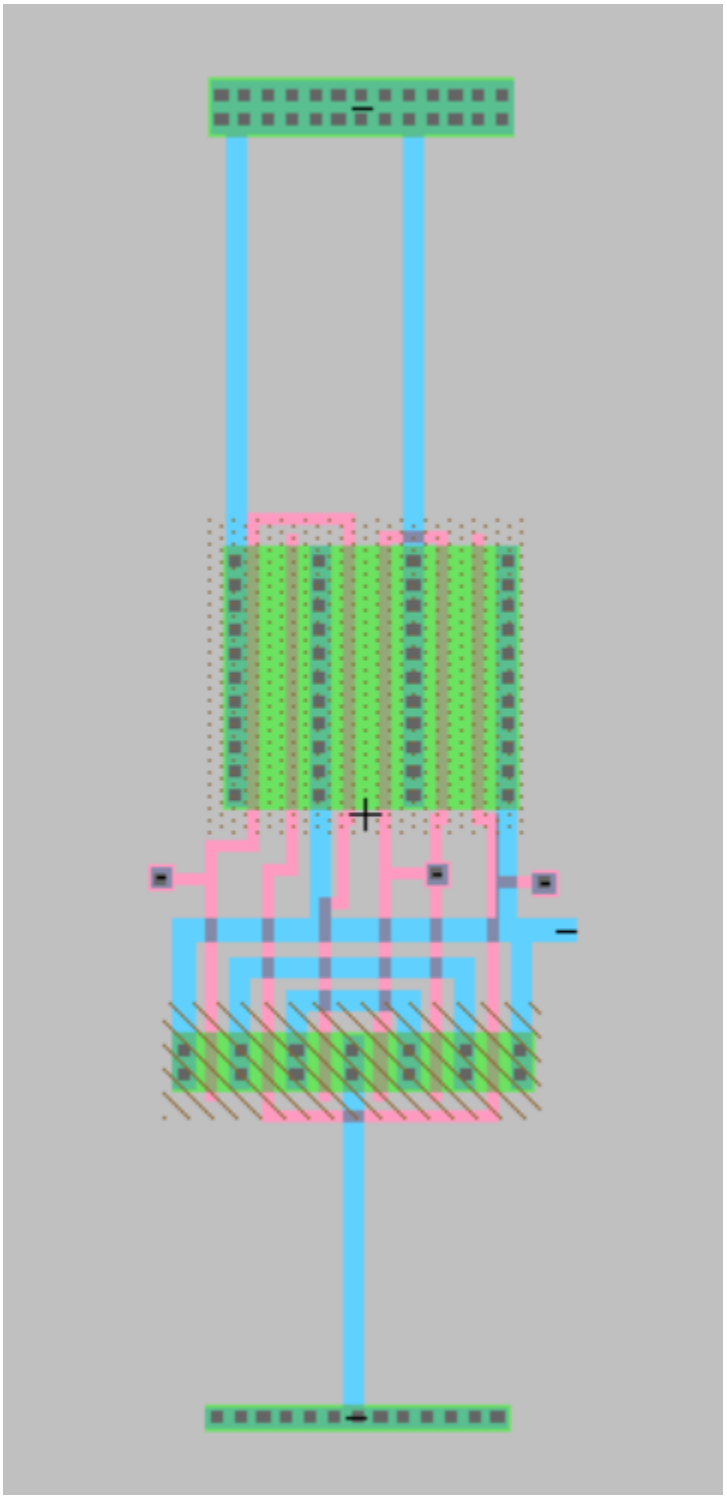
g(x,y,z) = [(x+y)(x+z)(y+z)]'



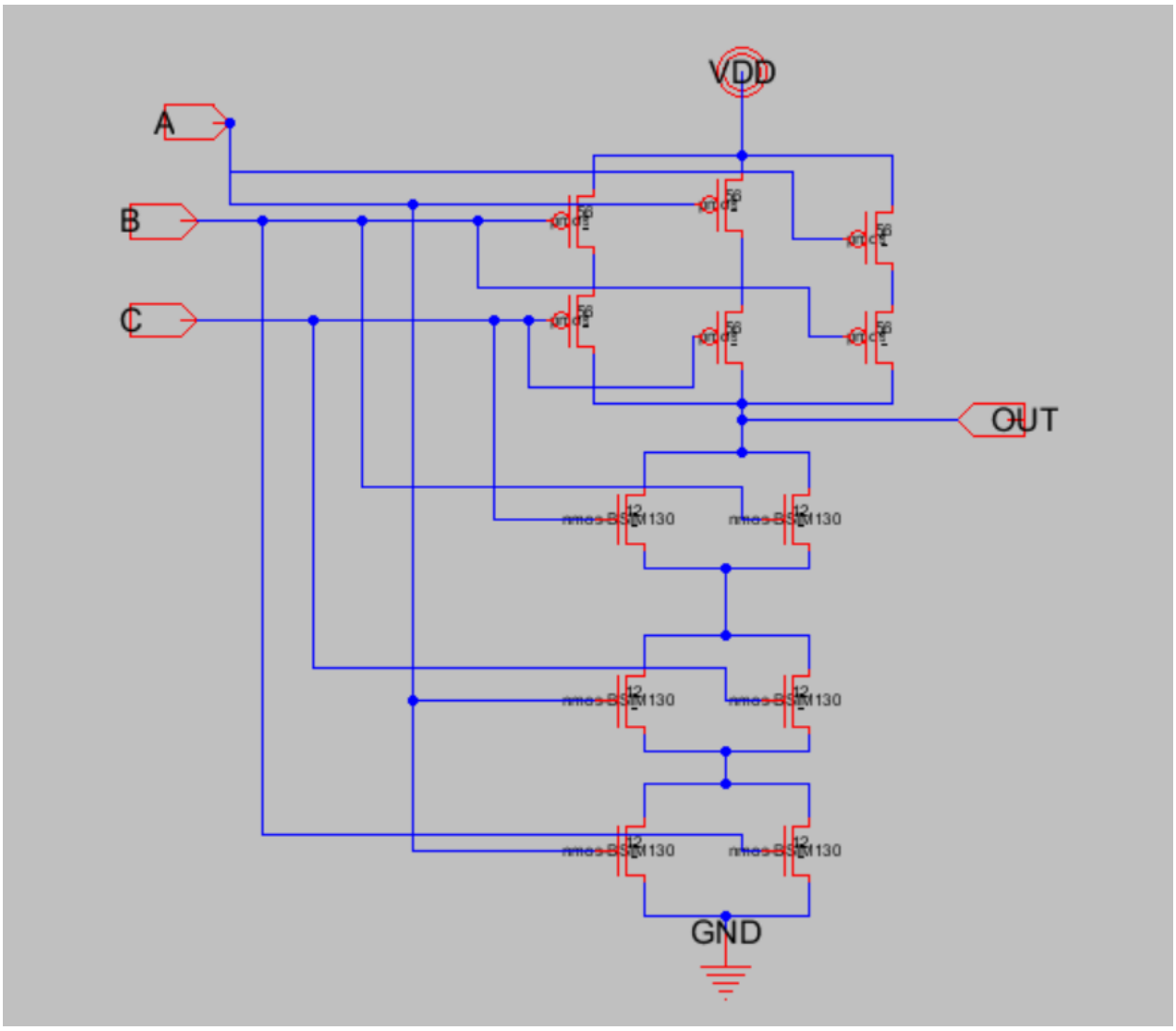
Height (size 1) = 128λ
Height (size 2) = 196λ

Cell 6 {size 1} - g(x,y,z) = [(x+y)(x+z)(y+z)]’

Layout:

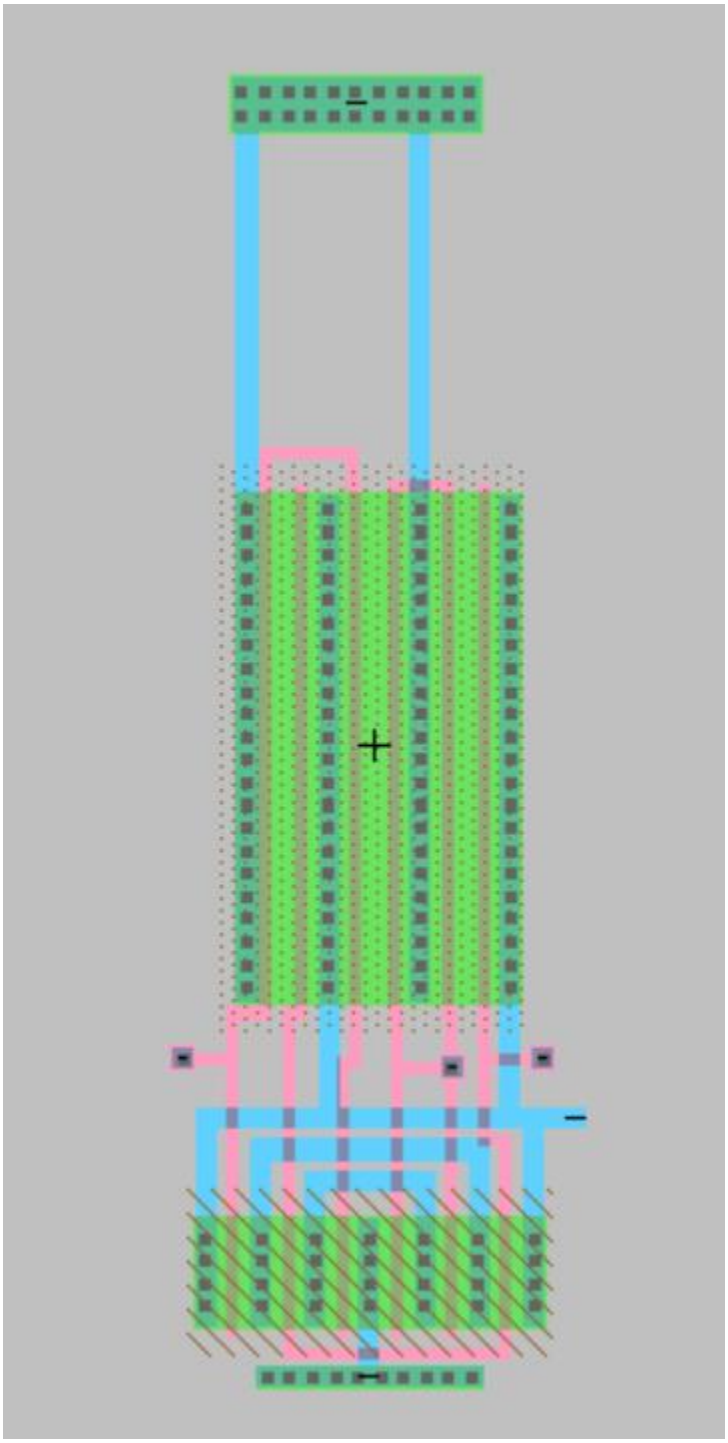


Schematic



Cell 6 {size 2} - g(x,y,z) = [(x+y)(x+z)(y+z)]’

Layout:



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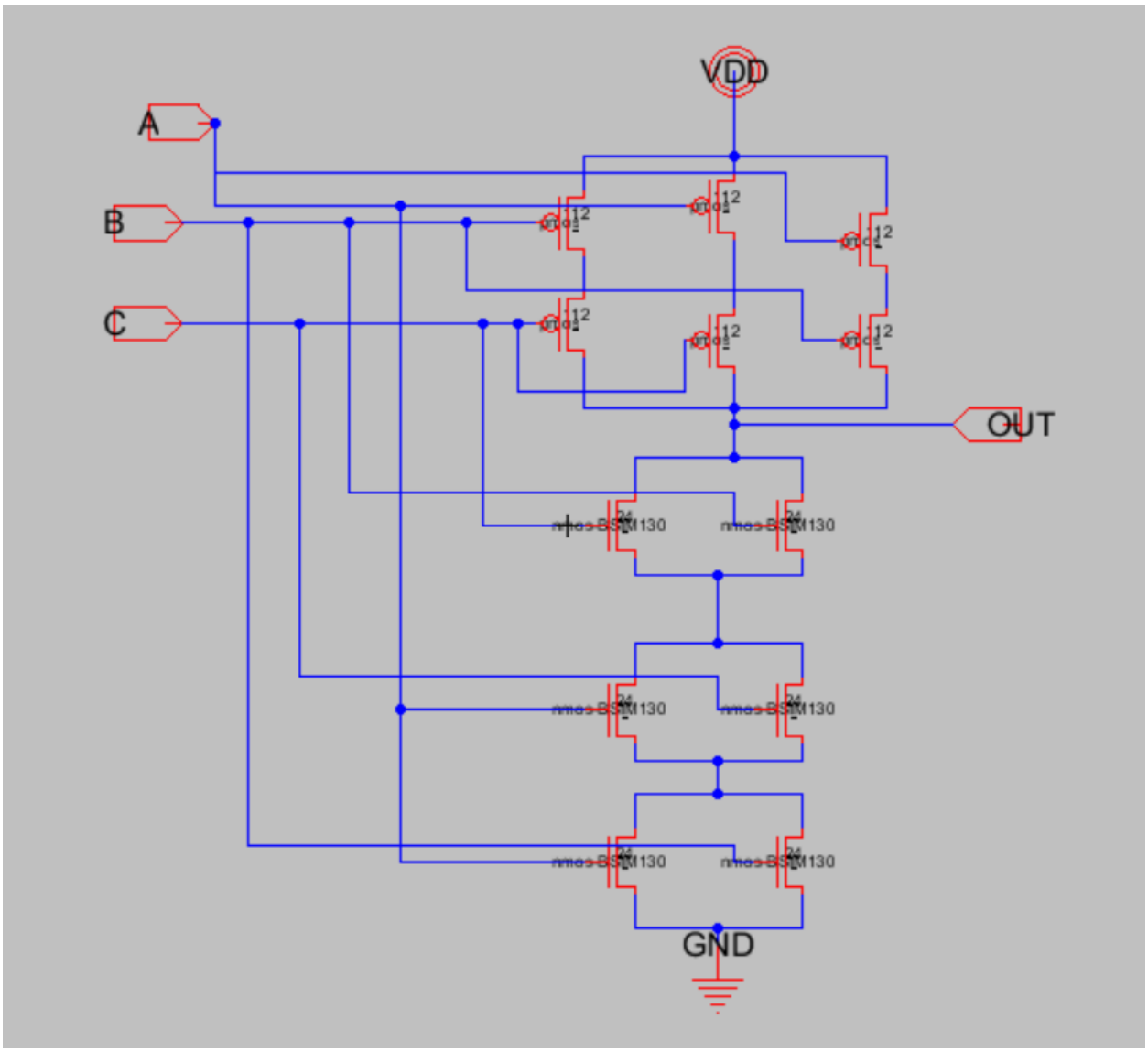
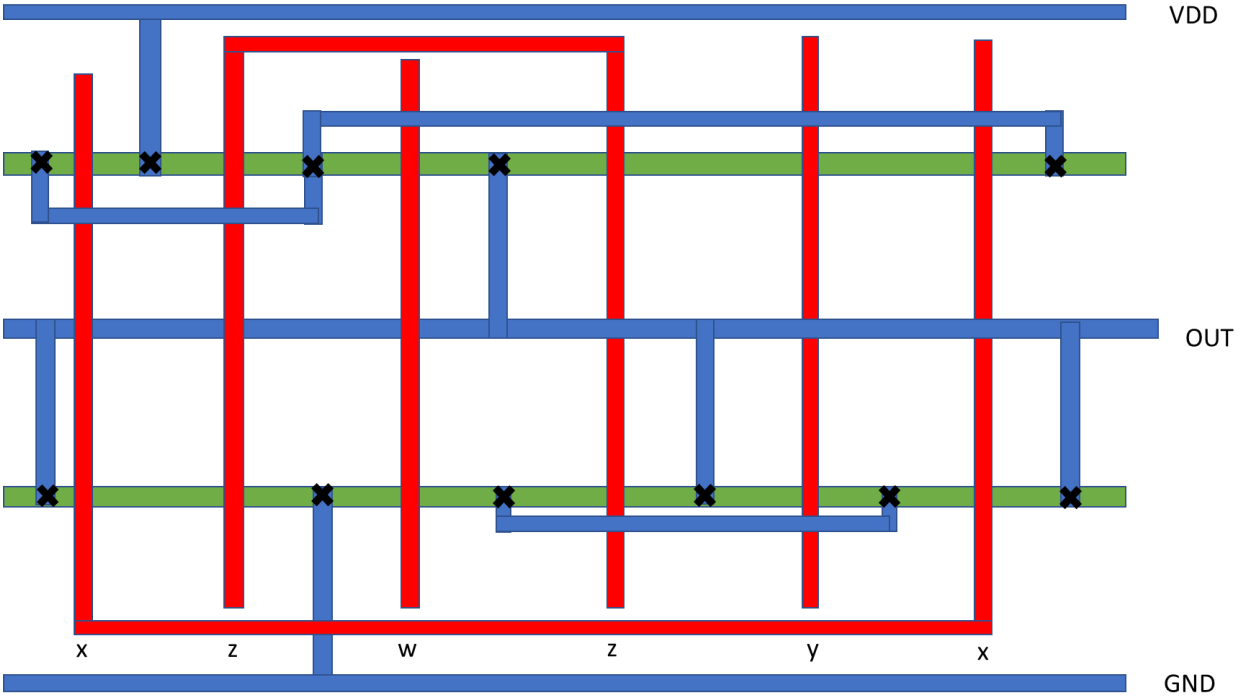


Cell 7

Stick Diagram

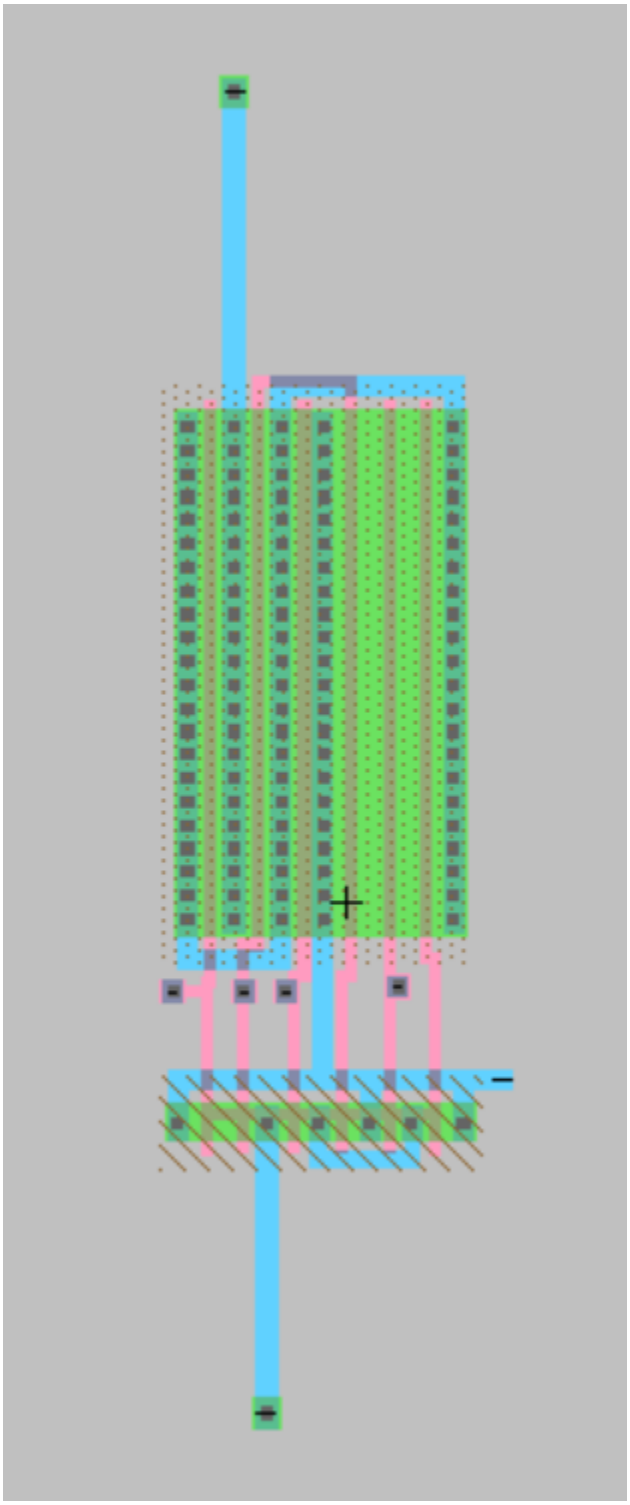
h(x,y,z,w) = [xz+(x+y+z)w]'



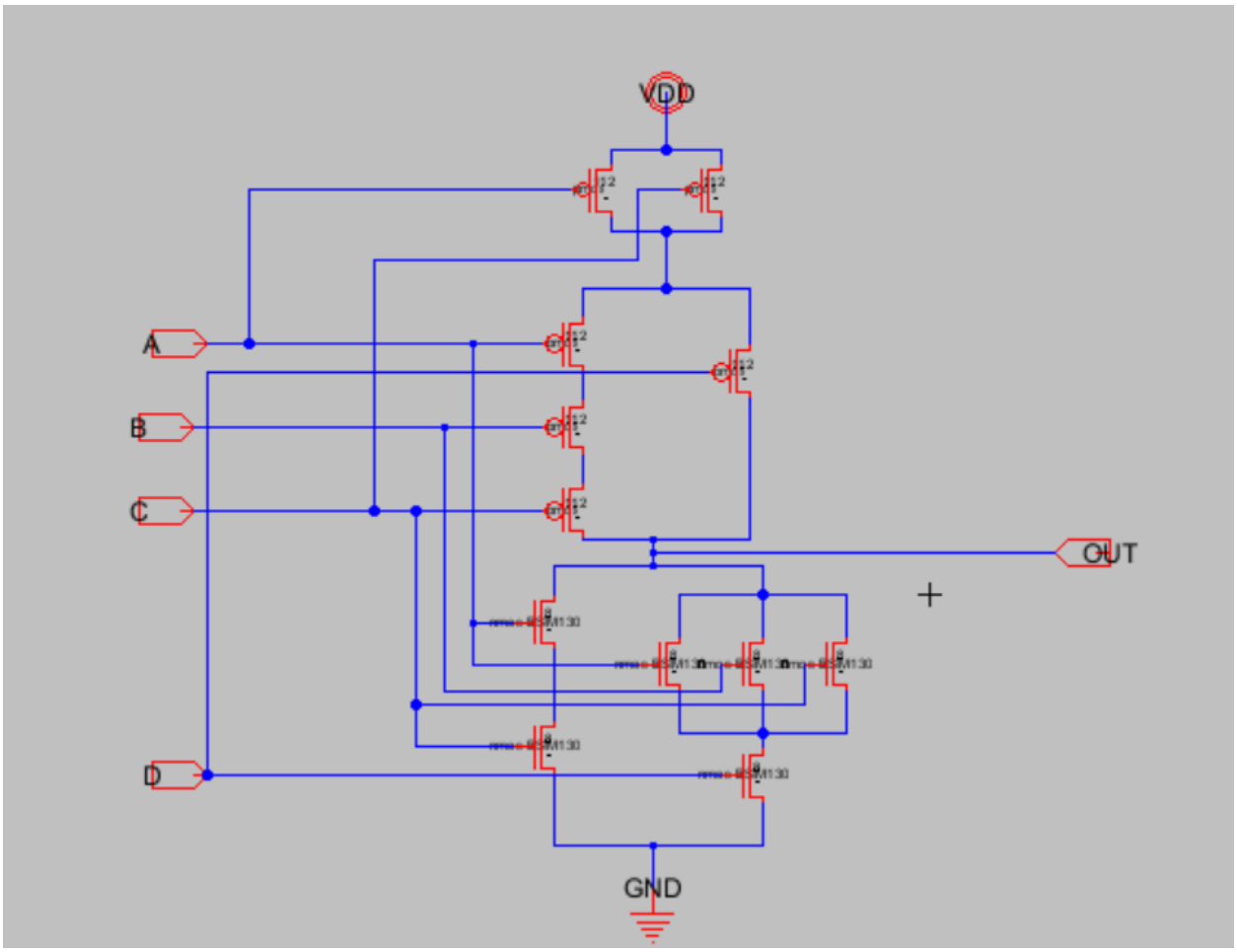
Height (size 1) = 172λ
Height (size 2) = 292λ

Cell 7 {size 1} - h(x,y,z,w) = [xz+(x+y+z)w]’

Layout:

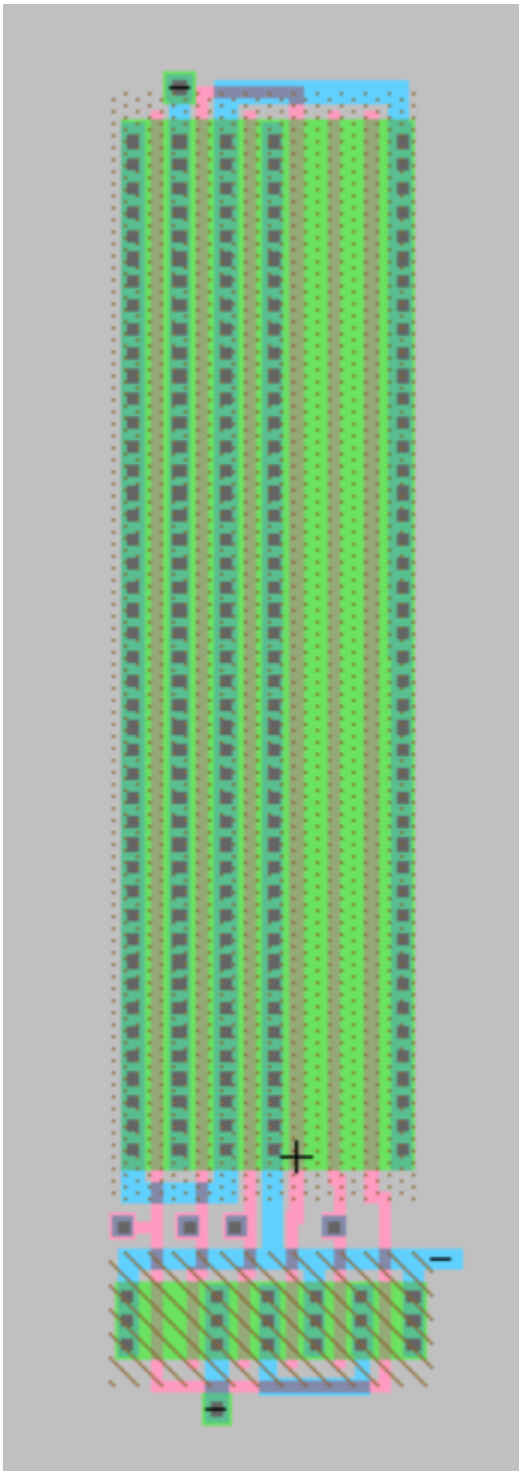


Schematic:

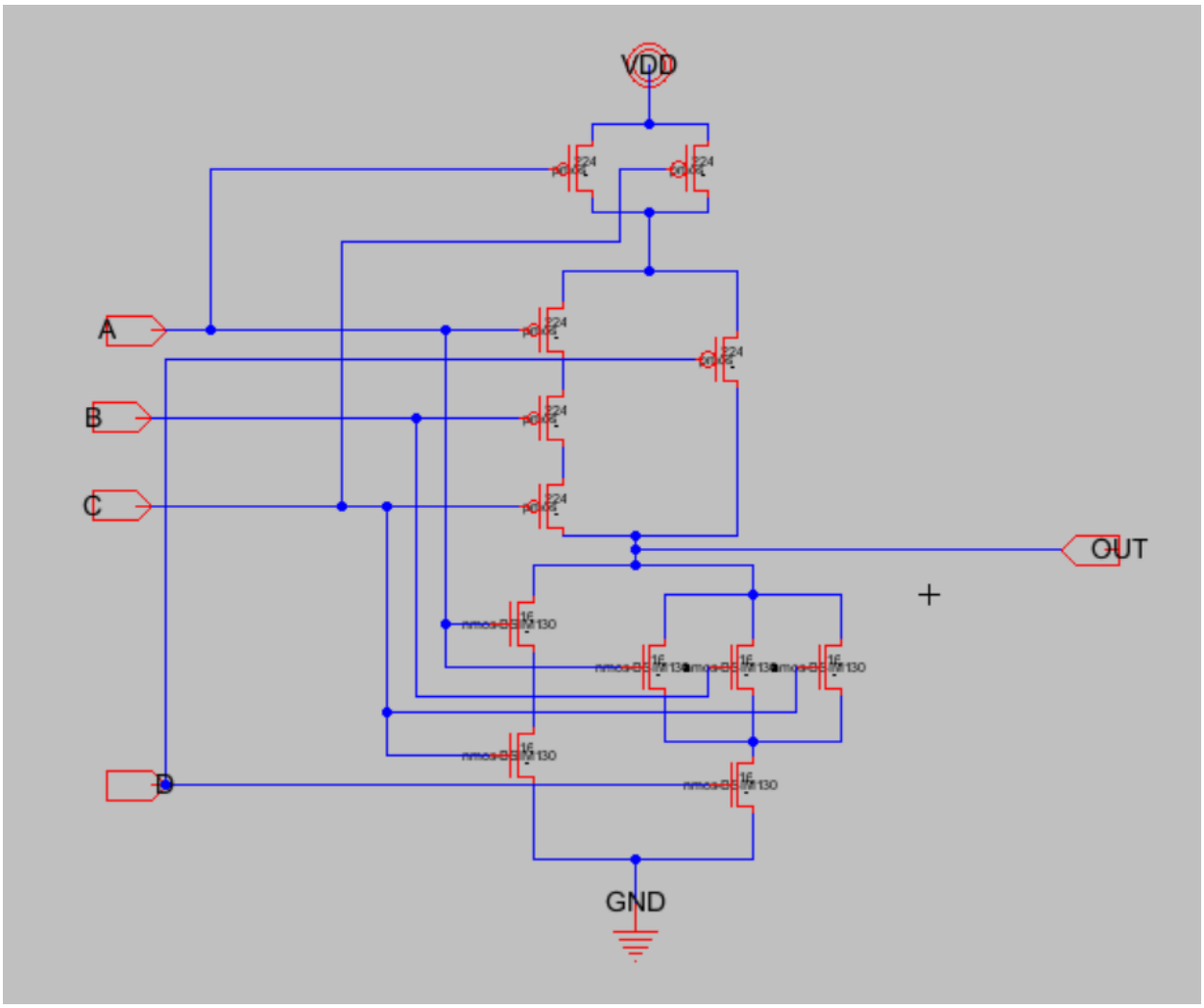


Cell 7 {size 2} - h(x,y,z,w) = [xz+(x+y+z)w]’

Layout:



Schematic:



Size 1 Inverter Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.0040E-10	5.7047E-10	6.8223E-10
100ps	2.4357E-10	3.0002E-10	4.1281E-10
400ps	4.4045E-10	5.0360E-10	6.1389E-10

Size 1 Inverter Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.0197E-09	6.0777E-09	6.1777E-09
125ps	5.3598E-09	5.4144E-09	5.5182E-09
500ps	5.8559E-09	5.9096E-09	6.0107E-09

Size 2 Inverter Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	4.5668E-10	5.0065E-10	5.7049E-10
125ps	2.1632E-10	2.4396E-10	3.0024E-10
500ps	3.9945E-10	4.4069E-10	5.0387E-10

Size 2 Inverter Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.9843E-09	6.0192E-09	6.0765E-09
125ps	5.3322E-09	5.3595E-09	5.4120E-09
500ps	5.8236E-09	5.8555E-09	5.9085E-10

Size 4 Inverter Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	4.3122E-10	4.5816E-10	5.0161E-10
125ps	2.0541E-10	2.1737E-10	2.4377E-10
500ps	3.7688E-10	4.0151E-10	4.4139E-10

Size 4 Inverter Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.9634E-09	5.985E-09	6.019E-09
125ps	5.3188E-09	5.332E-09	5.359E-09
500ps	5.8050E-09	5.824E-09	5.855E-09

Size 1 NAND Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.8807E-10	6.4034E-10	7.5122E-10
125ps	3.1242E-10	3.6840E-10	4.8043E-10
500ps	5.1648E-10	5.7077E-10	6.8294E-10

Size 1 NAND Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.9764E-09	6.0197E-09	6.1009E-09
125ps	5.3804E-09	5.4219E-09	5.5024E-09
500ps	5.8275E-09	5.8685E-09	5.9505E-09

Size 2 NAND Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.5784E-10	5.8736E-10	6.4112E-10
125ps	2.8394E-10	3.1197E-10	3.6805E-10
500ps	4.9051E-10	5.1737E-10	5.7149E-10

Size 2 NAND Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.9524E-09	5.9760E-09	6.0189E-10
125ps	5.3589E-09	5.3799E-09	5.4204E-09
500ps	5.8045E-09	5.8267E-09	5.8688E-09

Size 1 NOR Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	4.89615E-10	5.5079E-10	6.5641E-10
125ps	2.54065E-10	3.0221E-10	4.0372E-10
500ps	4.34678E-10	4.9525E-10	5.9218E-10

Size 1 NOR Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.1200E-09	6.1732E-09	6.2804E-09
125ps	5.4494E-09	5.5105E-09	5.6288E-10
500ps	5.9507E-09	6.0052E-09	6.1137E-10

Size 2 NOR Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	4.5408E-10	4.9141E-10	5.5175E-10
125ps	2.3261E-10	2.5512E-10	3.0297E-10
500ps	4.0246E-10	4.3678E-10	4.9538E-10

Size 2 NOR Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.0938E-09	6.1198E-09	6.1721E-09
125ps	5.4197E-09	5.4499E-09	5.5098E-09
500ps	5.9241E-09	5.9509E-09	6.0038E-09

Size 1 AOI22 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.90698E-10	5.7764E-10	7.4571E-10
125ps	3.36530E-10	3.8877E-10	4.9137E-10
500ps	5.26136E-10	6.4210E-10	6.8201E-10

Size 1 AOI22 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.18713E-09	6.11569E-09	6.44615E-09
125ps	5.56180E-09	5.65874E-09	5.84553E-09
500ps	6.02724E-09	6.27347E-10	6.29039E-10

Size 2 AOI22 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.6019E-10	5.2674E-10	6.4286E-10
125ps	3.1174E-10	3.3686E-10	3.8788E-10
500ps	5.0149E-10	5.9137E-10	5.7811E-10

Size 2 AOI22 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.14386E-09	6.02623E-09	6.27159E-09
125ps	5.51209E-09	5.56076E-09	5.65769E-09
500ps	5.98269E-09	6.18579E-09	6.11403E-09

Size 1 Cell 5 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.1437E-09	6.1906E-09	6.2808E-09
125ps	5.5508E-09	5.6000E-09	5.6980E-09
500ps	6.1437E-09	6.1906E-09	6.2808E-09

Size 1 Cell 5 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.2498E-10	6.8378E-10	7.9650E-10
125ps	3.8409E-10	4.4088E-10	5.5646E-10
500ps	6.2498E-10	6.8378E-10	7.9650E-10

Size 2 Cell 5 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.2595E-09	6.3080E-09	5.8192E-09
125ps	5.6669E-09	5.7182E-09	5.8192E-09
500ps	6.2595E-09	6.3080E-09	6.3991E-09

Size 2 Cell 5 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	5.6395E-10	6.0418E-10	4.3131E-10
125ps	3.5066E-10	3.7651E-10	4.3131E-10
500ps	5.6395E-10	6.0418E-10	6.7024E-10

Size 1 Cell 6 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.1891E-09	6.2273E-09	6.2983E-09
125ps	5.6286E-09	5.6655E-09	5.7374E-09
500ps	6.1891E-09	6.2273E-09	6.2983E-09

Size 1 Cell 6 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	7.2285E-10	7.8359E-10	9.0292E-10
125ps	5.1153E-10	5.6988E-10	6.9074E-10
500ps	7.2285E-10	7.8359E-10	9.0292E-10

Size 2 Cell 6 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.1704E-09	6.1897E-09	6.2261E-09
125ps	5.6098E-09	5.6282E-09	5.6659E-09
500ps	6.1704E-09	6.1897E-09	6.2261E-09

Size 2 Cell 6 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.9337E-10	7.2390E-10	7.8447E-10
125ps	4.7975E-10	5.1219E-10	5.7285E-10
500ps	6.9337E-10	7.2390E-10	7.8447E-10

Size 1 Cell 7 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.7036E-09	6.7355E-09	6.8179E-09
125ps	6.1683E-09	6.1994E-09	6.2832E-09
500ps	6.7036E-09	6.7355E-09	6.8179E-09

Size 1 Cell 7 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	7.1355E-10	7.3838E-10	8.0397E-10
125ps	5.0319E-10	5.2498E-10	5.8730E-10
125ps	7.1355E-10	7.3838E-10	8.0397E-10

Size 2 Cell 7 Tpdr			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.6778E-09	6.6851E-09	6.7229E-09
100ps	6.1394E-09	6.1459E-09	6.1854E-09
400ps	6.6778E-10	6.6851E-10	6.7229E-09

Size 2 Cell 7 Tpdf			
Transition/Cinv	Cinv	2Cinv	4Cinv
0ps	6.9616E-10	7.0209E-10	7.3463E-10
100ps	4.8920E-10	4.9290E-10	5.2214E-10
400ps	6.9616E-10	7.0209E-10	7.3463E-10