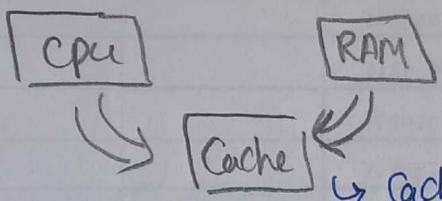
- Memory
  - Volatile "RAM"
  - non-volatile "ROM"
  - hybrid

- ROM
  - Mask program ROM ⇒ OTP (one time program ⇒ يُبرمج مرة واحدة) "firmware", "BIOS chip"
  - PROM ⇒ programmable ROM, OTP ⇒ user
  - EPROM ⇒ Erasable ——— , noise corruption
    - ↳ UV [5:30] min

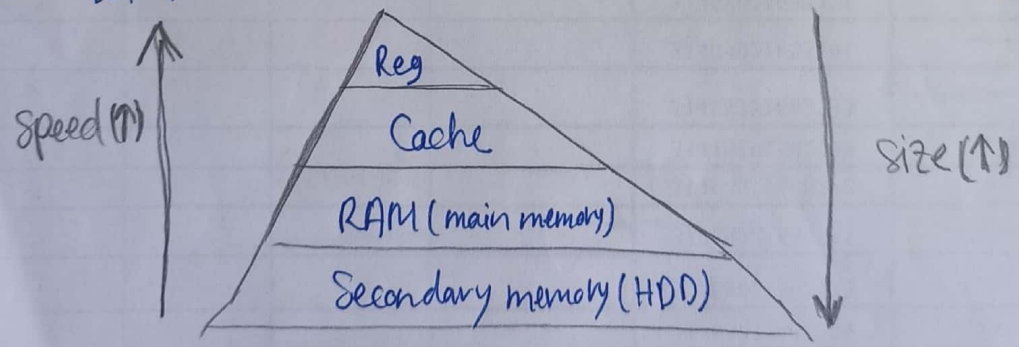
- Hybrid (↑ RAM: R/W, ROM: non-volatile)
  - E^2PROM (→ Internal/External) ⇒ Electrical EPROM, Endurance = 100,000, Byte access, ↑ cost per bit
  - Flash ⇒ Block access → sector by sector, Endurance = 10,000, ↓ cost per bit
  - NVRAM ⇒ SRAM + battery / SRAM + EEPROM + battery, ↑ cost per bit

* Cache Memory: "SRAM"



↳ Cache Memory + Controller
↳↳ Cache Coherence

$$\text{hit ratio} = \frac{\text{Cache hit}}{\text{Total}}$$



* FPU: Floating Point Unit
* MPU: Memory Protection Unit
* MMU: ——— Management ———

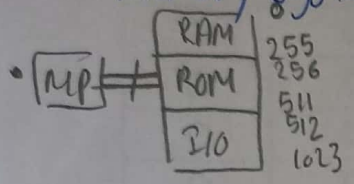
CPU → Cache → MPU → RAM

divide RAM into Ranges

ARCH

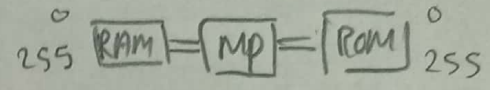
Von-neumun "PC"

- one memory system

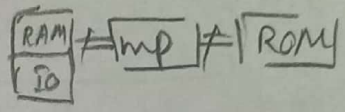


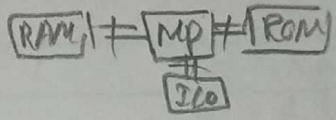
- memory mapped
- Can't support pipeline → (CISC)

Harvard "MCU"

- 

- port mapped





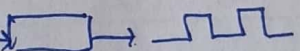
- support pipeline (+ RISC)

*pipeline :

F d e
F d e
F d e

- RISC ⇒ 1 inst/cycle

*

*Clocks
- electrical : RC_oscillator
- Mechanical : power → 

		RC	Ceramic Reasonator	Crystal Oscillator
Cost		↓ (✓)	~	↑
Accuracy		↓	~	↑ (✓)
Settling time		↕	~	↓ (✓)
noise	Temp	↓	↑ (✓)	↑ (✓)
	EMI	↓	↑ (✓)	↑ (✓)
	Vibr	↑ (✓)	↓	↓