

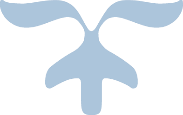
Credit Hours System

CMPN301 – Computer Architecture

Cairo University Faculty of Engineering



Phase 1 -Arch Project



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# Types of Instructions (32bits)

Opcode (5 bits):

|  |  |
| --- | --- |
| 2 bits (Type of instruction) | 3 bits (its number in this type) |

00 🡪 R-Type

01 🡪 I-Type

10 🡪 J-Type

We have 8 registers, so we need 3 bits to identify which register in the register file. (Rs, Rt, Rd).

Each register is 32bits.

There are 2 additional registers: PC and SP.

## R-Type: (total so far: 14 out of 32)

|  |  |  |  |
| --- | --- | --- | --- |
| OpCode (5) | Rs (3) | Rt (3) | Rd (3) |

## I-Type: (total so far: 27 out of 32)

|  |  |  |  |
| --- | --- | --- | --- |
| OpCode (5) | Rs (3) | Rt (3) | Immediate value or address (16) |

## J-Type: (total so far: 21 out 32)

|  |  |
| --- | --- |
| OpCode (5) | Target (number of jumped instructions) (16) |

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Control Signals | | | | | | | | | | Type | OpCode |
| X | ALU Op | ALU Src | Branch | Mem  Read | Mem  toReg | Mem  Write | Reg  Write | Reg  Dst |  |  | X | X |
| NOP |  |  |  |  |  |  |  |  |  |  |  |  |
| HLT |  |  |  |  |  |  |  |  |  |  |  |  |
| SETC |  |  |  |  |  |  |  |  |  |  |  |  |
| NOT Rdst |  |  |  |  |  |  |  |  |  |  | R |  |
| INC Rdst |  |  |  |  |  |  |  |  |  |  | R |  |
| OUT Rdst |  |  |  |  |  |  |  |  |  |  | R |  |
| IN Rdst |  |  |  |  |  |  |  |  |  |  | R |  |
| MOV Rsrc, Rdst |  |  |  |  |  |  |  |  |  |  |  |  |
| SWAP Rsrc, Rdst |  |  |  |  |  |  |  |  |  |  |  |  |
| ADD Rdst,  Rsrc1, Rsrc2 |  |  |  |  |  |  |  |  |  |  | R |  |
| SUB Rdst,  Rsrc1, Rsrc2 |  |  |  |  |  |  |  |  |  |  | R |  |
| AND Rdst,  Rsrc1, Rsrc2 |  |  |  |  |  |  |  |  |  |  | R |  |
| IADD Rdst, Rsrc  ,Imm |  |  |  |  |  |  |  |  |  |  | I |  |
| PUSH Rdst |  |  |  |  |  |  |  |  |  |  | I |  |
| POP Rdst |  |  |  |  |  |  |  |  |  |  | I |  |
| LDM Rdst, Imm |  |  |  |  |  |  |  |  |  |  | I |  |
| LDD Rdst,  offset(Rsrc) |  |  |  |  |  |  |  |  |  |  | I |  |
| STD Rsrc1,  offset(Rsrc2) |  |  |  |  |  |  |  |  |  |  | I |  |
| JZ Imm |  |  |  |  |  |  |  |  |  |  | J |  |
| JN Imm |  |  |  |  |  |  |  |  |  |  | J |  |
| JC Imm |  |  |  |  |  |  |  |  |  |  | J |  |
| JMP Imm |  |  |  |  |  |  |  |  |  |  | J |  |
| CALL Imm |  |  |  |  |  |  |  |  |  |  | J |  |
| RET |  |  |  |  |  |  |  |  |  |  |  |  |
| INT index |  |  |  |  |  |  |  |  |  |  |  |  |
| RTI |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset |  |  |  |  |  |  |  |  |  |  |  |  |
| Interrupt |  |  |  |  |  |  |  |  |  |  |  |  |