Project Proposal for Digital Logic Design

Project title:	**UACRT Serial Communication (**Universal Asynchronous correction Receiver/Transmitter)

Students:

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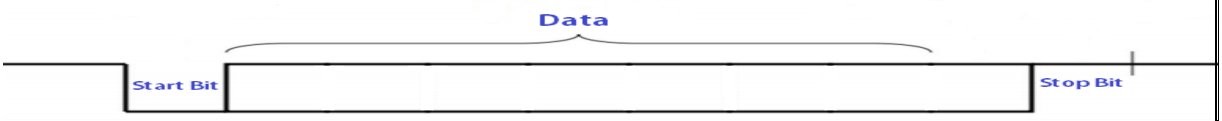
Project Description :

In our project we need to send data from one device to another with the smallest number of wires so we choose UART serial communication to use, but UART detect errors only in case one bit has changed and can't detect when 2 Bit have changed by parity and not correct it so we looked for ways to detect error and correct it, finally we choose hamming method to correct it.

UART SERIAL DATA FLOW:-



UART DATA (9 Bit With parity)

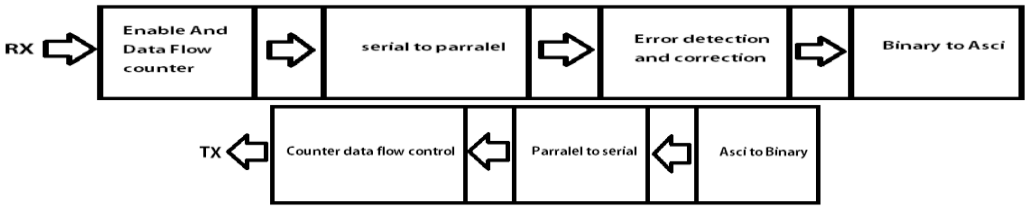
D1	D2	D3	D4	D5	D6	D7	D8	parity

UACRT DATA (11 Bit With parity)

D7	D6	D5	P4	D4	D3	D2	P3	D1	P2	P1

By replace UACRT DATA With UART DATA we can detect error and correct it (Detect any number of errors But correct it in one error case)

We can process this data throw this diagram:-



In Asci Block we save data with parity (11 Bit)

Expected start date:	THU 5-3 (week 4)
Expected completion date:	Sun 19-4 (weak 11)