It is an Integrated circuit (Ic). it is consist of CPU only. ALU CU it is composed of. registers ALU cu registers cache it is called 1. - Micro pro cessor (MP) CPU -Hicro Processing unit (MPU) - Central processing unit (CPU) It is an integrated circuit. Micro controller 1. It is composed of CPUIC> peripherals mensy Deripherals it is called i. -Micro controller (Mc) -Micro controller (MC) -Micro controller unit (MCU) Mcu Embedded systems: it is a special purpose computer used to do a one or arew tasks with real-time constrains. Single Purpose embedded | > (5w) (Constrains) Mechatronic systems: it is the system in which mechnical hardware are integrated with information - driven Systems like as micro controller. processors-it is the number of bits of data which can be processed by the cpu at the same time. - it is the number of data lines which are Fed to the CPU, - an n-bit CPU means that its ALU operates on n-bit data word per clock cycle. - A Processor with an n-bit register can address up to (2"n) addresses. CHANTER KIND OFFICE

Test terminate	micro-processor	micro Controller
29	in a single chip. in a single chip. it composed of Cu registers Arithmetic logic unit (Alu) used to perform calculations control unit (Cu) used to decode instructions cregisters it is asmall, fast storage are for data & instructions	- it is a small computer used to perform specific task - it composed of: CPU Themory peripherals + all of this are on a single chip,
E (MAY)	Von-Neumann	Harvard
	- it used the same memory and bus to store the data & and the instruction. - We can't Fetch instruction and store data for anthor instruction at the same time. - it used in computers & PCs.	-it store instruction & data in separate memory and use different busses to access them. - we can Fetch instruction and store data For anthor instruction at the same time. -it used in MCU & SOC
	CISC	RISC
No.	- Complex instruction set computer. - large instruction set. - Multi cycles Per instruction. - Complex hardware. - expensive. - used in laptops & computers. - made by a intel Amd	- wsed in Smart Phones based on Arm Processor
NA.	RAM	
	- Volatile memory	- stow - large
	- Based on Mos Fet - Read / write memory,	- Read only memory.

(Read only Memory)

(PROM)

- it is a blank memory when it manufactured.
- it can be Programmed by the user.
- -it is programmed by burnner.
- the data store in it cannot be deleted or modified.
- it is OTP no server all availles (vomit) (100 all data is deleted. (one-time programmable)

Programmable ROM

(Masked ROH)

- it is programmed during the manfacturing it by the Ic-manfacturer.
- the duta store in it cannot be deleted or modified.
- cheaper
- it is OTP (one-time Programmable)



- it is can be programmed many times.
- we use UV-EPROM todelete the contents OF EPROM.
- we com't use electrical signals to delete its content.
- . We can't delete a Particular part of data

Evasable PROM

RAM (Random Access Memory)



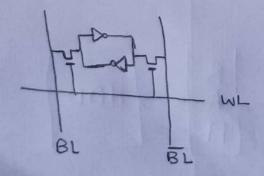
- Static Random Access memory
- bit carrier consists of 6T
- it is volatile memory
- Data access in it is Faster then
- it is not require refreshing time to save its content.
- it is work by inverse Feed back
- it is expensive
- it has more complex design.
- we can acress data at any time.

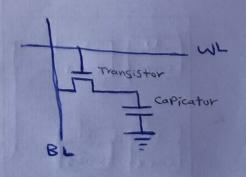


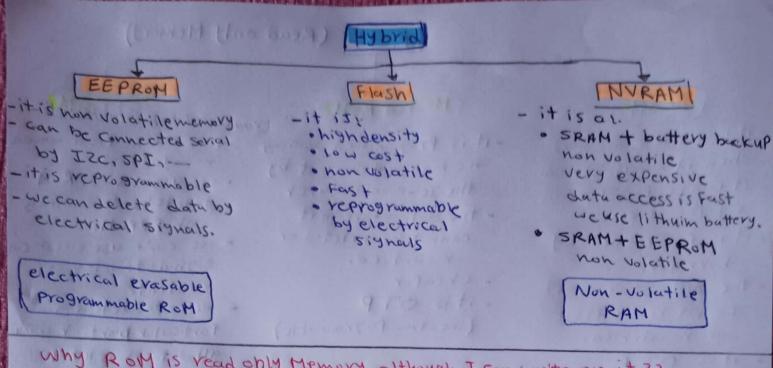
- Dynamic Random Access Hemory.
- bit carrier consist of IT & IC
 - it is volatile memory
 - Duta access is Faster than Flash
 - it is require refreshing time to save its content (64 ms)
 - it is cheap.

Mod of strive of third gos sitted

- We comnot access the doctor when DRAM is refreshed.







Why RoM is read only Memory although I can write on it??

because in the normal operations, the cpu does not have the capability to write to ROM. but we can write on it by external device (burner). or there is a special contiguration within the system Wherein the CPU is granted access to write on ROM.

1- Carche	Lz Cache	126
- in the core - in the cpu - smallest cache - cache level by one Primary internel - Fastest cache	- not in the care - but in the CPU	L3 Cache - not in the cpu - but in the mother board - Largest cache - cache - called — cache lever three externel - 5 lowest cache.
Coved Cove 1 Cove Cove 3 Cove 3 Cove 3 Cove 3	LZ L3 R A M	HDD

SRAM I Byte unlimited expensive Fast PRAM I Byte unlimited expensive Fast PRAM Washed EPRAM X one Time evase data expensive Fast EPRAM X bowney data (see the datasheet) Fast Fiash X Byte (see the datasheet) Madevate Fast to read Fiash Fiash X Byte unlimited expensive Fast Fiash Fiash								
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Wolatile Writable ensessize max exase cast Perbyte	Belleri	*	(See the data sheet)	by the	_	×	Flash	orid
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volatile writable erase size max exase			unlimited	By tc	7	1	SRAM	М
	st per byte		max exasc	emse size	writable	Volatile	TYPE	