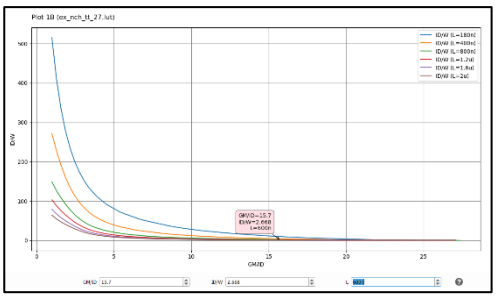
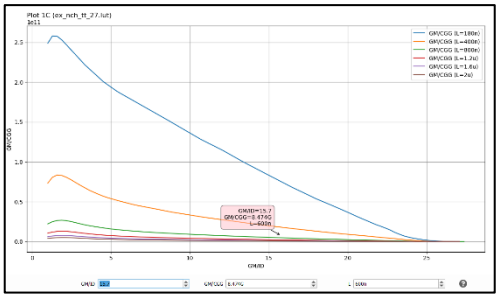
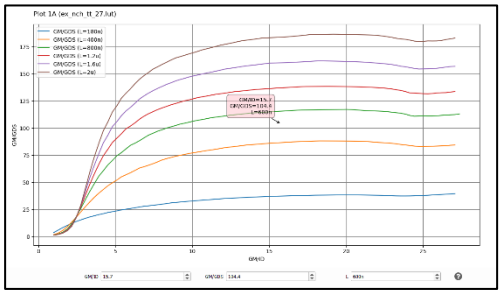
Lab09

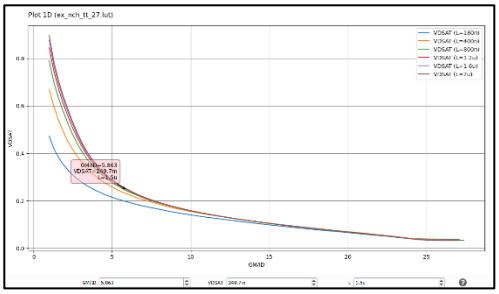
Part01

NMOS LOAD:

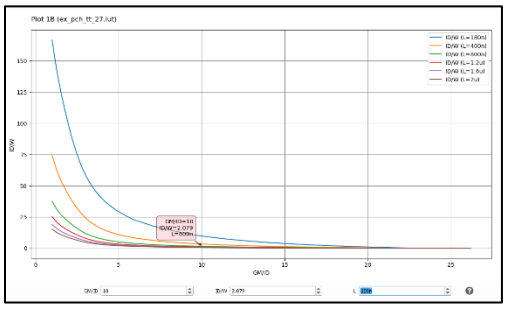


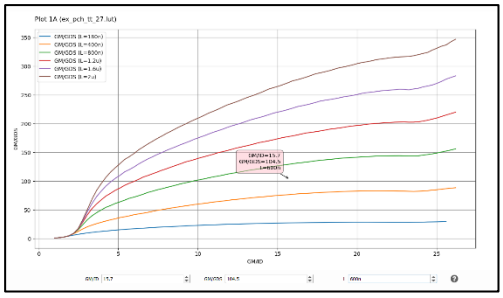


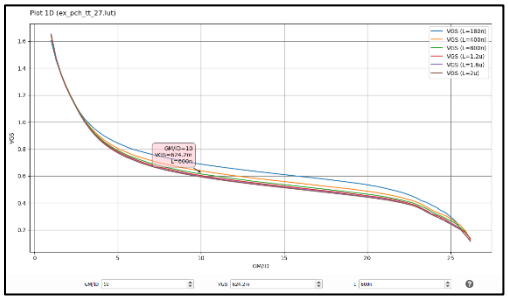


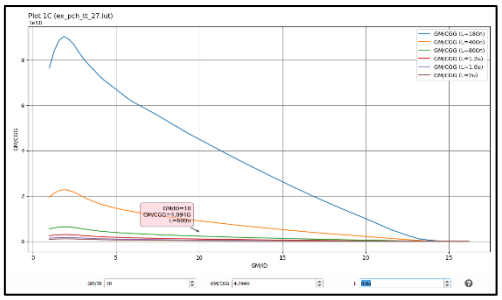


PMOS LOAD:

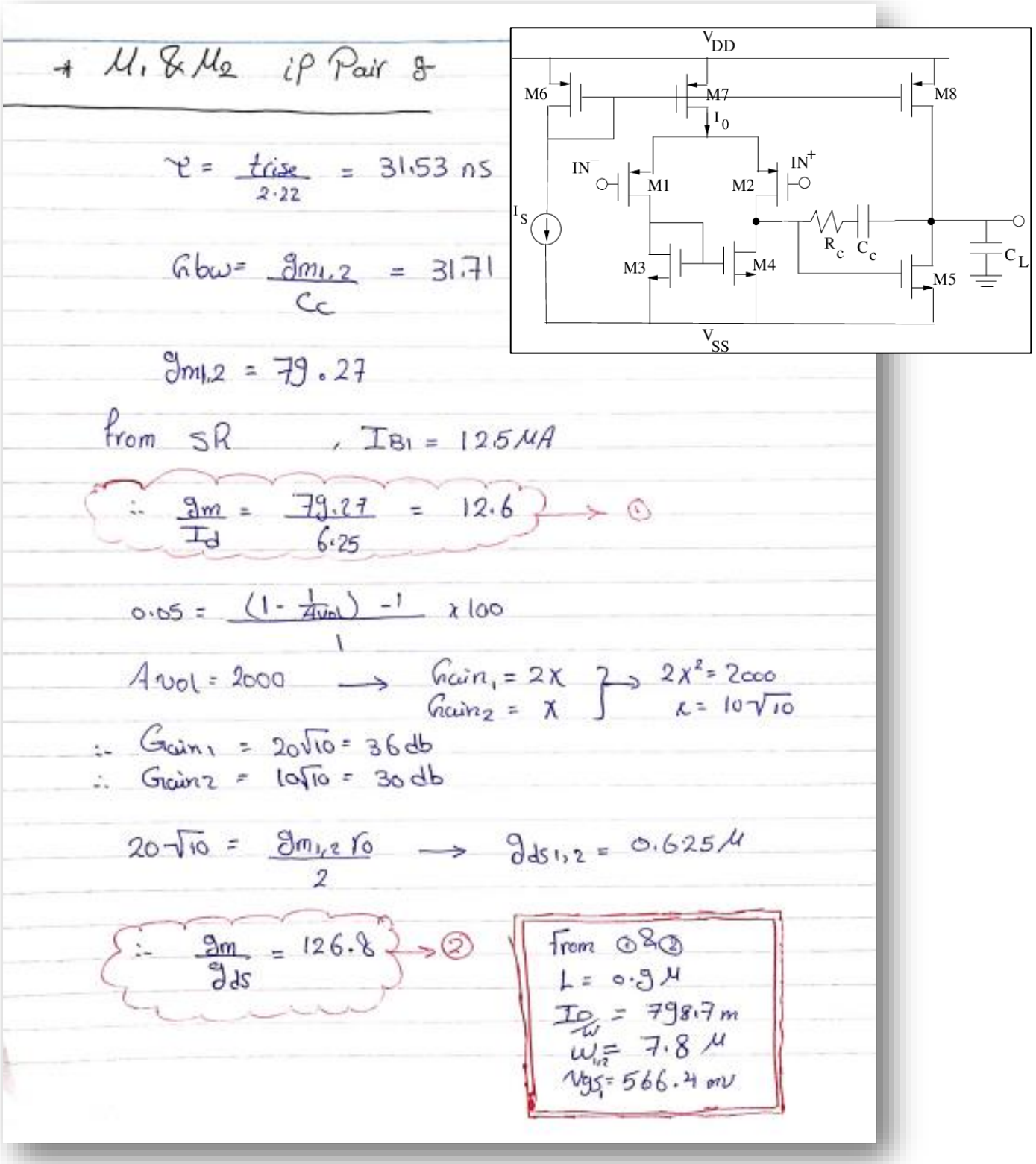








1) Detailed design procedure and hand analysis.



* M6, M7, M8 tail Current Sources :-

$V_{icm\,high} < -V_{gs_1} - V_{ds_7} + V_{dd}$

$1V$ ← $0.556V$ ← 1.8

$\therefore V_{ds_7} = 0.234\,V$

from Swing $V_{dd} - 2V_{ov} = 1.4$

$V_{ds_8} = 0.2V$ ← take This value.

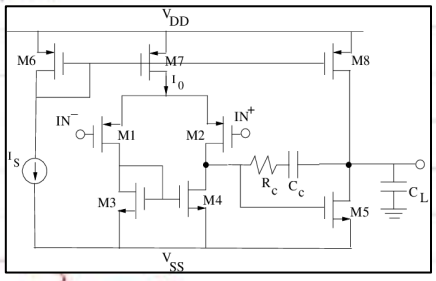
from CMRR $A_{vcm} = 36 - 74 = -38\,db$

$$\therefore -38\,db = \frac{1}{2 g_{m_{3,4}} r_{o_7}} = 0.0125$$

assume Current load $\frac{g_m}{I_d} = 10$

$\therefore g_{m_{3,4}} = 62.5$

$\therefore g_{ds_7} = 1.5625$



from V^* → $\left(\frac{g_m}{I_d}\right)_7 = \frac{2}{V^*} = 10$ → ①

$\therefore g_m = 125$

→ $\left(\frac{g_m}{g_{ds}}\right)_7 = 80$ → ②

$L = 580n = 0.58\mu$

$\frac{I_d}{W} = 2.166$

$W_7 = 5.77$

* M_6, M_7 & M_8 Same L Because Thy come from Current mirror also Same $\frac{g_m}{I_d} = 10$

$W_7 = 5.77 \longrightarrow 12.5\,\mu A$

$W_8 = x \longrightarrow 47.5\,\mu A$

$W_6 = x' \longrightarrow 10\,\mu A$

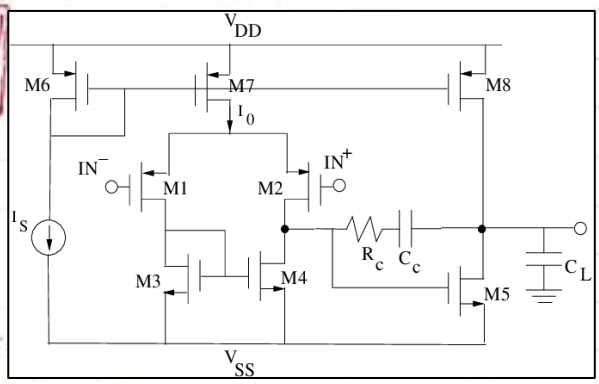
$W_8 = x = 22\mu$

$W_6 = x' = 4.66\mu$

$g_{ds7} = 1.5625 \longrightarrow 12.5\,\mu A$

$g_{ds8} = x \longrightarrow 47.5\,\mu A$

$g_{ds8} = x = 5.93\mu$

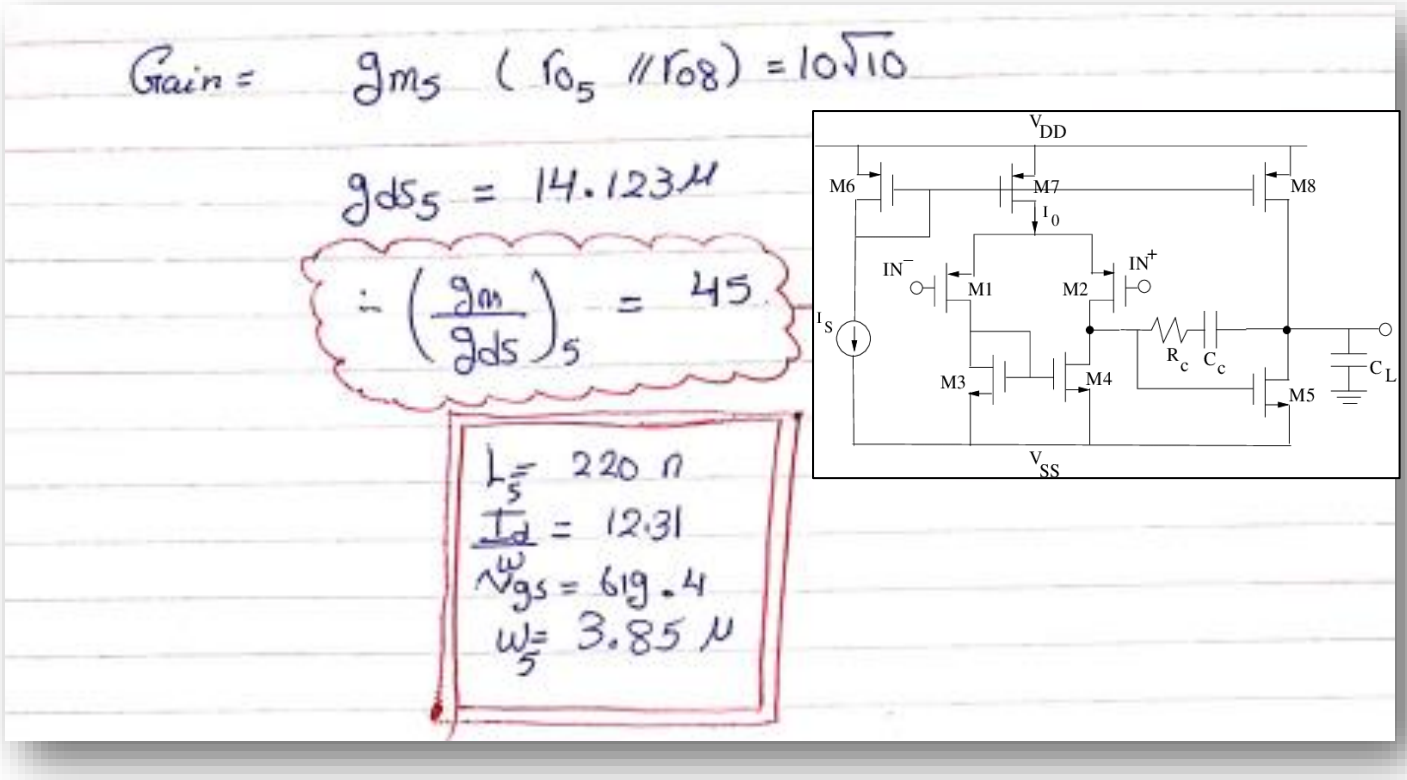


* M_5 $\frac{G_{m2}}{C_L} = \frac{4G_{m1}}{C_c}$

$G_{m2} = 8G_{m1} = 631.16$ =

$I_{B2} = 4I_{B1}$ => but we have budget ∴ $I_{B2} = 47.5\,\mu A$

$\frac{g_{m5}}{I_d} = 13.35$ → ①



- **Vgs of 2nd input stage should follow Vgs of 1st stage current mirror so**

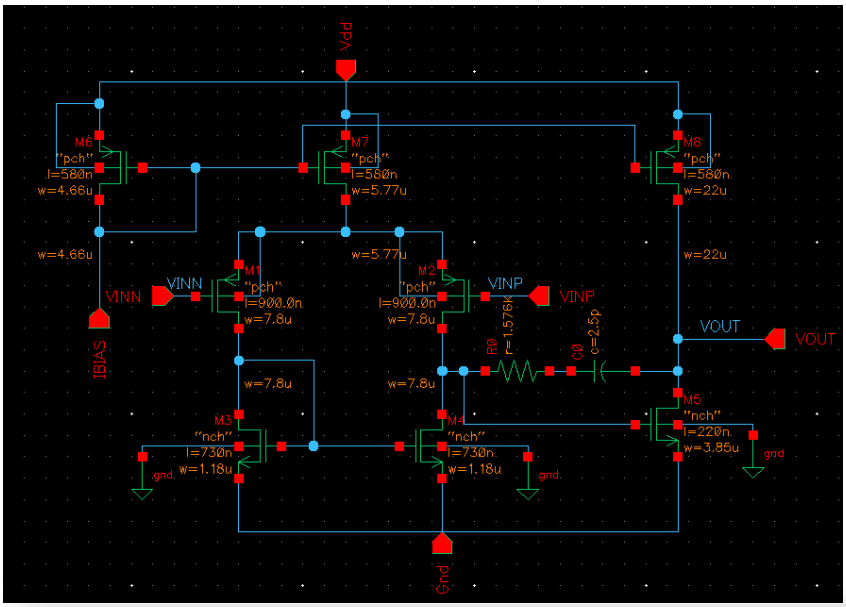
  $Vgs_{3,4}$=619mv , gds=0.62u and Id=6.25u

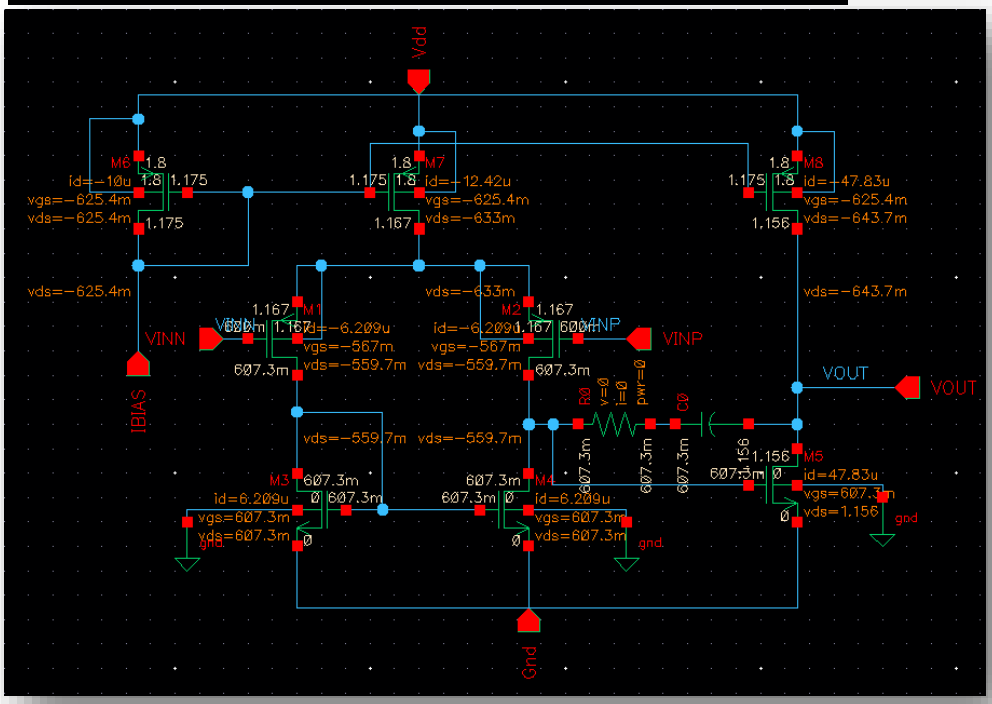
  From ADT L=730n W=1.18u

  Gm/id=10.27 > 10 Condition satisified

- **Rz = 1/Gm2 =1.567 kohm**

Parameter	W	L	Gm	ID	Gm/ID	Vov	V*
Input Pair M0&M1	7.8u	0.9u	79.27u	6.25u	12.6	15.25m	160.18m
Tail CS M7	5.77u	580n	125u	12.5u	10	195.19m	200.74m
Current Mirror M6	4.66u	580n	100u	10u	10	195.19m	200.74m
CM Load M3&M4	1.18u	730n	82.62u	6.25u	10.27	200.33m	151.56m
2nd input M5	3.58u	220n	628u	47.5u	13.35	139.85m	151.56m
Output Load M8	22u	580n	475u	47.5u	10	195.19m	200.74m





- **Yes,current and gm and vgs are exactly equal for both branches**
- **1st stage output should be close to VDD/3** Well Defined
- **2nd stage should be close to Vdd/2** iLL Defined so output higher by $\Delta I R_o$

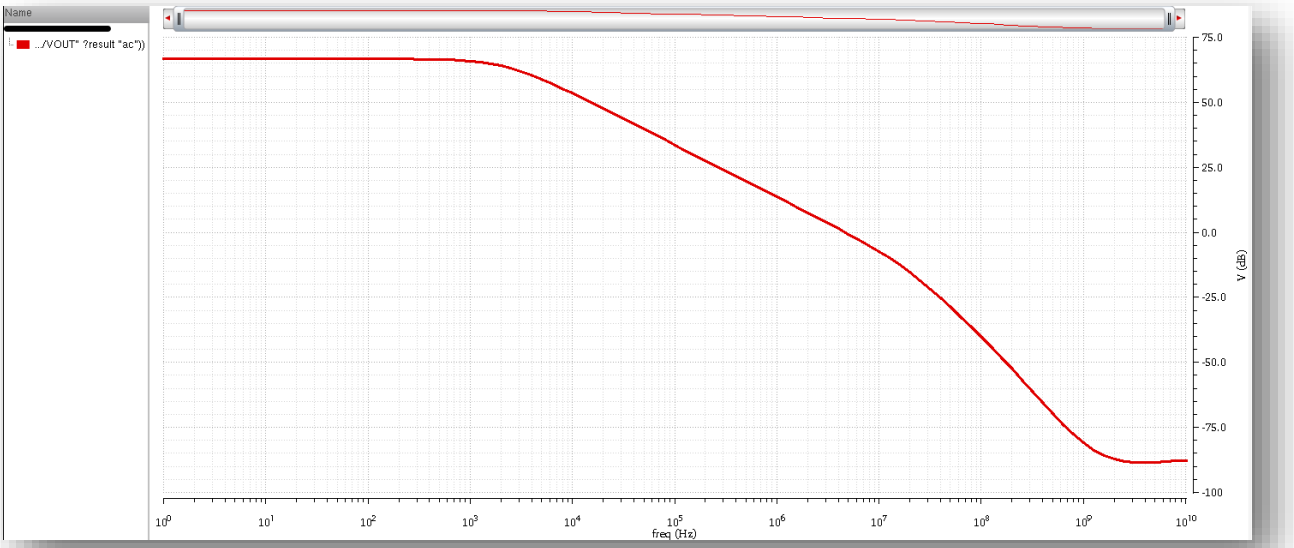
	1
vid	0.000
/VOUT (V)	1.156
/I0/net18 (V)	607.3E-3

1) Diff small signal ccs:

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_ANALOG2:Labo9_TB:1	ymax(dB20(v("/VOUT" ?resul...	66.53			
ITI_ANALOG2:Labo9_TB:1	ymax(mag(v("/VOUT" ?result...	2.121k			
ITI_ANALOG2:Labo9_TB:1	unityGainFreq(v("/VOUT" ?r...	4.685M			
ITI_ANALOG2:Labo9_TB:1	bandwidth(v("/VOUT" ?result...	2.241k			
ITI_ANALOG2:Labo9_TB:1	gainBwProd(v("/VOUT" ?res...	4.764M			

- **diff gain (in dB) vs frequency.**

  66.52db



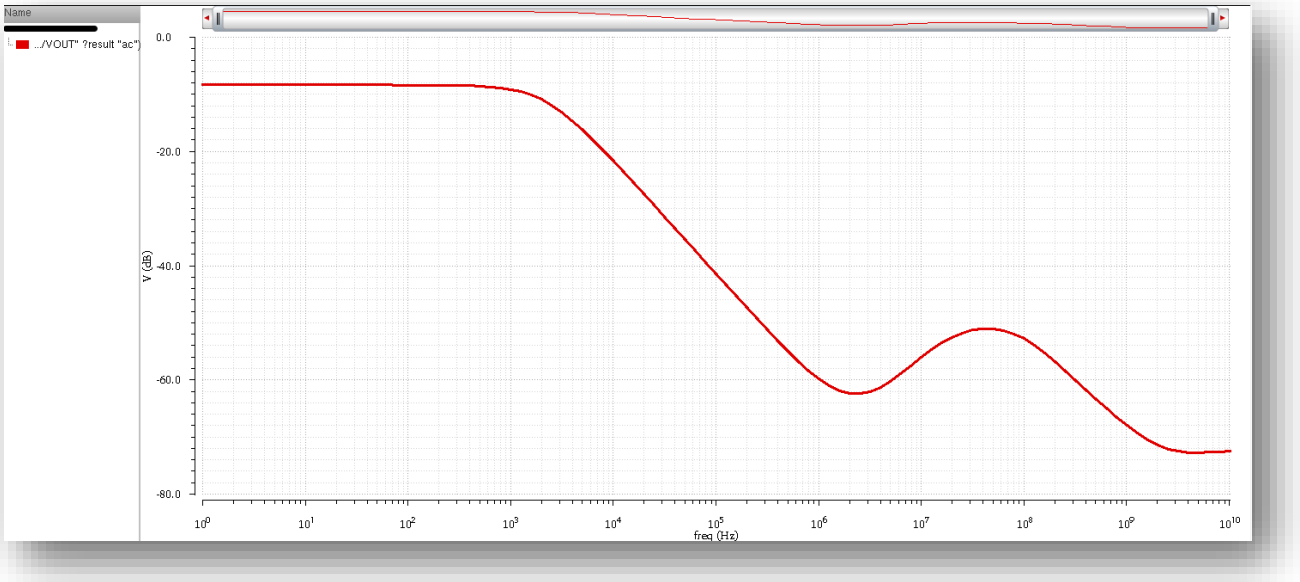
Parameter	Hand	Simulation
Gain	2000	2121
GBW	5M	4.76M
BW	2500	2241

- **GBW and BW less than calculated due to parasetics.**

2)CM small signal ccs:

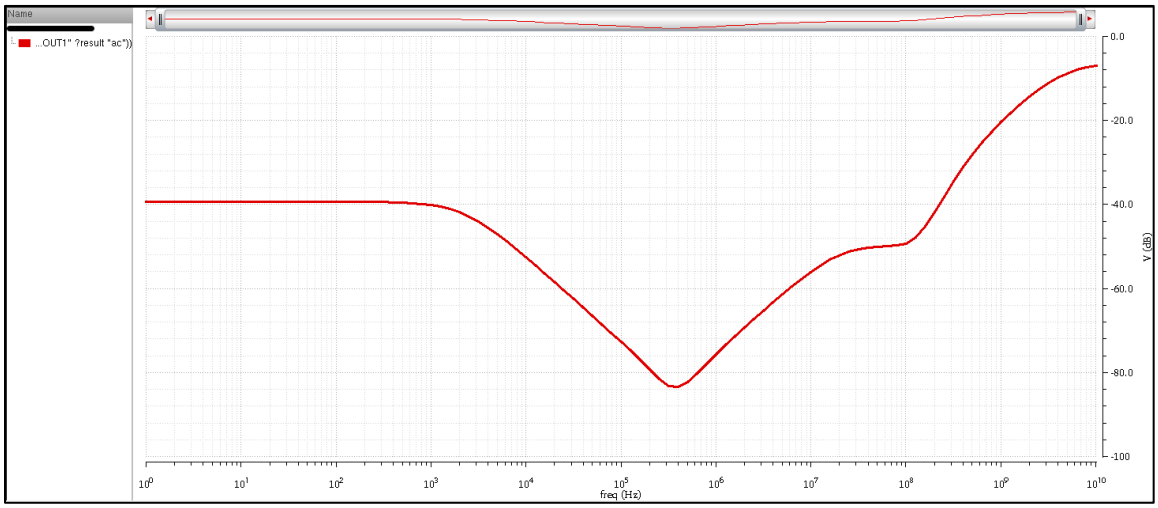
- **CM gain in dB vs frequency.**

  -8.4db this gain after multiplying by 2nd stage gain = 30db



Parameter	Hand	Simulation
Gain	-38db	-39.34db

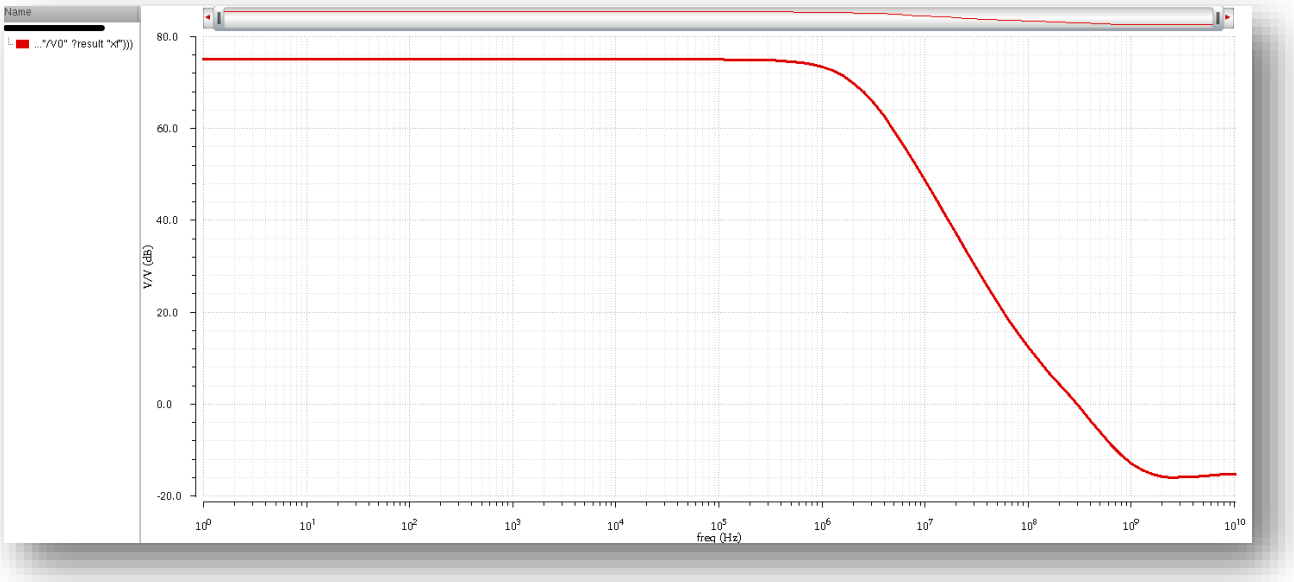
- **At the first stage**



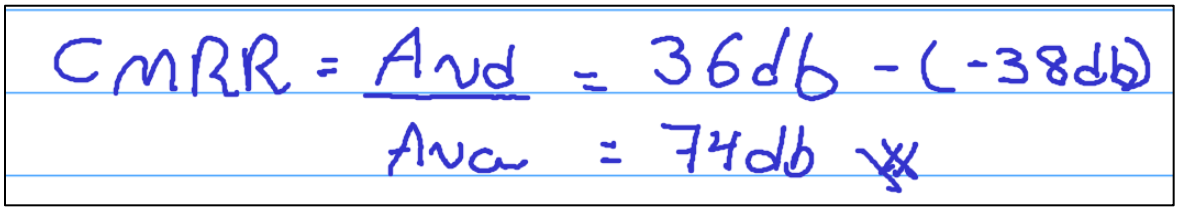
3) (Optional) CMRR:

- **CMRR in dB vs frequency**

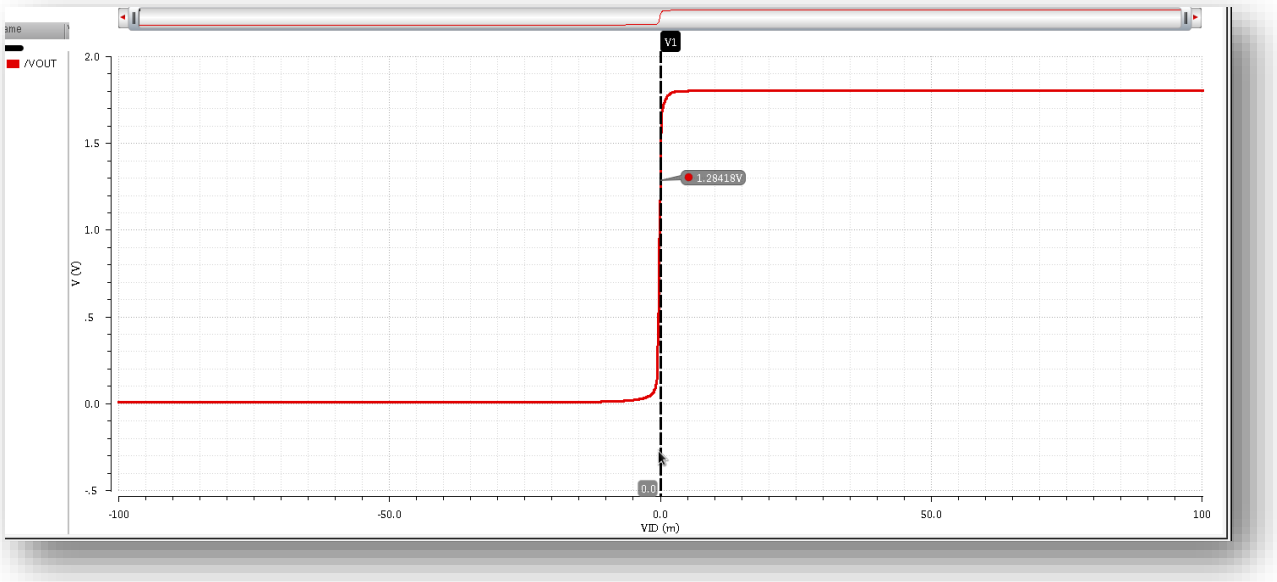
  75db



Parameter	Hand	Simulation
CMRR	74db	75db

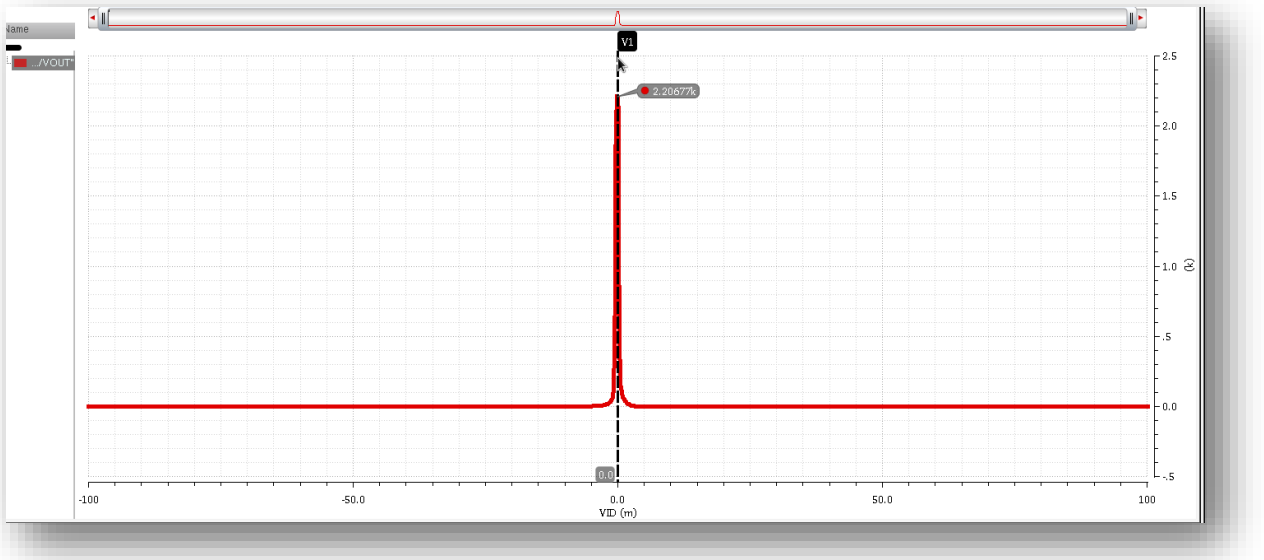


4) (Optional) Diff large signal ccs:



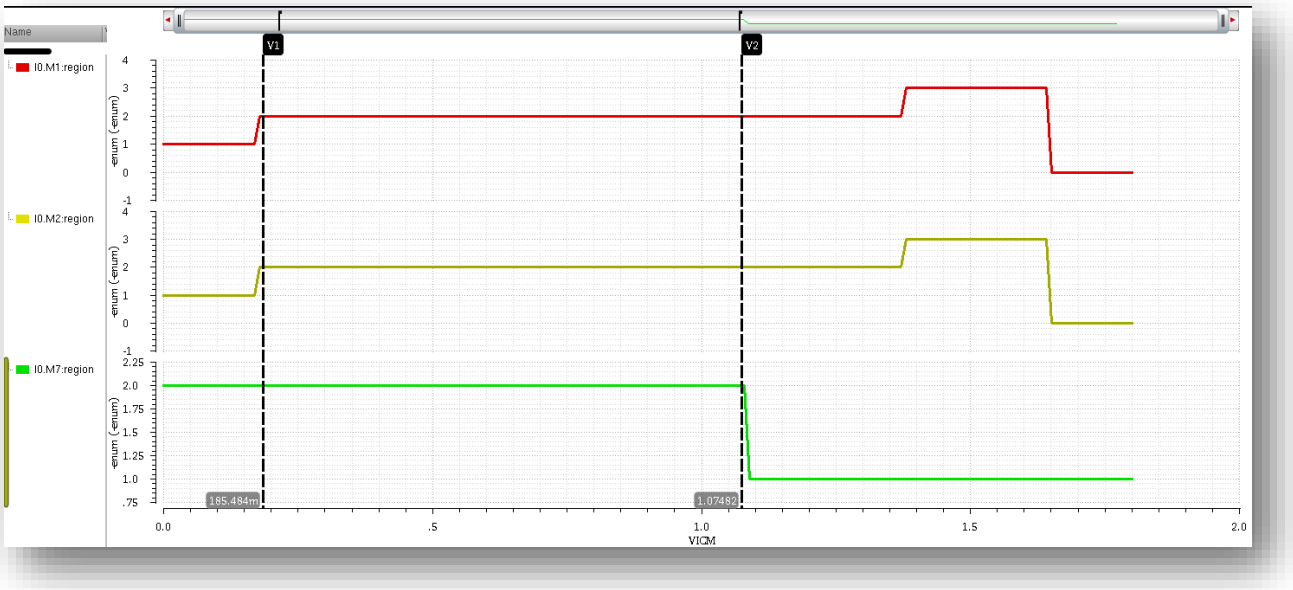
- **equal values**

	vid	/VOUT (V)
1	0.000	1.285

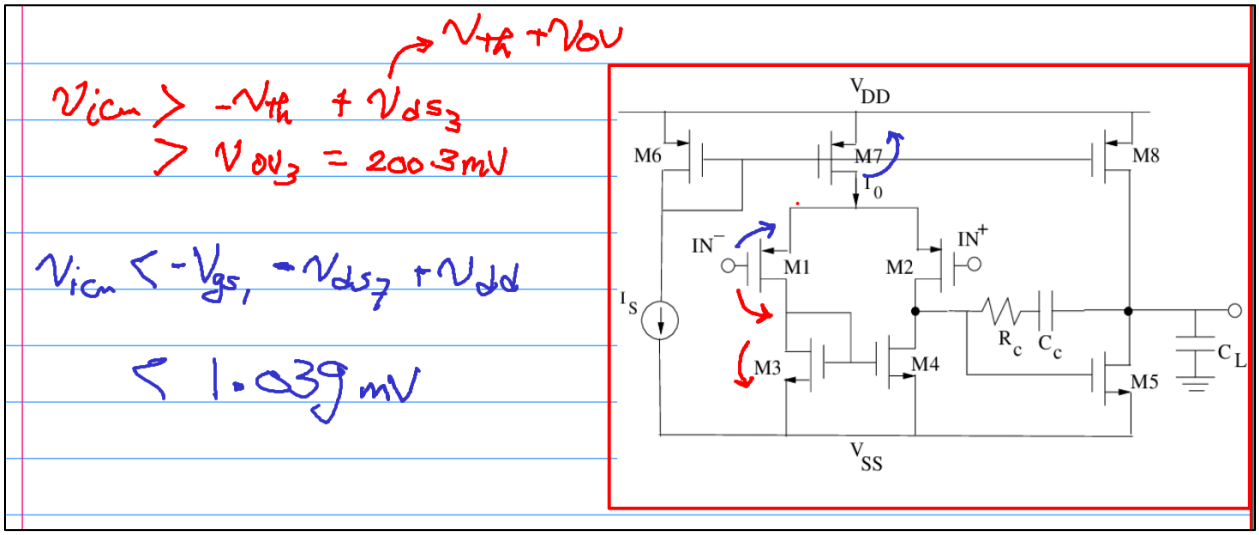


- **~ equal the Avd**

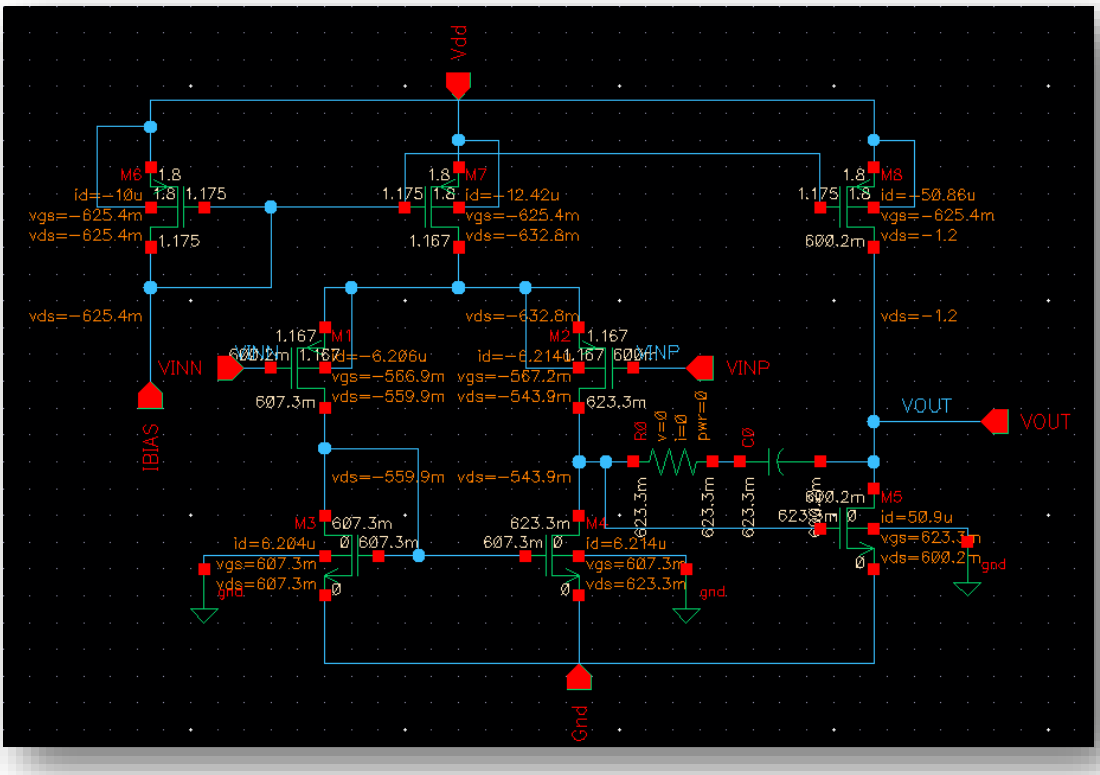
5) CM large signal ccs (region vs VICM):



Simulation	0.185	1.07
Hand	0.203	1.039

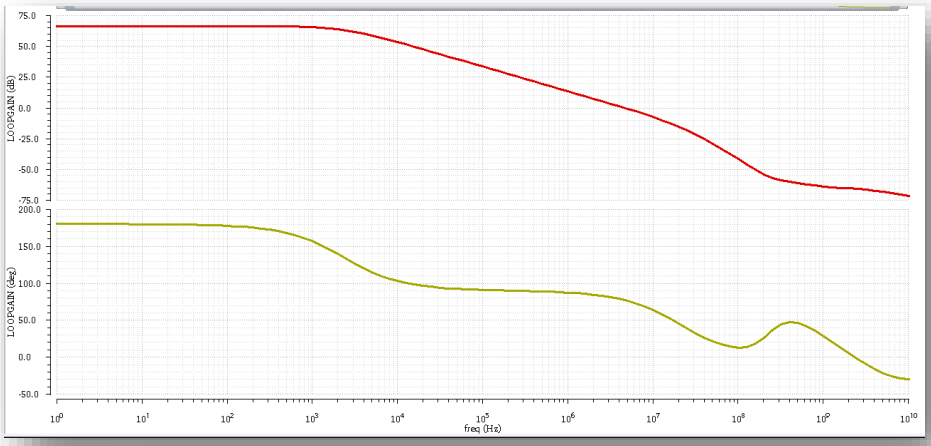


PART 4: Closed-Loop OTA Simulation



- **Dc voltages not equal in input terminals due to the error of the feedback system**
- **DC voltage at the output of the first stage not exactly equal to the value in the open-loop simulation due to diff in Vicm**
- **current (and gm) in the input pair not exactly equal there is difference due to the mismatch in input pair**

2) Loop gain:



Test	Output	Nominal
ITI_ANALOG2:Labo9_TB2:1	bandwidth(getData("loopGain...	2.341k
ITI_ANALOG2:Labo9_TB2:1	unityGainFreq(getData("loop...	4.684M
ITI_ANALOG2:Labo9_TB2:1	gainBwProd(getData("loopGa...	4.757M
ITI_ANALOG2:Labo9_TB2:1	ymax(mag(getData("loopGain...	2.027k

- **Values are equal to those from open loop gain because Beta=1**
- **LG=Beta x Aol = Aol**
- gainMargin(dB)=65.475506
  gainMarginFreq(Hz)=2.3205746e+09
  phaseMargin(Deg)=77.390461
  phaseMarginFreq(Hz)=4631467.5

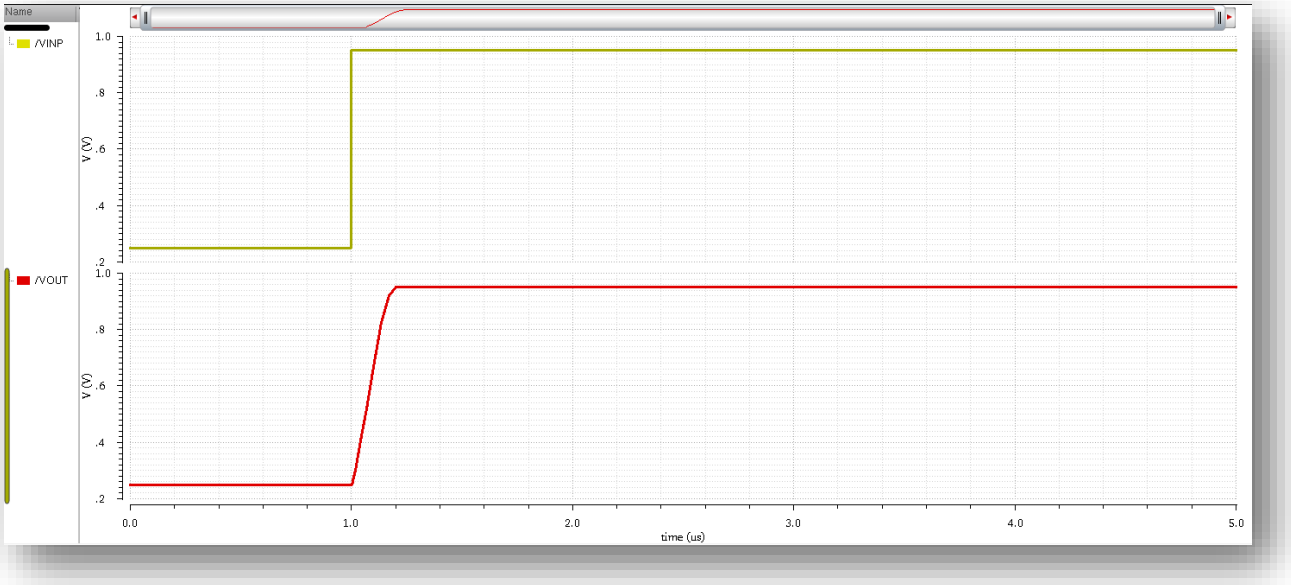
$$PM=90-tan^{-1}\left(\frac{\frac{gm0}{Cc}}{\frac{gm7}{cl}}\right)= 75.83$$

- **PM=77.4deg >70 condition satisfied**

LG = βAOL = AOL = 2000 (β=1)
GBW = LG x BW = 5MHz
↳ same BW of open loop BW is freq independent

Parameter	Hand	Simulation
Gain	2000	2300
GBW	5M	4.757M
BW	2500	2027

3) Slew rate:

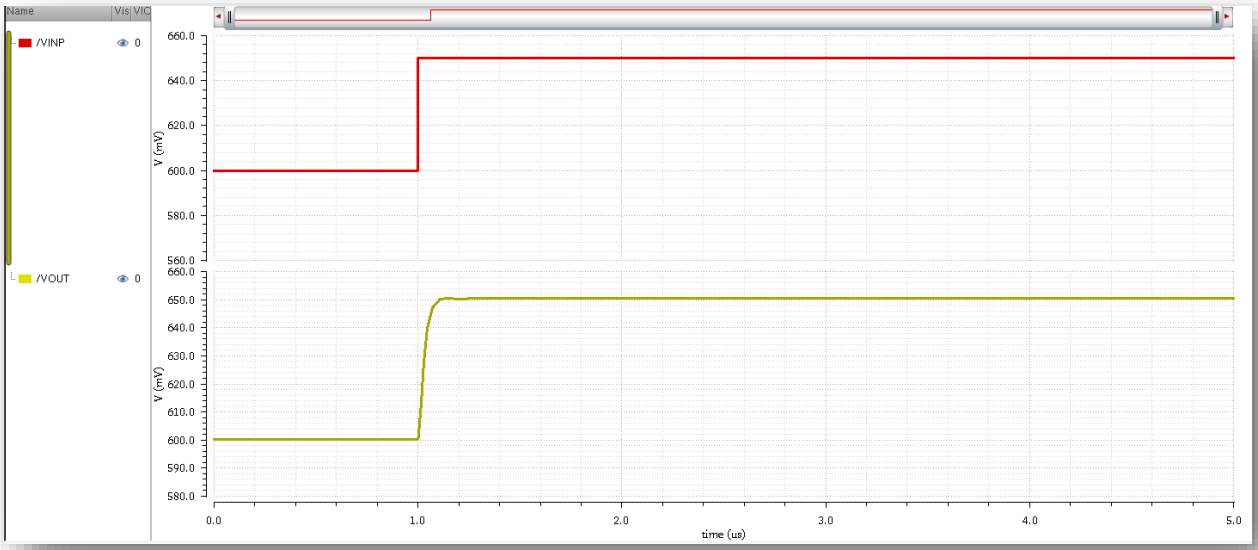


ITI_ANALOG2:Labo9_TB2:1	slewRate(v("/VOUT" ?result "...	4.205M

Parameter	Hand	Simulation
Slew rate	Id/Cc=5M/us	4.2M/us

- **Could be better with using smaller Cc , hence BW1 and GBW increases and PM dec slightly since second stage pole is not changed (**CL dependent not Cc , Cc just make the output node LIN and hence Wp2 go outwards**).**

4) Settling time:



ITI_ANALOG2:Labo9_TB2:1	riseTime(v("/VOUT" ?result "t...	54.88n

$$\tau_{rise} = \frac{2.22}{ugf} = \frac{2.22}{2\pi \times 5M} = 70.6nS$$

Parameter	Hand	Simulation
Rise time	70.6nS	54.88nS

No ringing since we have PM = 77 , the system is criticaly damped