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Signals – sensors 3.

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Overview of digital interfaces

- The handling of binary values needs multiple bits to be written or read simultaneously.
- Multiple bits mean multiple pins and wires.
- These wires form „bus”.
- A processing unit can communicate with other units on this bus.
- A bus can be serial or parallel.

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Transmission techniques

Two methods:

- Baseband: converting data bits into electrical or optical pulses, without modulation.
- Broadband: modulating the carrier signal’s frequency, amplitude or phase depending on the data bits.

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Baseband

- Two main techniques:
  - Return-to-Zero (RZ): signal’s amplitude always returns to zero state within the symbol period.
  - Non-Return-to-Zero (NRZ): signal’s amplitude does not return to zero state within the symbol period.
- Assign physical states to transmitting logical states (for example, 5V represents logical „1” value).
- The other logical state represented by 0v (unipolar coding) or negative value (bipolar coding).
- Problem: syncing the bitrate clock of the source and destination.

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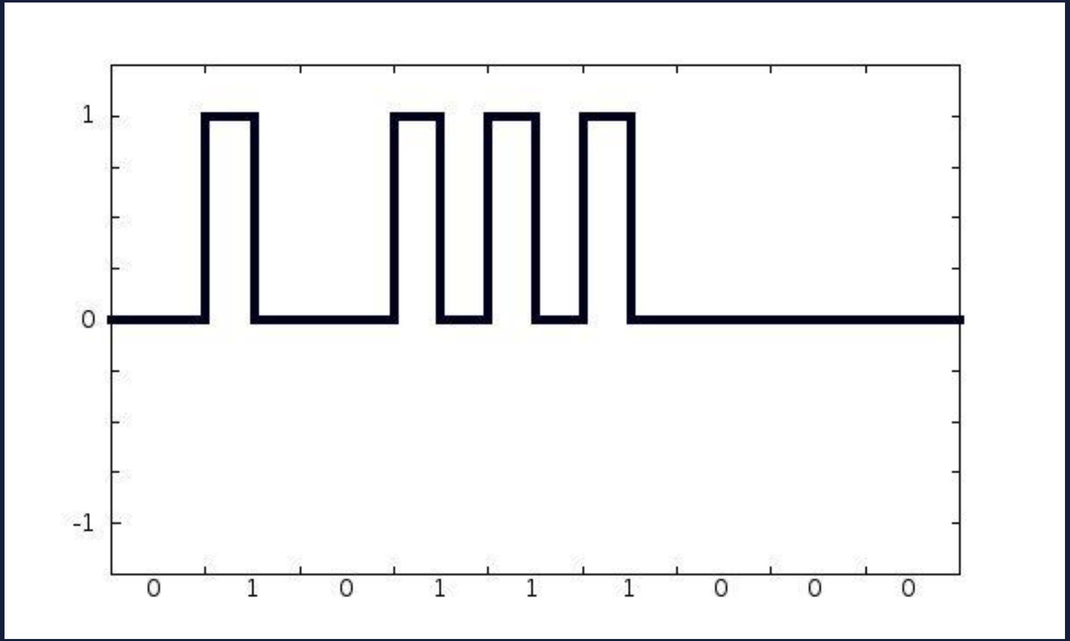
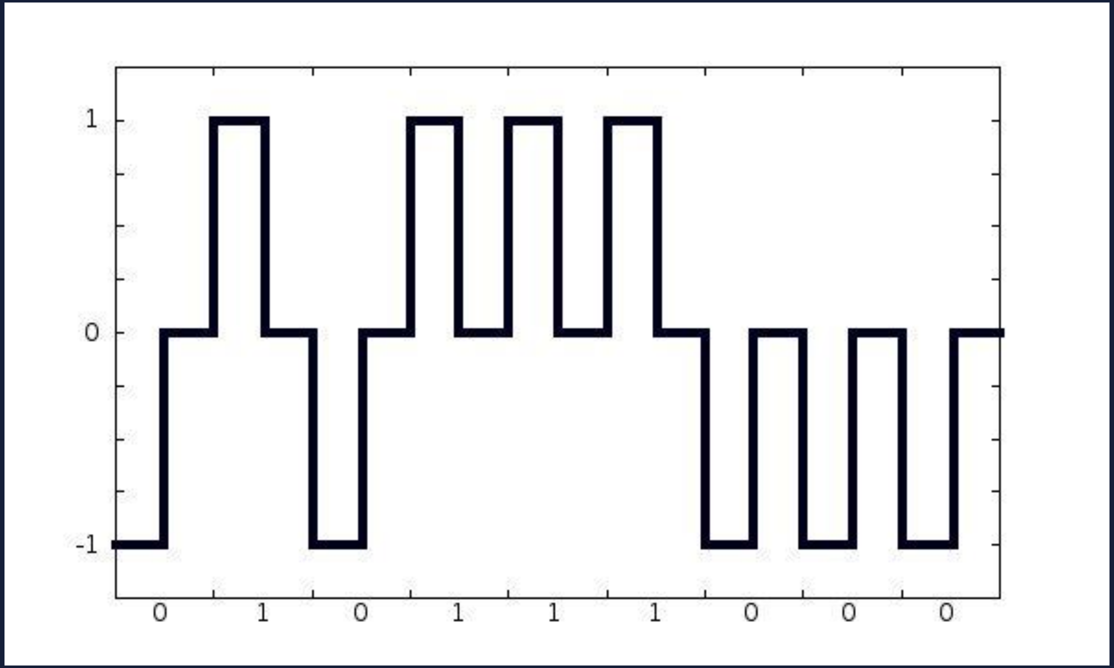
Unipolar RZ coding

- Bit „1” state represented by „+A” physical state (in the picture +1V).
- Bit „0” state represented by 0V.
- In the middle of symbol period the physical state always returns to 0V.
- Problem: data containing all „0” bits cause permanent 0V physical state. Impossible to synchronize the clock.



Polar RZ coding

- Bit „1” state represented by „+A” physical condition (in the picture +1V).
- Bit „0” state represented by „-A” physical condition (in the picture -1V).
- In the middle of symbol period the physical state always return to 0V.
- Advantage: the line’s condition changes in every bits. Synchronization is relatively easy.



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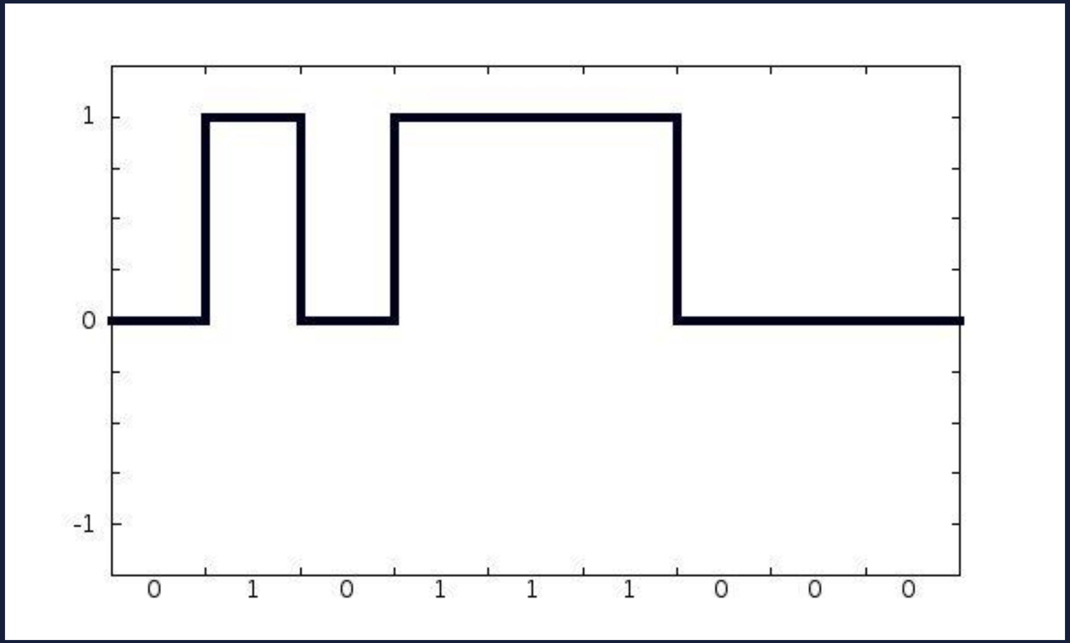
Unipolar NRZ coding

- Bit „1” state represented by „+A” physical state (in the picture +1V).
- Bit „0” state represented by 0V.
- Problem: no physical condition change in case payload data contains „1” or „0” bits only.



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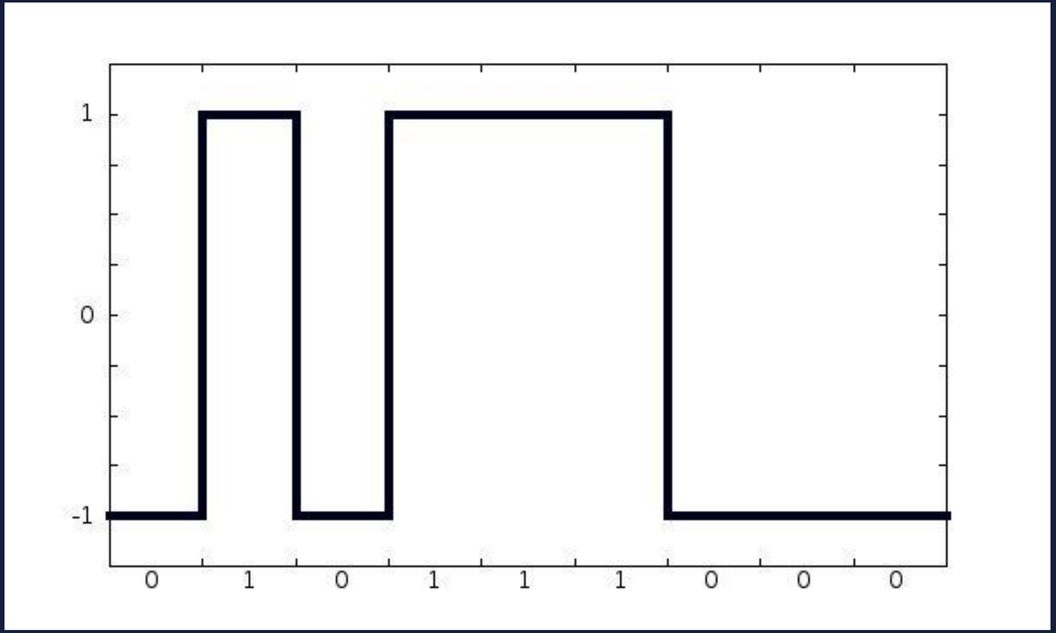
Polar NRZ coding

- Bit „1” state represented by „+A” physical condition (in the picture +1V).
- Bit „0” state represented by „-A” physical condition (in the picture -1V).
- Problems are the same as unipolar NRZ coding.



Alternate Mark Inversion (AMI) coding

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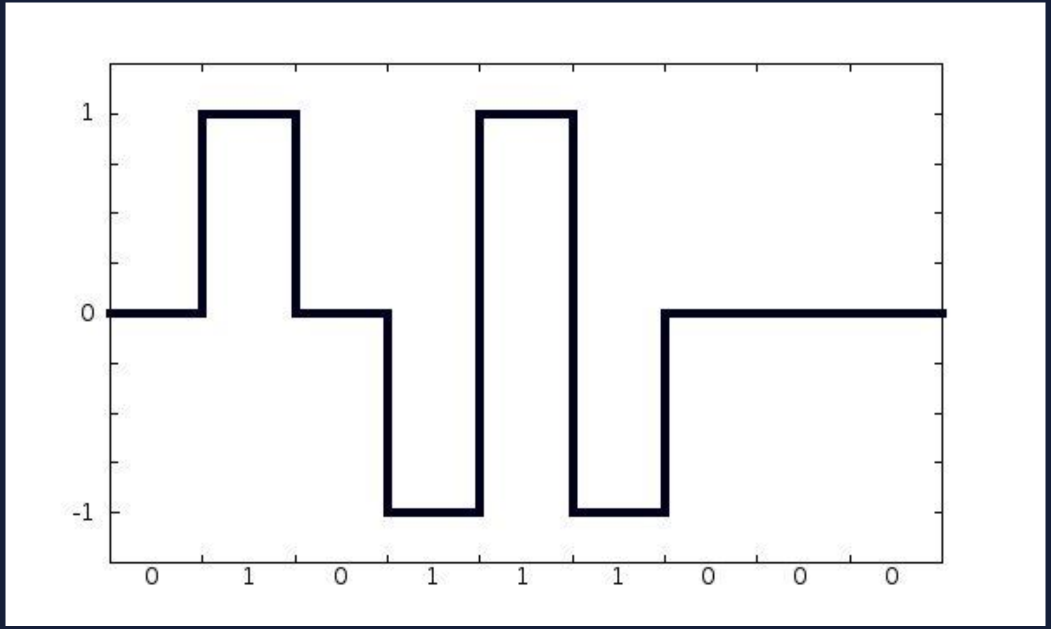
- Bit „1” state represented by „+A” and „-A” physical condition (in the picture +1V and -1V).
- Bit „0” state represented by 0V.
- Polarity inverting in two consecutive „1” bits.
- Problem: synchronization impossible in case of data streams containing „0” bits only.



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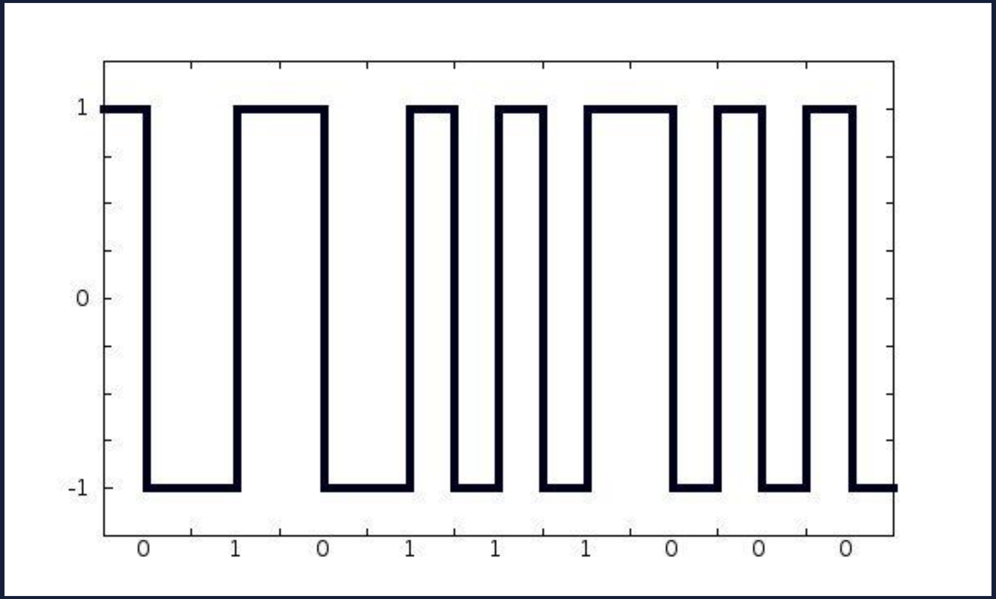
Manchester coding

- Bipolar coding (in the picture +1V and -1V).
- „0” bits represented by a falling edge in the middle of symbol period.
- „1” bits represented by rising edge in the middle of symbol period.
- Every bit state has falling or rising edge, provide easily synchronization.
- Average value of the line would be 0V.



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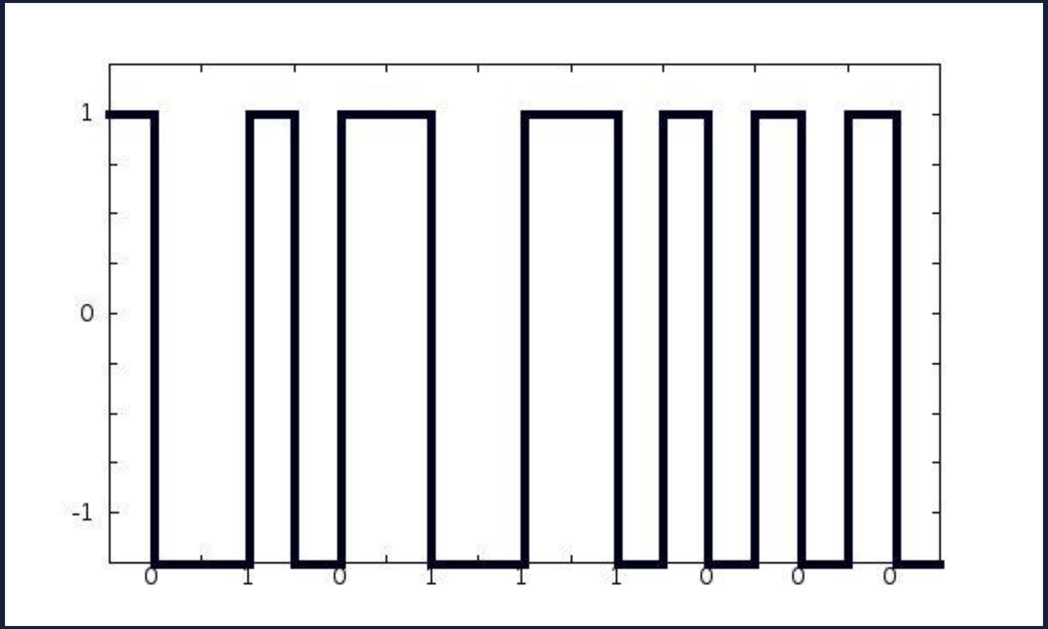
Differential Manchester coding

- Difference to Manchester coding: in case of „0” bits, the direction of the edge in the middle of symbol period does not change.
- In case of „1” bit, the direction of edge inverting (if the previous edge was falling, the actual direction would be rising).



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Parallel bus

- More than 1 bit can be transferred simultaneously. It needs as many wires as bits (for example 8 wires for 1 byte), plus synchronizing line.
- Transfer speed is significantly higher than in serial bus, but needs more wires and has limited length.
- Typical usage: communication between memory chips and microprocessors (DDR4 SO-DIMM memory modules have 256 pins).

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Serial bus

- Data bits will be transferred from source to destination sequentially, in one wire.
- Separating these bits or higher layer communication units (bytes, words, frames) can be difficult.
- Asynchronous bus: data line itself contains information for detecting and separating data bits. For example: UART (RS232C interface), USB, 1Wire.
- Synchronous bus: it using a separated synchronizing line (clock). For example: SPI, or I2C interfaces.

Shift register in serial communication

- A digital shift register is a sequential logic circuit that is used to store and shift data.
- It consists of flip-flops connected in series, where each flip-flop stores a single bit of data.
- The main function of a shift register is to move data (bits) from one flip-flop to the next with each clock pulse.
- There are different types of shift registers:
  - Serial in – serial out.
  - Parallel in/out – serial in/out (different combinations are used in different applications).

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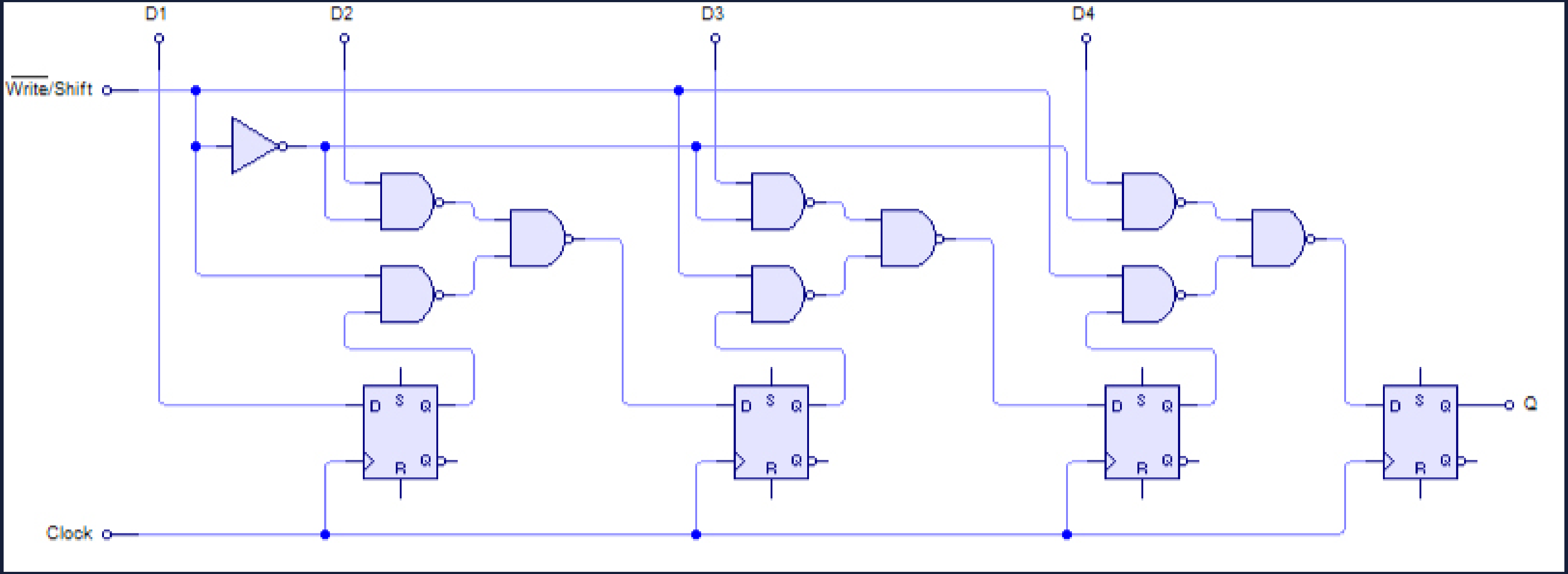
Shift register with parallel input



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SPI (Serial Peripheral Interface)

- Full-duplex synchronous serial communication.
- Designed by Motorola.
- Relatively high data speed, short distance.
- Master-slave communication model, master generates communication clock (up to 50Mbit/s).
- Four-wire interface.
  - MOSI: Master Output, Slave Input (SDO).
  - MISO: Master Input, Slave Output (SDI).
  - SCLK: Serial Clock (output from master).
  - SS: Slave Select (for multi-slave configuration).

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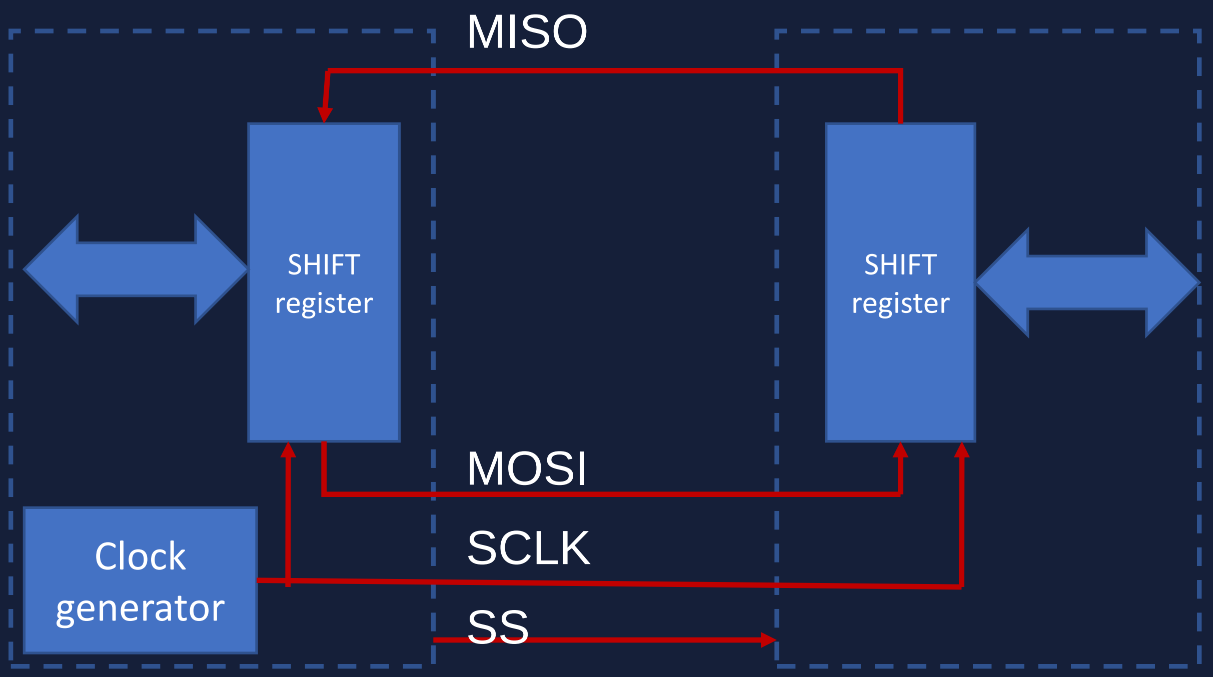
SPI interface model

- SPI interface contains two shift registers.
- Both master and slave send and receive data at the same time.



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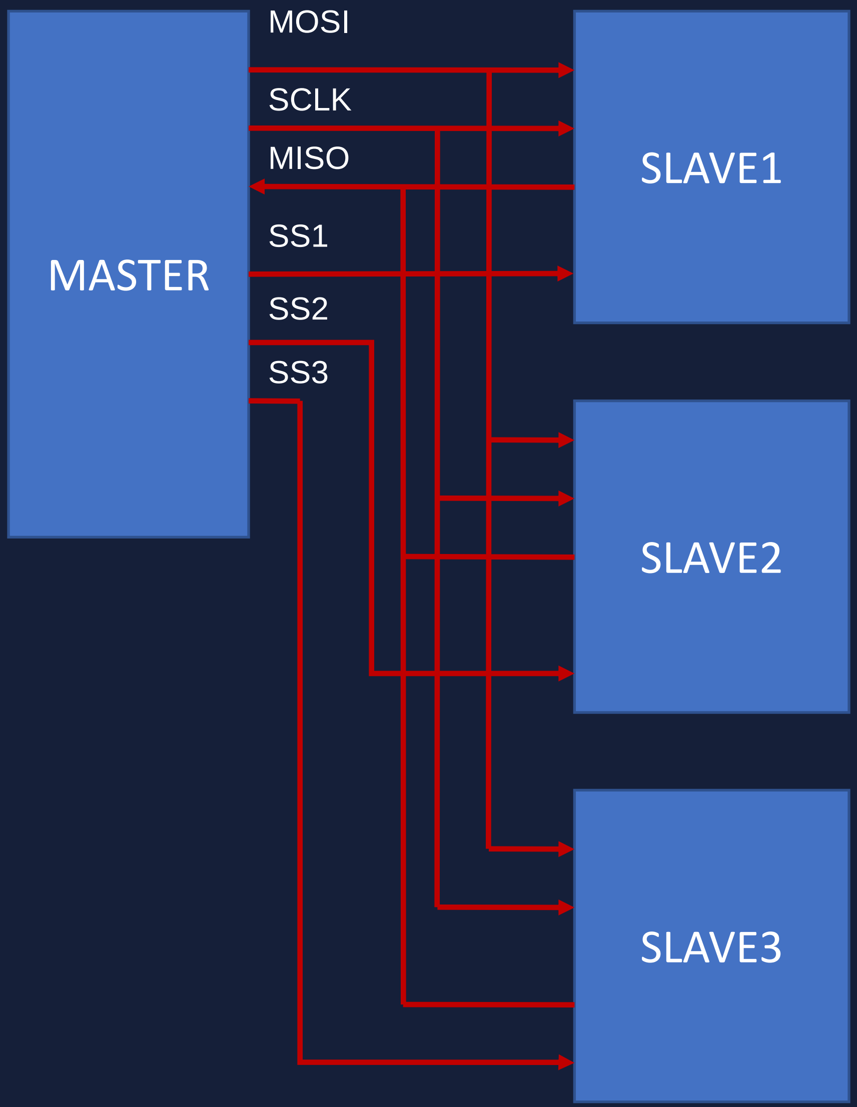
Slave Select

- Master enables communication with slave by Slave Select signal.
- If a slave device is inactive (Slave Select is high), its output (MISO) will go to high impedance state.
- Multiple slave devices can connect to master, but only one device can be in active state.
- Master selects the active slave by providing active state on the corresponding Slave Select pin.
- Always the master provides the serial clock. In dsPIC this means, user program must write data to SPI output register.

Multi slave configuration

- Master starts data transfer by providing active level on the corresponding slave select.
- Master provides serial clock and sends data to selected slave.
- Every clock cycle a bit sending and receiving occurs in the same time.



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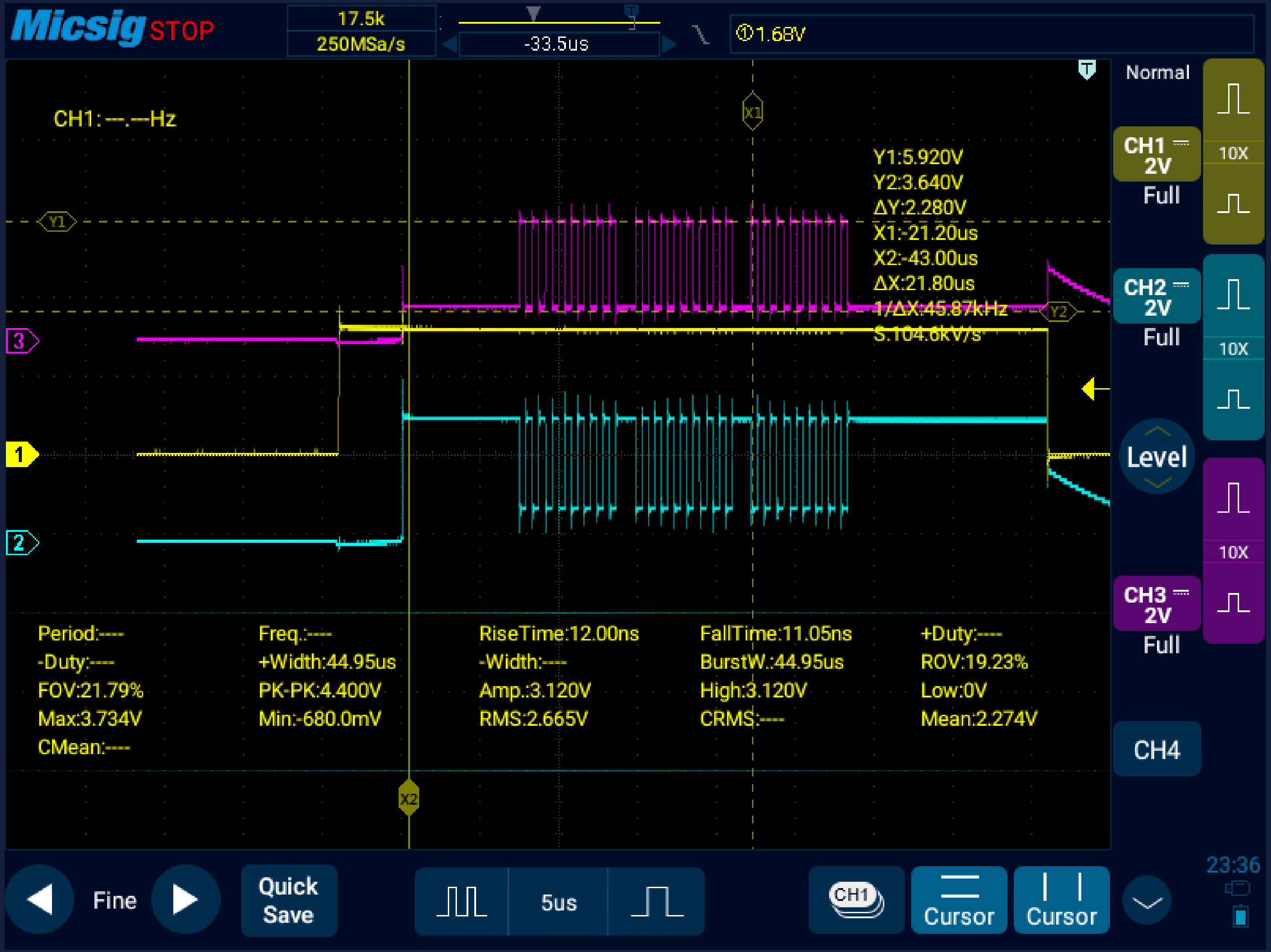
Communication



```
17.5k
250MSa/s
-33.5us
①1.68V

CH1:---.---Hz

Y1:5.920V
Y2:3.640V
ΔY:2.280V
X1:-21.20us
X2:-43.00us
ΔX:21.80us
1/ΔX:45.87kHz
S:104.6kV/s

Period:----      Freq.:----        RiseTime:12.00ns   FallTime:11.05ns   +Duty:----
-Duty:----       +Width:44.95us    -Width:----        BurstW.:44.95us    ROV:19.23%
FOV:21.79%       PK-PK:4.400V      Amp.:3.120V        High:3.120V        Low:0V
Max:3.734V       Min:-680.0mV      RMS:2.665V         CRMS:----          Mean:2.274V
CMean:----
```

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I2C (Inter-Integrated Circuit)

- Developed by Philips, synchronous serial, half-duplex, multi-master, multi-slave protocol.
- Uses 2 bidirectional lines: SDA (Serial Data Line) and SCL (Serial Clock Line).
- Instead of independent slave select signals, device addresses are used to communicate with multiple devices.
- Advantages: Fewer wires, supports multiple devices in the same bus.
- Disadvantages: Slower than SPI. 100kbit/s, 400kbit/s were originally the standards, but faster speeds (up to 5Mbit/s) are available.
- More complex due to addressing and half-duplex communication.

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I2C (Inter-Integrated Circuit) design

- All devices on the bus have a 7 bit address (10 bit addresses also available).
- Multiple master devices can control the bus.
- All target (slave) nodes are listening to the communication, but the device with the target address must be responding.
- There are 4 different modes:
  - Master transmit: Controller node is sending data to a target (slave).
  - Master receive: Controller node is receiving data from a target.
  - Slave transmit: Target node is sending data to the controller (master).
  - Slave receive: Target node is receiving data from the controller.

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I2C (Inter-Integrated Circuit) signals

- Different signal levels assigned to „1” and „0” bits.
- When the bus is inactive, both SDA and SCL lines are in HIGH state.
- SDA must be examined after the SCL rise to HIGH state.
- There are two special signals:
  - START condition: SDA is pulling LOW while SCL remains in the HIGH state.
  - STOP condition: SDA is pulling HIGH while SCL remains in the HIGH state.
- After the START condition, data can be transferring from the master to the slave devices.
- First data byte contains the slave device address and a R/W bit.

I2C (Inter-Integrated Circuit) communication

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- Master send the START condition, the address and the R/W bits.
- When master writes to the slave, the slave must generate an ACK or NAK bit after the received byte. Master must provide an extra clock for this bit.
- When master reads from the slave, the master must generate an ACK or NAK bit after the received byte.
- Master can generate a START condition during the data transmission. This called REPEATED START condition.
- Combined operation can be performed within a transaction, e.g.: START,Command to the slave,REPEATED START,Read from slave,STOP

UART (Universal Asynchronous Receiver/Transmitter)

- Serial, asynchronous communication method.
- Uses 2 lines: TX (Transmit) and RX (Receive).
- No clock signal, the devices must recover clock from data signal.
- Usually, the devices agree on the data rate (baud rate).
- Predefined communication speeds from 300 bps up to ~1Mbit/s.
- UART is just the digital side, multiple line coding standards (RS-232, RS-422, RS-485).
- Disadvantages: Slower data transfer rates, does not support multiple devices easily.

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UART (Universal Asynchronous Receiver/Transmitter) communication

- The communication could be simplex, half-duplex or full-duplex.
- Communication data element could be between 5 and 9 bits (a single character).
- The line is idle when no data is transferring.
- Every character starts with a „Start” bit, followed by the data bits.
- Error checking is optional: parity bit after data bits.
- Character ends with the „Stop” bit.

Parity check

- Every communication can be distorted by noise or some other communication problem.
- For error detection a redundancy must be added.
- Parity check is one of the simplest method.
- Transmitter counts the number of „1” bits in the transmitted character.
- Depending on the parity check method („odd” or „even” parity), adds a parity bit to the end of the character.

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Odd and even parity

- In case of „odd” parity method:
    - Parity bit will be „1” if the number of „1” is even (make the number odd).
    - Parity bit will be „0” if the number of „1” is odd (keep the number odd).
- In case of „even” parity method:
    - Parity bit will be „1” if the number of „1” is odd (make the number even).
    - Parity bit will be „0” if the number of „1” is even (keep the number even).

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UART communication settings

- For UART to work some settings must be the same on both ends:
  - Line coding voltage level.
  - Communication speed (bit rate or baud rate).
  - Number of data bits (5-9).
  - With parity or without parity.
  - Number of stop bits (1 or 2).
  - Flow control.
- Most common mode: 8N1 (8 data bits, no parity, 1 stop bit).
- UART is widely used for terminal applications (for example: Cisco routers use 9600bps, 8N1 by default).

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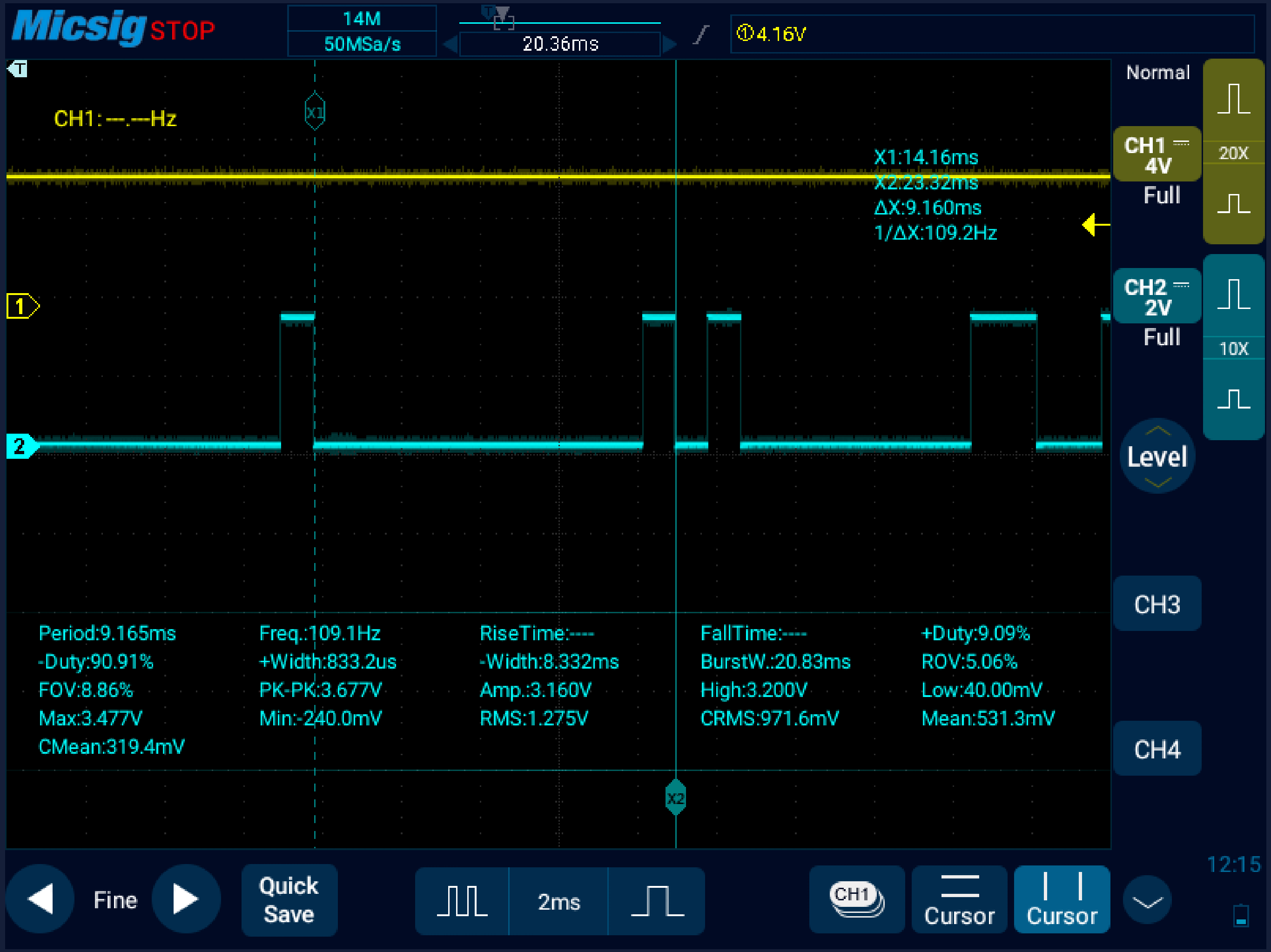
UART communication (8N1)



X1:14.16ms
X2:23.32ms
ΔX:9.160ms
1/ΔX:109.2Hz

```
Period:9.165ms     Freq.:109.1Hz       RiseTime:----       FallTime:----        +Duty:9.09%
-Duty:90.91%       +Width:833.2us      -Width:8.332ms      BurstW.:20.83ms      ROV:5.06%
FOV:8.86%          PK-PK:3.677V        Amp.:3.160V         High:3.200V          Low:40.00mV
Max:3.477V         Min:-240.0mV        RMS:1.275V          CRMS:971.6mV         Mean:531.3mV
CMean:319.4mV
```

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1wire interface

- Developed by Dallas Semiconductors.
- It uses 2 wires: communication line and ground.
- Communication line provides the power supply for the slave devices.
- Every device connects to the communication wire with an open-drain output with a pull-up resistor, which means every device can pull the wire to the „0” level.
- Every device can monitor the state of the wire.
- Quite slow (16.3kbit/s, but there is a „burst” mode with 160kbit/s).
- It can work via fairly long wires (~100m).

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1wire interface communication

- Wire idle state is „1”.
- Master device can initiate the data transfer by pulling the wire to the zero level for at least 480us (this resets all slave devices).
- After that, slave devices send a „presence” signal by pulling the wire to the zero level for 60us.

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1wire interface protocol

- If master wants to transmit data, it pull the wire to the zero level:
  - 1-15us for „1” logical value.
  - 60us for „0” logical value.
- When master reads data, it will send a short pulse (1-15us).
  - After that, the slave device can pull down the line for value „0” for 60us.
  - For sending value „1”, the slave will do nothing.
- The basic sequence contains a reset pulse, 8 bits of command and a data byte.
- Multi slave system is possible, every device has a 64 bit ID.

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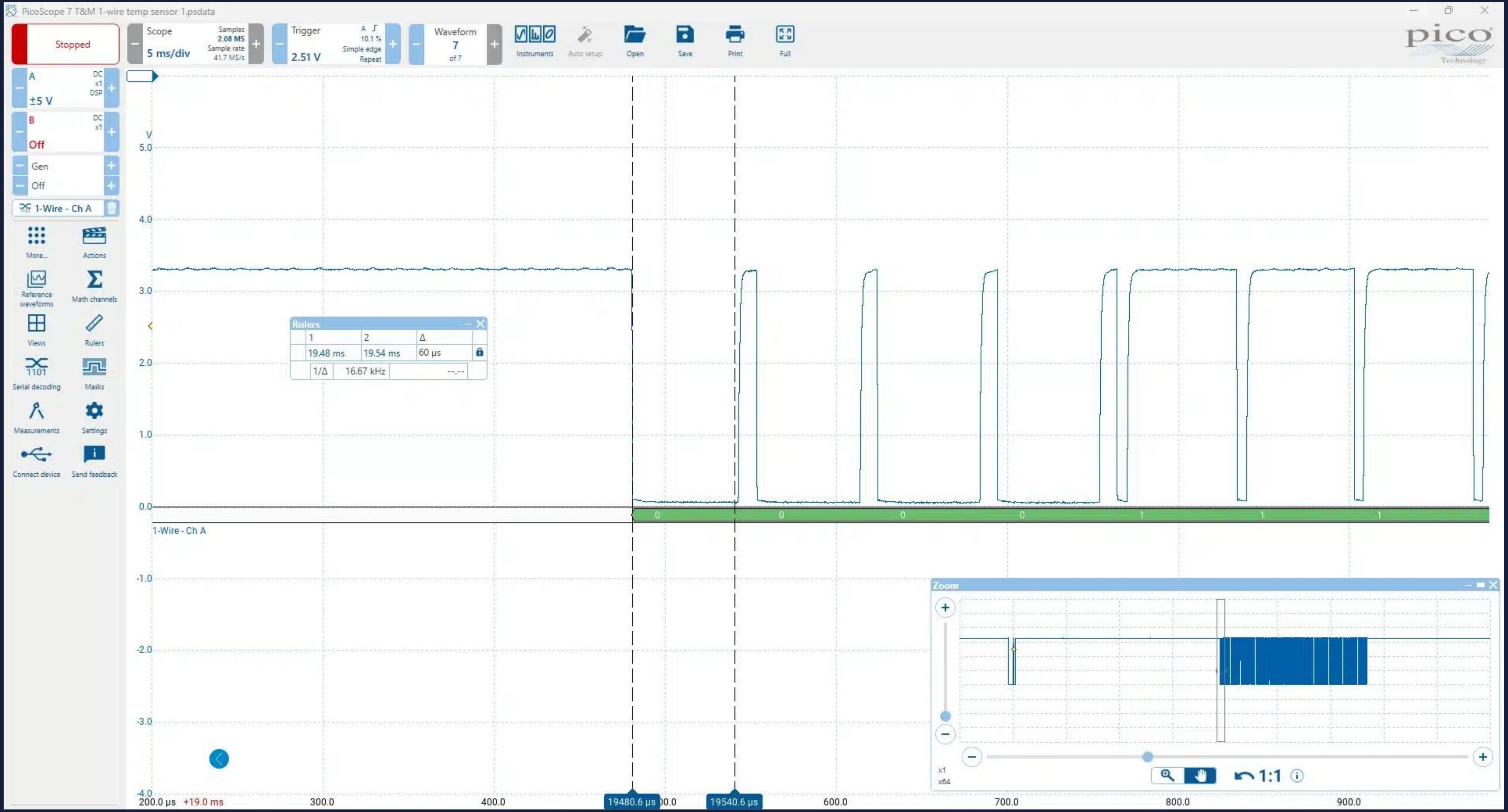
1wire interface timing



Rulers

	1	2	Δ
	19.48 ms	19.54 ms	60 µs
1/Δ	16.67 kHz		--.--

Signals - Sensors

Universal Serial Bus (USB)

- A standardized serial bus system used for communication and power supply between computers and peripherals.
- Full-duplex communication, supports multiple speeds (USB 2.0, USB 3.0, etc.).
- Can deliver power to connected devices (5V DC, 0.5A or 0.9A).
- High-speed data transfer, widely adopted, plug-and-play functionality.
- Disadvantages: More complex than SPI, I2C, UART.
- Not for IC-IC communication.