Three-Stage BJT Common-Emitter Amplifier

Infinity Explorers 2

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Abstract

This project presents the design, implementation, and analysis of a three-stage BJT common-emitter amplifier using NPN 2N2222 transistors. The primary objective is to achieve high voltage and current gain, making the amplifier suitable for practical applications such as audio and communication systems. Each amplification stage is directly coupled to preserve signal continuity, and biasing components are carefully selected to ensure optimal operating conditions and stability. The circuit includes resistors for biasing, capacitors for coupling and bypassing, and a speaker as the final output load. Both DC and AC analyses are performed to evaluate the amplifier's performance, demonstrating effective signal amplification across all three stages. The project highlights fundamental concepts such as signal coupling, impedance matching, and bypassing techniques. It concludes with suggestions for future improvements, including enhancing frequency response and minimizing signal distortion.

Contents

1. Introduction

The three-stage common-emitter amplifier is a classic electronic circuit used to amplify weak AC signals. Each stage provides voltage gain, with coupling capacitors ensuring signal transfer between stages while blocking DC components. This project highlights the role of biasing, bypassing, and coupling in achieving stable amplification.

2. Circuit Components

Transistors

Q1, Q2, Q3: NPN transistors (2N2222) configured in common-emitter mode for amplification.

Resistors

-Stage 1

R1 (47 kΩ): Base bias resistor to Vcc.

R2 (4.7 kΩ): Base bias resistor to GND.

R3 (4.7 kΩ): Collector load resistor.

R4 (820 Ω): Emitter resistor for stabilization.

-Stage 2 & 3: Similar configuration with R6-R12.

-Output: 47 kΩ resistor to match speaker impedance.

Capacitors

C1 (100 μF): Input coupling capacitor.

C2 (100 μF), C3 (50 μF), C4 (22 μF): Inter-stage coupling capacitors.

C5-C7 (4.7 μF): Emitter bypass capacitors to improve gain.

Speaker

LS1: 8 Ω speaker for output.

3. Challenges and Issues Faced

During the implementation of the **three-stage common-emitter amplifier using 2N2222 transistors**, we encountered several technical challenges, including:

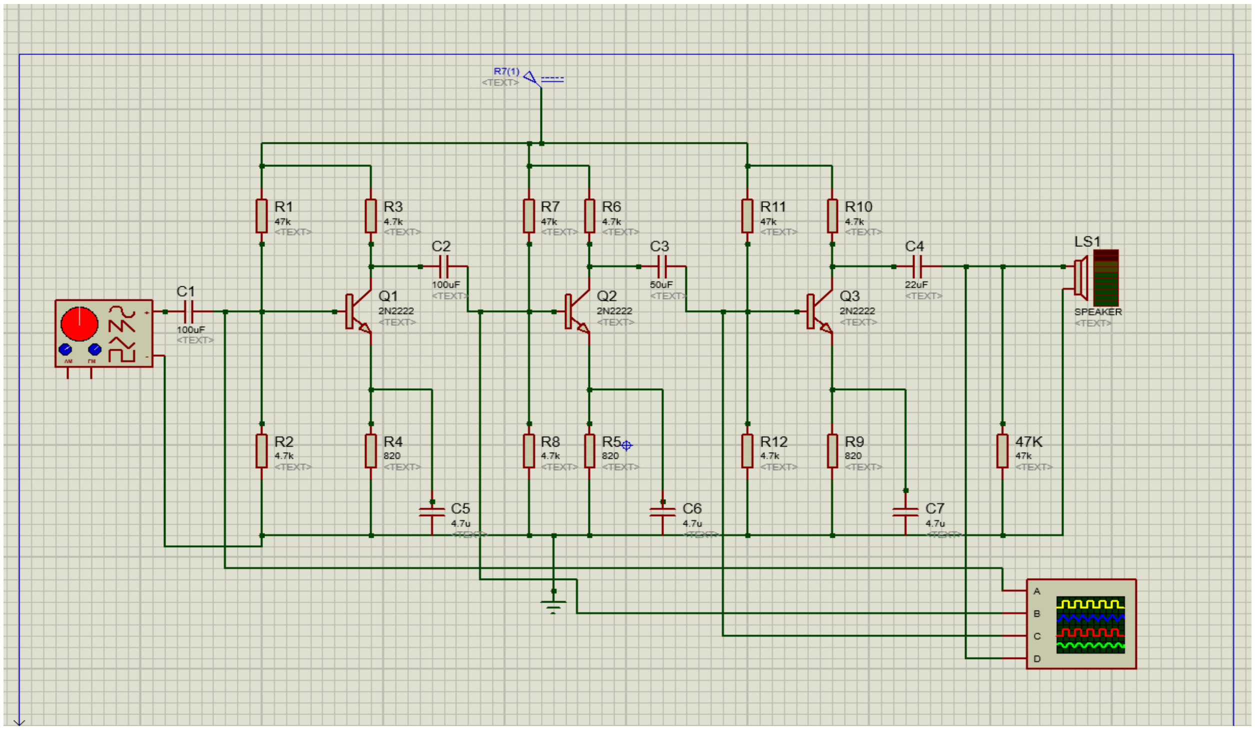
-At one point, we noticed that the **circuit was not providing any amplification**. This raised concerns, so we began testing each stage individually. After isolating the problem, we discovered that **one of the transistors was damaged.**

-Initially, we were using the **2N3904** transistor. However, after some testing, we realized that it **was not well-suited for continuous operation** in this circuit. We decided to replace it with the **2N2222** transistor, which offered **better performance and higher current handling capability**, making it more reliable for our application.

-Another issue we faced was that, although **the gain was present**, the **output sound was unclear and weak**. Upon further investigation, we found that this was due to **signal loss across the emitter resistor**. To fix this, we added **bypass capacitors (C5, C6, and C7)** across the emitter resistors in each stage, which **increased the gain and significantly improved the clarity of the output signal**.

Thankfully, after making these adjustments, the circuit performed as expected, delivering clear audio output with stable amplification.

4. Circuit Design and Operation



Biasing: Resistors set the DC operating point for each transistor.

Coupling: Capacitors pass AC signals while blocking DC.

Bypassing: Emitter capacitors (C5-C7) reduce AC feedback, increasing gain.

Output: The final stage drives the speaker via a coupling capacitor (C4).

5. DC and AC Analysis

DC Analysis

Each of the three amplifier stages (Q1, Q2, Q3) uses a common-emitter configuration. The DC biasing points are calculated as follows (example based on Q1):

1. Base Voltage (VB):

   VB ≈ Vcc * (R2 / (R1 + R2))

   VB ≈ 12V * (4.7k / (47k + 4.7k)) ≈ 1.09V

2. Emitter Voltage (VE):

   VE ≈ VB - VBE ≈ 1.09V - 0.7V = 0.3909V

3. Emitter Current (IE):

   IE = VE / RE ≈ 0.3909V / 820Ω ≈ 0.475 mA

4. Collector Current (IC):

   IC ≈ IE ≈ 0.475 mA

5. Collector Voltage (VC):

   VC = Vcc - (IC * RC) ≈ 12V - (0.475mA 4.7kΩ) ≈ 9.77V

   Collector-emitter voltage VCE

   VCE = VC -VE = 9.77 - 0.39 = 9.38V (Active Region)

Repeat similar calculations for Q2 and Q3 using identical resistor values.

AC Analysis

1. gm:

    gm = IC / VT = 0.475mA / 26V = 18.27 mS

    rπ = B / gm = 100 / 18.27mS = 5.47KΩ

    re = VT / IE = 26mV / 0.475 mA = 54.73

    Av ≈ -gm * Rc = -18.27mS * 4.7KΩ = -85.869

    Zin = R1 ‖ R2 ‖ rπ = 47kΩ ‖ 4.7kΩ ‖5.47kΩ ≈2.45kΩ

    A similar gain is assumed for Q2 and Q3.

2. Total Voltage Gain:

    Av(total) = Av1 * Av2 * Av3 ≈ (-85.86) ^3 ≈ -632954

    (Negative sign indicates phase inversion)

3. Input and Output Impedance:

    - Input Impedance ≈ Resistors at the base.

    - Output Impedance ≈ Rc of each stage.

4. Capacitor Roles:

    - C1, C2, C3, C4: Coupling capacitors for AC signal transfer.

    - C5, C6, C7: Bypass capacitors to enhance gain by bypassing emitter resistors.

6. Conclusion

The three-stage amplifier successfully demonstrates multi-stage signal amplification. Proper biasing and component selection ensure stability and performance. Future improvements could include frequency response analysis and distortion reduction techniques.

7. Reference

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