Assignment 1 (ADC specs)

ADC Selection Criteria

Specifications:

- Resolution: 12 bits
- Sample rate: ≥ 1 MSps
- Channels: 1
- Input type: Differential
- Maximum DNL: < 1 LSB
- Maximum INL: < 1 LSB
- Minimize power consumption

SPEC	**ADI AD9613**	**TI ADC12C105**	**Research ADC**
Price	Starting from $49.43	Starting from $25.555	Not specified
Min Power Supply (V)	1.8 V	3 ,3.3 V	0.8 V
Architecture	PIPELINED	PIPELINED	Successive Approximation Register (SAR)
Peak-to-Peak Input Range (V)	1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)	2 V p-p	0.8 Vp-p
Power consumption	3.08 mW	3.3 mW	0.78 mW
MAX DNL (LSB)	0.5 LSB	±0.5 LSB	+0.6/-0.4LSB
Max INL (LSB)	1 LSB	±1.0 LSB	+0.9/-0.8LSB
ENOB(bits)	Approximately 11.3 bits at 250 MSps	Approximately 11.5 bits at 105 MSps	9.9 bits
SNR(dB)	69.6 dBFS at 185 MHz input and 250 MSps	69 dBFS at 240 MSps	61.5 dB
SINAD(dB)	60 dB	70 dB	61.3 dB
SFDR(dB)	86 dBc at 185 MHz input and 250 MSps	82 dBFS at 240 MHz input	82 dB
Digital Output Format	LVDS (ANSI-644 levels)	Parallel CMOS	Serial
Internal Reference	Yes	Yes	NO

Internal Sampling Clock	NO	NO	NO
Walden FoM (fJ/step)	≈1.45 fJ/step	4.19 fJ/step	8.2 fJ/step
Schreier FoM (dB)	137 dB	146.8 dB	169.2dB

BLOCK DIAGRAM FOR **ADI AD9613 :**

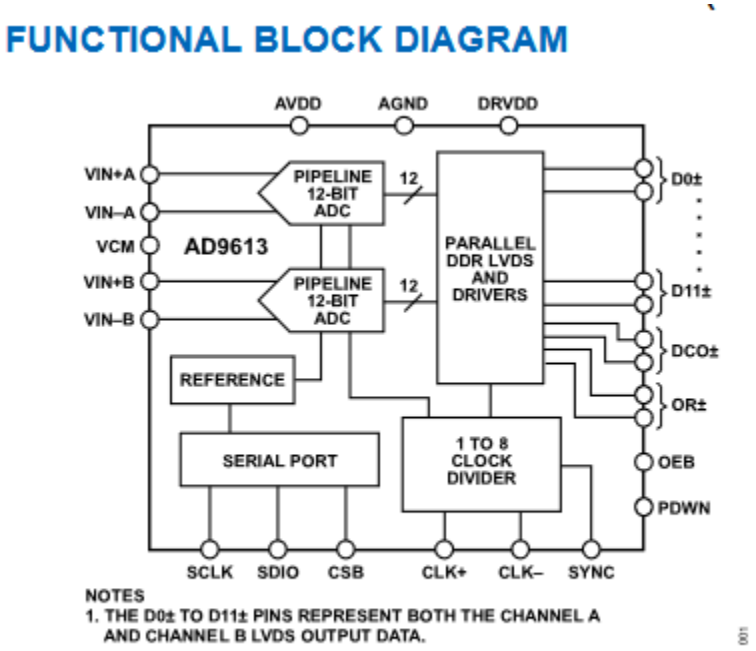
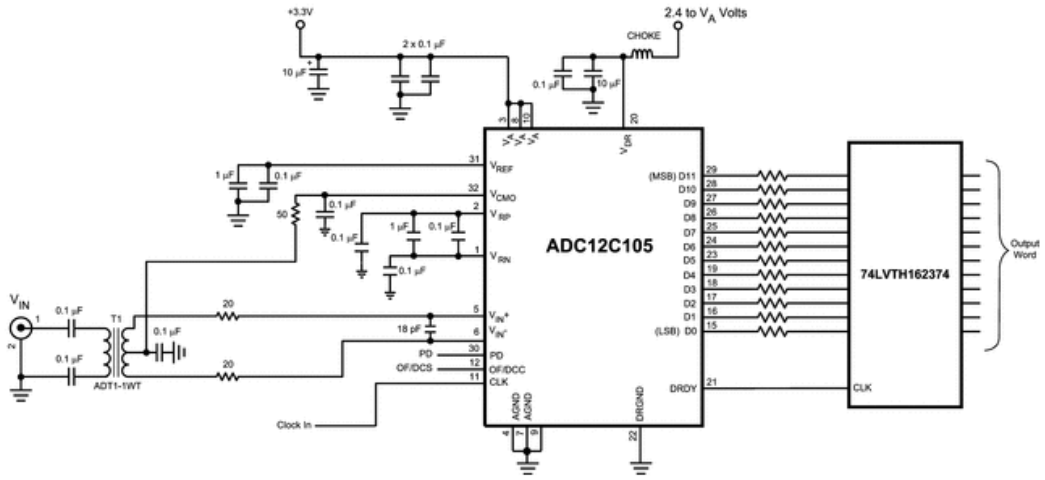


Figure 1.

BLOCK DIAGRAM FOR **TI ADC12C105 :**



BLOCK DIAGRAM FOR **SAR ADC:**

"A 12-bit 100MS/s SAR ADC With EquivalentSplit-Capacitor and LSB-Averaging in 14-nm CMOS FinFET"

https://www.researchgate.net/publication/357005765_A_12-bit_100MSs_SAR_ADC_With_Equivalent_Split-Capacitor_and_LSB-Averaging_in_14-nm_CMOS_FinFET

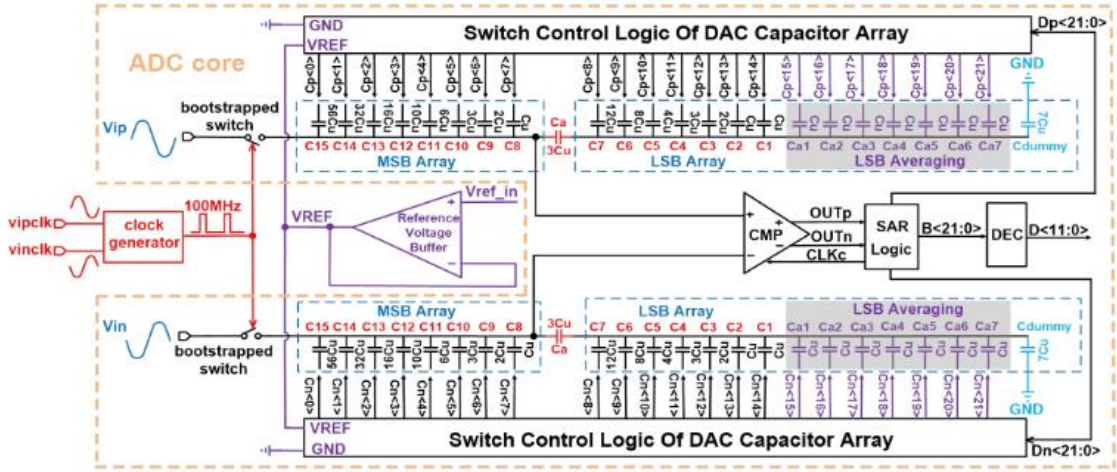


FIGURE 1. The overall architecture of the proposed SAR ADC