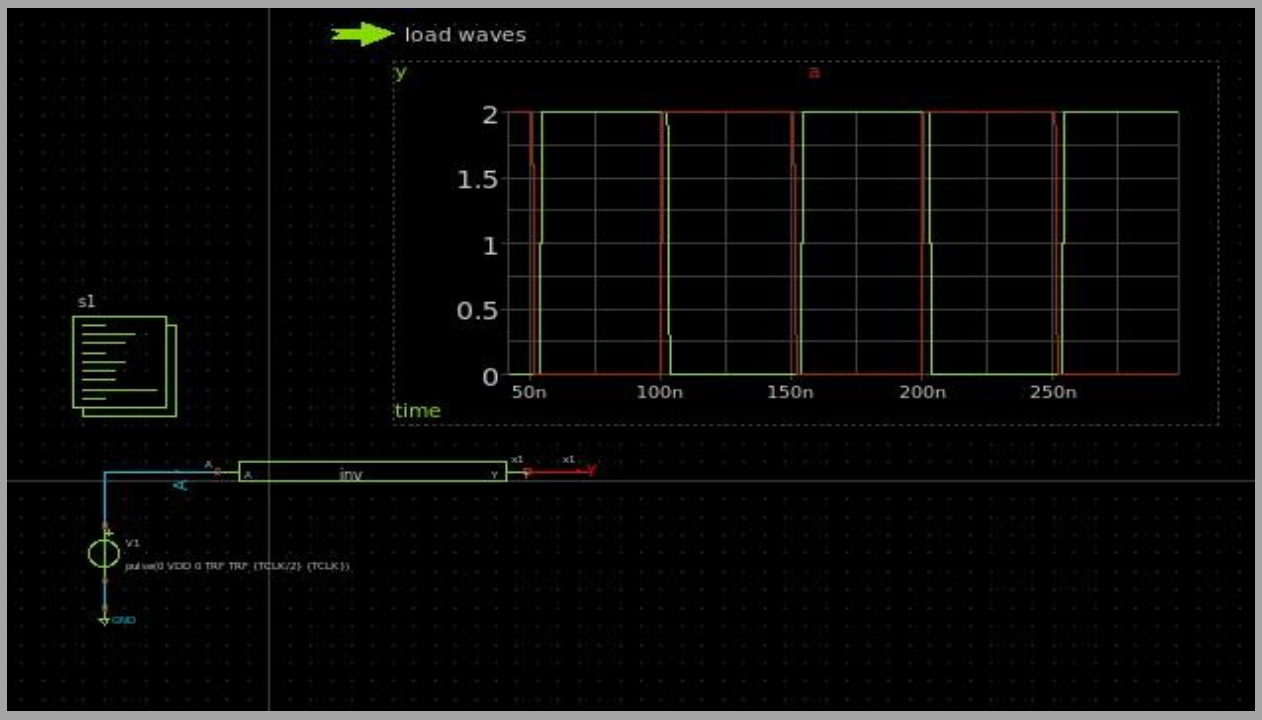
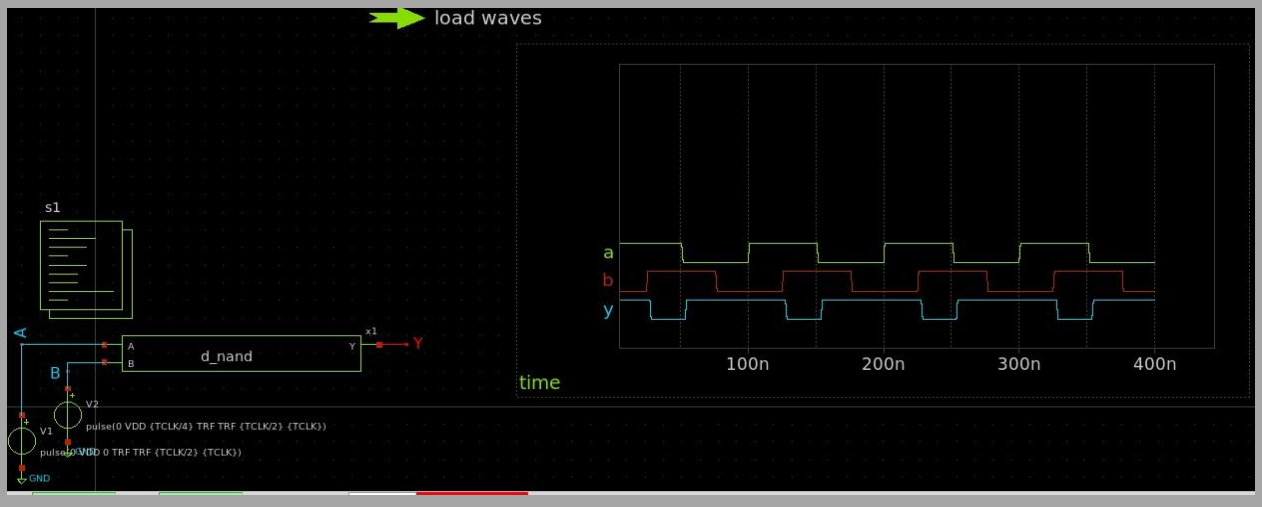
SAR ADC PROJECT

Introduction (Behavioral Models)

1- Inverter

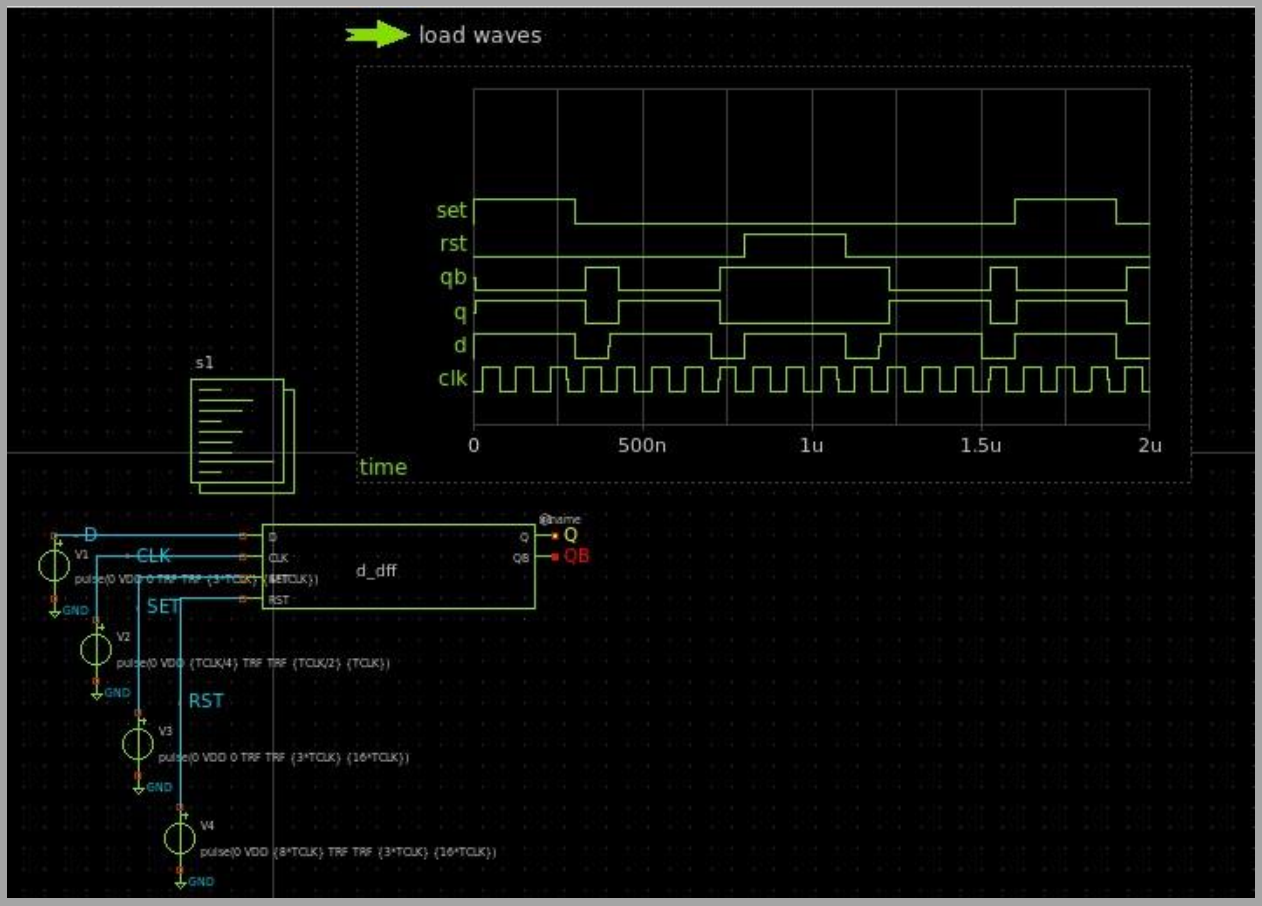


2-nand gate

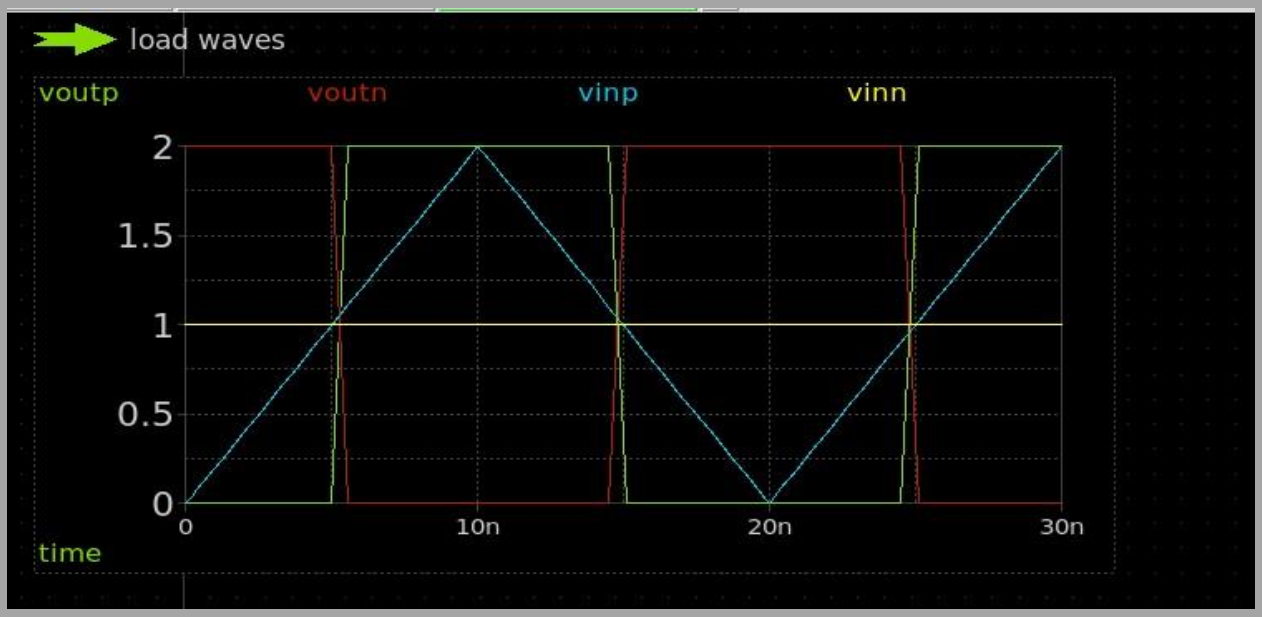


3-Nor gate

4- d-flipflop

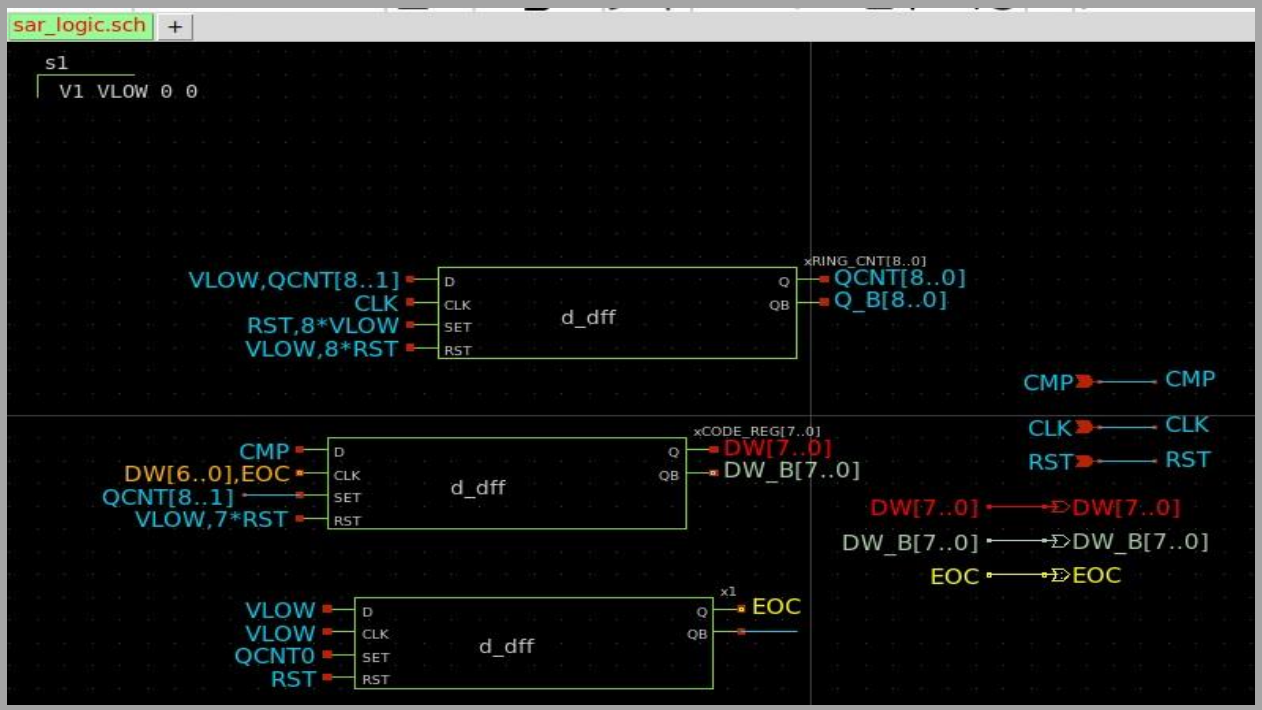


5- comparator

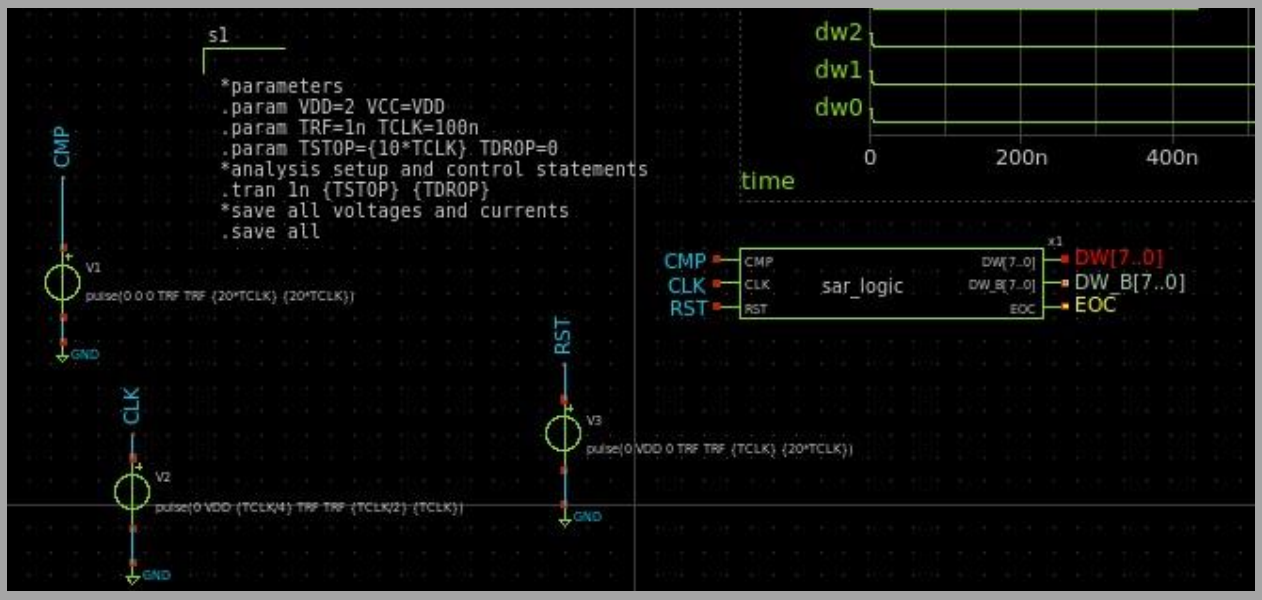


Part 1

Sar logic schematic

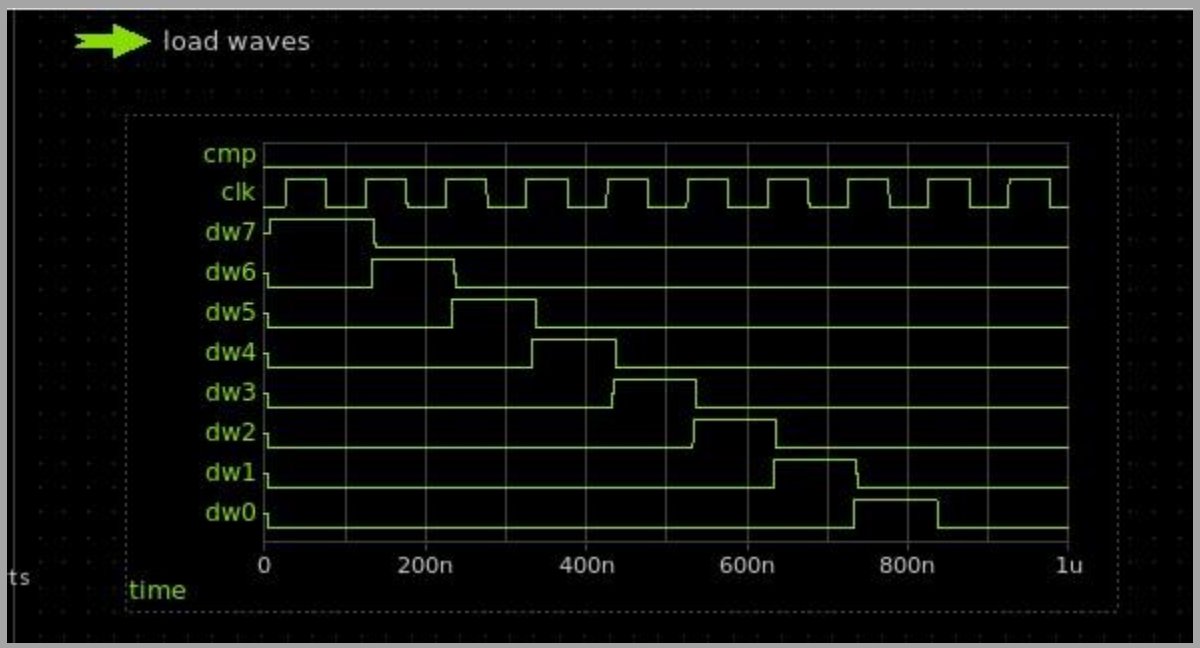


Sar logic tb

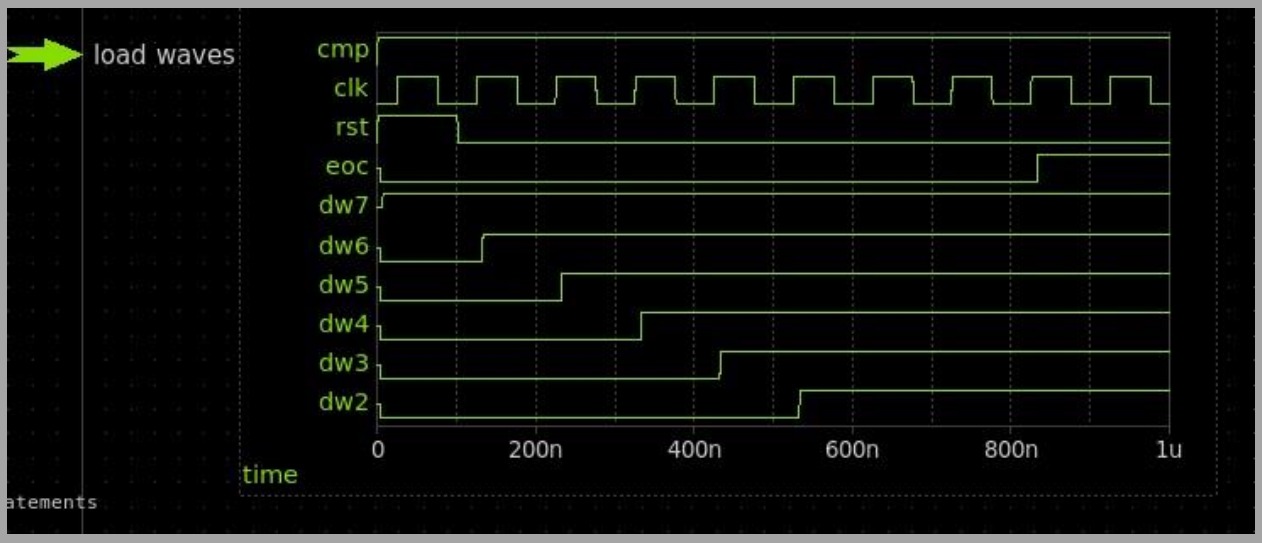


Simulation results when:

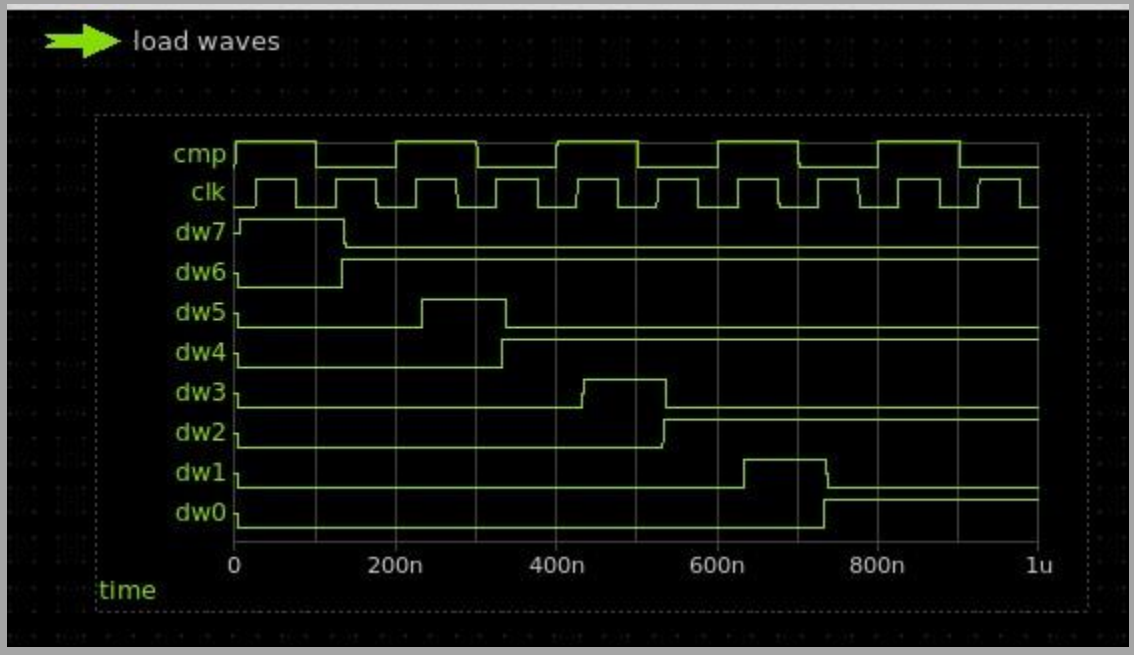
a-CMP is all zeros



b-CMP is all ones



c-CMP is alternating



Clock cycle	DW 7	DW6	DW5	DW4	DW3	DW2	DW1	DW0	CMP
1 (RESET)	0	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	B7
3	1	1	0	0	0	0	0	0	B6
4	1	1	1	0	0	0	0	0	B5
5	1	1	1	1	0	0	0	0	B4
6	1	1	1	1	1	0	0	0	B3
7	1	1	1	1	1	1	0	0	B2
8	1	1	1	1	1	1	1	0	B1
9	1	1	1	1	1	1	1	1	B0

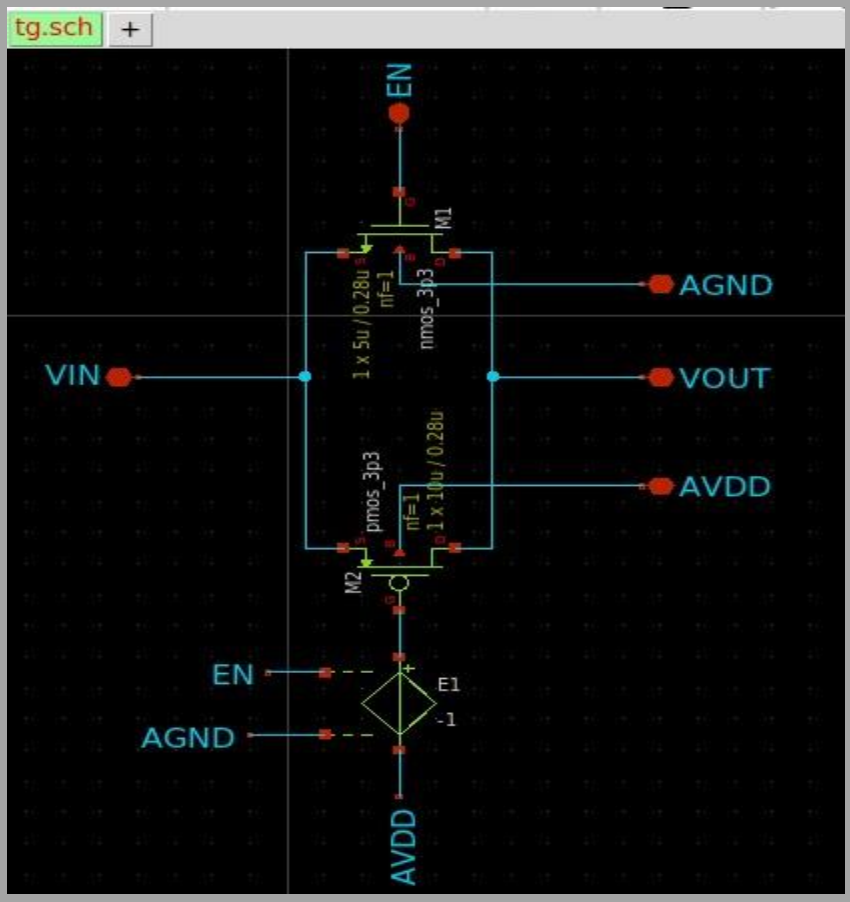
This table states how the SAR logic works in case CMP = all ones .

Comment :

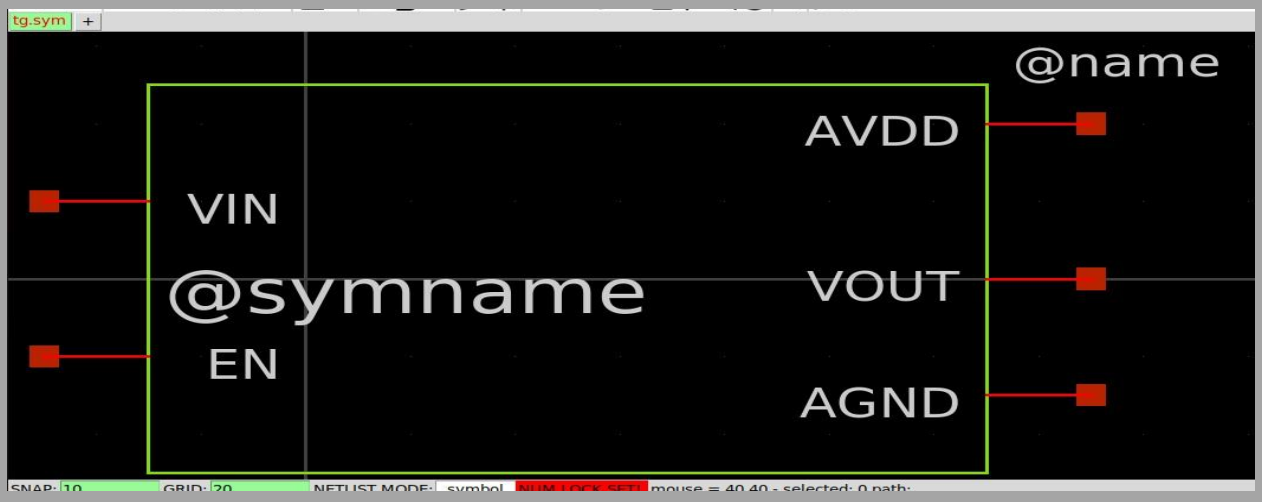
The SAR ADC operates by using a binary search method to approximate the input signal. It starts by setting the most significant bit (MSB) to 1 while keeping the rest as 0. This digital value is converted to an analog voltage using a DAC, which is then compared to the input signal. If the DAC output is higher than the input, the bit is cleared back to 0. otherwise, it remains 1. The process then moves to the next bit, setting it to 1 and repeating the comparison. This iterative approach continues from MSB down to the least significant bit (LSB), progressively doing the digital approximation of the input signal. Once all bits are determined, the EOC signal is asserted, indicating that the final digital output is ready.

Part 2

Transmition gate schematic

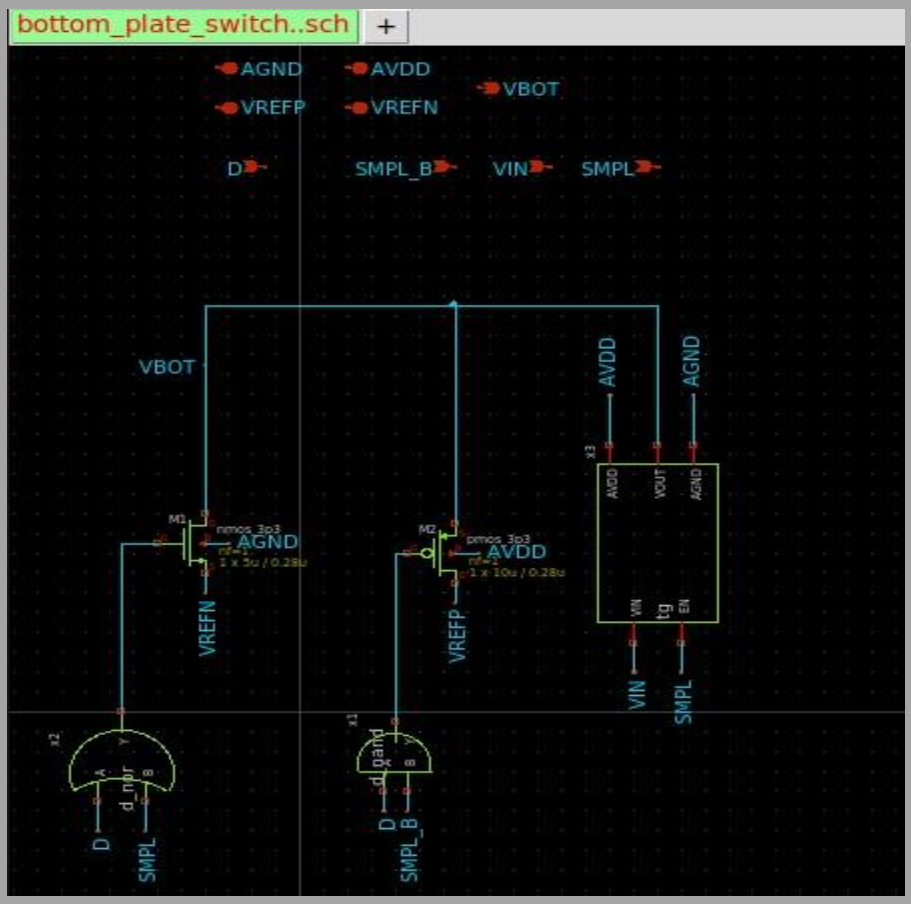


Symbol:

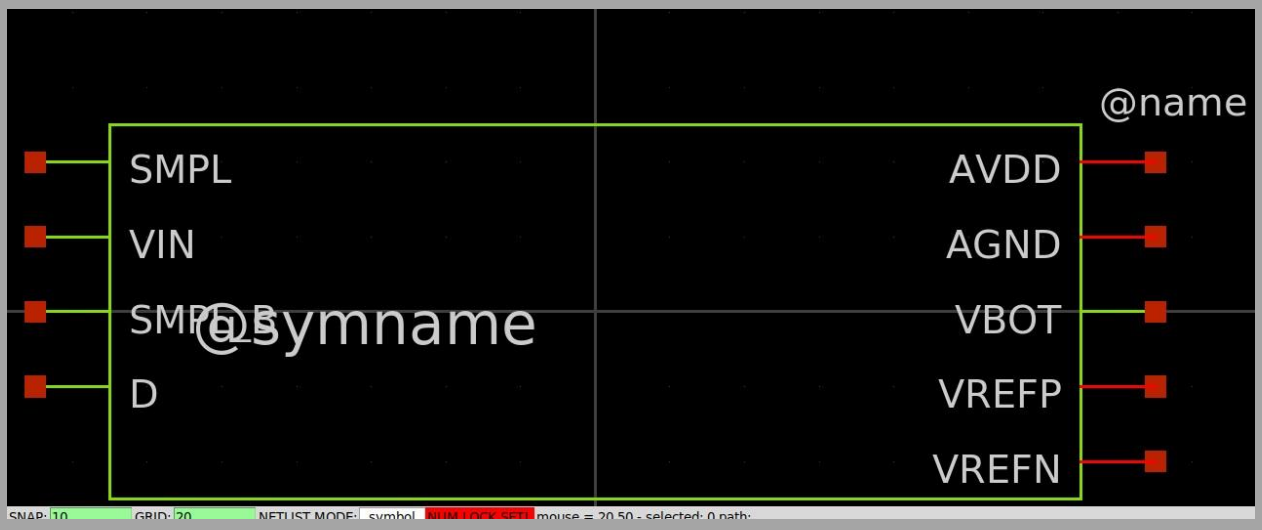


Part 3

Bottom-Plate Switch

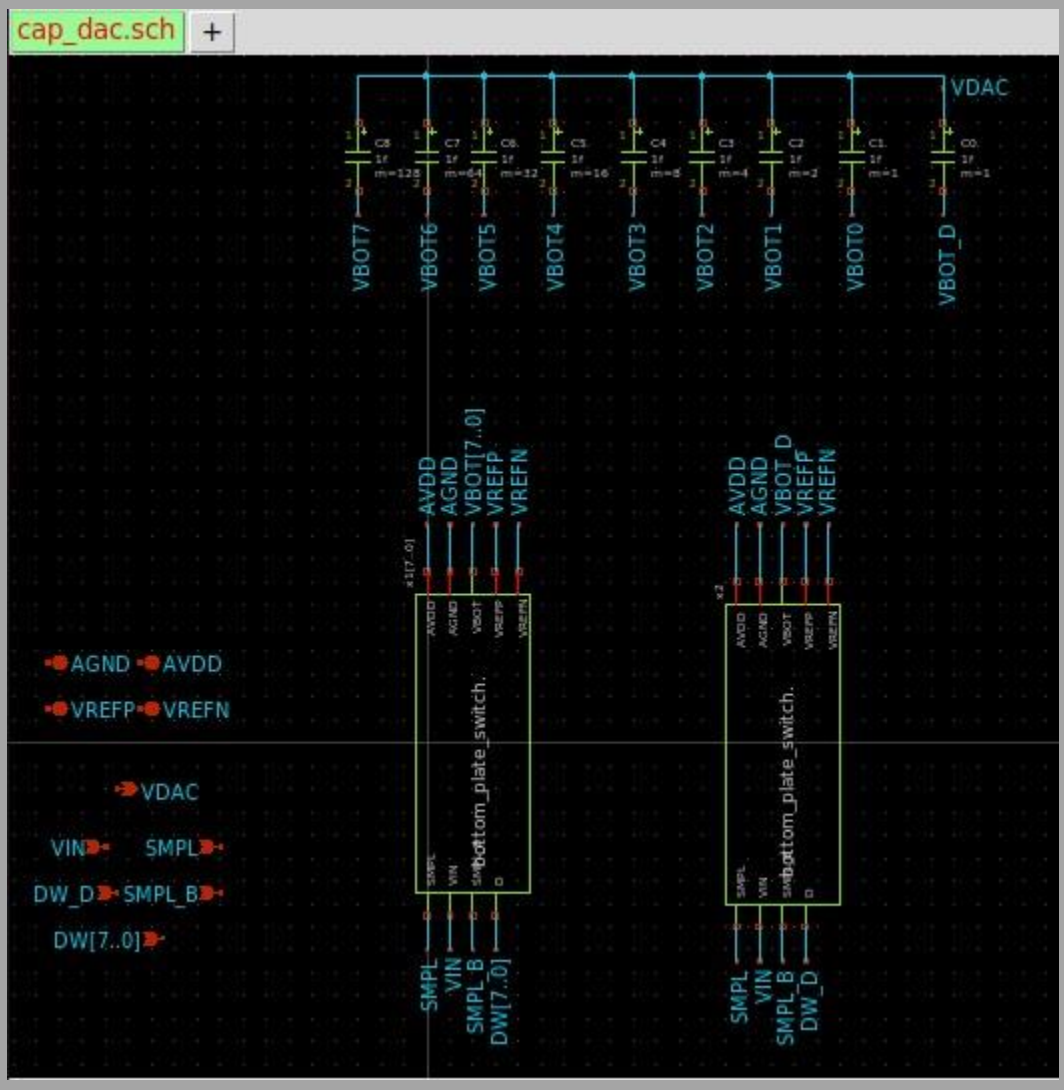


Symbol:



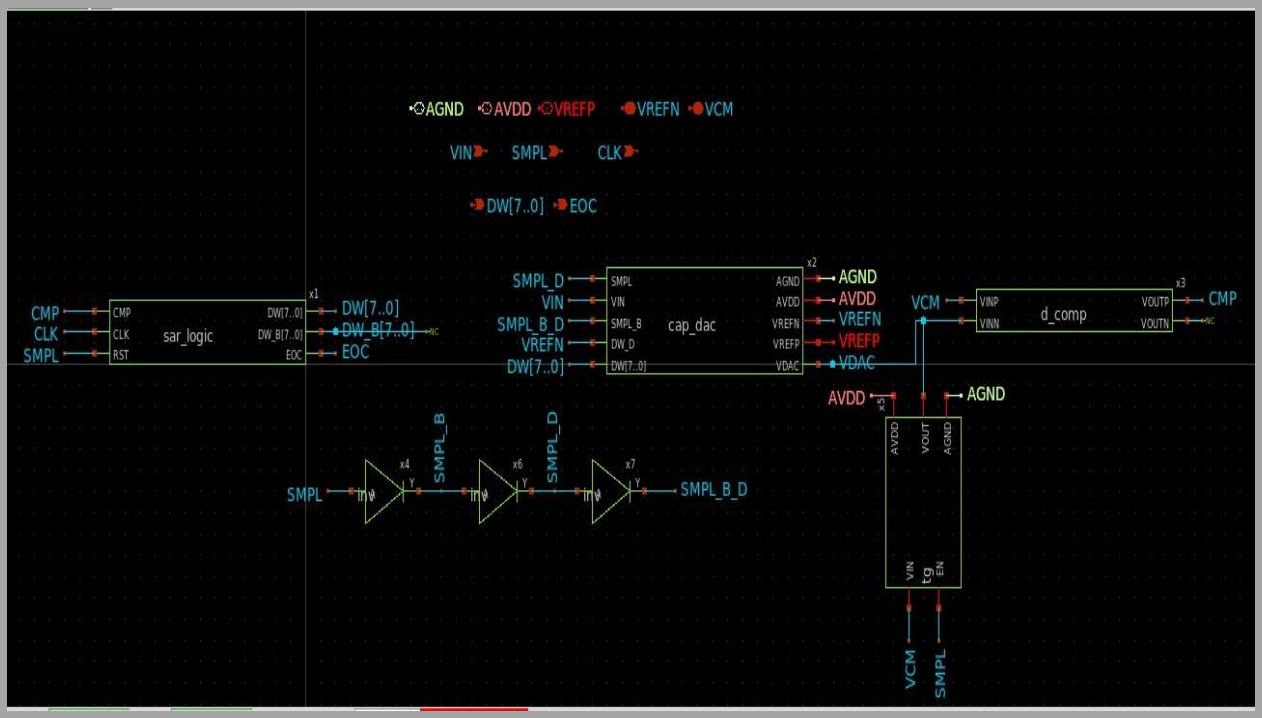
Part4

Capacitave DAC schematic :



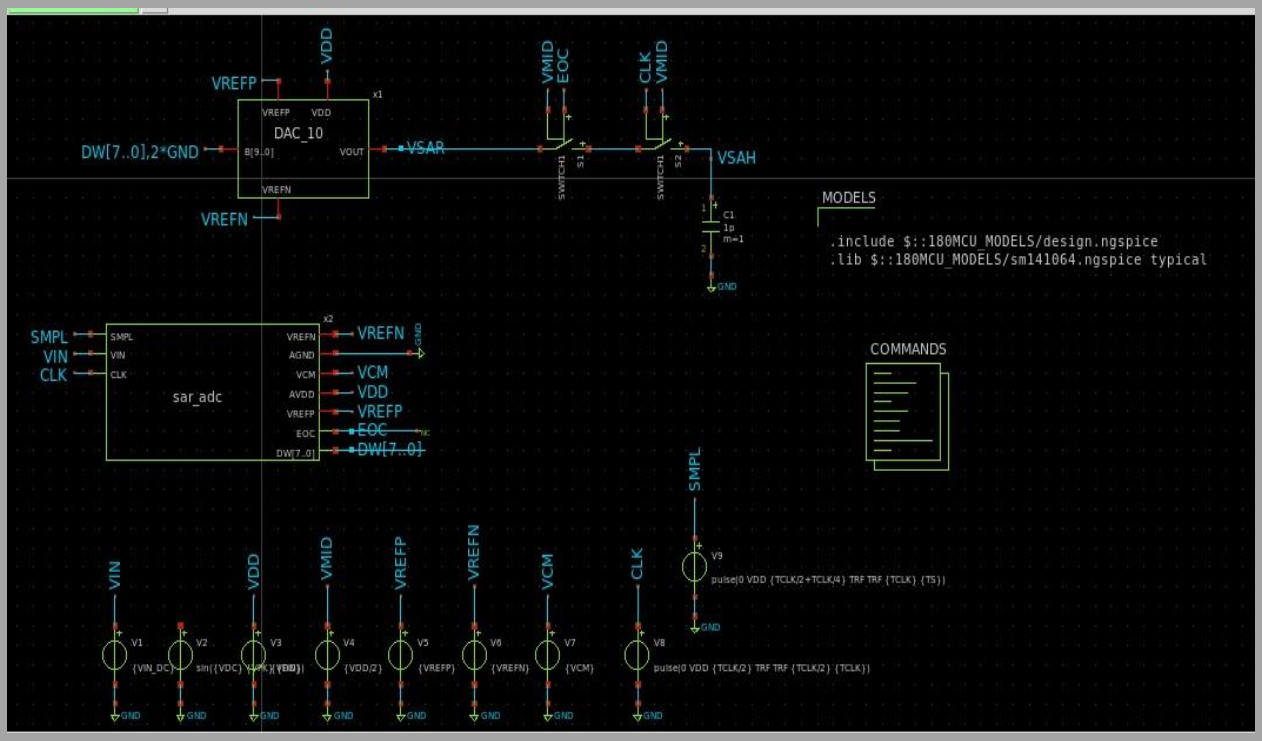
Symbol:

SAR ADC DESIGN



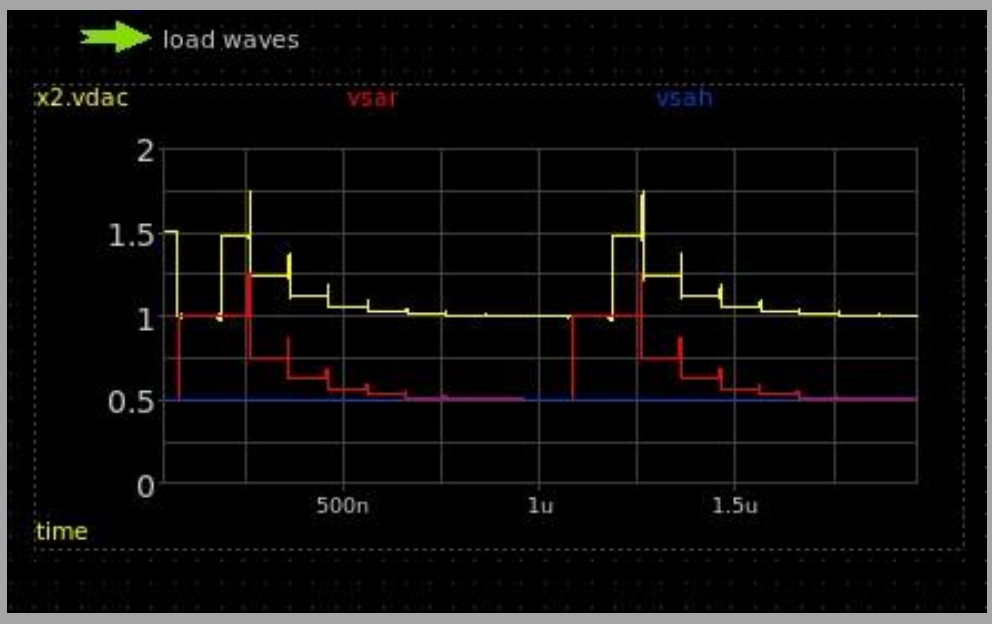
Symbol :

SAR ADC TestBench:

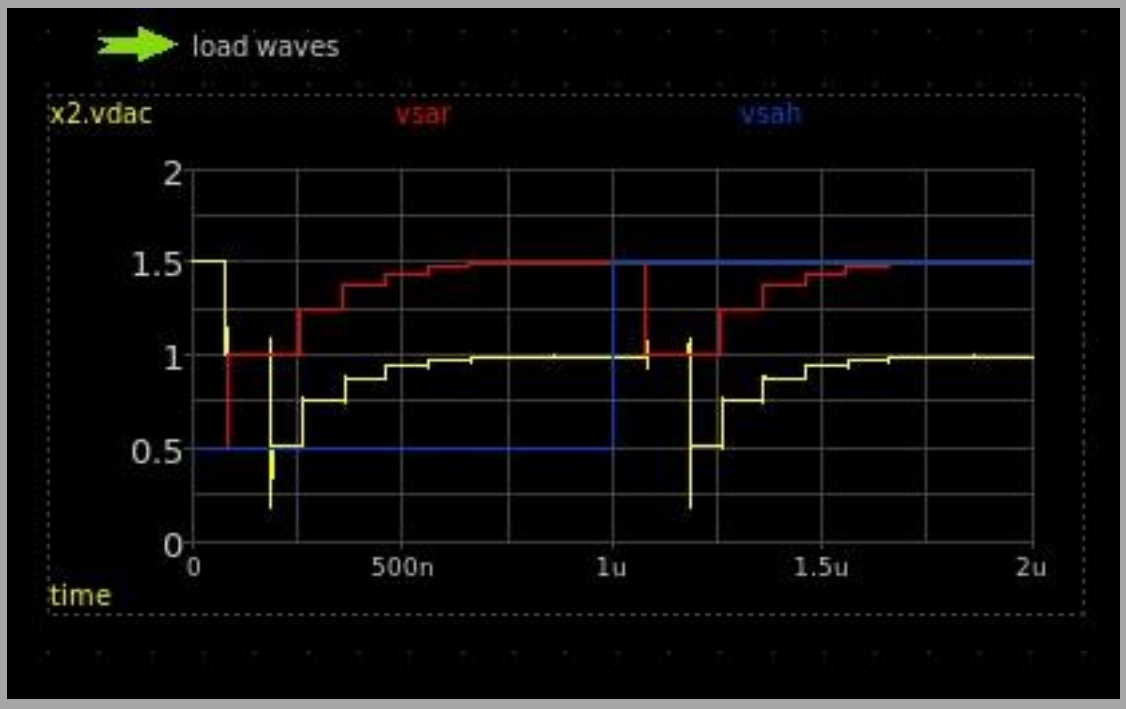


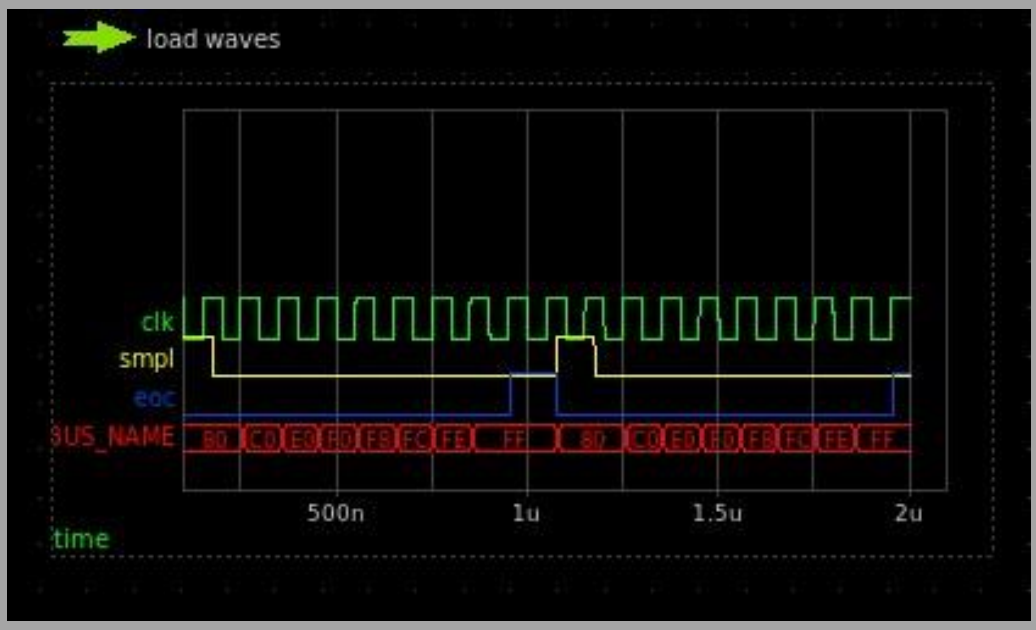
Part5(DC TEST)

Case (1) VIN = VREFN :

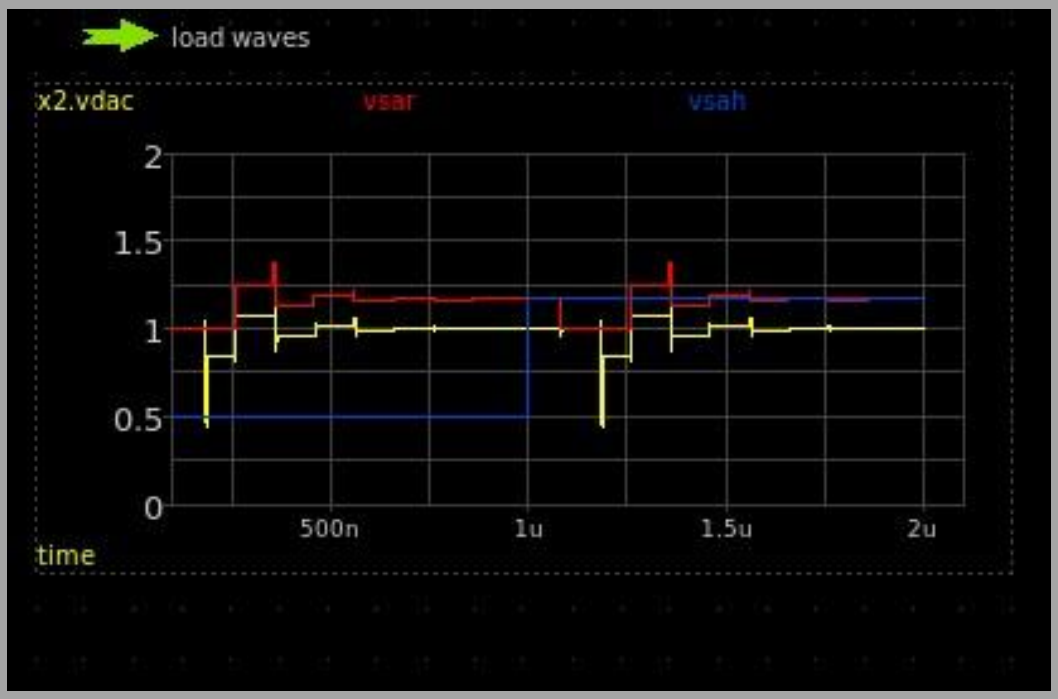


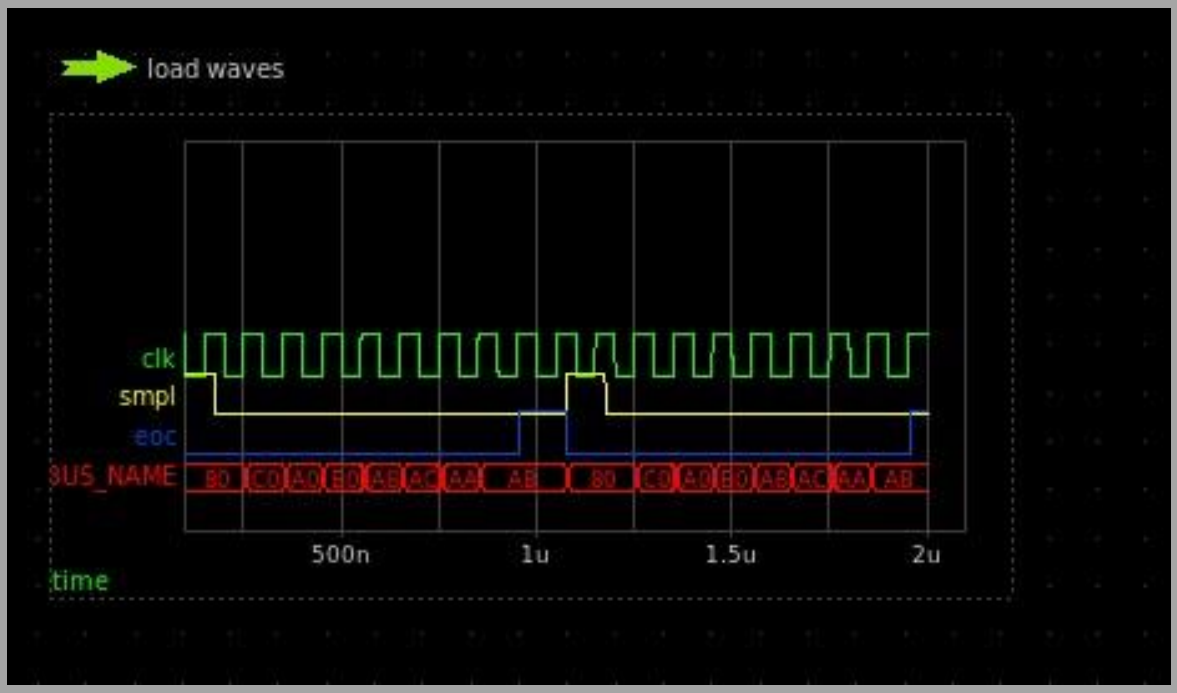
Case (2) VIN = VREFP :



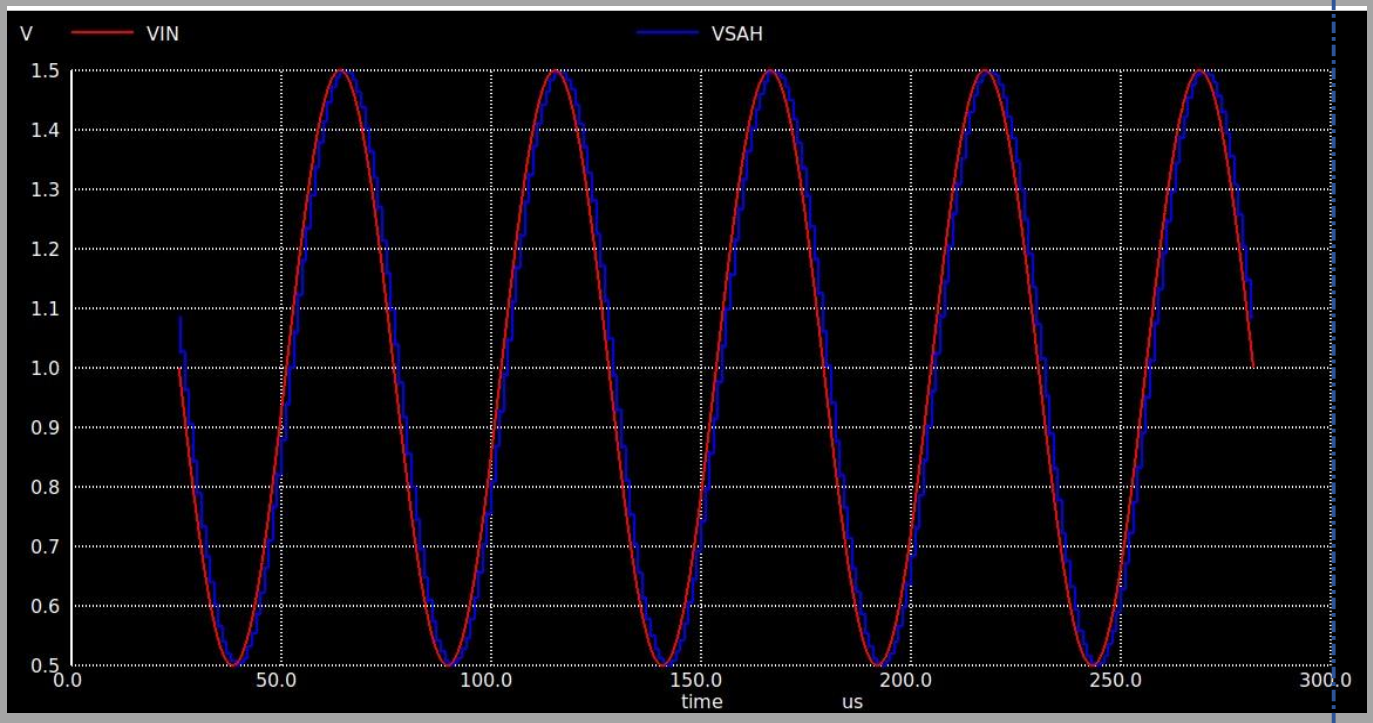


Case (3) VIN = VREFN + (128+32+8+2+0.5)*VLSB:

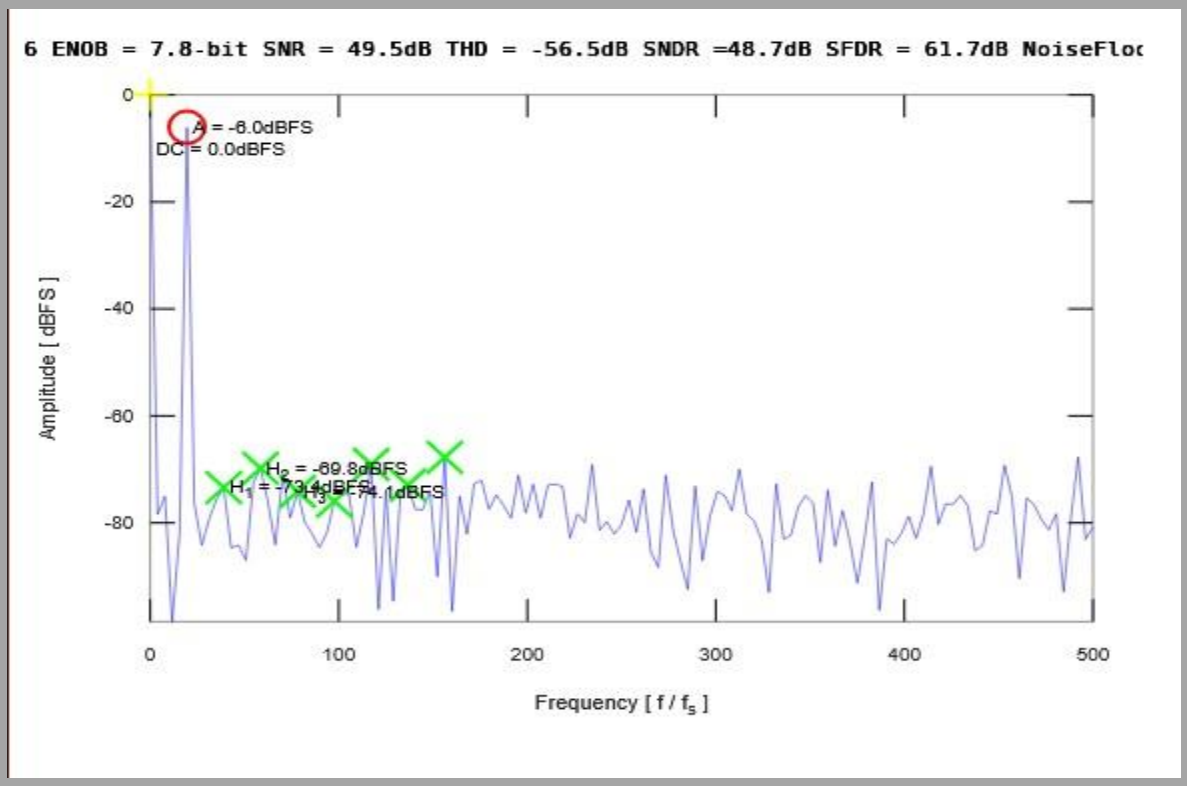


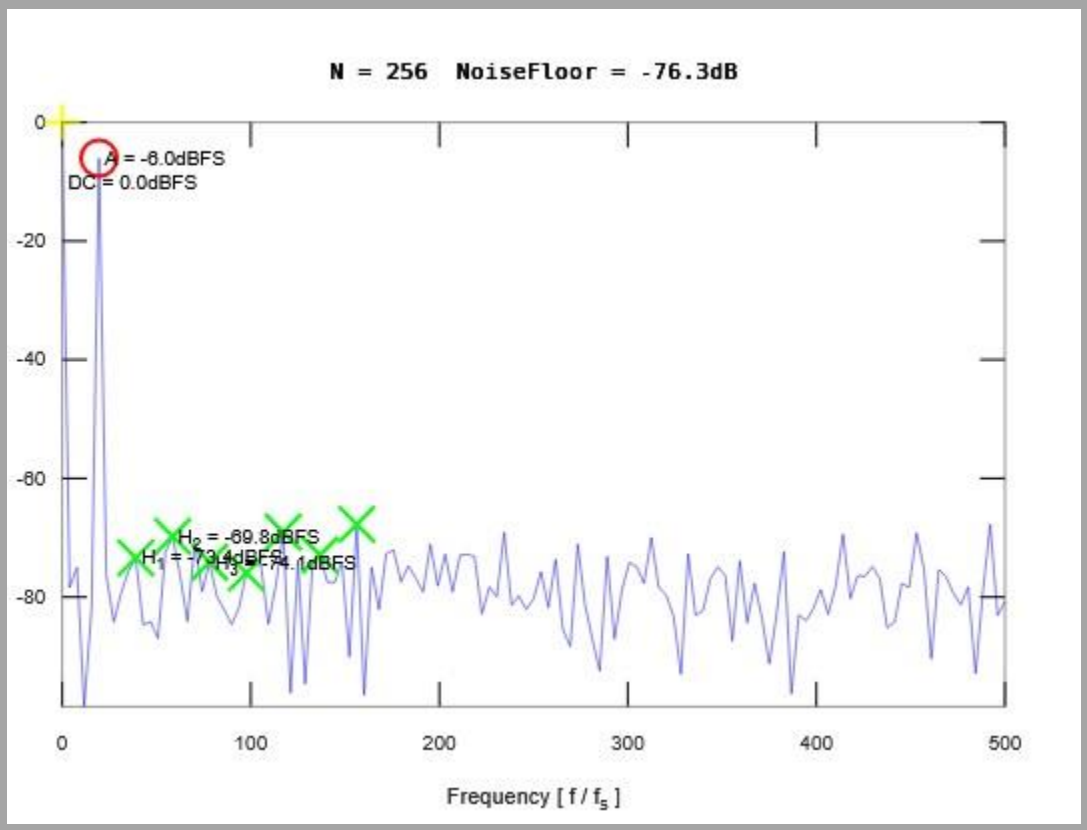


Part 6 (Sine Wave Test)



FFT:


6 ENOB = 7.8-bit SNR = 49.5dB THD = -56.5dB SNDR =48.7dB SFDR = 61.7dB NoiseFloo
A = -6.0dBFS
DC = 0.0dBFS
H2 = -69.8dBFS
H1 = -73.4dBFS
H3 = -74.1dBFS
Amplitude [dBFS]
Frequency [f / fs]
0
-20
-40
-60
-80
0
100
200
300
400
500


N = 256 NoiseFloor = -76.3dB
A = -6.0dBFS
DC = 0.0dBFS
H2 = -69.8dBFS
H1 = -73.4dBFS
H3 = -74.1dBFS
Frequency [f / fs]
0
-20
-40
-60
-80
0
100
200
300
400
500

Spec	Reported value
ENOB	7.8 bit
SINAD	48.7 dB
SNR	49.5 dB
SFDR	61.7 dB
THD	-56.5 dB
SIGNAL POWER	-9 dB (-6 dB rms)
DC POWER	0 dB

COMMENT :

SNR – SNDR = 0.9 dB (a reasonable value that state that the distortion effect on SNR is very weak here).

Effective number of bits is 7. 8 Which is nearly 8 bits and this is what we aim to design (8-bit SAR ADC).

SFDR is large due to the weakness of distortions components (low level of harmonics) and power efficiency .

Noise floor is -76.3 dB indicates a good design .