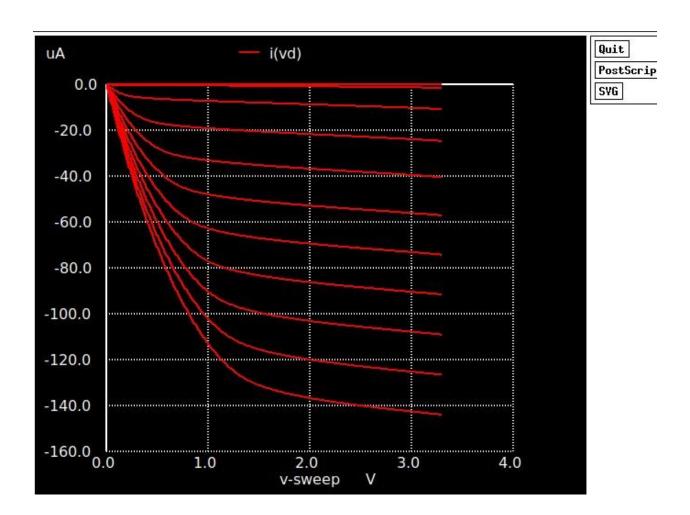
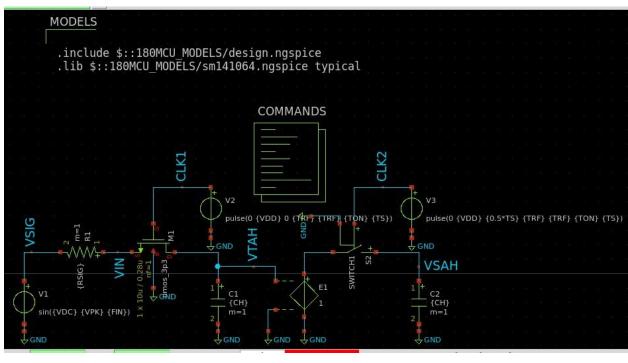
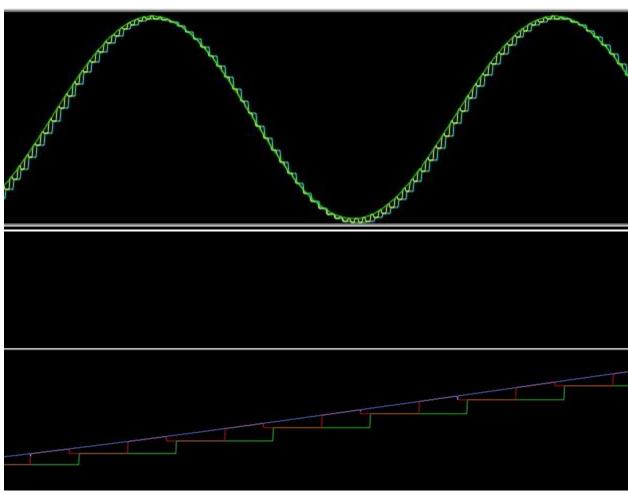
Lab 3

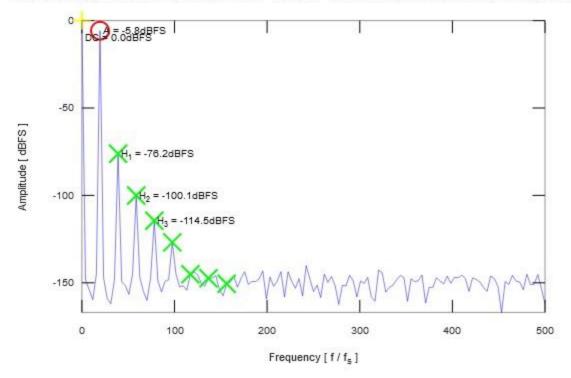
Part 1 (prelab)



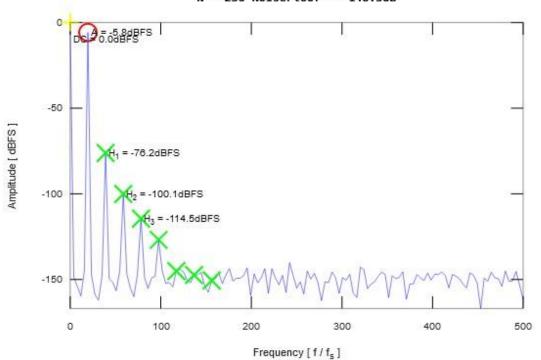




ENOB = 11.4-bit SNR = 121.8dB THD = -70.4dB SNDR =70.4dB SFDR = 70.4dB NoiseFlc







	Lab3	Lab2
ENOB	11.4 bit	20.4 bit
SINAD	70.4 db	124.4 db
SNR	121.8 db	124.8 db
SFDR	70.4 db	139.5 db
THD	-70.4 db	-136.2 db
SIGNAL POWER	-8.85 db	-9 db
DC POWER	0 db	0db
Highest harmonic	Second harmonic	Fourth harmonic
	(H1)	(H3) but with
		weak effect

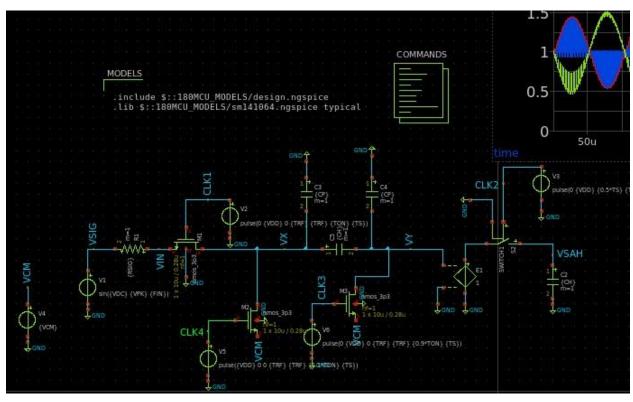
From the result we observe that replacing an ideal switch with Nmos increased the harmonic effect in frequency domain .

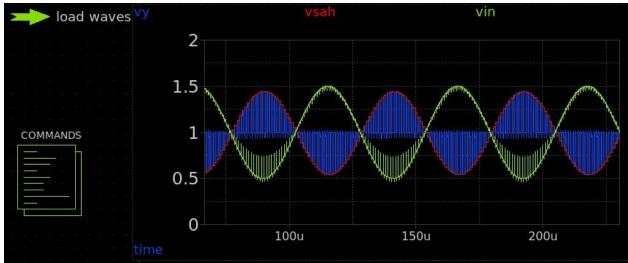
Second harmonic has large power decreasing noise floor.

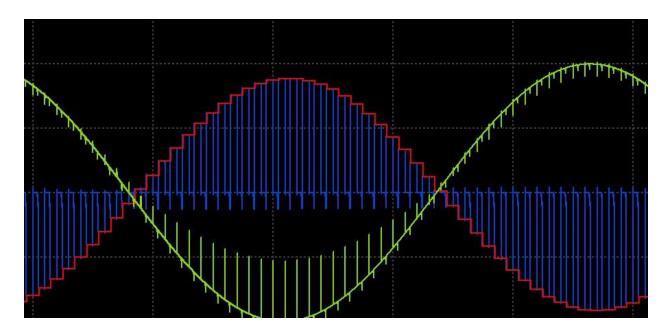
This observable harmonic effect leads to decreasing SNR , SNDR THD SFDR and the effective number of bits .

Replacing an ideal switch with a practical NMOS transistor introduces signal-dependent resistance, parasitic capacitances, charge injection, and body effect, all of which contribute to nonlinear distortion. These effects are asymmetric, which enhances even-order harmonics, particularly the second harmonic

PART 2

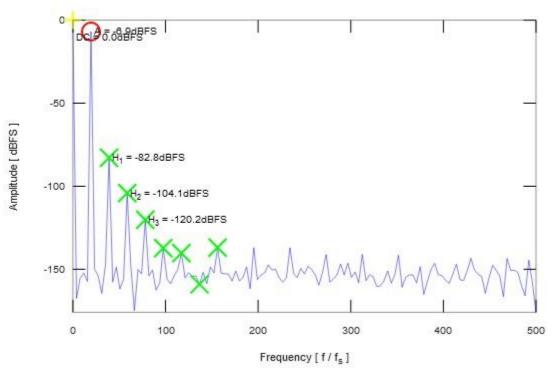






FFT:

ENOB = 12.3-bit SNR = 121.7dB THD = -75.9dB SNDR =75.9dB SFDR = 76.0dB NoiseFlc



N = 256 NoiseFloor = -149.4dB

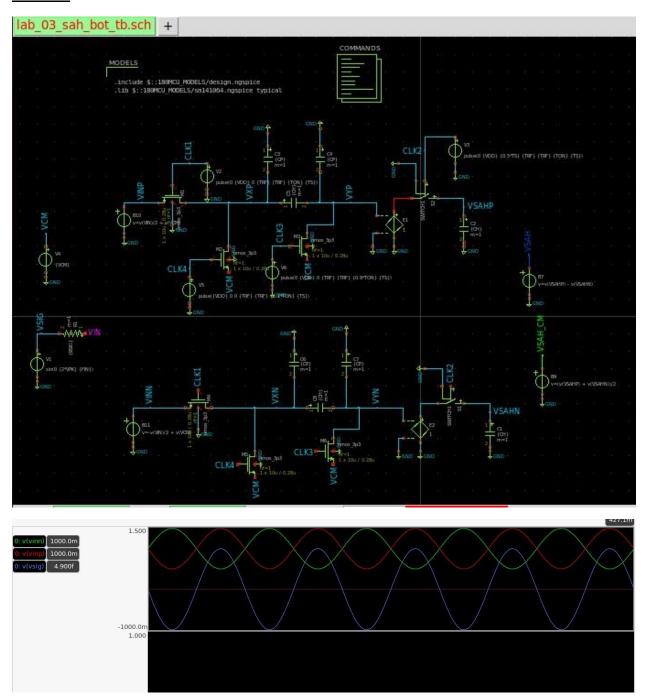
	Part 1	Part 2
ENOB	11.4 bit	12.3 bit
SINAD	70.4 db	75.9 db
SNR	121.8 db	121.7 db
SFDR	70.4 db	76 db
THD	-70.4 db	-75.9 db
SIGNAL POWER	-8.85 db	-13.8 db
	(-5.8db rms)	(-6.9db rms)
DC POWER	0 db	0db
Highest harmonic	Second harmonic	Second harmonic
	(H1)	(H1)

from the plot we can see that bottom plate sampling enhance SFDR and SNDR due to decreasing the effect of harmonic distortion

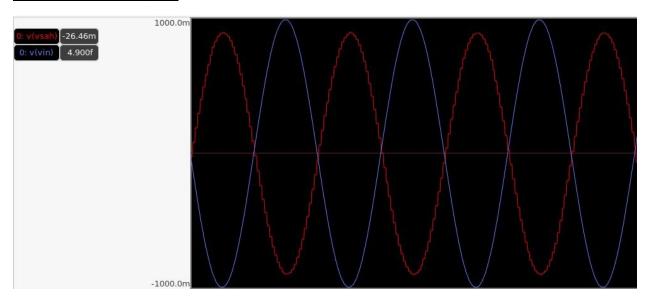
SNR is nearly the same as the harmonics doesn't affect it
Signal power is affected with the bottom plate parasitic capacitance
The effective number of bits increased.

A practical NMOS transistor introduces signal-dependent resistance, parasitic capacitances, charge injection, and body effect, all of which contribute to nonlinear distortion. These effects are asymmetric, which enhances even-order harmonics, particularly the second harmonic

<u>Part 3:</u>



Differential output

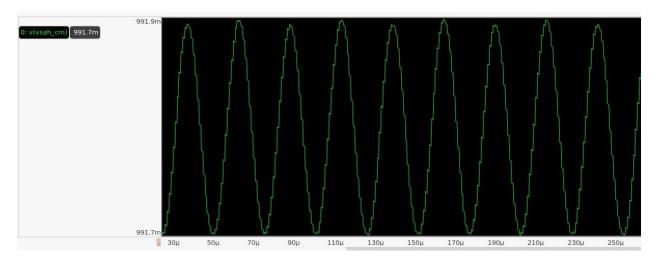


Comment:

Remains equal to the input peak-to-peak differential voltage but inverted.

Less distortion compared to a single-ended design and rejects even harmonics

Common mode waveform:

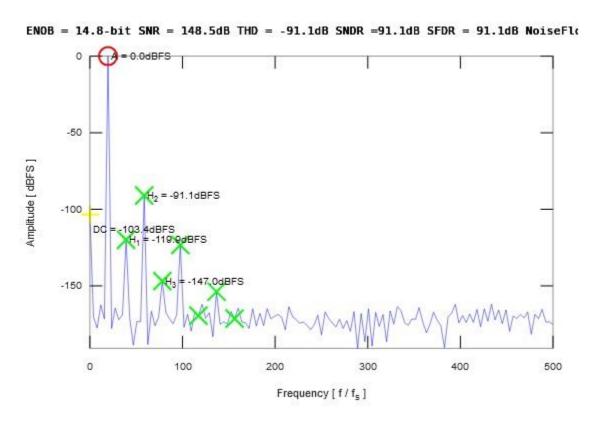


Comment:

Ideally constant but may exhibit small ripples due to mismatches.

Should be well-controlled to ensure minimal interference with the differential signal.

FFT:



N = 256 NoiseFloor = -170.1dB

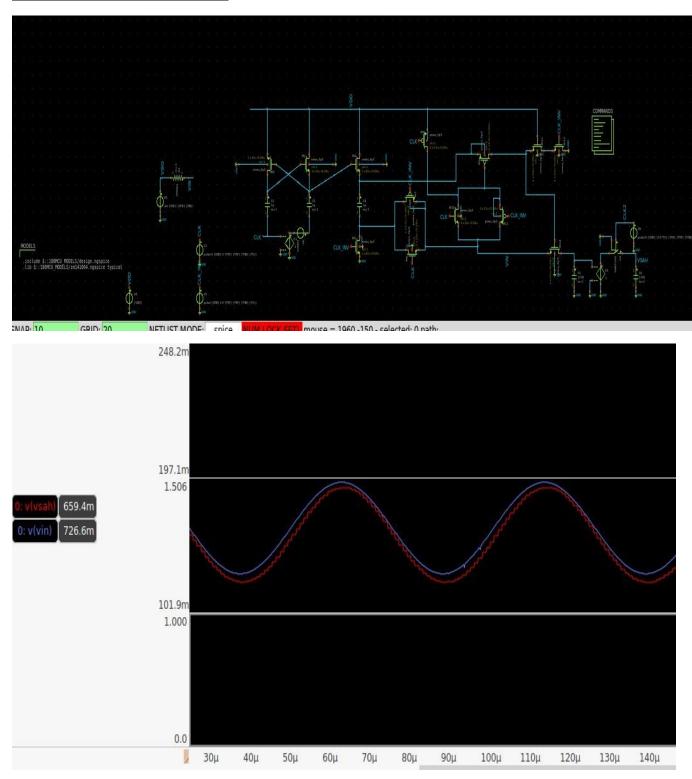
	Part 3	Part 2
ENOB	14.8 bit	12.3 bit
SINAD	91.1 db	75.9 db
SNR	148.5 db	121.7 db
SFDR	91.1 db	76 db
THD	-91.1 db	-75.9 db
SIGNAL POWER	0 db	-9.8 db
		(-6.9db rms)
DC POWER	0 db	0db
Highest harmonic	Third harmonic	Second harmonic
	(H2)	(H1)

We can notice that using fully differential circuit enhanced both the SNR and SNDR as it helps in canceling even-order distortions, improving linearity, and reducing supply noise sensitivity.

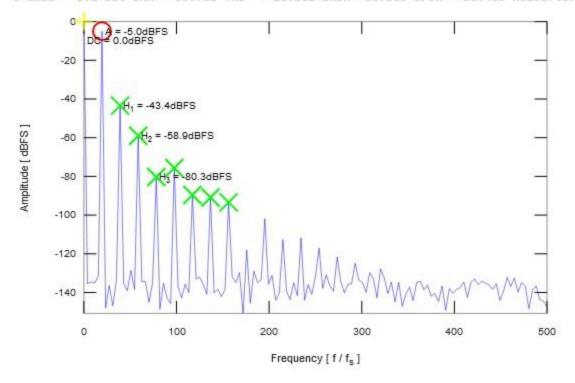
The rejection of even harmonics enhanced SFDR and now the third harmonic has the most peak .

The effective number of bits and signal power increased .

Bootstrabing circuit



6 ENOB = 6.1-bit SNR = 95.7dB THD = -38.3dB SNDR =38.3dB SFDR = 38.4dB NoiseFlox



We notice that the effective number of bits is low compared to the last parts and the harmonic distortion is highly observed .