Lab 3

Part 1 (prelab):

1-Lib file :

```
*----------------------------------*
* Part 1.1
.model nmos_part1_1 NMOS (LEVEL=1 VTO=0.4 KP=183.7u LAMBDA=0)

*----------------------------------*
```

I= 0.5 *KP*(w/l)*(Vgs-VT0)**2

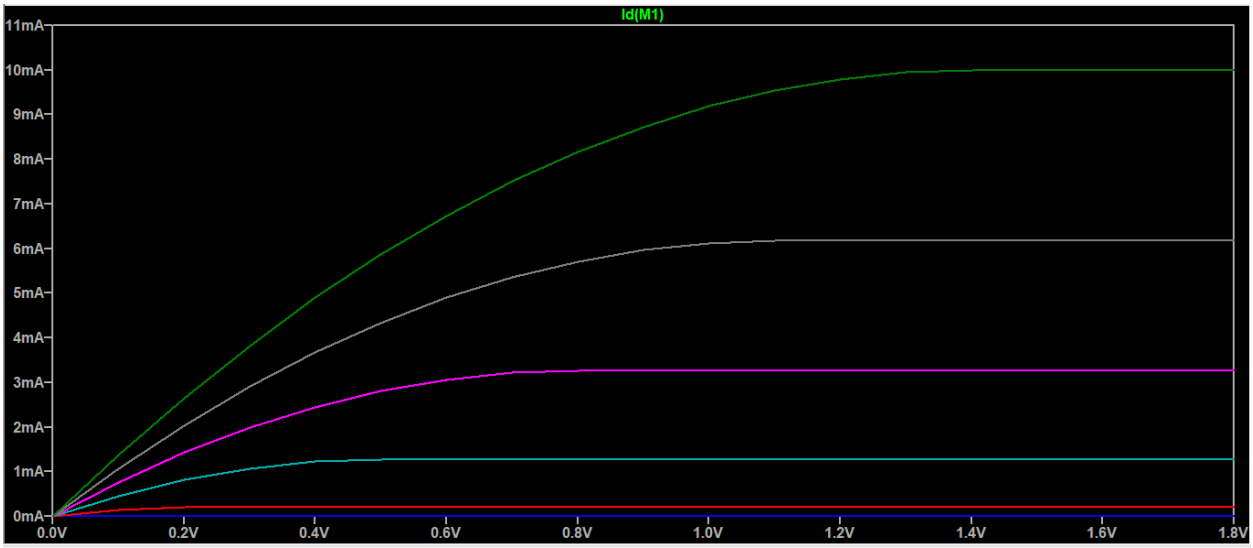
10m=0.5*KP*(10/0.18)*(1.8-0.4)**2 KP = 183.7u

Netlist :

```
NMOS testbench

* add a line here to include the model library
.lib "C:/Users/DELL/Desktop/Siemens AMS 2025/lab3/my_nmos.lib"

** Circuit Description **

VGS 1 0 DC 1.8V
* add a line here (VDS source)
VDS 2 0 DC 1.8V
* add a line here (MOSFET instantiation)
M1 2 1 0 0 nmos_part1_1 W=10u L=180n
** Analysis Requests **
* add a line here to do the nested DC sweep
.DC VDS 0 1.8 0.1 VGS 0 1.8 0.3
.plot dc i(VDS) v(2)
.END
```

Results:

```
LTspice 24.1.9 for Windows
Circuit: C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\nmos_tb.cir
Start Time: Fri Aug  1 03:38:05 2025
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = trap
Instance "M1": Length shorter than recommended for a level 1 MOSFET.
Instance "M1": Width narrower than recommended for a level 1 MOSFET.
.OP point found by inspection.
.step VGS=0
.step VGS=0.3
.step VGS=0.6
.step VGS=0.9
.step VGS=1.2
.step VGS=1.5
.step VGS=1.8
Total elapsed time: 0.205 seconds.
```



Comment:

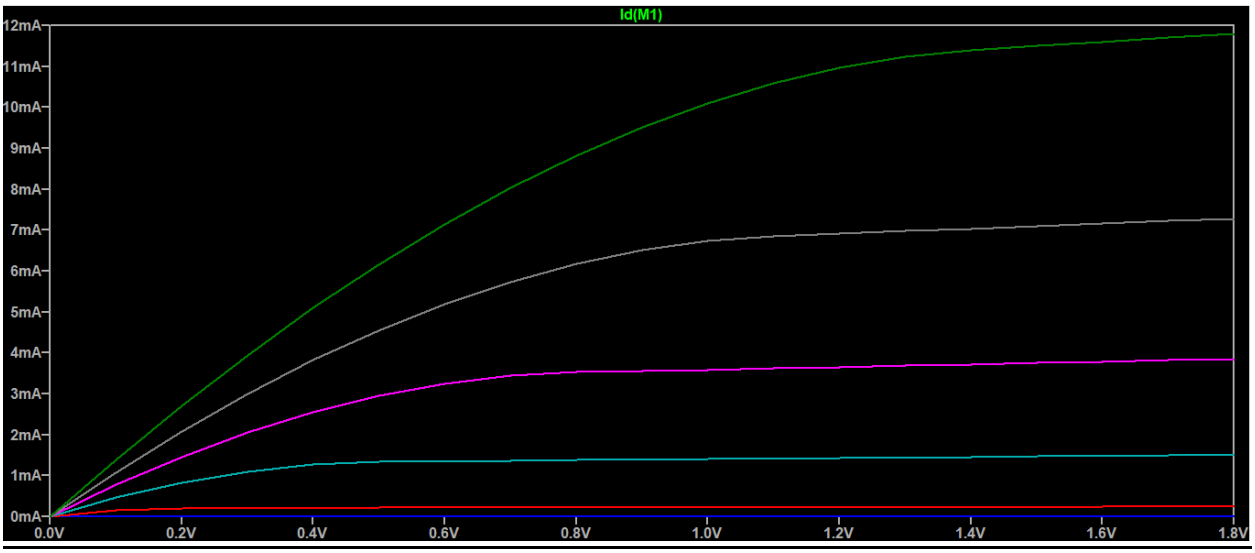
The two warnings are because we are using level 1 model which is used for long and wide channels so the 180nm technology with w=10um is considered small to be used with this model.

2-Lib file :

```
*-----------------------------------*
* Part 1.1
.model nmos_part1_1 NMOS (LEVEL=1 VTO=0.4 KP=183.7u LAMBDA=0)

*-----------------------------------*

* Part1.2
* add a line here (same as Part 1.1 except for one more parameter)
* Don't forget to change the model name to nmos_part1_2
.model nmos_part1_2 NMOS (LEVEL=1 VTO=0.4 KP=183.7u LAMBDA=0.1)
```

Lambda = 1/VA = 1/10 =0.1

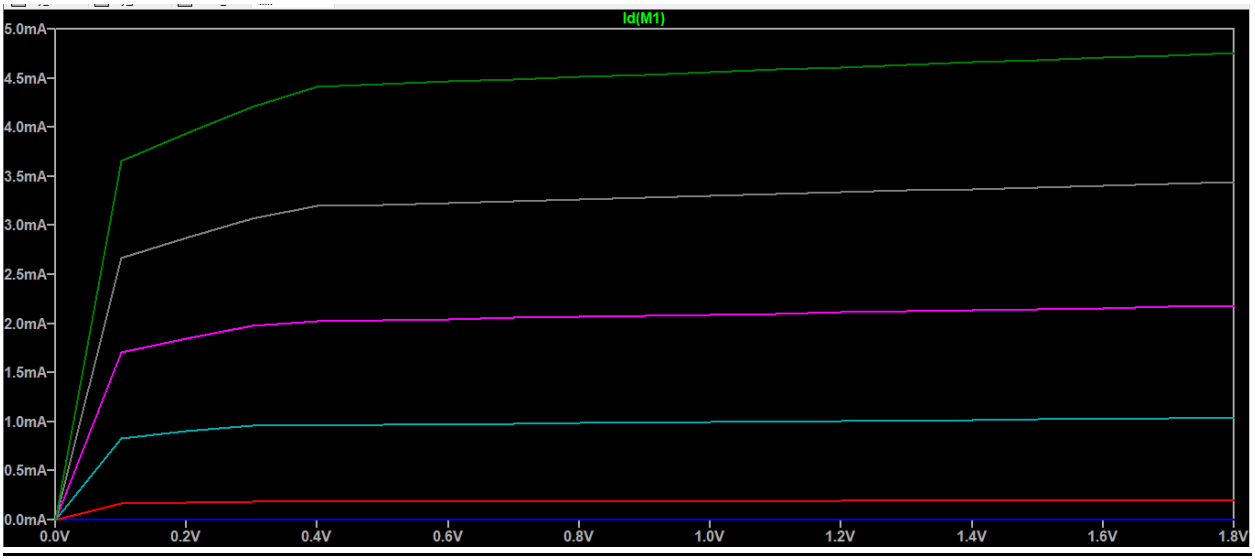
Simulation:



3-lib file

```
* Part 1.3
*.add a line here (same as Part 1.2 except for one more parameter)
.model nmos_part1_3 NMOS (LEVEL=2 VTO=0.4 KP=183.7u LAMBDA=0.1 vmax= 1.5e5 CJ=0 CJSW=0)

*-----------------------------------*
```

Simulation :



4- lib file :

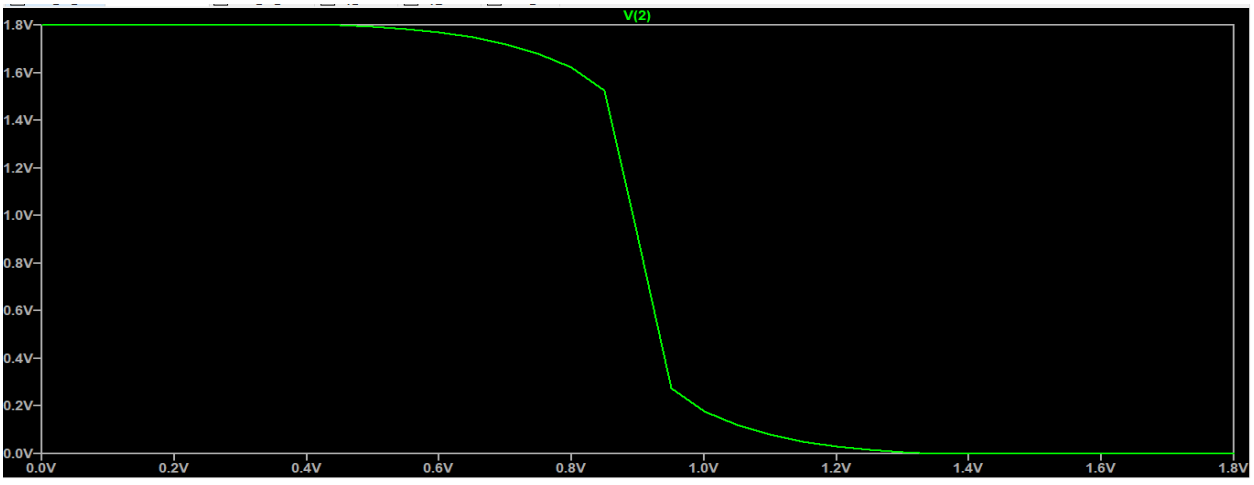
```
* my_pmos.lib
.model pmos_part1_2 PMOS (LEVEL=1 VTO=-0.4 KP=91.85u LAMBDA=0.1)


*-----------------------------------*
```

Note: the vt0 is negative

Netlist:

```
* Power supply
VDD 3 0 DC 1.8V

* Input
VIN 1 0 DC 0V

* Circuit (PMOS on top, NMOS on bottom)
M1 2 1 0 0 nmos_part1_2 W=10u L=180n
M2 2 1 3 3 pmos_part1_2 W=20u L=180n

* Include model files
.lib "my_nmos.lib"
.lib "my_pmos.lib"

** Analysis Requests **
.DC VIN 0 1.8 0.05

** Output Requests **
*.PROBE

.plot V(2) vs V(1)
.meas vm find V(1) when V(2)=V(1)

.END
```

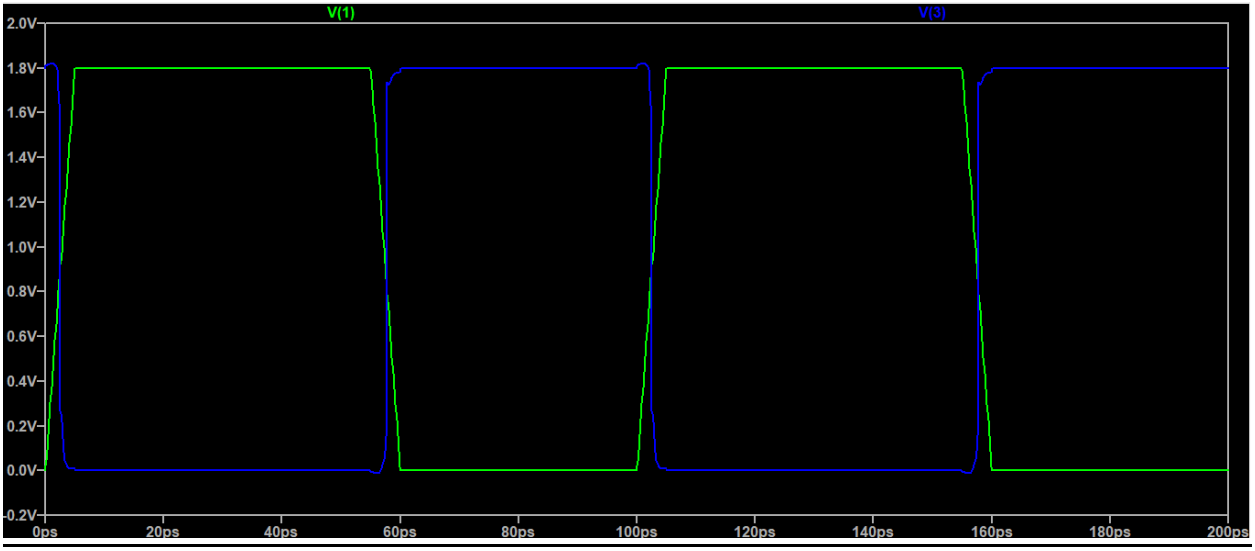
Simulation:



5- netlist :

```
* Include model
.lib "my_nmos.lib"
.lib "my_pmos.lib"

** Circuit Description **

VDD 2 0 DC 1.8V

* Pulse input: VIN from 0V to 1.8V, period=100ps, rise/fall=5ps, pulse width=50ps
VIN 1 0 PULSE(0 1.8 0 5p 5p 50p 100p)

* Circuit (PMOS on top, NMOS on bottom)
M1 3 1 0 0 nmos_part1_6 W=10u L=180n AD=4.5 AS=4.5 PD=20.9 PS=20.9
M2 3 1 2 2 pmos_part1_6 W=20u L=180n AD=4.5 AS=4.5 PD=20.9 PS=20.9

** Analysis Requests **
.TRAN 1p 200p

** Output Requests **
.MEAS TRAN t_PHL TRIG V(1) VAL=0.9 RISE=1 TARG V(3) VAL=0.9 FALL=1
.MEAS TRAN t_PLH TRIG V(1) VAL=0.9 FALL=1 TARG V(3) VAL=0.9 RISE=1

.measure tran tp param='(t_PHL+t_PLH)/2'

.END
```

Simulation:



Delay measurement :

```
t_phl=1.16779178032e-15 FROM 2.50000003844e-12 TO 2.50116783022e-12
t_plh=2.05234585604e-13 FROM 5.75000000356e-11 TO 5.77052346212e-11
tp: '(t_PHL+t_PLH)/2'=1.03201188692e-13
```

6-

λ = Lmin / 2 → λ = 180nm / 2 = 90nm = 0.09µm

LDIFF = 5 × λ = 0.45µm

W = 10µm

Junction Area = LDIFF × W = 4.5 µm²

Junction Perimeter = 2 × (LDIFF + W) = 2 × (0.45 + 10) = 20.9 µm

Model modifications :

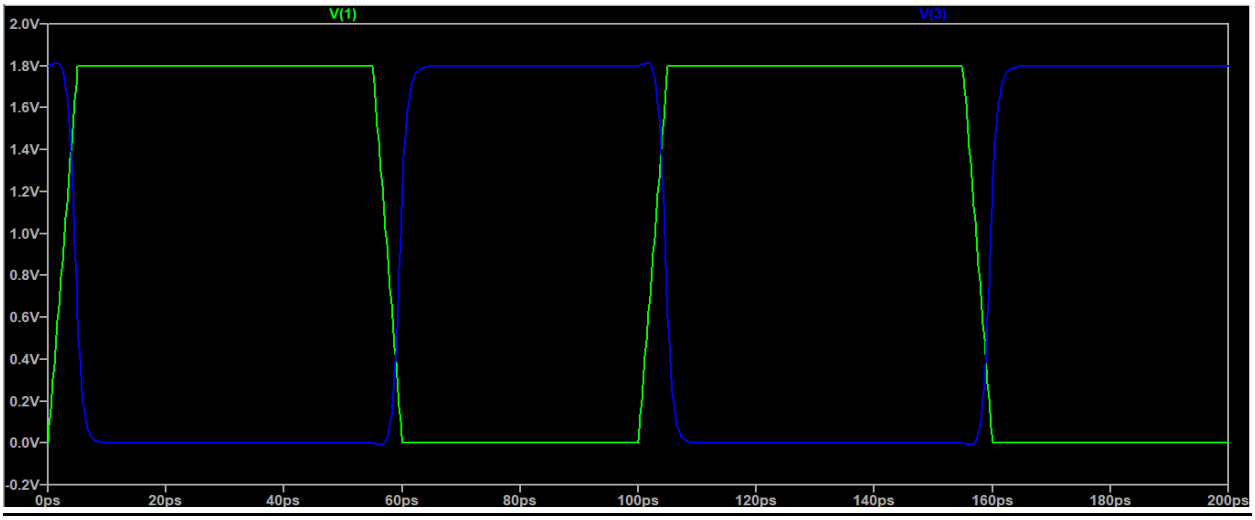
```
* Part 1.6
* add a line here (same as Part 1.3 but you have to add CJ and CJSW. Take care of the units)
.model nmos_part1_6 NMOS (LEVEL=3 VT0=0.4 KP=183.7u CJ=1e-15 CJSW=1e-16)
*-----------------------------------*
```

```
* Part 1.6
* add a line here (same as Part 1.3 but you have to add CJ and CJSW. Take care of the units)
.model pmos_part1_6 PMOS (LEVEL=3 VT0=-0.4 KP=91.85u CJ=1e-15 CJSW=1e-16)
*-----------------------------------*
```

Delay measurement :

```
t_phl=2.10587723147e-12 FROM 2.50000003844e-12 TO 4.60587726991e-12
t_plh=2.10678372286e-12 FROM 5.75000000568e-11 TO 5.96067837796e-11
tp: '(t_PHL+t_PLH)/2'=2.10633047716e-12
```

Simulation :



We can notice that adding the capacitances effect made the delay much bigger

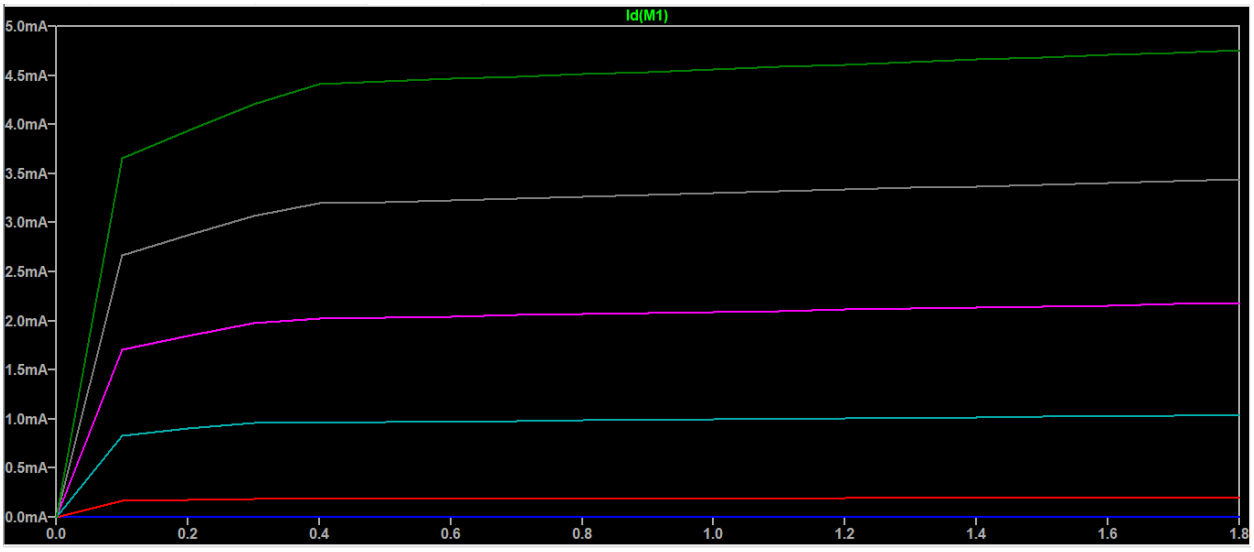
Added effect is (AD*CJ , AS*CJ , PD*CJSW , PS*CJSW)

Part 2:

1- nmos_tb_param.cir

```
* Include model library
.lib "C:/Users/DELL/Desktop/Siemens AMS 2025/lab3/my_nmos.lib"

** Parameter definition **
.param VGSval = 0
.param VDSval = 0
** Circuit Description **
VGS 1 0 DC 'VGSval'
VDS 2 0 DC 'VDSval'
M1 2 1 0 0 nmos_part1_3 W=10u L=180n

** Analysis Requests **
*.DC VDS 0 1.8 0.1
.step param VDSval 0 1.8 0.1
.step param VGSval 0 1.8 0.3
.op
.plot dc i(VDS) v(2)

.END
```

Simulation:



Simulation time for parametric sweep case :

```
.step vgsval=1.8
Total elapsed time: 1.683 seconds.
```

Simulation time for nested DC sweep case :

```
.step VGS=1.8
Total elapsed time: 0.190 seconds.
```

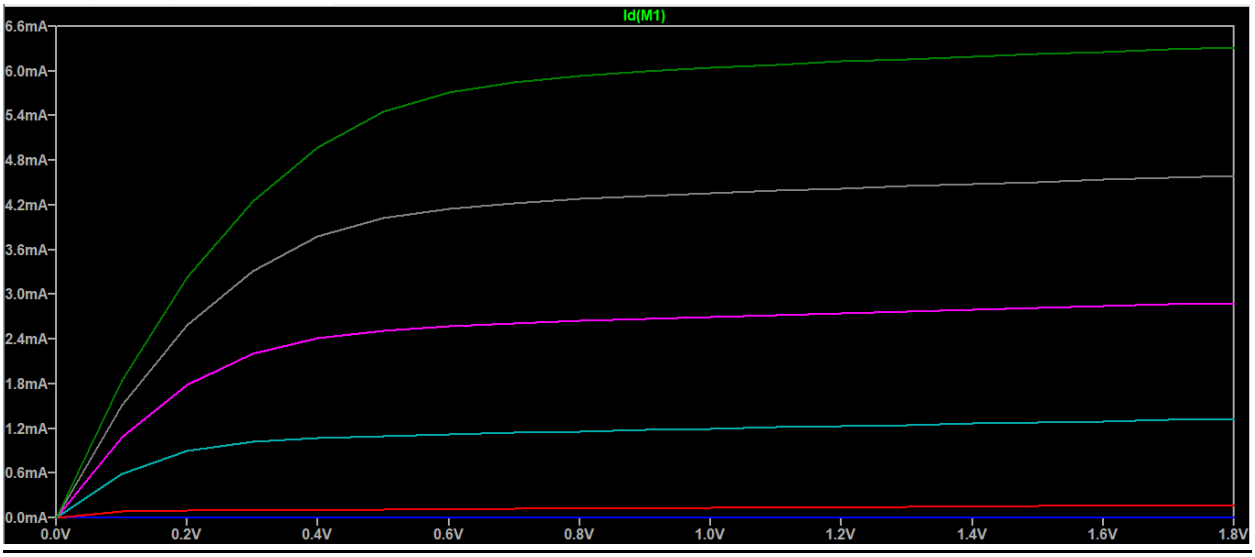
Comment:

Although the two cases gives the same simulation results but the parametric sweep takes more time than the nested dc sweep case because in parametric sweep the simulator solves the whole circuit again for each step taken

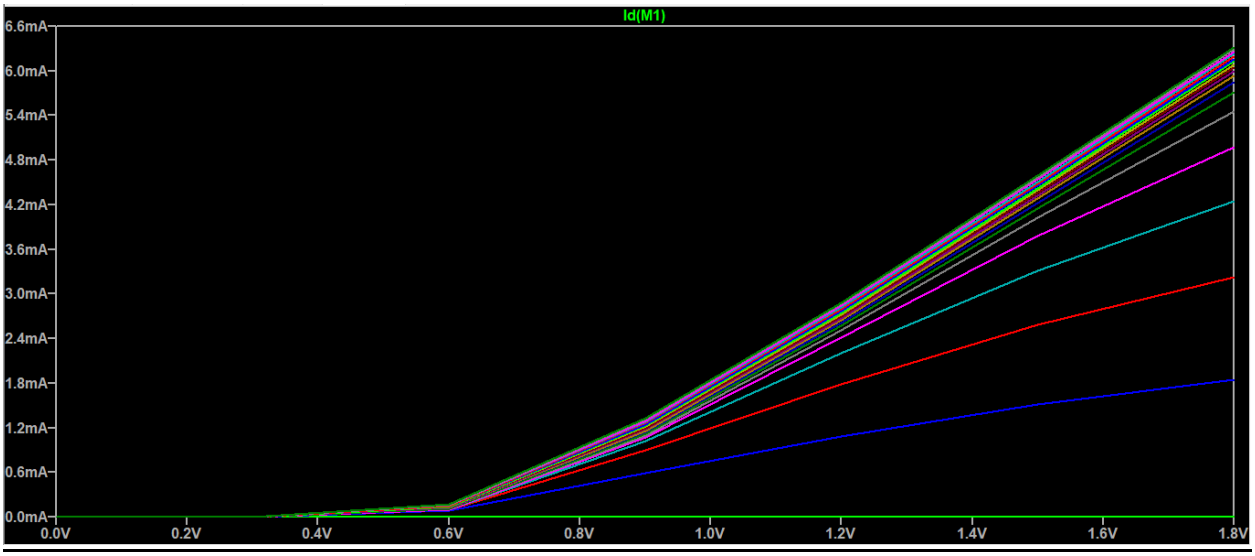
2- netlist :

```
* add a line here to include the model library
.inc "C:/Users/DELL/Desktop/Siemens AMS 2025/lab3/ee214b_hspice.sp"

** Circuit Description **

VGS 1 0 DC 1.8V
* add a line here (VDS source)
VDS 2 0 DC 1.8V
* add a line here (MOSFET instantiation)
M1 2 1 0 0 nch W=10u L=180n
** Analysis Requests **
* add a line here to do the nested DC sweep
.DC VDS 0 1.8 0.1 VGS 0 1.8 0.3
.plot dc i(VDS) v(2)
.END
```

Simulation: (I vs VDS)



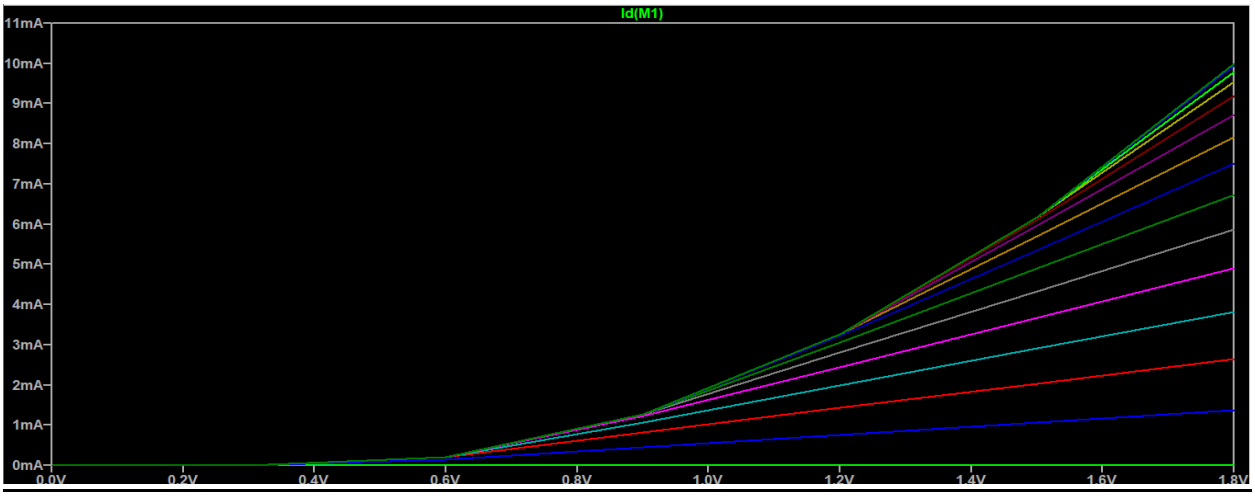
(I vs VGS)



Velocity saturation limitation can be easily observed here.

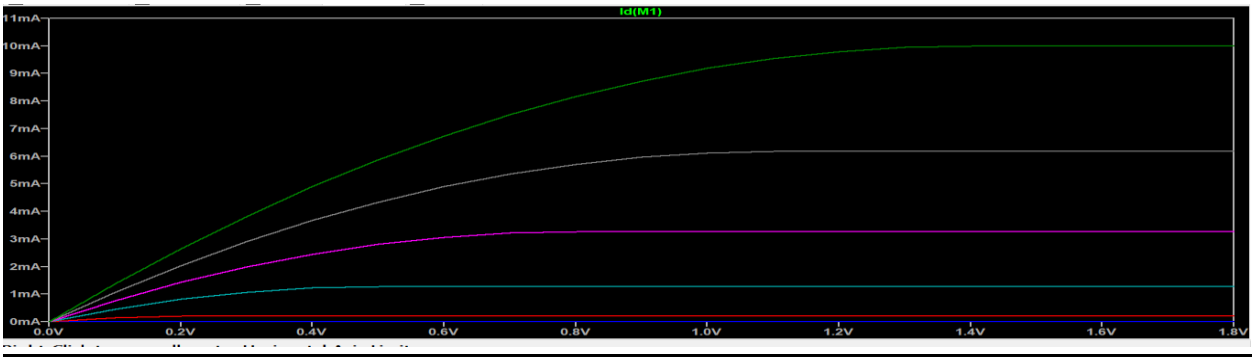
For the level 1 model

I vs VGS



No velocity saturation limitations .

I vs VDS



What version of BSIM is this HSPICE model?

BSIM3 V3.3

How to set the LEVEL parameter appropriately for LTspice in this case?

In LTSpice the model BSIM3 V3.3 corresponds to level 8 so we should set the level parameter LEVEL =8

Compare the results to your LEVEL 1 model.

Velocity saturation limitation can be easily observed for the HSpice model but for level 1 there is no saturation limitation

```
LTspice 24.1.9 for Windows
Circuit: C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\nmos_tb.cir
Start Time: Mon Aug  4 03:49:41 2025
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(17): Ignoring unknown model parameter. This may or may not be a problem.
+ xtf=200 itf=80m ikf=12m ikr=10.5m nkf=0.9
                                  ^^^^^^^^
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(103): Ignoring unknown model parameter. This may or may not be a problem.
+PVSAT    = 1.19774E3      PETA0    = 9.968409E-5    PKETA    = -2.51194E-3###>

+cjgate   = 0<###              noimod   = 6              noia     = 1e19
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(183): Ignoring unknown model parameter. This may or may not be a problem.
+PVSAT    = -50            PETA0    = 1.003159E-4    PKETA    = -3.89914E-3###>

+cjgate   = 0<###              noimod   = 6              noia     = 1e19
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(199): Ignoring unknown model parameter. This may or may not be a problem.
.model dwell d cj0=2e-4 is=1e-5 m=0.5 pb=0.8
                                  ^^^^^^^
Ignoring BSIM parameter ACM
Ignoring BSIM parameter HDIF
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
solver = Normal
```

3-

Parameter	Meaning	Expected impact
ACM	Area Calculation Method: Defines how the area of source/drain junctions is computed	Affects junction capacitance and leakage modeling.
HDIF	Source/Drain diffusion height	Affects parasitic resistance and capacitance.
XL ,XW	Length/Width offsets to model layout-dependent effects.	Refines effective `L` and `W`.
cjgate	Gate-to-body junction capacitance per area	Impacts input capacitance and delay modeling.
noia,noimod	Noise modeling parameters	Affects flicker and thermal noise in analog/RF simulation.
PVTH0, PKETA	Process variation parameters	Used for modeling process-dependent shifts in threshold, mobility

Parameter	Value in model
ACM	3
HDIF	0.32e-6
XL,XW	0, -1E-8
cjgate	0
noia	1e19
noimod	6
PETA0	9.968409E-5
PKETA	-2.51194E-3

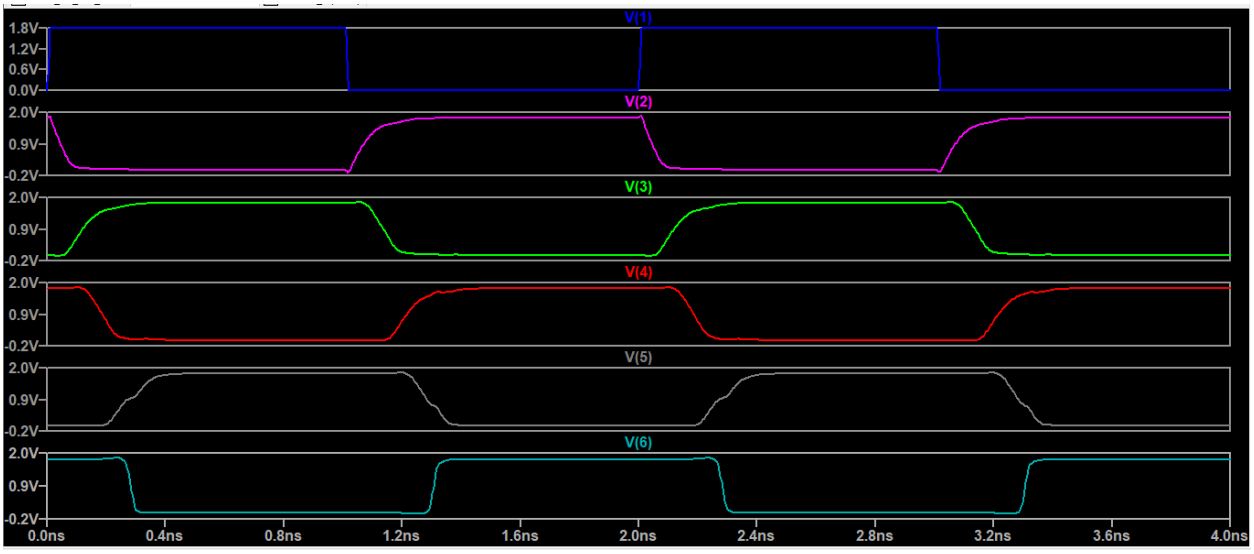
How do you expect they will affect the simulation results?

This can lead to Incorrect Capacitance Modeling , Inaccurate Delay and Slew , Poor Noise Modeling and Neglecting Layout Effects

4-netlist :

```
** Inverter Subcircuit **
.SUBCKT inverter 1 2 3 PARAMS: MULT=1
M1 3 1 0 0 nch L=0.18um W=1um M={MULT}
M2 3 1 2 2 pch L=0.18um W=2um M={MULT}
.ENDS inverter

** Circuit Description **
* power supply
V_VDD VDD 0 DC +1.8V

* input
V_VIN 1 0 PULSE (0 1.8V 0 5p 5p 1n 2n)

* inverters FO4
X_I1 1 VDD 2 inverter PARAMS: MULT={4**0}     ; shape input
X_I2 2 VDD 3 inverter PARAMS: MULT={4**1}     ; shape input
X_I3 3 VDD 4 inverter PARAMS: MULT={4**2}     ; circuit under test
X_I4 4 VDD 5 inverter PARAMS: MULT={4**3}     ; load output
X_I5 5 VDD 6 inverter PARAMS: MULT={4**4}     ; load output

** MOSFET Model **
.inc "C:/Users/DELL/Desktop/Siemens AMS 2025/lab3/ee214b_hspice.sp"

** Analysis Requests **
.TRAN 2p 4n

** Outputs Requests **
*.PROBE

.END
```

Simulation :



Log output :

SPICE Output Log: C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\cmos_inv_tran_fo4.log

```
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(17): Ignoring unknown model parameter. This may or may not b
+ xtf=200 itf=80m ikf=12m ikr=10.5m nkf=0.9
                                ^^^^^^^^
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(103): Ignoring unknown model parameter. This may or may not
+PVSAT   = 1.19774E3      PETA0   = 9.968409E-5    PKETA   = -2.51194E-3###>â€¨â€¨+cjgate  = 0<###             noimod  =
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(183): Ignoring unknown model parameter. This may or may not
+PVSAT   = -50            PETA0   = 1.003159E-4    PKETA   = -3.89914E-3###>â€¨â€¨+cjgate  = 0<###             noimod  =
C:\Users\DELL\Desktop\Siemens AMS 2025\lab3\ee214b_hspice.sp(199): Ignoring unknown model parameter. This may or may not
.model dwell d cj0=2e-4 is=1e-5 m=0.5 pb=0.8
                                ^^^^^^^
Ignoring BSIM parameter ACM
Ignoring BSIM parameter HDIF
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter ACM
Ignoring BSIM parameter HDIF
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = trap
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
Total elapsed time: 0.246 seconds.
```

Delay measurement:

```
t4=2.78476349994e-09 FROM 1.21523650006e-09 TO 4e-09
t1=2.8626688897e-09 FROM 1.1373311103e-09 TO 4e-09
fo4_delay: 't1 - t4'=7.79053897552e-11
fo4_normalized: 'FO4_delay / 90e-9'=0.000865615441725
```

Fo4 measured delay = 77.905 ps

Lambda = Lmin / 2 = 90 nm

Fo4_delay normalized = 77.905 / 90 = 0.8656 ps/nm

For the 65nm technology :

We expect less delay may be in range of 12 -15ps

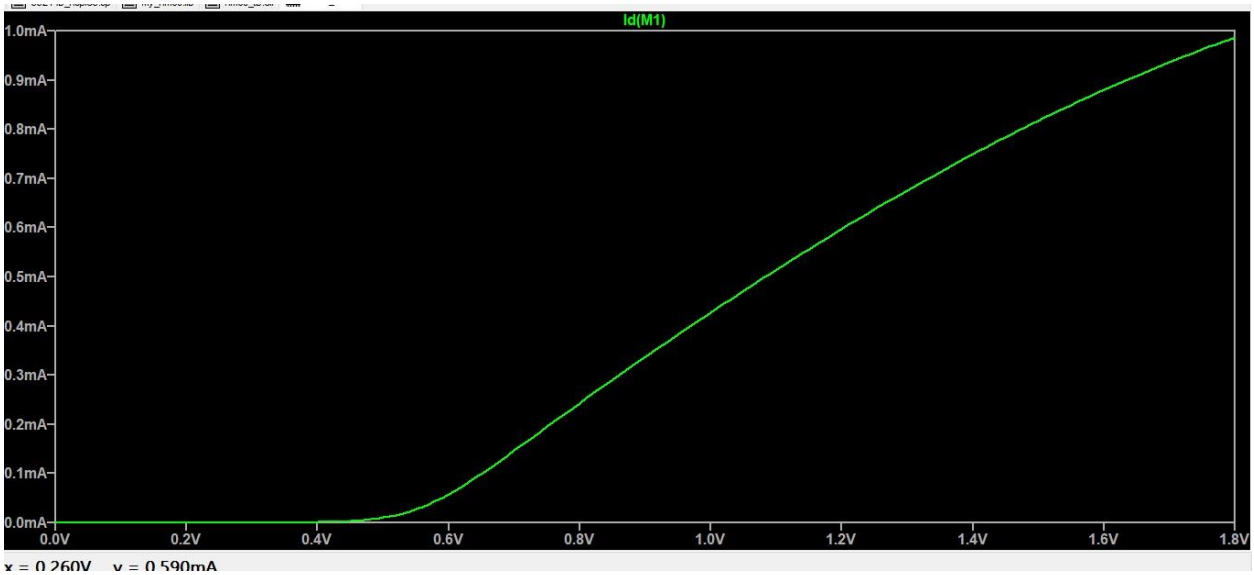
Lambda = 32.5nm

Fo4_delay normalized = 12 / 32.5 = 0.369 ps/nm

Bonus mearuments :

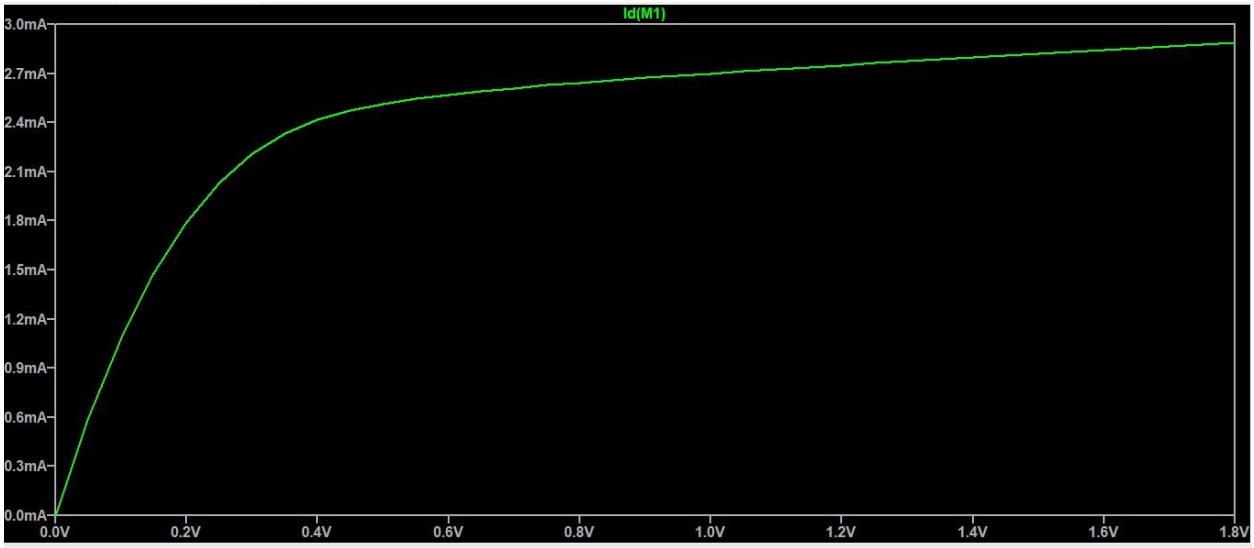
1- Vth

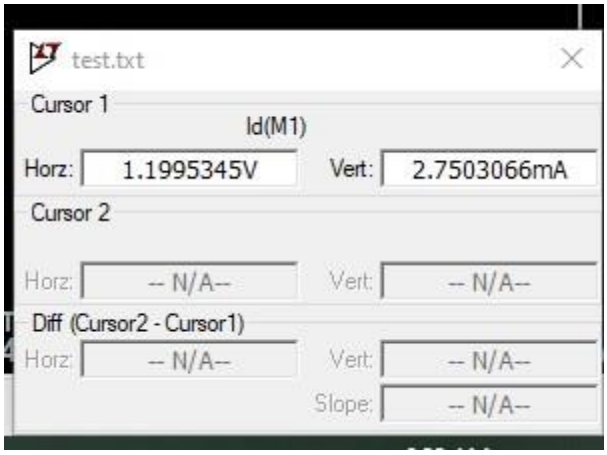
```
* add a line here to include the model library
.inc "C:/Users/DELL/Desktop/Siemens AMS 2025/lab3/ee214b_hspice.sp"

VGS 1 0 DC 0
VDS 2 0 DC 0.05
M1 2 1 0 0 nch W=10u L=180n
.dc VGS 0 1.8 0.01
.plot dc I(VDS)
.end
```



By sweeping vgs with constant small vds we obtain from the curve when we exit the cutoff region (vgs=vth) nearly at 4.3V

2- LAMBDA





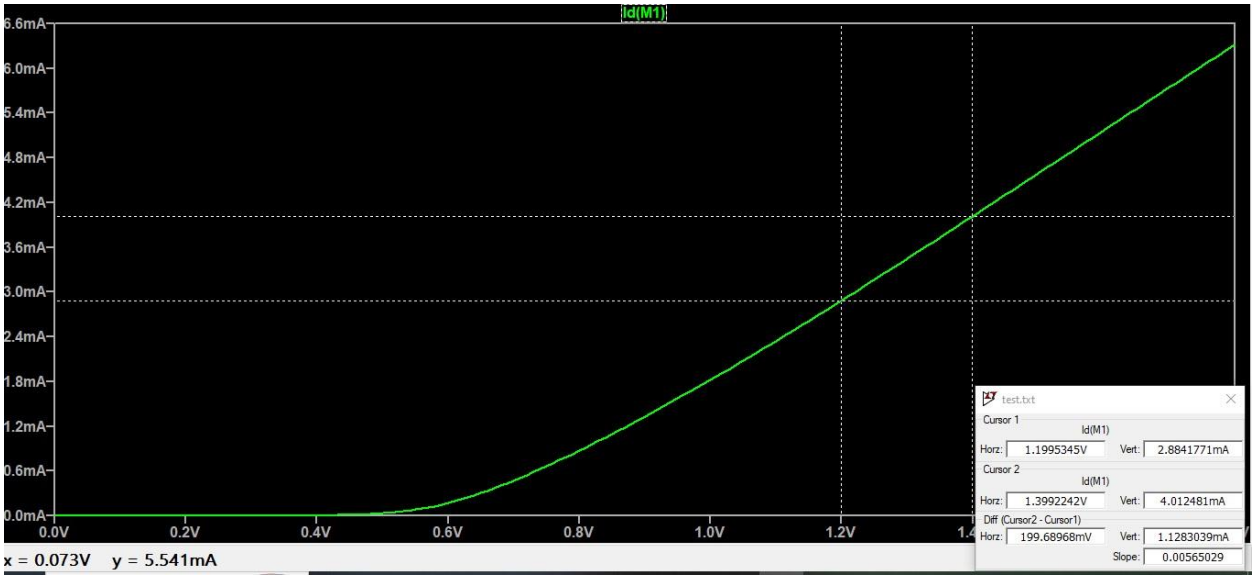
Id= 2.75 mA , Idsat =2.48mA nearly , Vds=1.2 V

Id = Idsat*(1+lambda*Vds)

Lambda= 0.08

3- <u>gm</u>

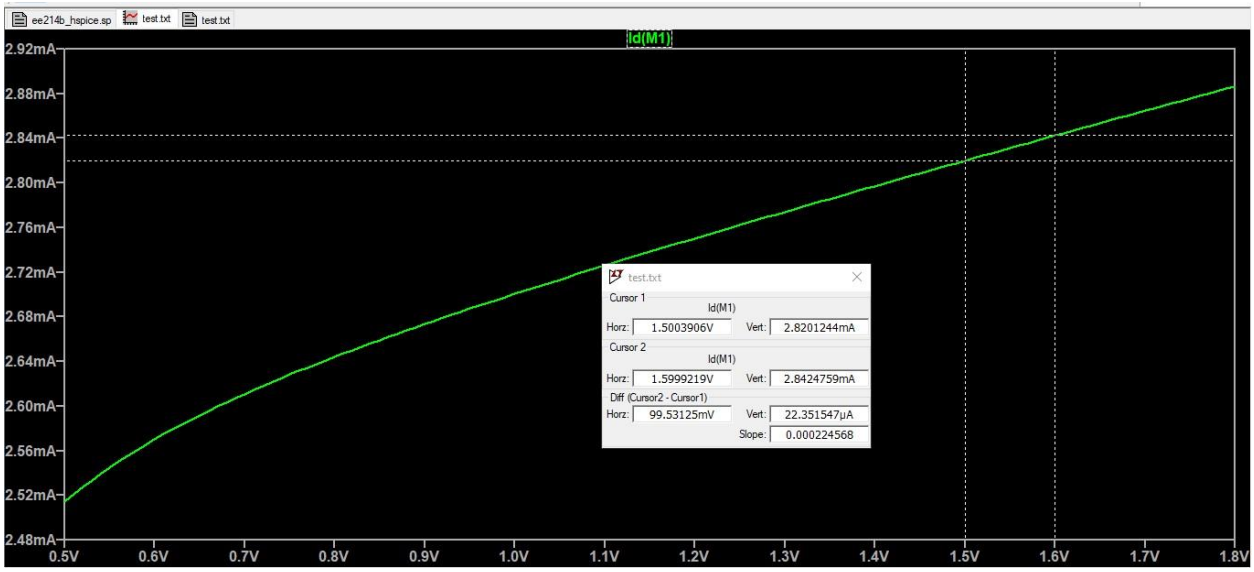
from Id vs VGS curve



gm = slope = $\frac{\partial Id}{\partial VGS}$ = $\frac{(4.012-2.884)mA}{1.4-1.2}$ = 5.64 mS

4- ro

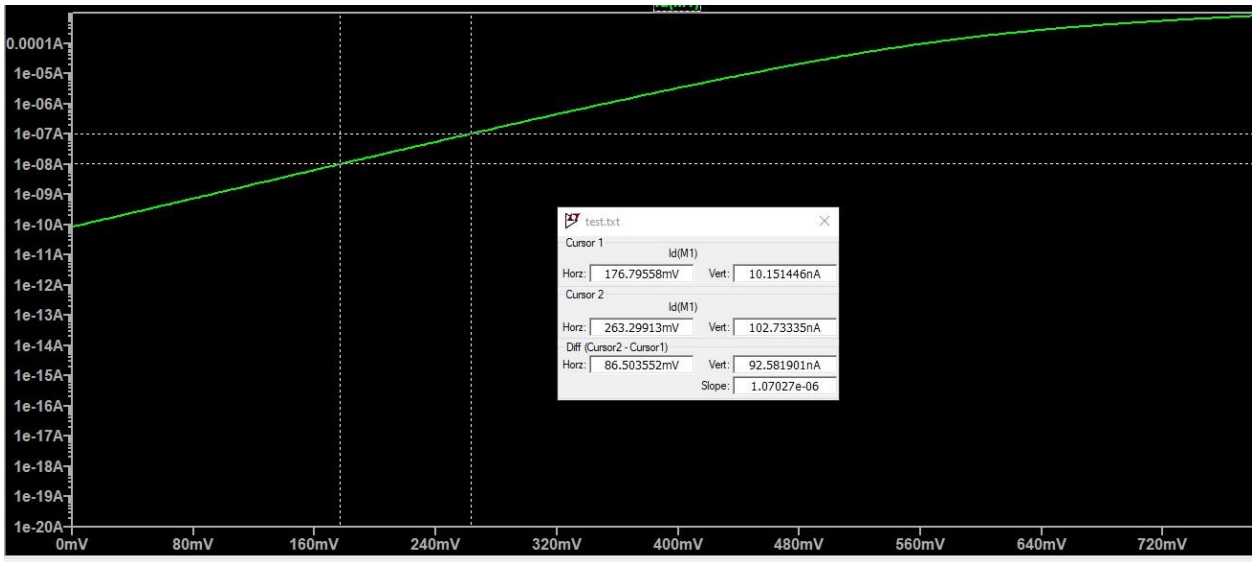
from Id vs VDS curve



1/ro = slope = $\frac{\partial Id}{\partial VDS} = \frac{(2.84-2.82)mA}{1.6-1.5}$ ro = 5 Kohm

5- Subthreshold Swing

From Id vs VGS log scale curve



SS = $\frac{\partial Vgs}{\partial log(ID)} = \frac{0.26329-0.17679}{1\ decade}$ *1000 = 86.5 mV/dec