وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog/Mixed-Signal Simulation and Modeling
Course Project
PLL Design and Verilog-A Behavioral Modeling

Objectives

1. Practice behavioral modeling using Verilog-A.
2. Appreciate the importance of top-down design methodology for a complex mixed-signal system.
3. Practice the top-down design methodology, e.g., using Cadence Virtuoso "Hierarchy Editor" tool.

Lab Instructions

1. Use a simulator that supports Verilog-A, e.g., Cadence spectre.
2. Follow the PLL design procedure described in the "pll_design.pdf" document available on the drive.
3. The only difference is that you will change VCO gain (kvco). To calculate your kvco, visit this random number generator website to get a random number between 50 and 400: https://www.calculator.net/random-number-generator.html?slower=50&supper=400&ctype=1&s=1922&submit1=Generate
4. Use kvco = your_random_num / 100 * 1e9 Hz/V

Deliverables

Index	Deliverable	Points
1.	Your Verilog-A model for the PFD.	1
2.	Make a simple testbench to test the PFD. Deliver a snapshot clearly illustrating the PFD operation (similar to Fig. 6.13 and Fig. 6.14).	1
3.	Your Verilog-A model for the CHP.	1
4.	Make a simple testbench to test the CHP. Deliver a snapshot clearly illustrating the CHP operation (similar to Fig. 6.18).	1
5.	Your Verilog-A model for the VCO.	1
6.	Make a simple testbench to test the VCO. Deliver a snapshot clearly illustrating the VCO operation (similar to Fig. 6.11, but a single tuning curve is enough, i.e., no corner sim required). **Add a marker to show the tuning voltage corresponding to the required output frequency.**	1
7.	Your Verilog-A model for the divider.	1
8.	Make a simple testbench to test the divider. Deliver a snapshot clearly illustrating the divider operation (similar to Fig. 6.20).	1
9.	Design the divider at the transistor level. Deliver a snapshot clearly illustrating the transistor level schematic of the DFF that you used in the design.	1
10.	Using the same previous divider testbench, test your transistor level divider. Deliver a snapshot clearly illustrating the divider operation (similar to Fig. 6.20).	1
11.	Integrate the PLL as shown in Fig. 6.2 using Verilog-A models only. Simulate the PLL **using config view and hierarchy editor**. Deliver a snapshot clearly illustrating the VCO control voltage (similar to Fig. 6.7). Add a cursor to show the value of the control voltage after lock.	1

12.	Given kvco, analytically calculate the control voltage at which the PLL should achieve lock.	1
13.	Compare the control voltage simulated value with the analytically calculated value. Comment.	1
14.	Integrate the PLL as shown in Fig. 6.2 using Verilog-A models only. Simulate the PLL **using config view and hierarchy editor**. Deliver a snapshot clearly illustrating the PLL operation (similar to Fig. 6.8). **Add "A/B marker" to indicate the reference and output frequencies.**	1
15.	Deliver a snapshot of the log file of the previous simulation clearly illustrating the success of the simulation and the simulation time.	1
16.	Replace the Verilog-A view of the divider with the schematic (transistor level) view. Deliver a snapshot of the new configuration in hierarchy editor.	1
17.	Integrate the PLL as shown in Fig. 6.2 using Verilog-A models of all blocks except the divider. Use the schematic view of the divider. Simulate the PLL **using config view and hierarchy editor**. Deliver a snapshot clearly illustrating the VCO control voltage (similar to Fig. 6.23).	1
18.	Integrate the PLL as shown in Fig. 6.2 using Verilog-A models of all blocks except the divider. Use the schematic view of the divider. Simulate the PLL **using config view and hierarchy editor**. Deliver a snapshot clearly illustrating the PLL operation (similar to Fig. 6.24). **Add "A/B marker" to indicate the reference and output frequencies.**	1
19.	Deliver a snapshot of the log file of the previous simulation clearly illustrating the success of the simulation and the simulation time.	1
20.	Compare the simulation time of (13) and (17). Comment.	1

Thanks to all who contributed to these labs. If you find any errors or have suggestions concerning these labs, please contact Hesham.omran@eng.asu.edu.eg.