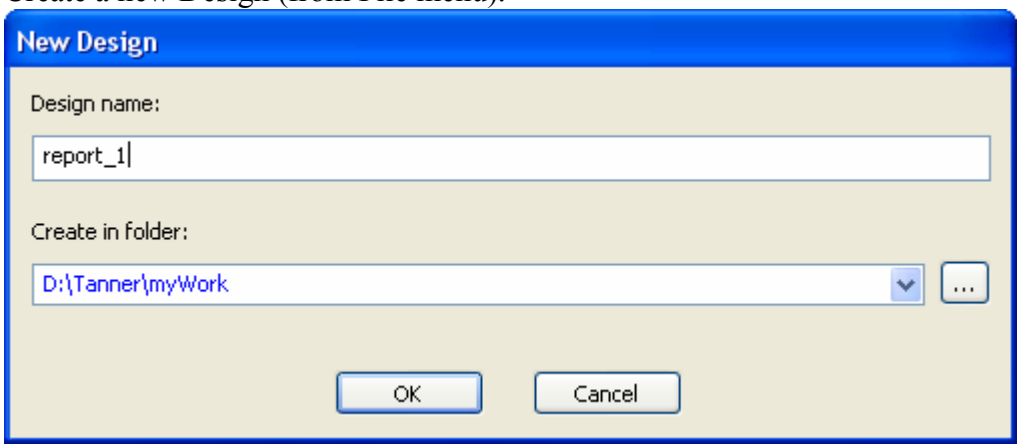
بسم الله الرحمن الرحيم والحمد لله رب العالمين والصلاة والسلام على خاتم النبيين سيدنا محمد وعلى آله وصحبه أجمعين

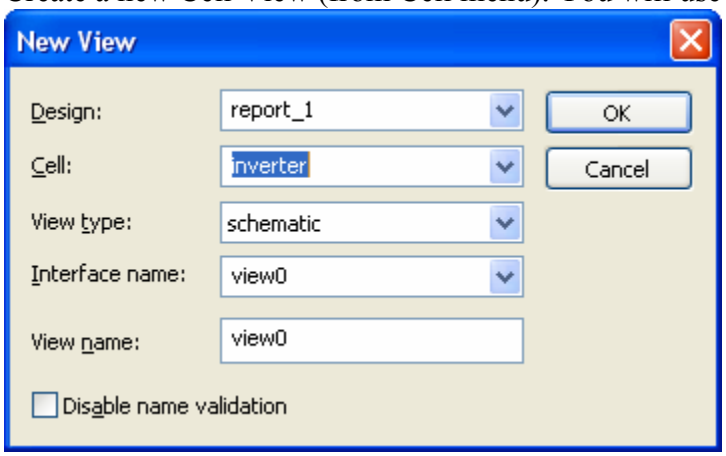
Report (1)
Report Guide

Static Behavior

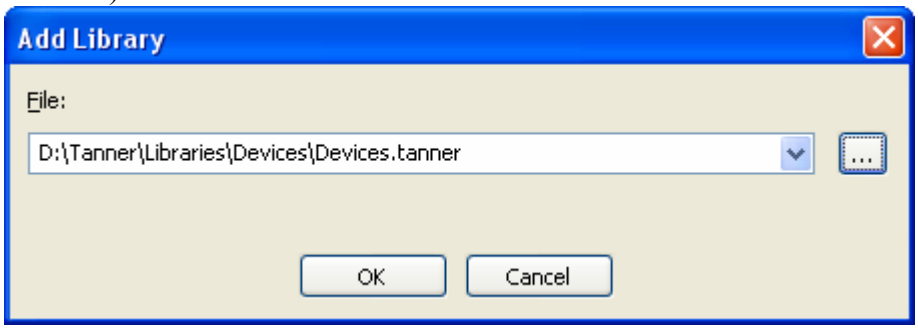
Create a new Design (from File menu).

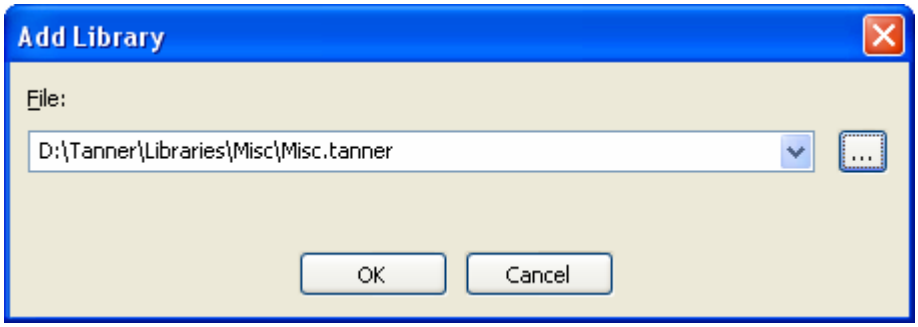


Create a new Cell View (from Cell menu). You will use it to draw your schematic.

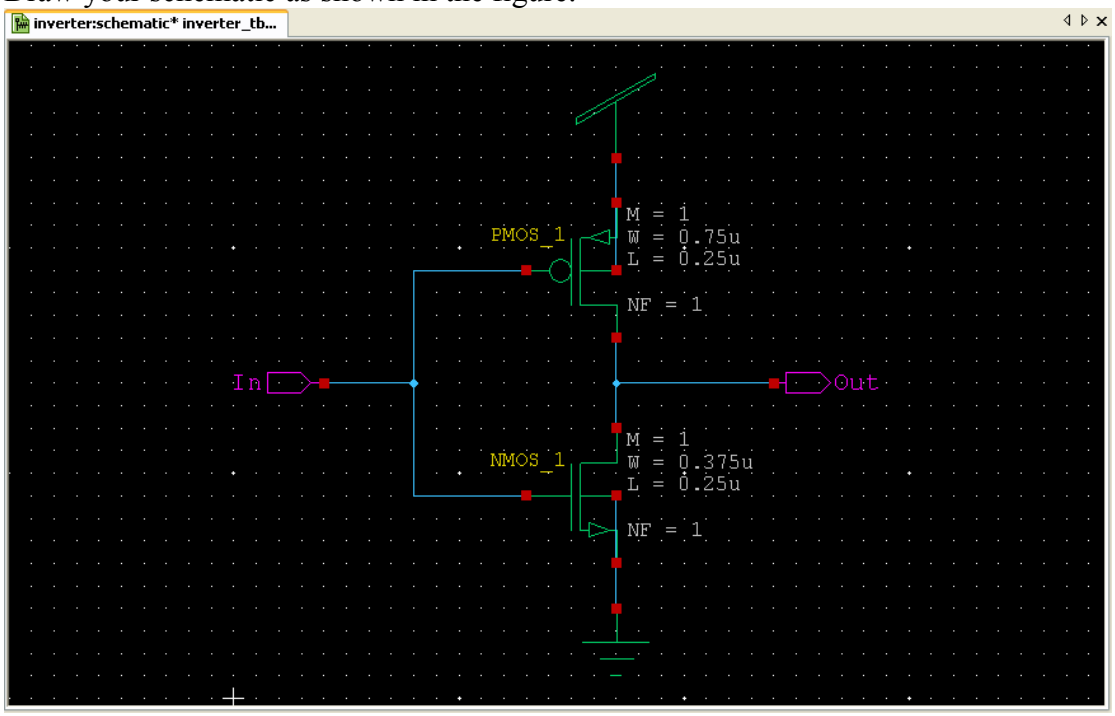


Add libraries to your design (the path is where you downloaded examples and tutorials).

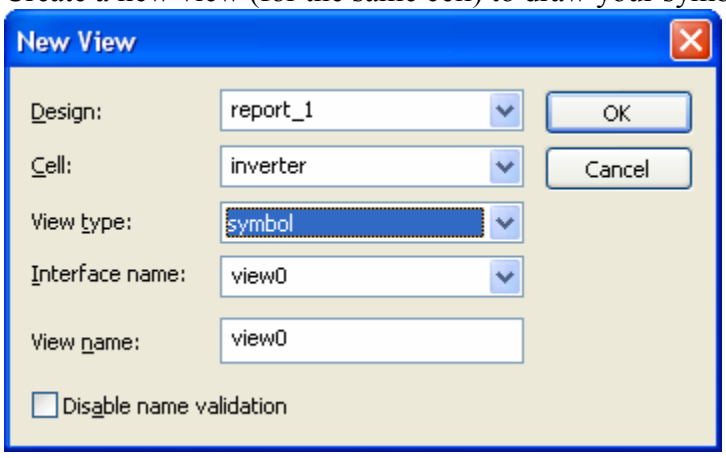




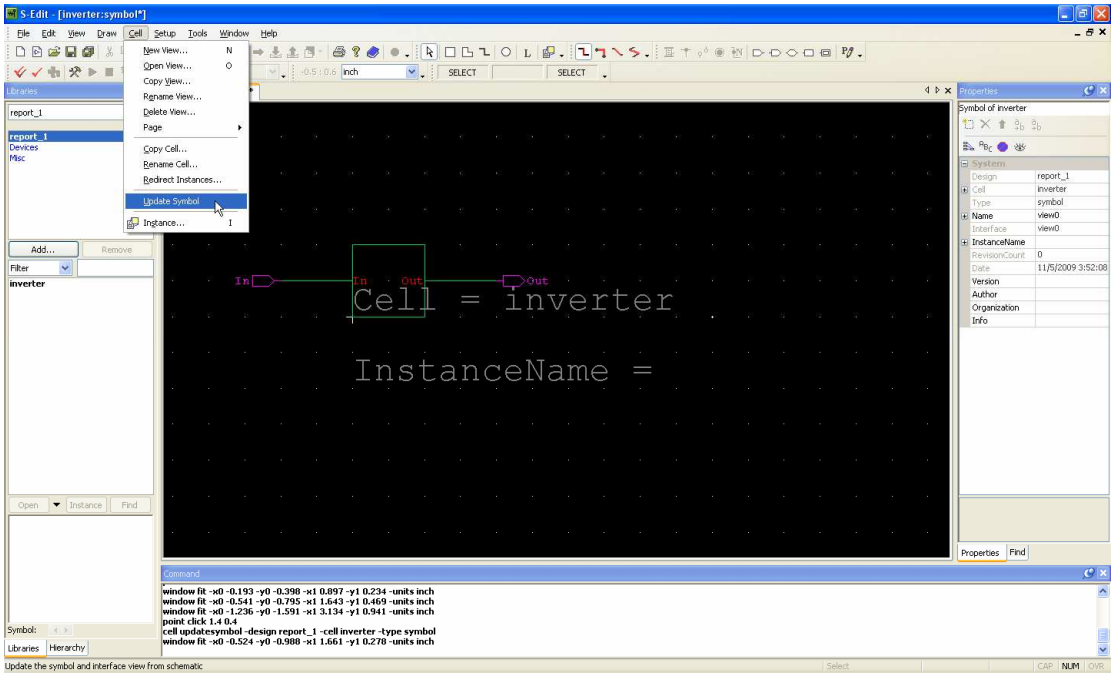
Draw your schematic as shown in the figure.



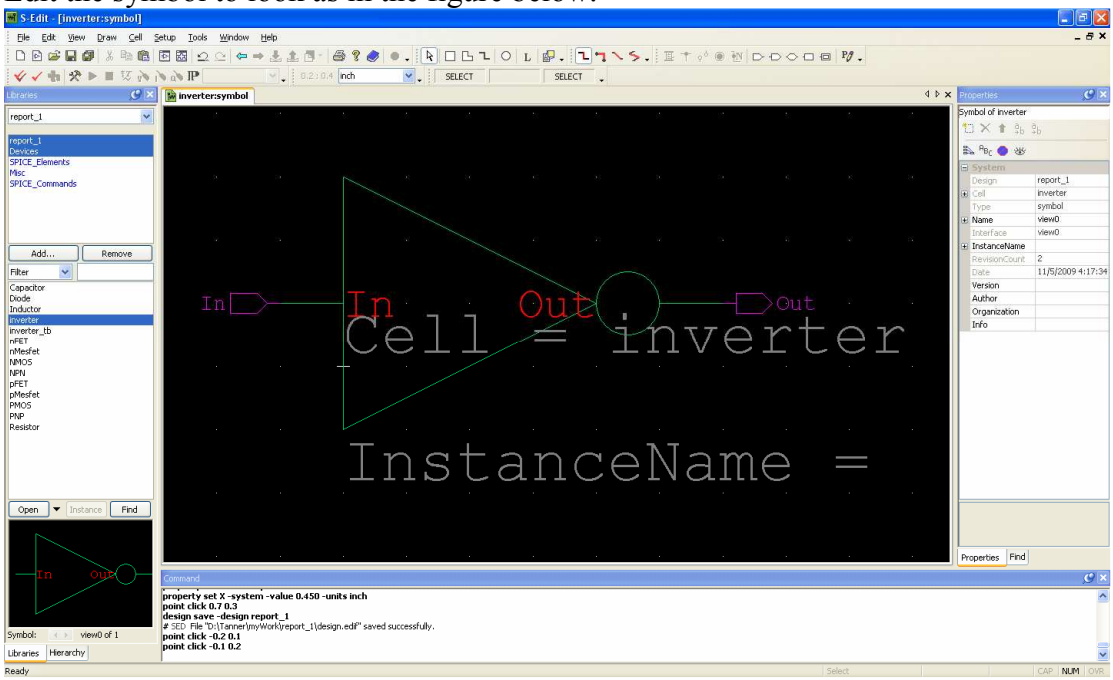
Create a new view (for the same cell) to draw your symbol.



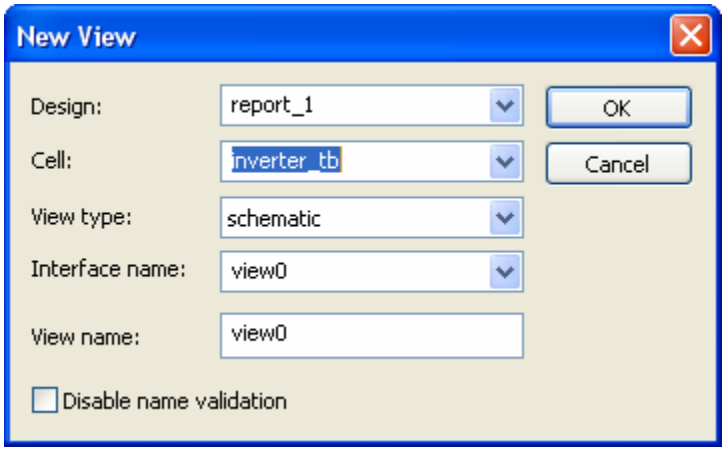
In the symbol view window choose Cell > Update Symbol. An automatic symbol will be created.



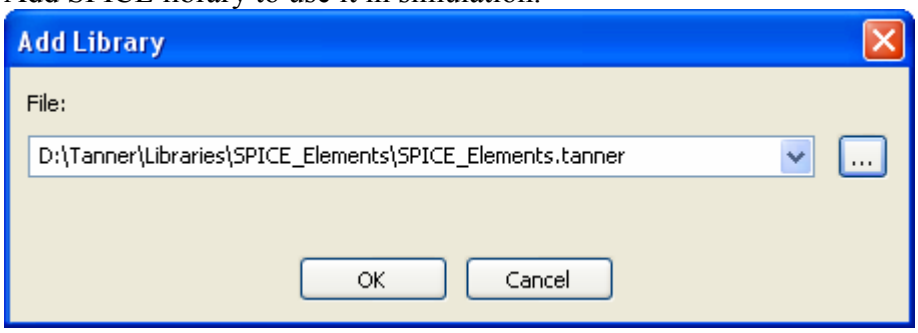
Edit the symbol to look as in the figure below.



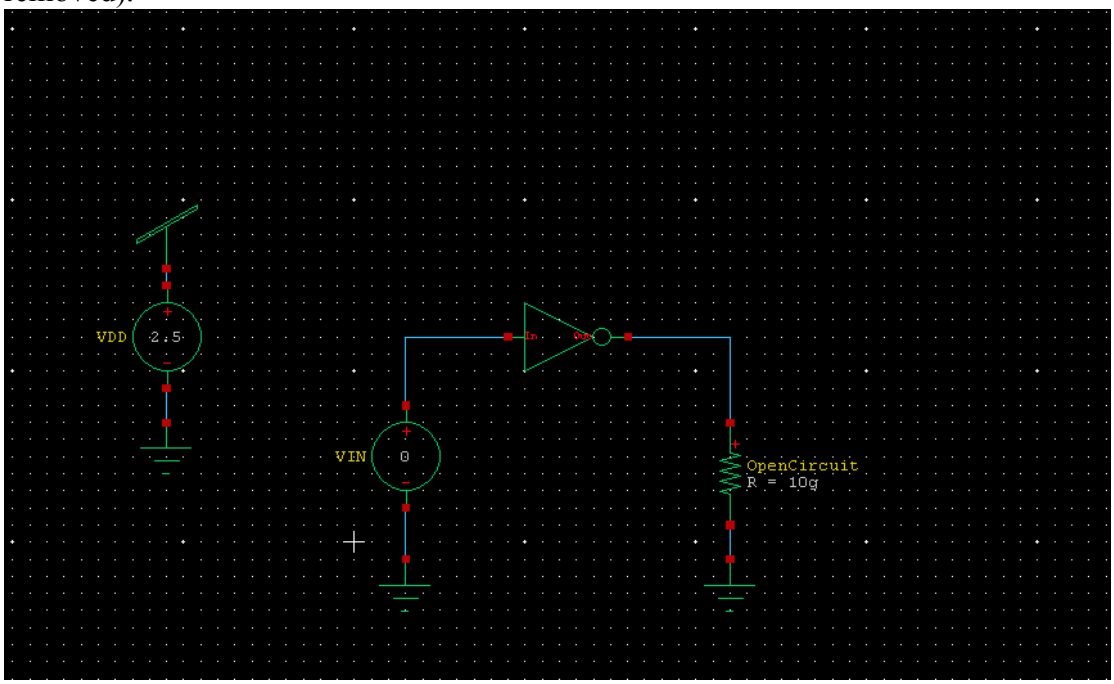
Next, we will create a test bench to test our inverter. Create a new Cell.



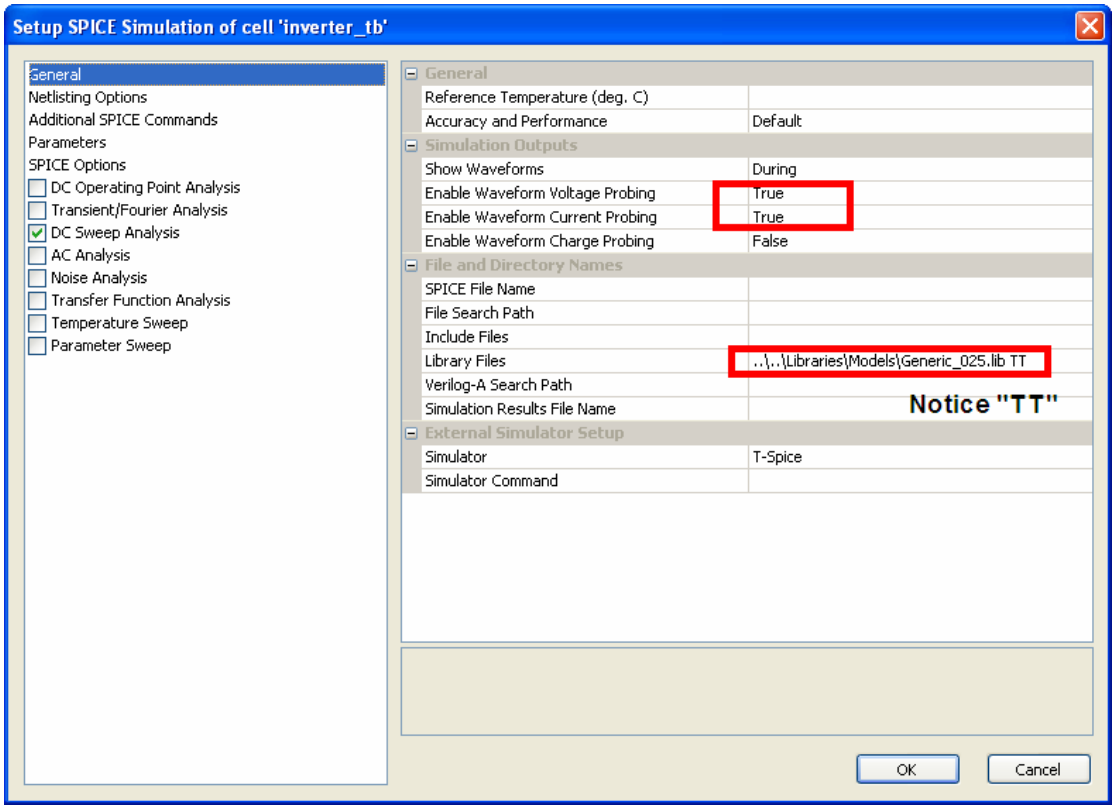
Add SPICE library to use it in simulation.

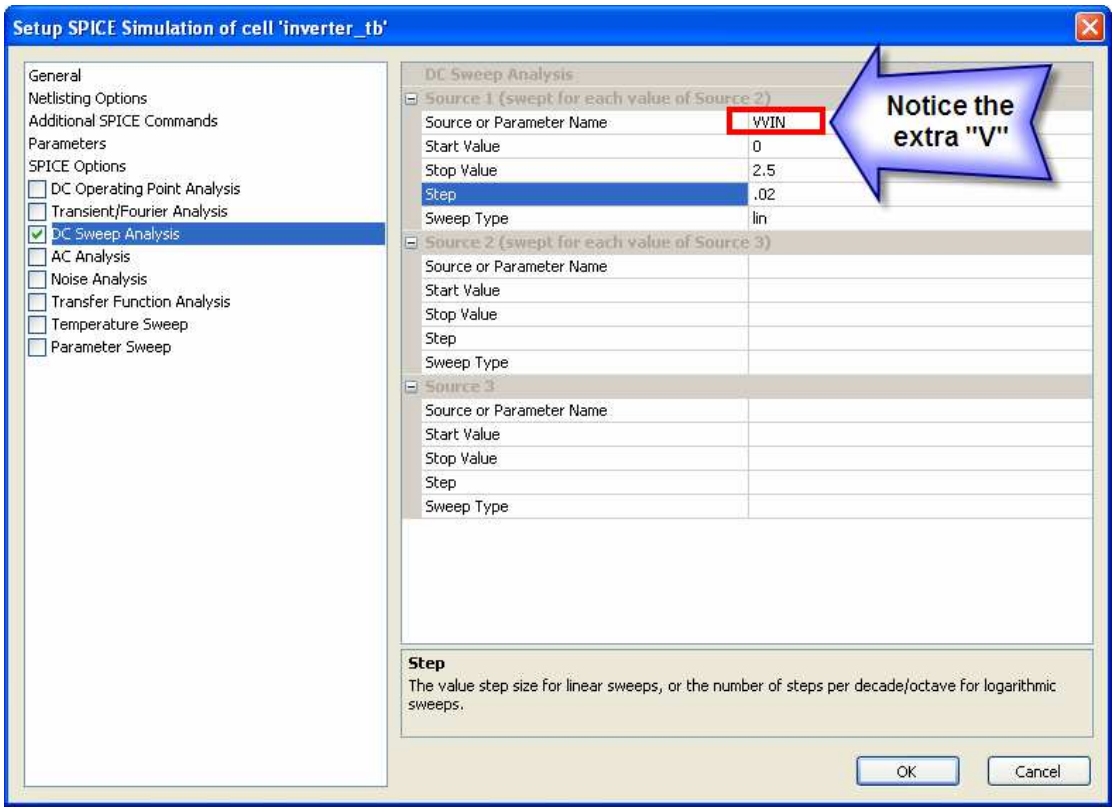


Create two DC sources and connect your circuit as shown (the resistance may be removed).



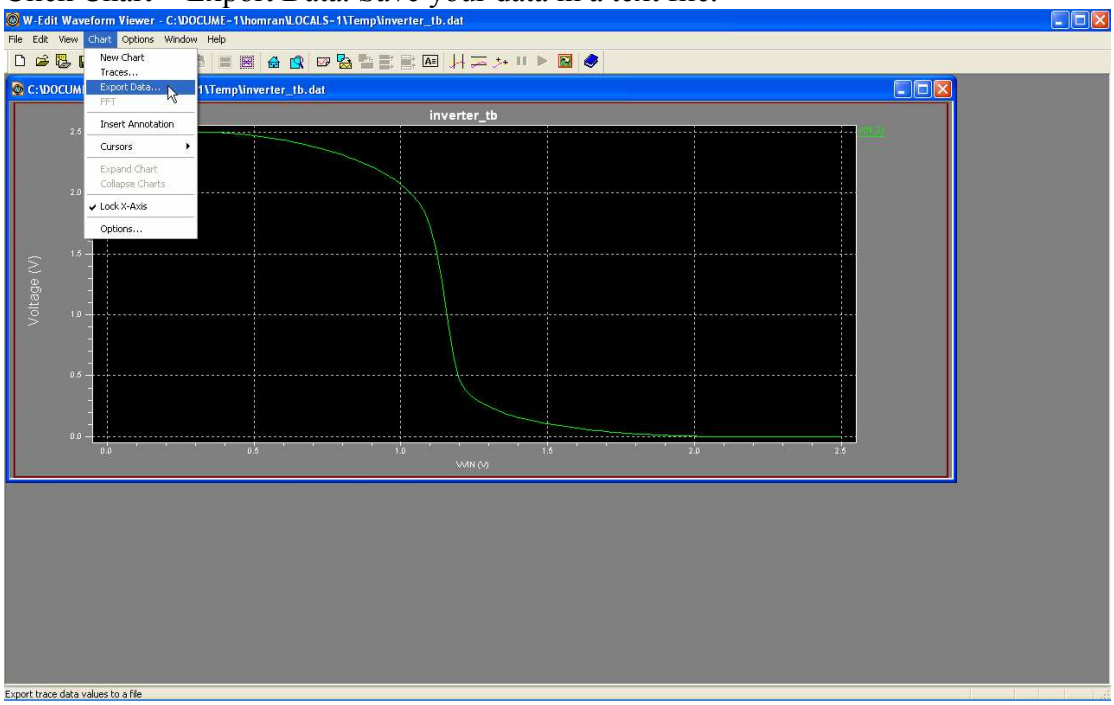
Now we want to adjust our simulation settings. Click Setup > SPICE Simulation. Adjust the setting as shown below.



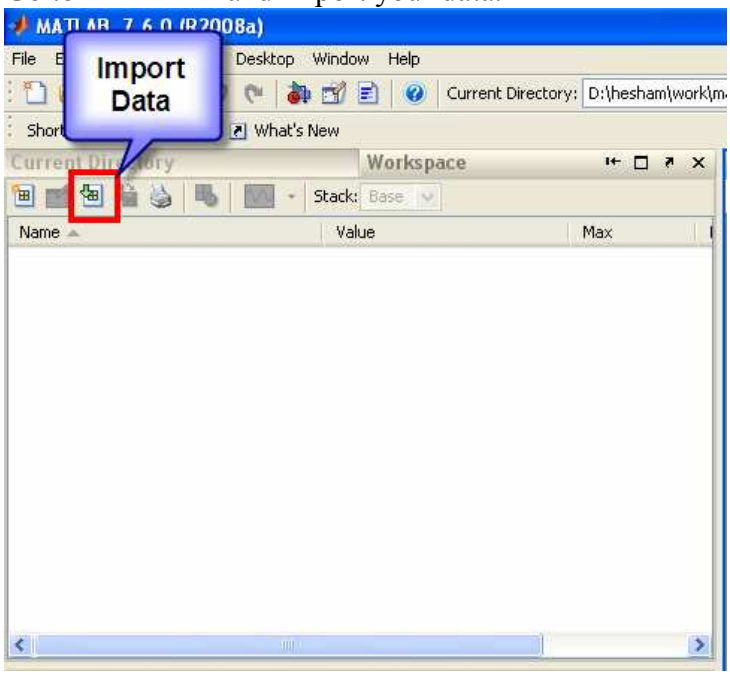


Click Tools > Start Simulation. T-Spice will automatically load, press Unblock if a warning is displayed. Return to the schematic and use the voltage probe at the output node. The VTC is automatically loaded in W-Edit.

W-Edit is a very poor wave analysis tool. It is not enough for us (e.g., we cannot use it to draw the gain). Thus we need to export our data to MATLAB to analyze it!!
Click Chart > Export Data. Save your data in a text file.



Go to MATLAB and import your data.



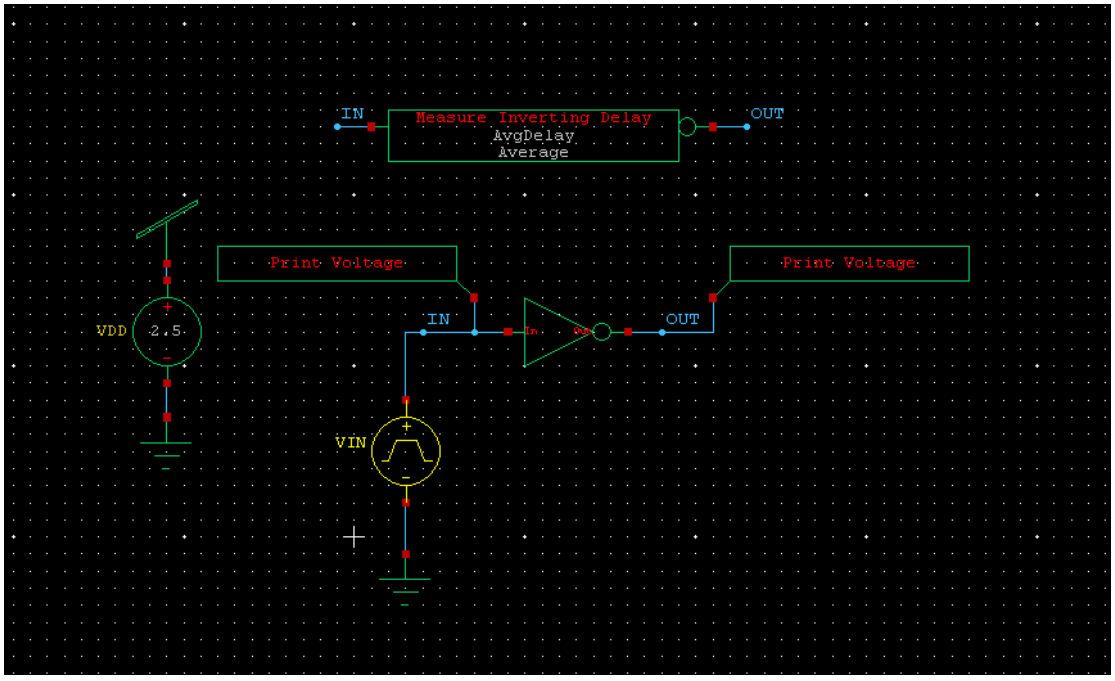
Here is a simple code to plot VTC and gain (you must make further manipulation in the figure).

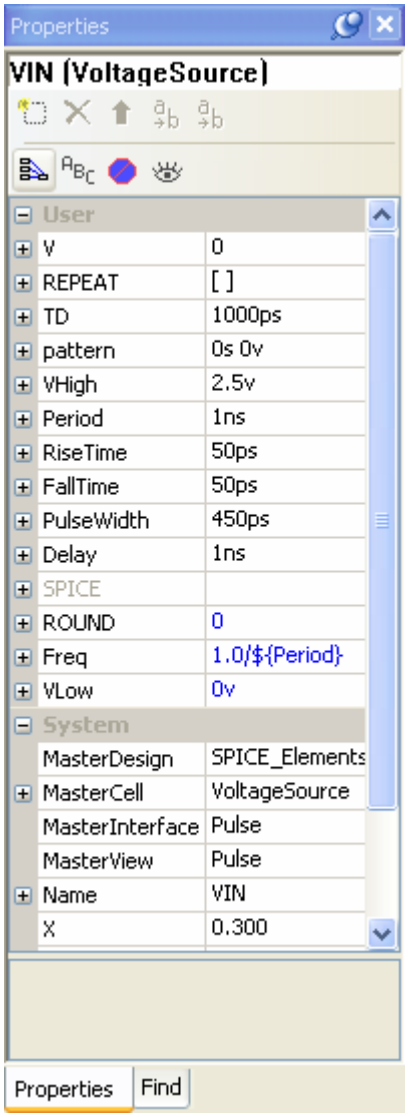
```
x = data(:,1);
y = data(:,2);
dy = diff(y)./diff(x);

subplot(211)
plot(x,y)
subplot(212)
plot(x(1:length(dy)),dy)
```

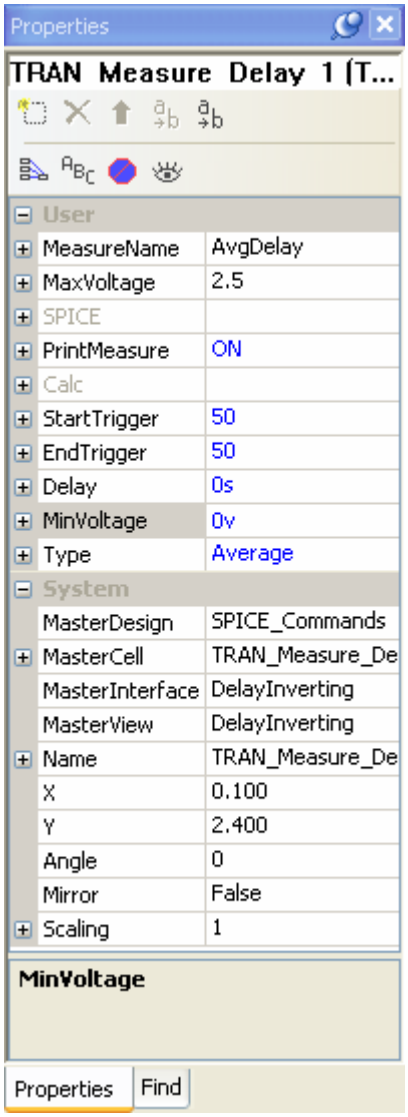
Complete your code.

Dynamic Behavior

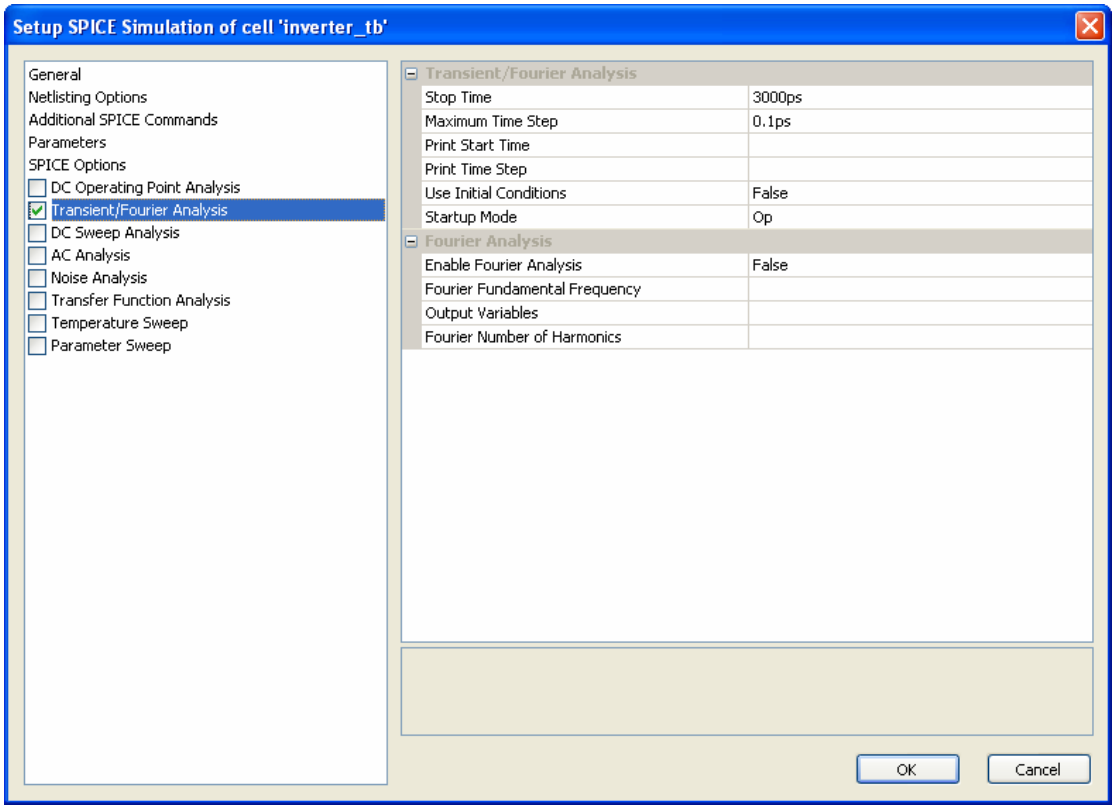
To analyze dynamic behavior change VIN to PULSE and add SPICE commands as shown.



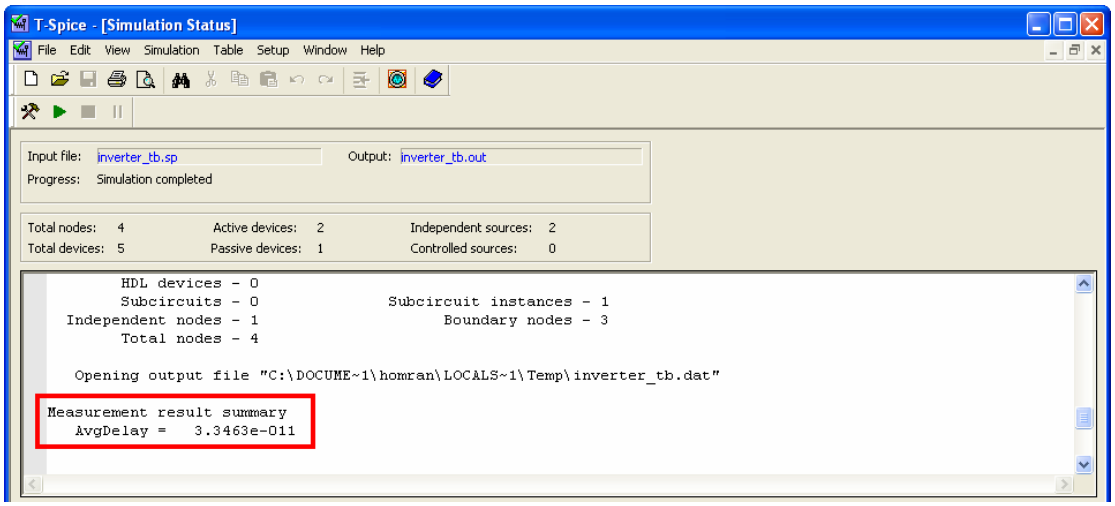

Properties
VIN (VoltageSource)
User
V 0
REPEAT [ ]
TD 1000ps
pattern 0s 0v
VHigh 2.5v
Period 1ns
RiseTime 50ps
FallTime 50ps
PulseWidth 450ps
Delay 1ns
SPICE
ROUND 0
Freq 1.0/${Period}
VLow 0v
System
MasterDesign SPICE_Elements
MasterCell VoltageSource
MasterInterface Pulse
MasterView Pulse
Name VIN
X 0.300
Properties
Find



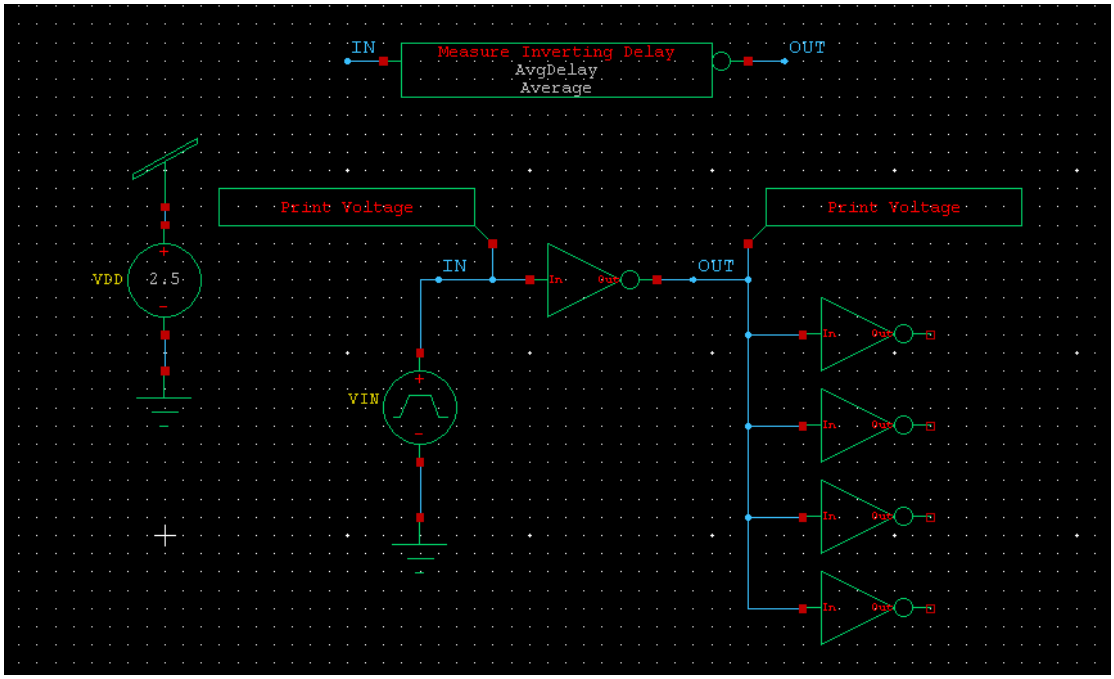
Change the simulation settings.



In T-SPICE u will find the result of your measurement. Measure it using W-Edit as well.

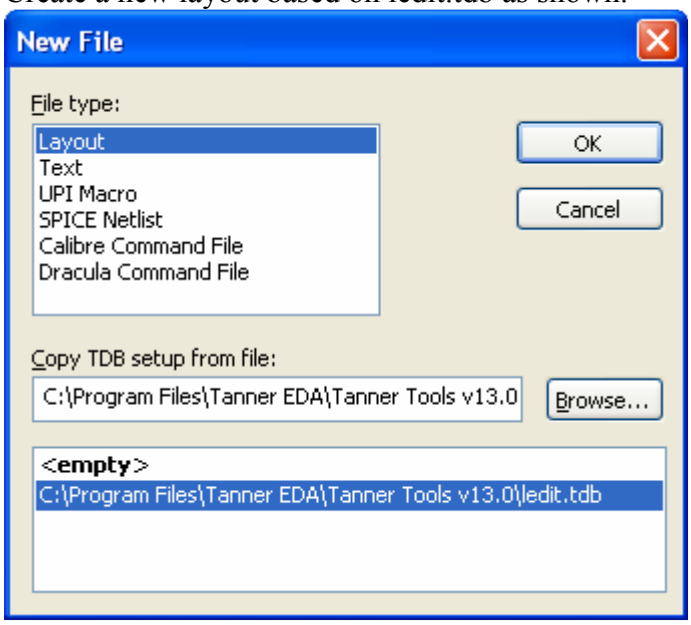


Create a new schematic view and repeat for FO4.

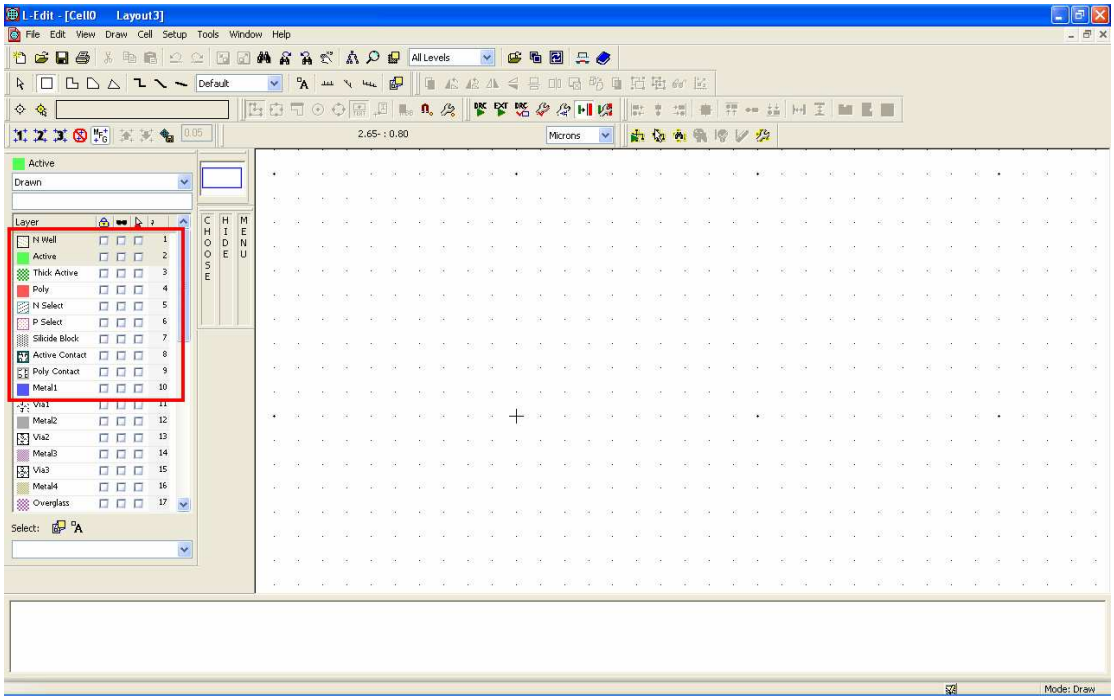


Layout

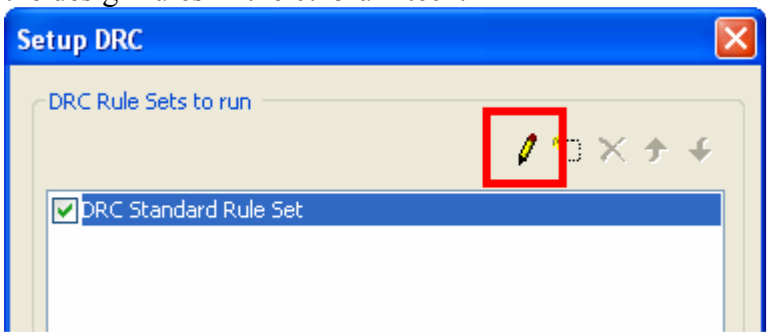
Create a new layout based on ledit.tdb as shown.



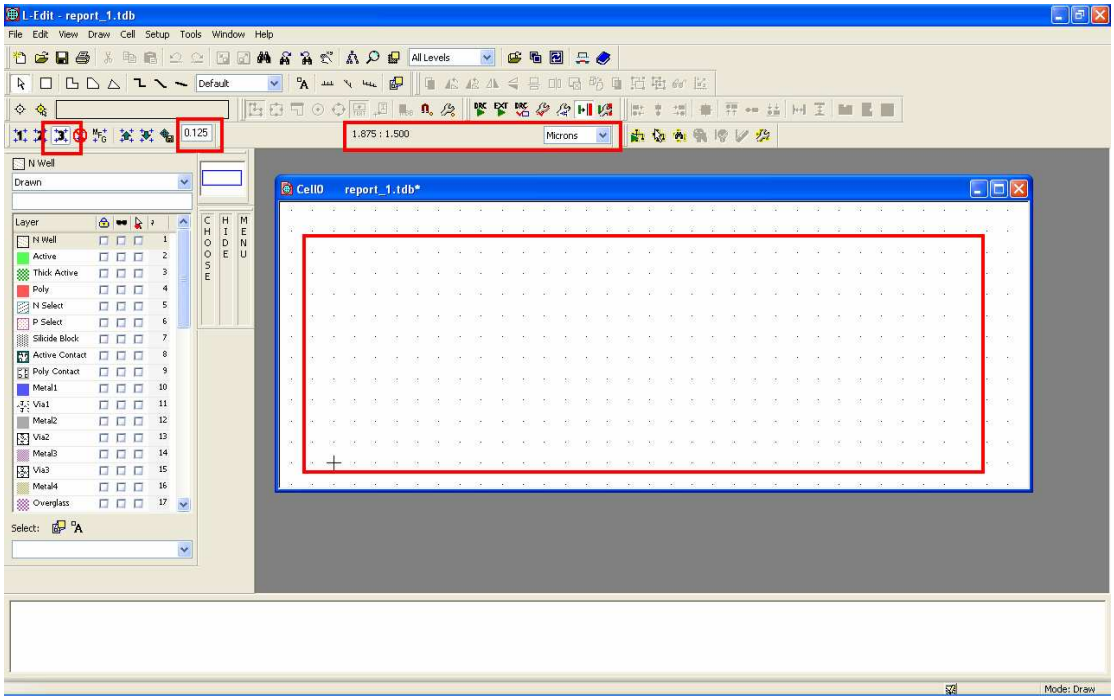
A new cell is created by default. We will draw the inverter in this cell.
Click Cell > Rename and call it inverter.
Zoom till you see the grid. The layers we will use are shown.

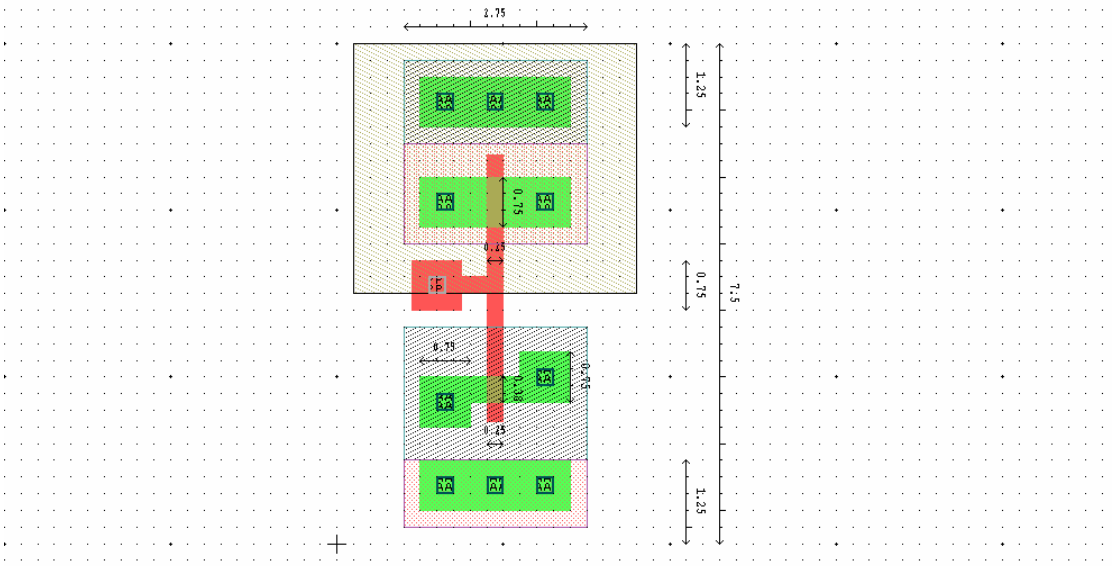


To see the Design Rules: Go to Tools > DRC Setup. Edit the DRC rules. These are all the design rules in the 0.25 um tech.

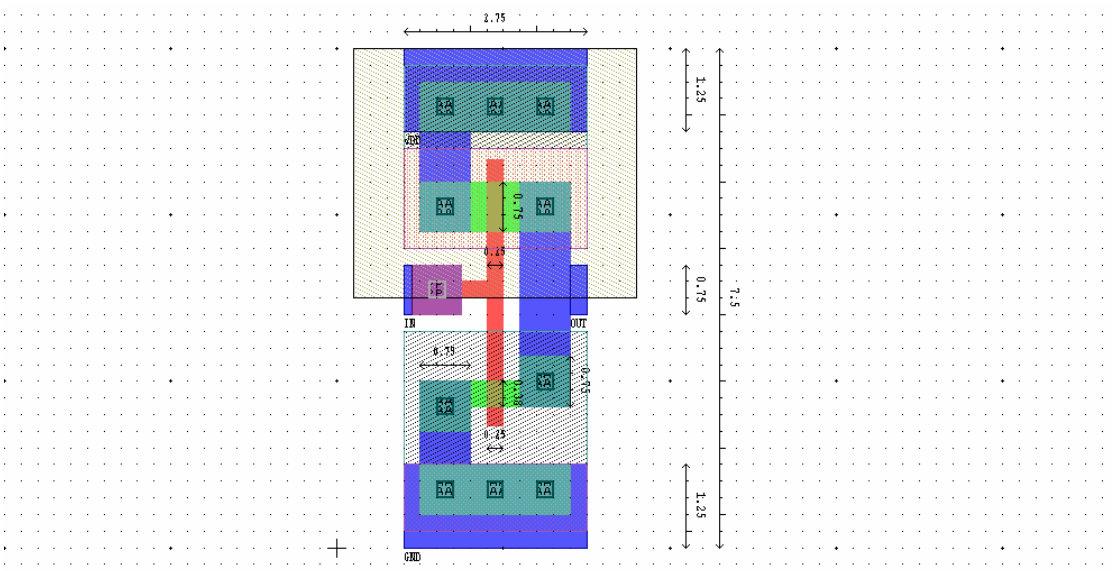


Modify the grid to 0.025 and 0.125 to be more suitable for drawing. Draw a compact layout for the inverter as shown.

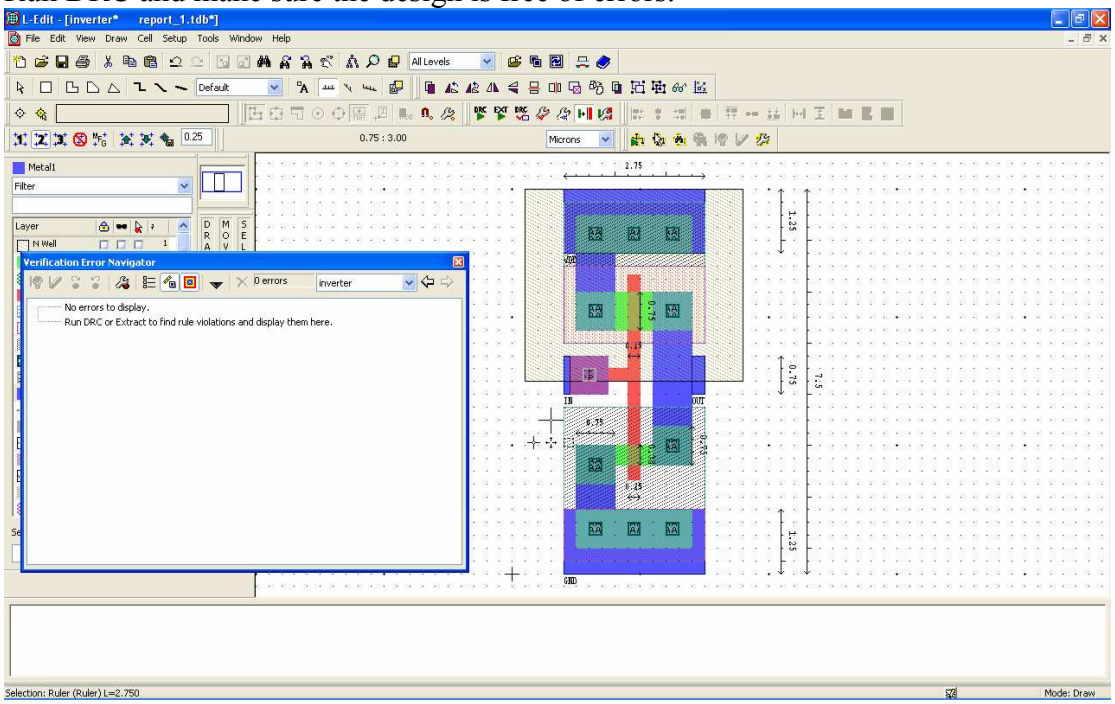




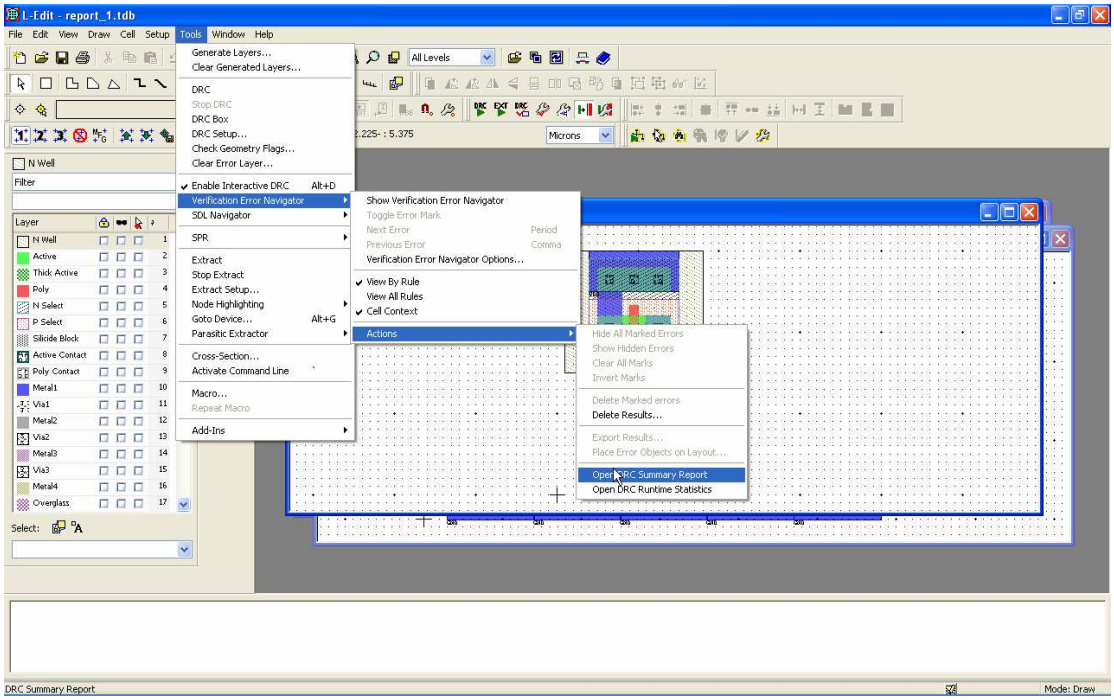
Complete the layout for the inverter as shown (some dimensions are shown as a guide).



Run DRC and make sure the design is free of errors.

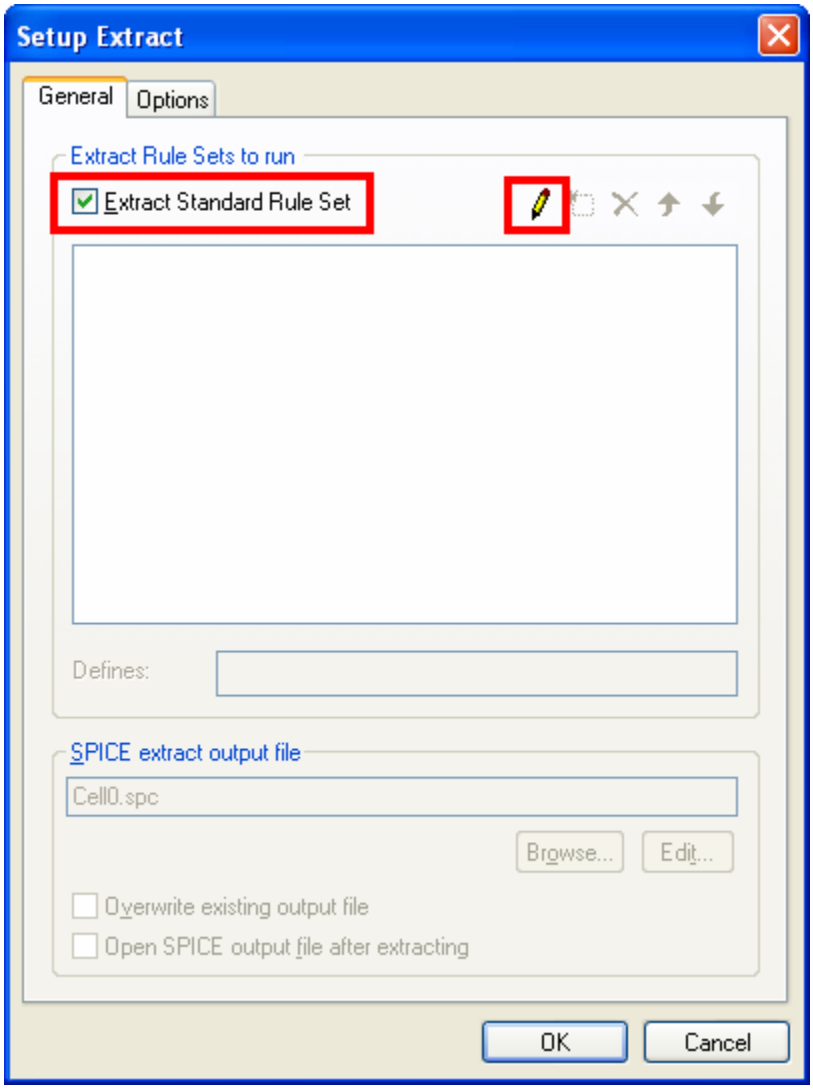


To display DRC summary report.

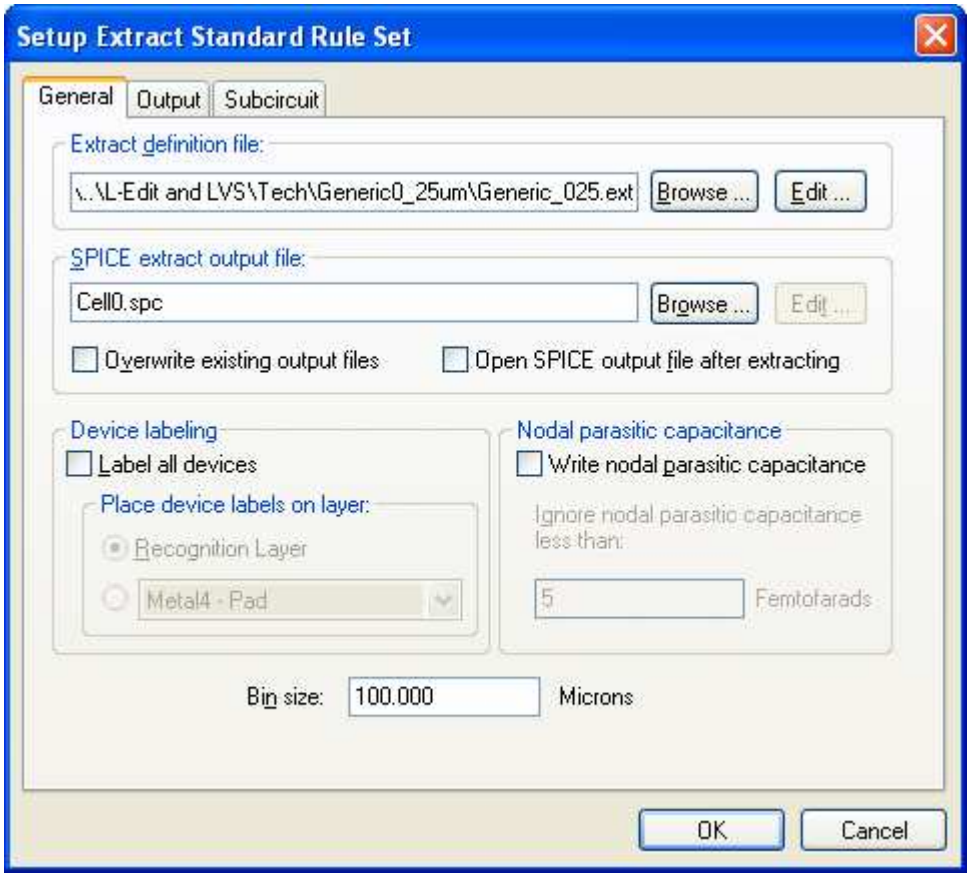


LVS

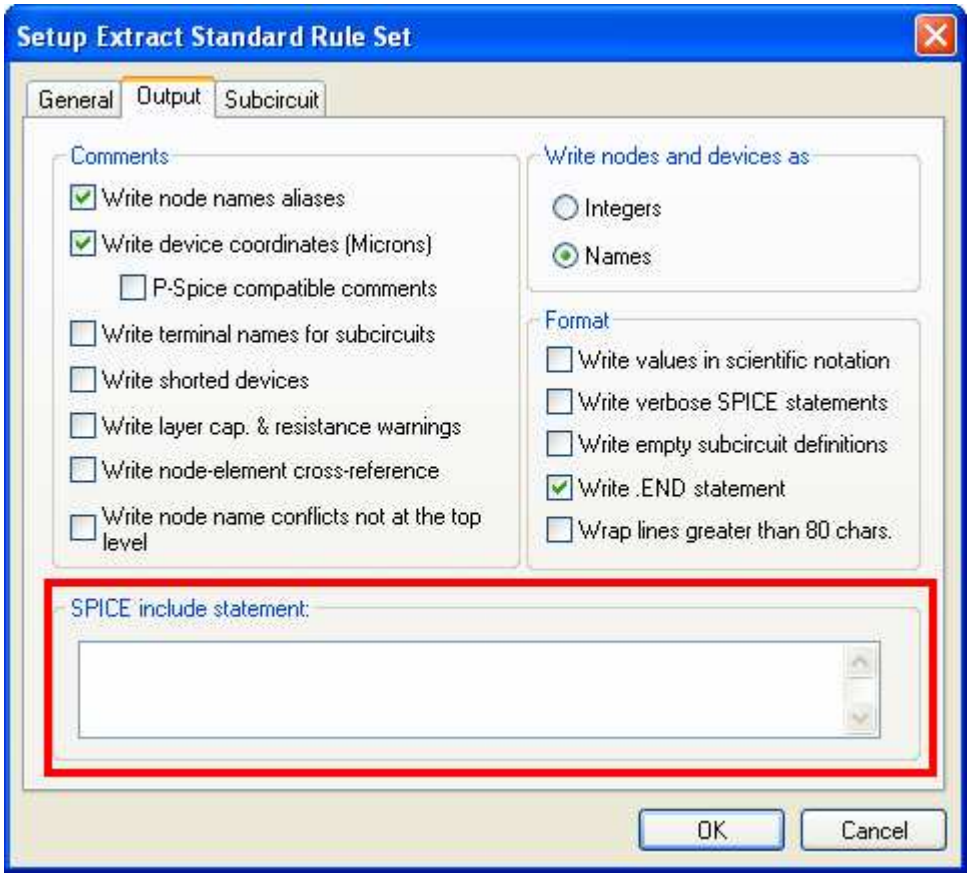
Start by generating a netlist for the inverter layout.
In L-Edit go to Tools > Extract Setup….
Select Standard Rule Set. Edit it to select the path of the extraction file.



Select the file Generic_025.ext.

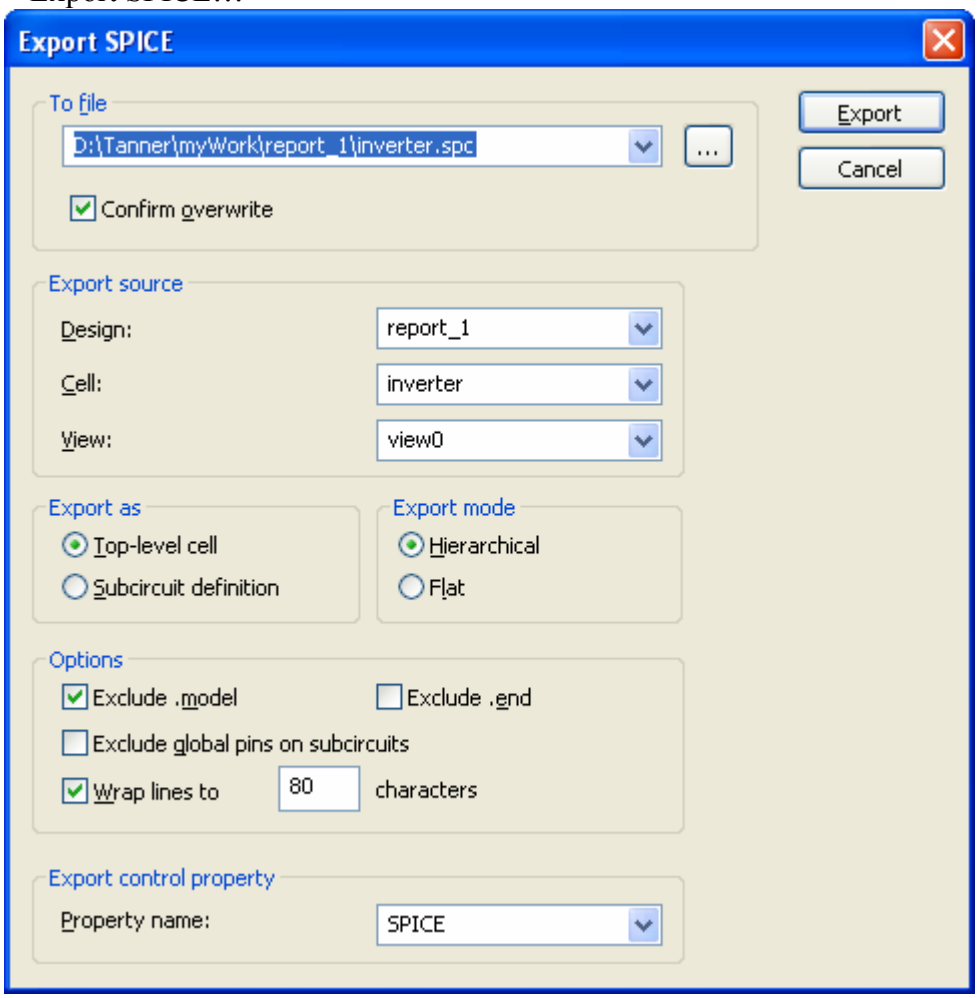


Remove the include statements.

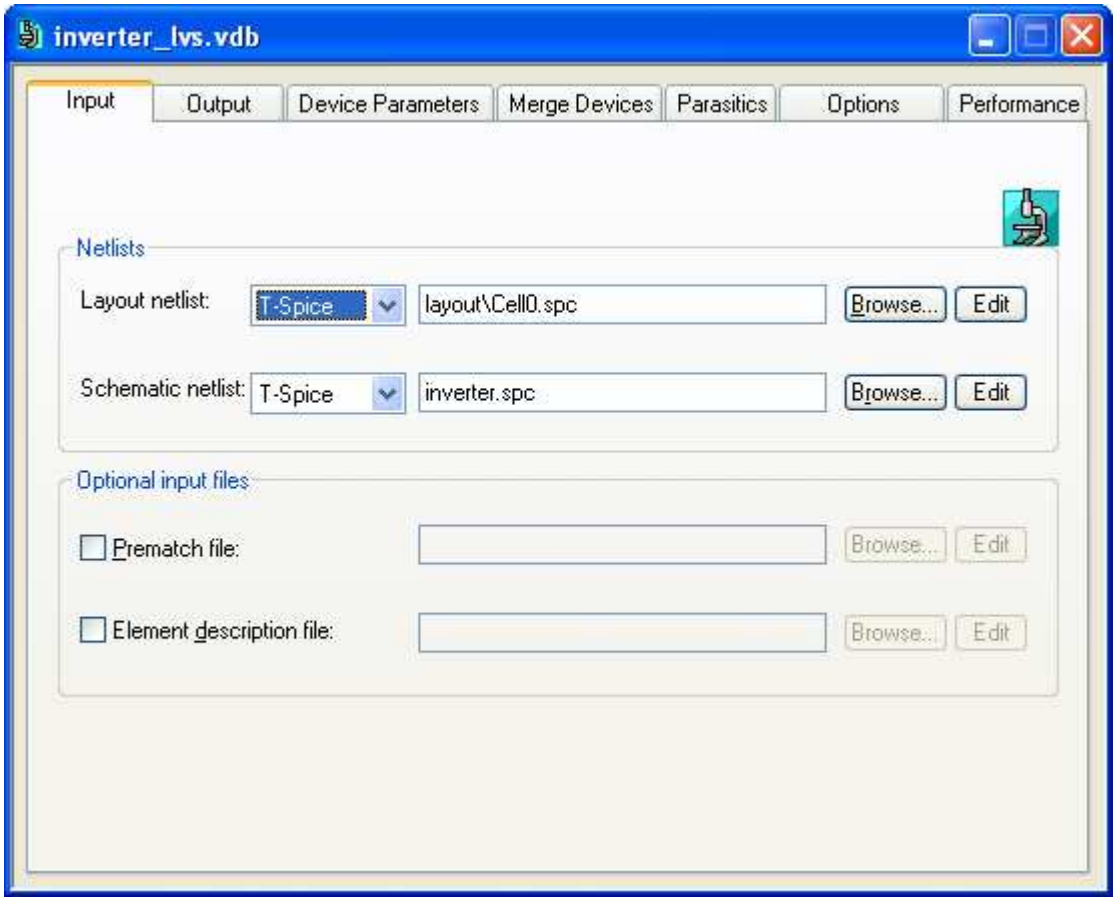


Run Tools > Extract to start extraction.

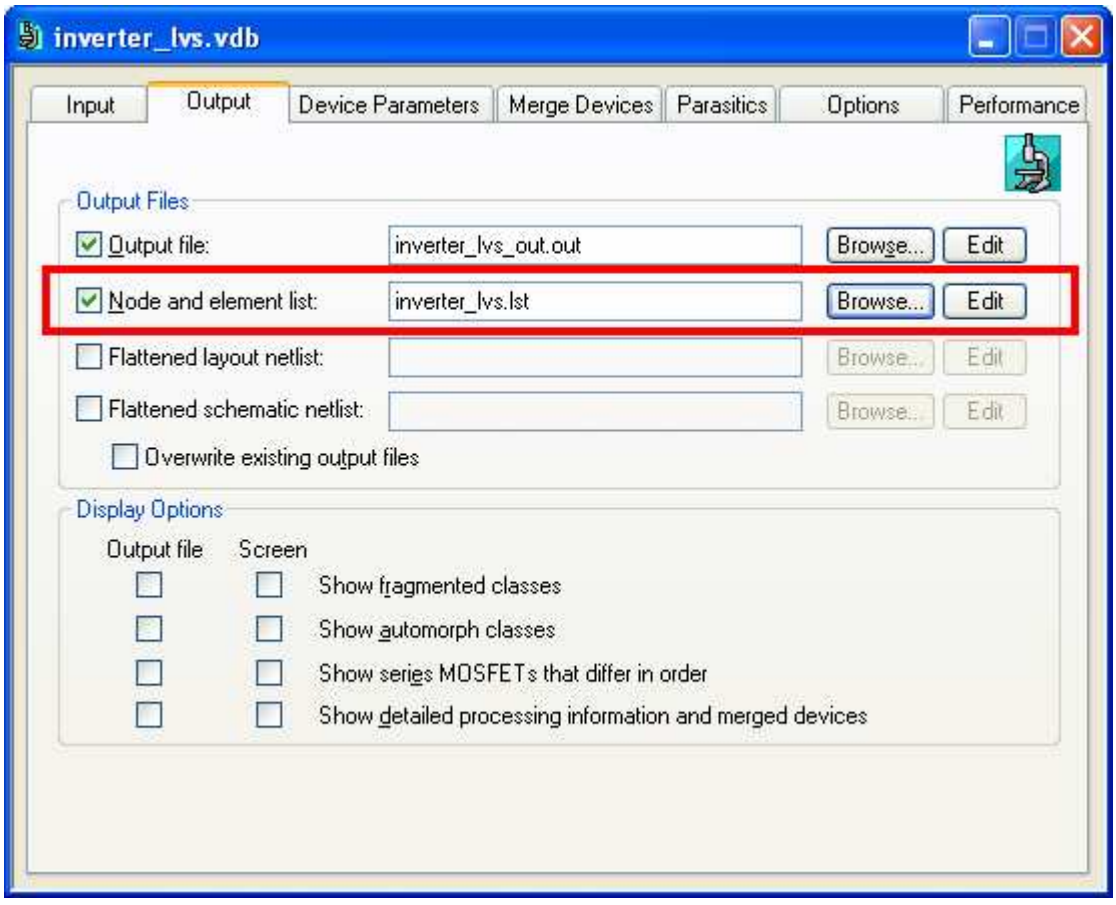
In S-Edit we want to generate a netlist for the inverter schematic. Select File > Export > Export SPICE…



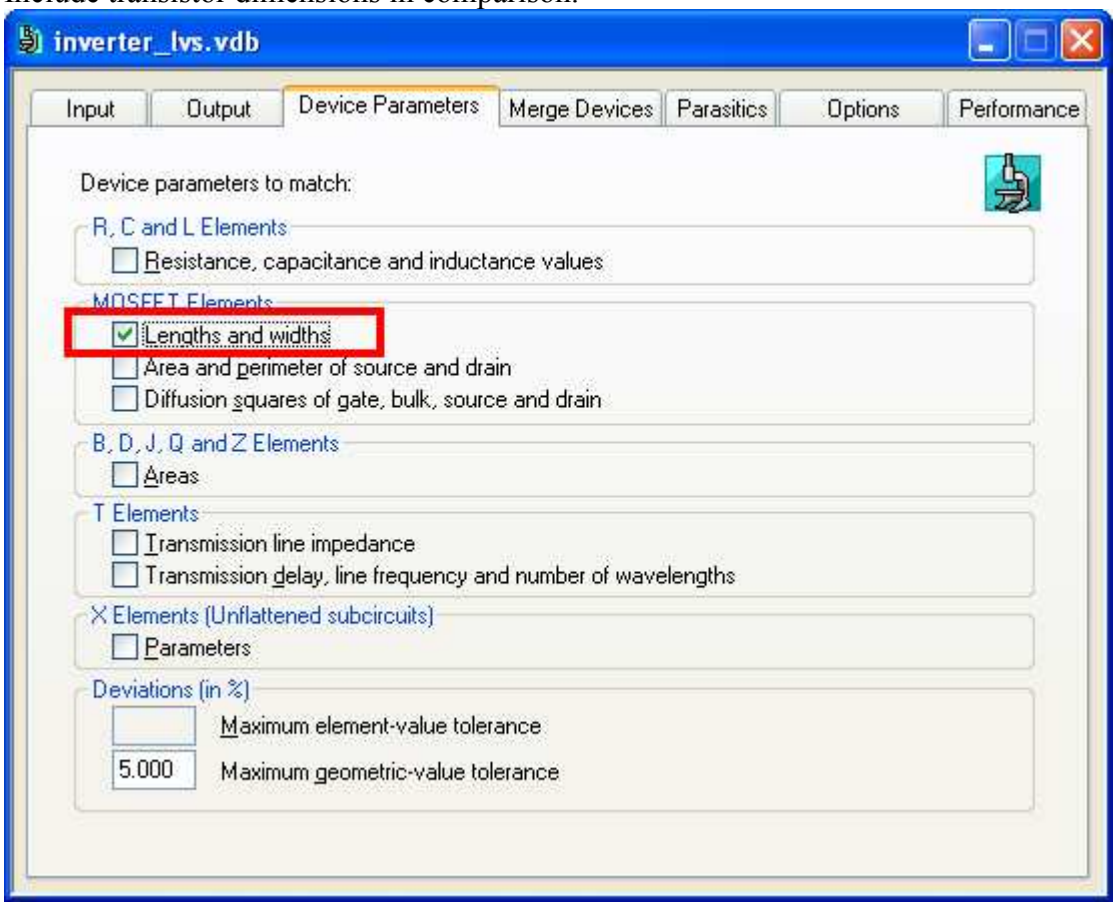
Now open LVS to start the comparison. Select the schematic and layout netlists.



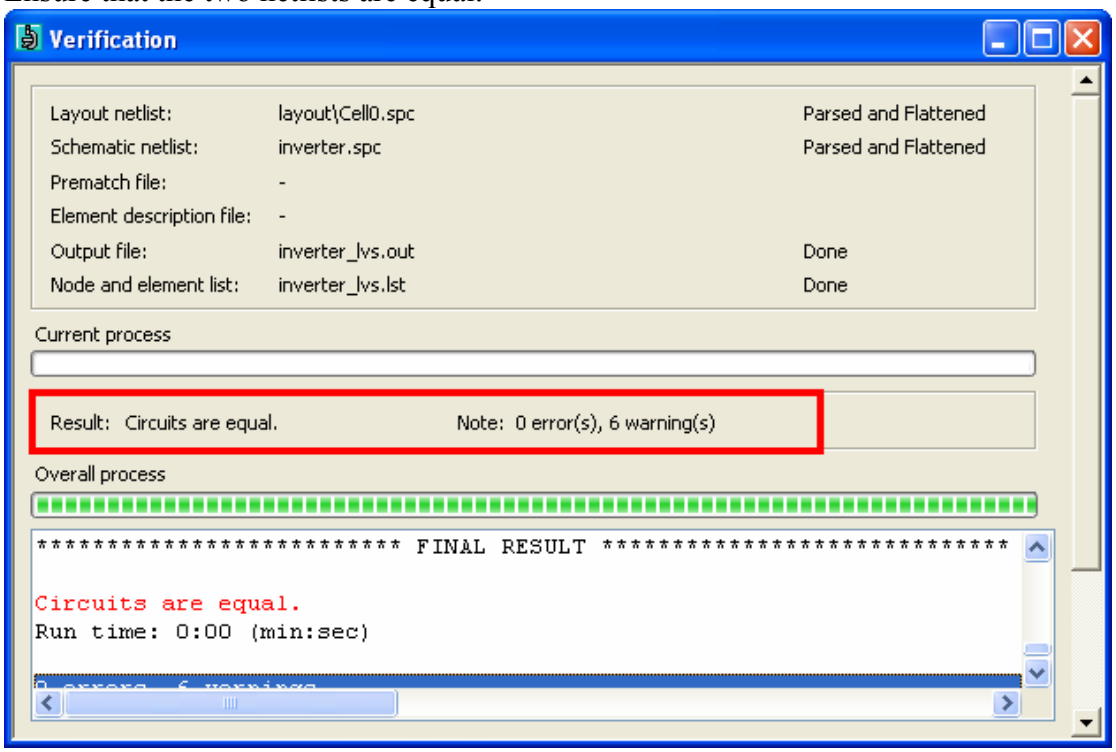
The results are saved in the Node and element list.



Include transistor dimensions in comparison.



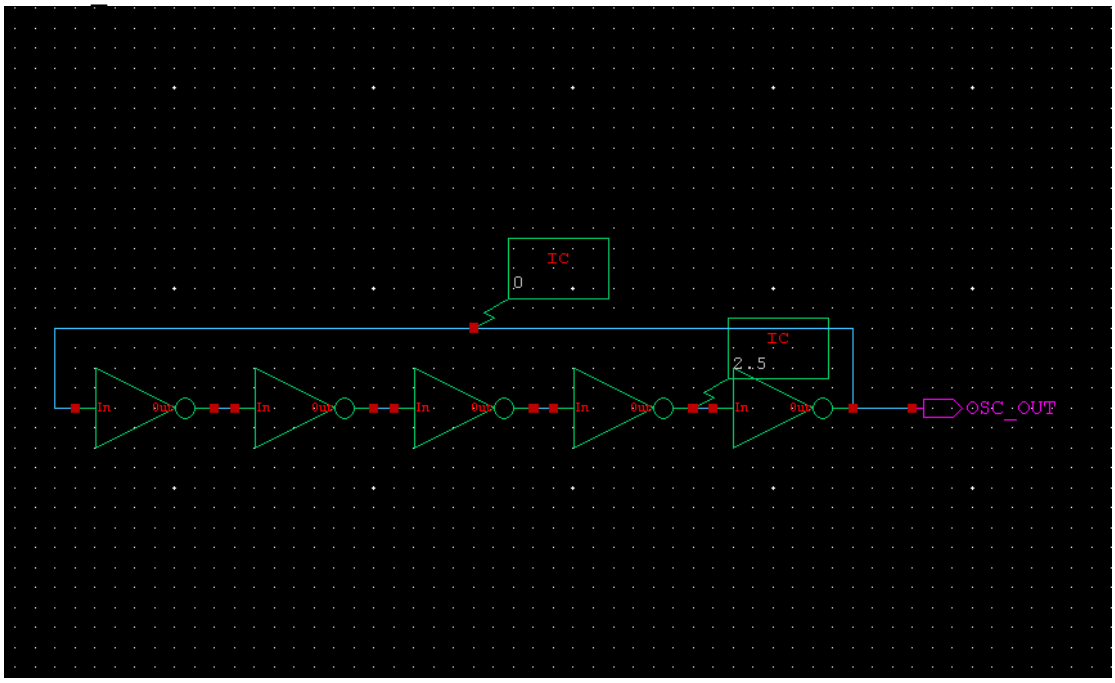
Ensure that the two netlists are equal.



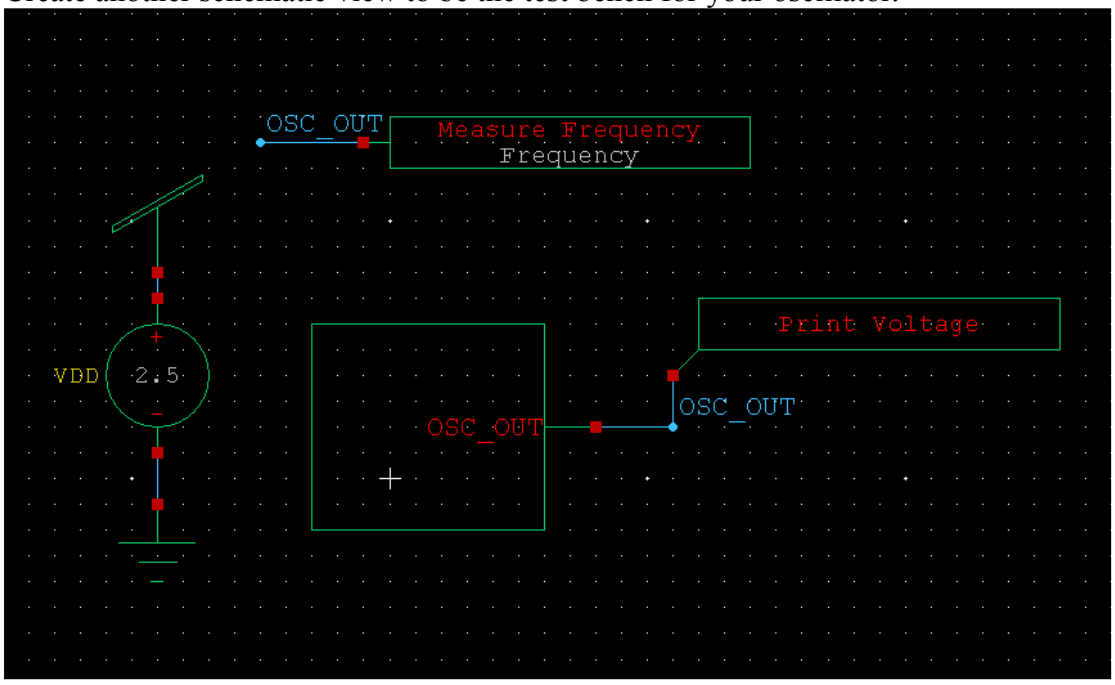
Ring Oscillator

S-Edit

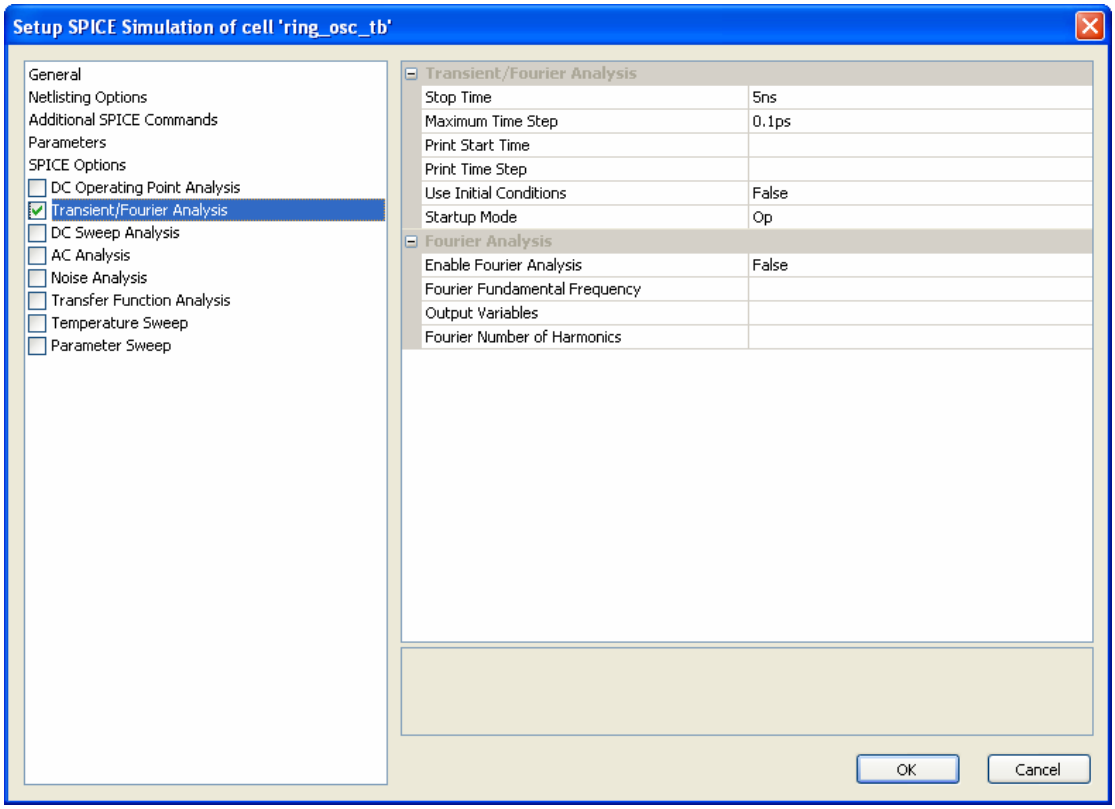
In S-Edit: Create a new cell view for ring oscillator. Setup initial conditions from SPICE_Commands.

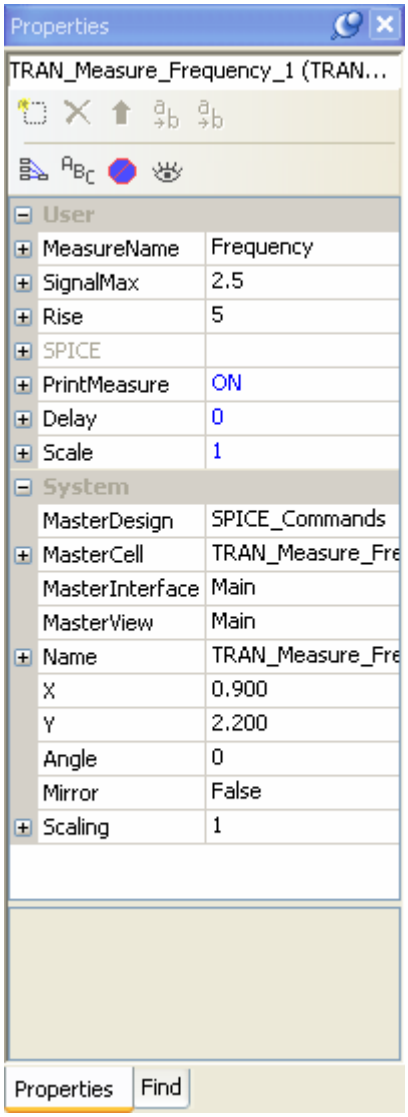


Create another schematic view to be the test bench for your oscillator.



Run transient simulation. Measure output frequency from W-Edit and T-Spice output window. Compare the simulation result with the analytical formula.

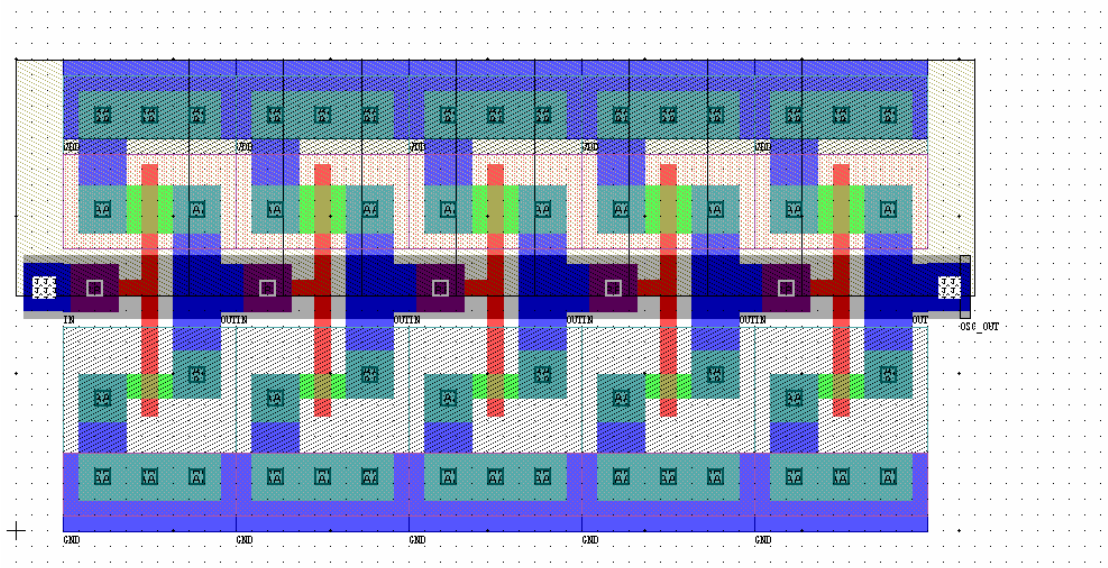

Setup SPICE Simulation of cell 'ring_osc_tb'
General
Netlisting Options
Additional SPICE Commands
Parameters
SPICE Options
DC Operating Point Analysis
Transient/Fourier Analysis
DC Sweep Analysis
AC Analysis
Noise Analysis
Transfer Function Analysis
Temperature Sweep
Parameter Sweep
Transient/Fourier Analysis
Stop Time
5ns
Maximum Time Step
0.1ps
Print Start Time
Print Time Step
Use Initial Conditions
False
Startup Mode
Op
Fourier Analysis
Enable Fourier Analysis
False
Fourier Fundamental Frequency
Output Variables
Fourier Number of Harmonics
OK
Cancel



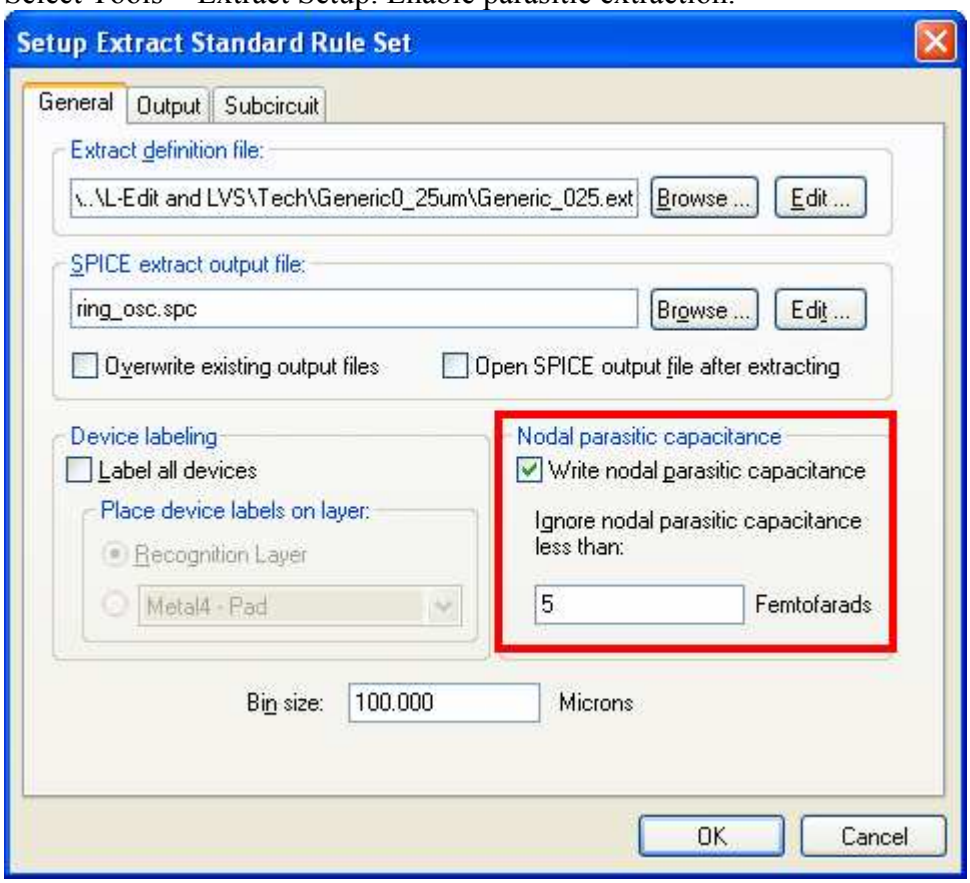
Export the ring oscillator circuit to SPICE netlist to use it in LVS.

L-Edit

In L-Edit: Create a new cell: Cell > New… and name it ring_osc.
Add 5 instances of inverter cell: Cell > Instance. Close the ring by M2.



Select Tools > Extract Setup. Enable parasitic extraction.



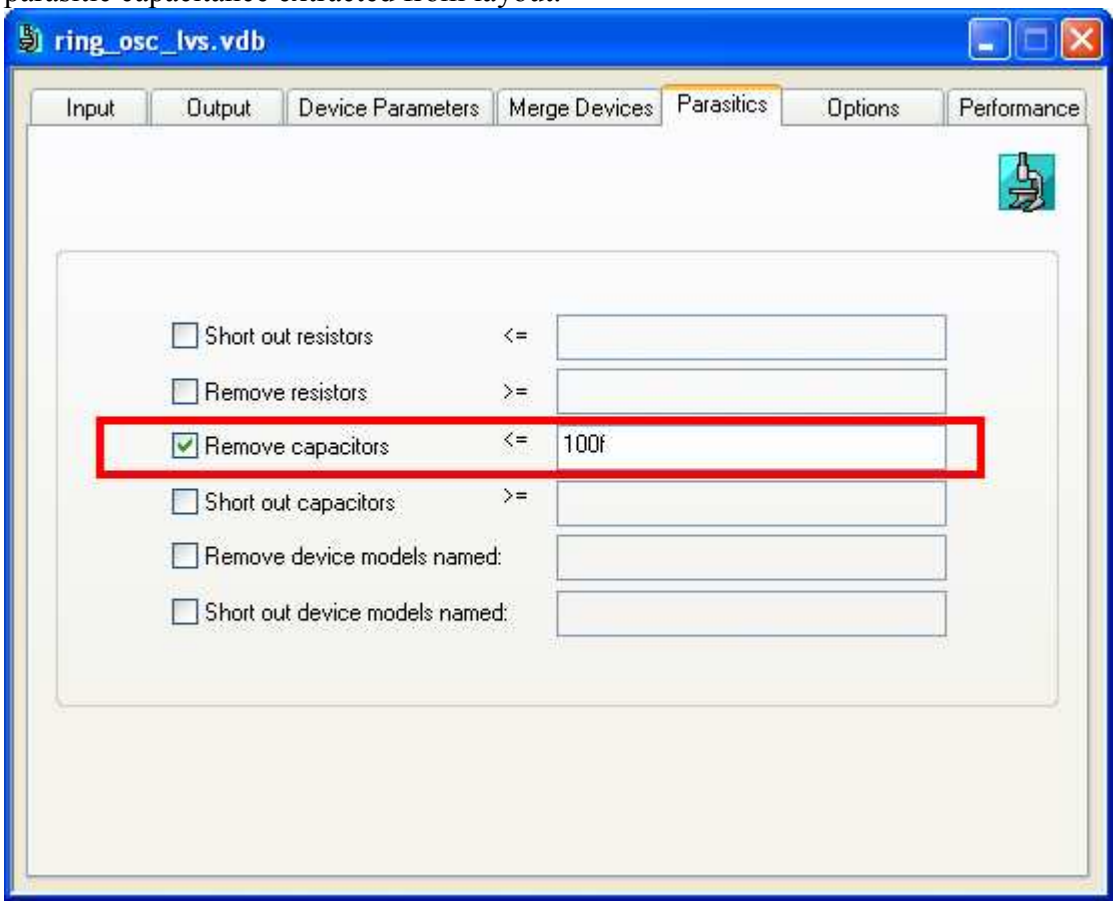
Run the extraction and ignore warnings. Open the generated Spice netlist. Notice the parasitic cap at the output of the oscillator. You will need it later.

```
*       1 = U5/OUT (14.25 , 3.5)
*       2 = U1/GND (0.75 , 0)
*       2 = U2/GND (3.5 , 0)
*       2 = U3/GND (6.25 , 0)
*       2 = U4/GND (9 , 0)
*       2 = U5/GND (11.75 , 0)
*       3 = U4/OUT (11.5 , 3.5)
*       3 = U5/IN (11.75 , 3.5)
*       4 = U1/VDD (0.75 , 6.25)
*       4 = U2/VDD (3.5 , 6.25)
*       4 = U3/VDD (6.25 , 6.25)
*       4 = U4/VDD (9 , 6.25)
*       4 = U5/VDD (11.75 , 6.25)
*       5 = U3/OUT (8.75 , 3.5)
*       5 = U4/IN (9 , 3.5)
*       6 = U2/OUT (6 , 3.5)
*       6 = U3/IN (6.25 , 3.5)
*       7 = U1/OUT (3.25 , 3.5)
*       7 = U2/IN (3.5 , 3.5)

Cpar1 OSC_OUT 0 5.9480744f
Cpar2 U1/GND 0 80.1181406f
Cpar3 U1/VDD 0 31.466875f

M1 OSC_OUT U4/OUT U1/VDD U1/VDD PMOS L=250n W=750n AD=750f PD=3.5u AS=750f PS=3.5u    $ (13 4.75 13.25 5.5)
M2 U4/OUT U3/OUT U1/VDD U1/VDD PMOS L=250n W=750n AD=750f PD=3.5u AS=750f PS=3.5u    $ (10.25 4.75 10.5 5.5)
M3 U3/OUT U2/OUT U1/VDD U1/VDD PMOS L=250n W=750n AD=750f PD=3.5u AS=750f PS=3.5u    $ (7.5 4.75 7.75 5.5)
M4 U2/OUT U1/OUT U1/VDD U1/VDD PMOS L=250n W=750n AD=750f PD=3.5u AS=750f PS=3.5u    $ (4.75 4.75 5 5.5)
M5 U1/OUT OSC_OUT U1/VDD U1/VDD PMOS L=250n W=750n AD=750f PD=3.5u AS=750f PS=3.5u    $ (2 4.75 2.25 5.5)
M6 OSC_OUT U4/OUT U1/GND U1/GND NMOS L=250n W=375n AD=656.25f PD=3.5u AS=656.25f PS=3.5u    $ (13 2.125 13.25 2.5)
M7 U4/OUT U3/OUT U1/GND U1/GND NMOS L=250n W=375n AD=656.25f PD=3.5u AS=656.25f PS=3.5u    $ (10.25 2.125 10.5 2.5)
```

LVS

Start LVS.

Compare layout and schematic netlists and make sure they are equal. Ignore the parasitic capacitance extracted from layout.



Parasitic Capacitance Effect

Create a new test bench for ring oscillator including the parasitic cap. Run the simulation again and record the new oscillation frequency. Comment (Can we neglect parasitics?).