وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog/Mixed-Signal Simulation and Modeling

Lab 03

MOSFET Modeling and Simulation

Objectives

1. Create simple SPICE MOSFET model cards.
2. Run and analyze SPICE MOSFET simulations.
3. Get familiar with different types of SPICE models and model parameters.

Instructions

1. Use LTSpice for design entry and simulation. Use this link: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html
2. You may use Notepad++ to write your netlist (it has SPICE highlight mode). Do NOT use a schematic entry GUI. Do NOT use any other program.
3. If necessary, make any reasonable assumptions.
4. Check LTSpice help if needed.

Part 1

Index	Deliverable
1.	Complete “my_nmos.lib” to model a 180nm LEVEL 1 MOSFET that has ideal VCCS characteristics, VTH = 0.4 V and ON current of 10 mA at W = 10 um, L = Lmin and VGS = VDS = 1.8 V. Complete and run “nmos_tb.cir”. This should plot the NMOS ID vs VDS with VGS as a parameter. Use nested DC sweep. Report the netlist and the results. Report any warning in the SPICE error log and comment on them.
2.	Modify the model to include VDS dependence with VA = 10 V. Report the netlist and the results.
3.	Modify the model to include the effect of velocity saturation such that the ON current saturates at 5 mA approximately. Report the netlist and the results.
4.	Create “my_pmos.lib” to model a LEVEL 1 PMOS that has half the mobility of the NMOS (use the NMOS model in Step 2). What should be the polarity of vt0? Complete and run “cmos_inv_dc.cir”. This should plot the DC transfer characteristics of a CMOS inverter. Report the netlist and the results.
5.	Complete and run “cmos_inv_tran.cir”. This should plot the transient characteristics of a CMOS inverter. Use pulse source with period = 100 ps and rise/fall = 5 ps. Report the netlist and the results. Measure the delay.
6.	Modify the model to include CJ = 1 fF/(um)^2 and CJSW = 0.1 fF/um (note the units). Use reasonable values for (AD,AS,PD,PS) when you instantiate the MOSFET. Assume diffusion (junction) length (LDIFF) = 5*lambda, lambda = Lmin/2, junction area = LDIFF*W and junction perimeter = 2*(LDIFF+W).

	Run “cmos_inv_tran.cir”. Report the netlist and the results. Measure the delay. Compare the results to the previous case. Comment.

Part 2

Index	Deliverable
1.	Copy “nmos_tb.cir” to a new file “nmos_tb_param.cir” and edit it to run parametric sweeps for both VGS and VDS instead of nested DC sweeps. Report the netlist and the results. Compare the simulation time to the nested DC sweep testbench.
2.	Edit “nmos_tb.cir” to use the “ee214b_hspice.sp” HSPICE model. What version of BSIM is this HSPICE model? How to set the LEVEL parameter appropriately for LTspice in this case? Compare the results to your LEVEL 1 model.
3.	When you run the previous testbench, you will see in the SPICE error log that LTspice had problems with some BSIM parameters in the model file. Refer to HSPICE documentation and explain the meaning and use of each parameter. Open the model file and see the values of these parameters? What are the meanings of these values? How do you expect they will affect the simulation results?
4.	Create “cmos_inv_tran_fo4.cir”. This should simulate a fanout-of-4 (FO4) chain of five CMOS inverters using the “ee214b_hspice.sp” model. Create a subcircuit for the inverter and instantiate it five times. Use the multiplier parameter to emulate the FO4 effect. Note that for LTspice, the multiplier parameter is not predefined for the subcircuit itself as a whole (it is predefined in other simulators such as spectre and HSPICE), but you can use the multiplier parameter of the MOSFET itself. Report the netlist and the results.
5.	Measure the FO4 delay for the middle inverter in the previous testbench. Calculate FO4 delay (in ps) divided by lambda (in nm), where lambda = Lmin / 2. This ratio is useful to get a quick estimate of the delay in any technology. How much FO4 delay do you expect for a 65nm technology?

Thanks to all who contributed to these labs. If you find any errors or have suggestions concerning these labs, please contact Hesham.omran@eng.asu.edu.eg.