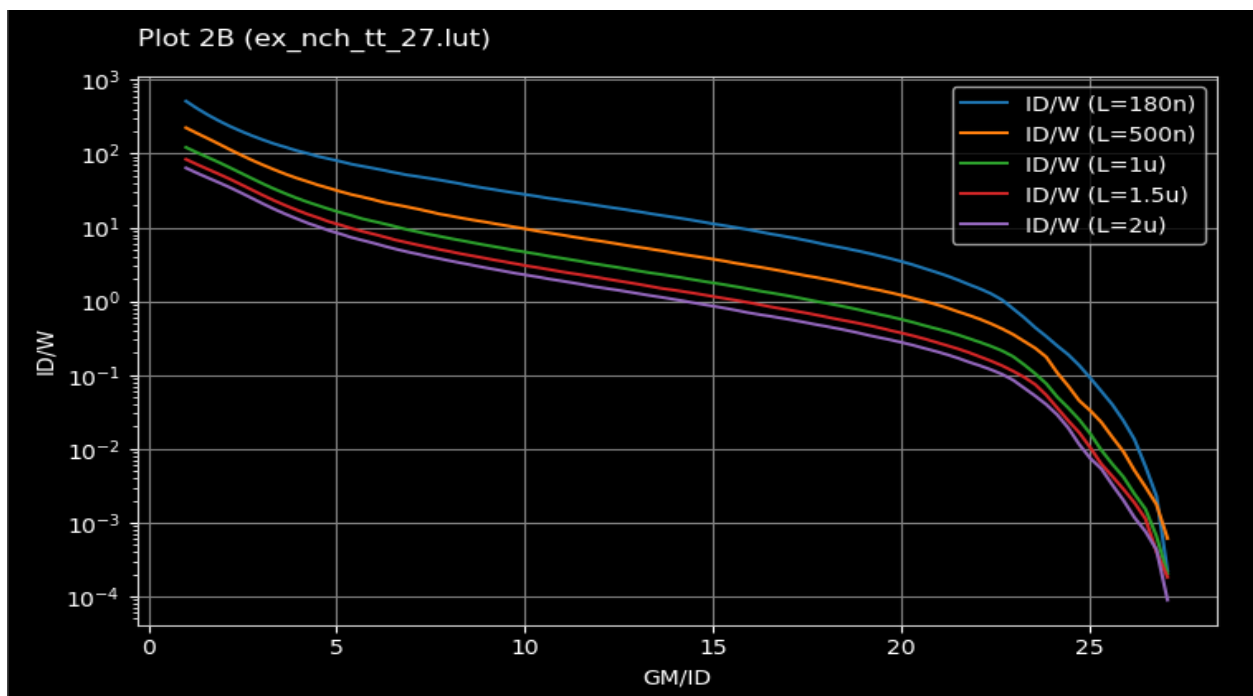
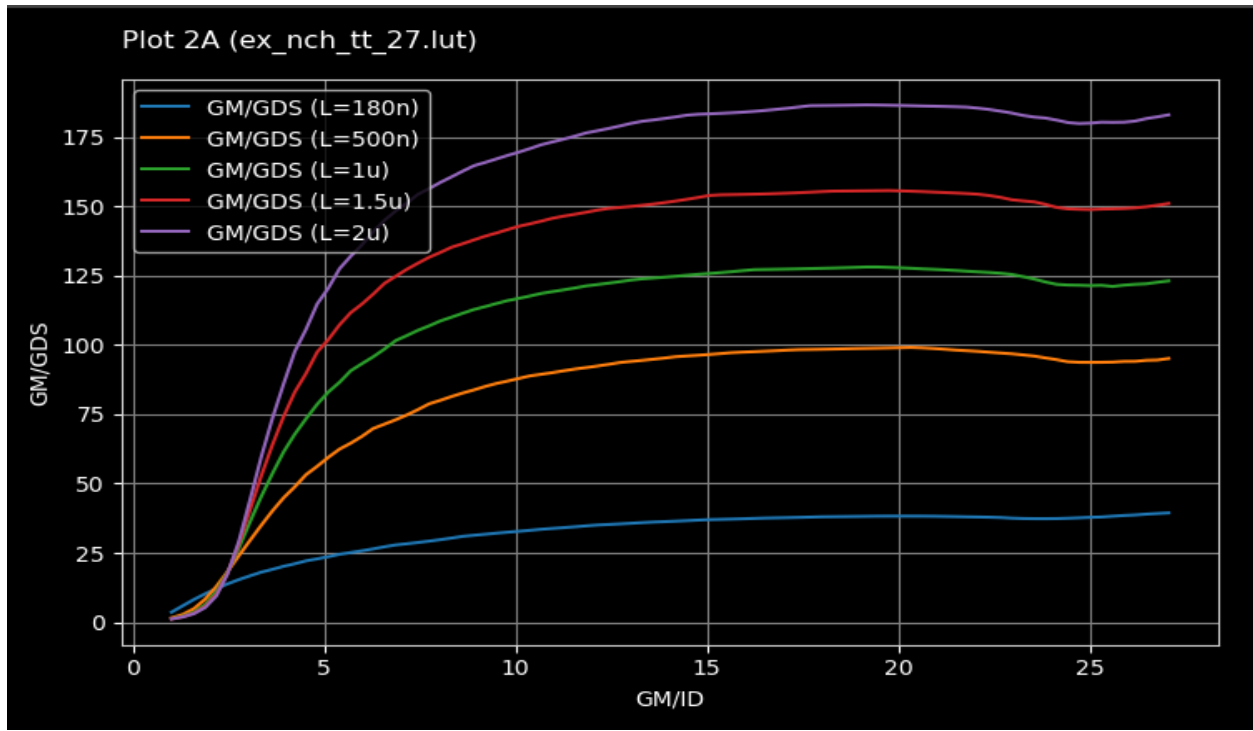
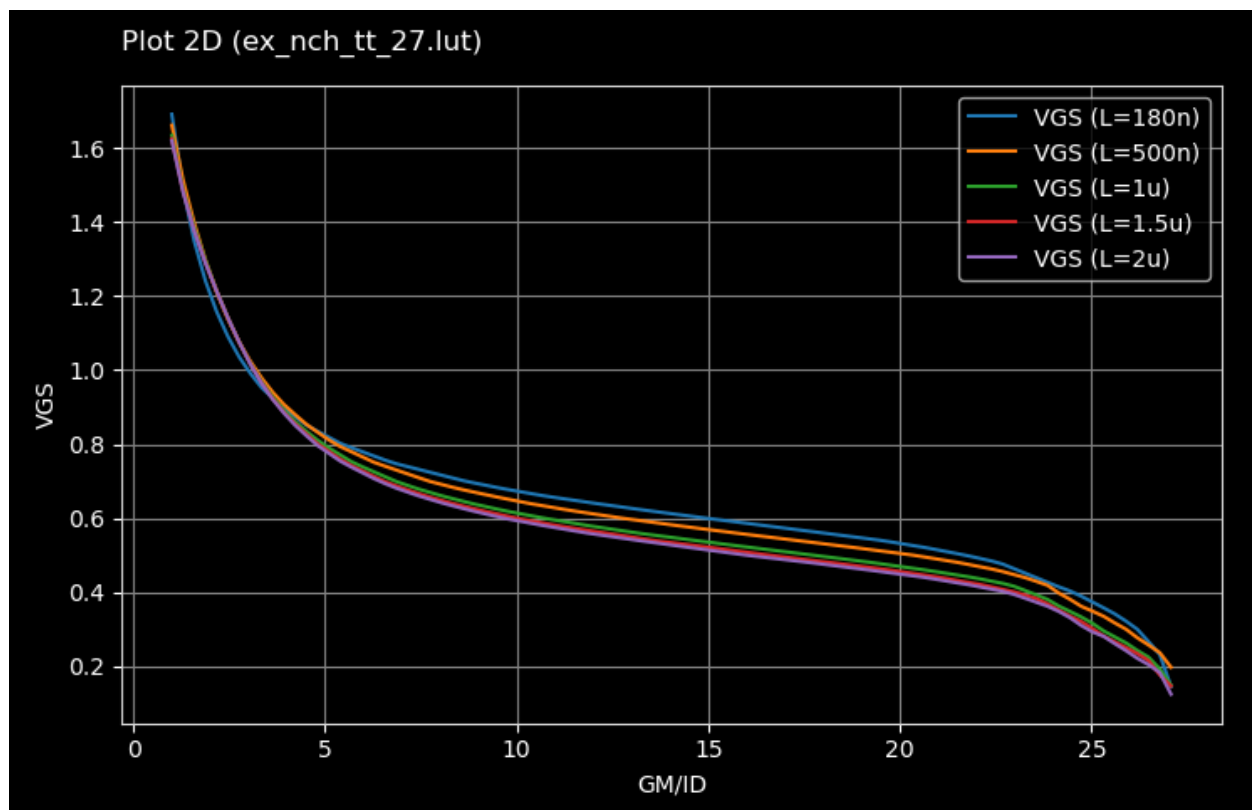
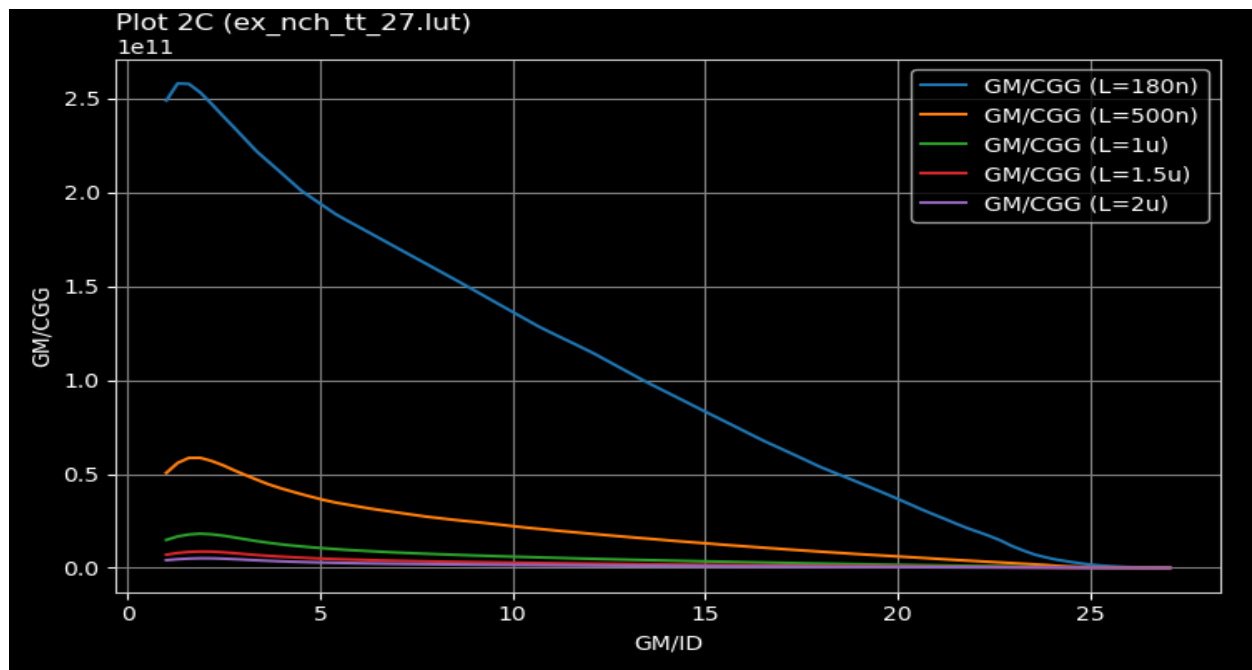


Lab 4

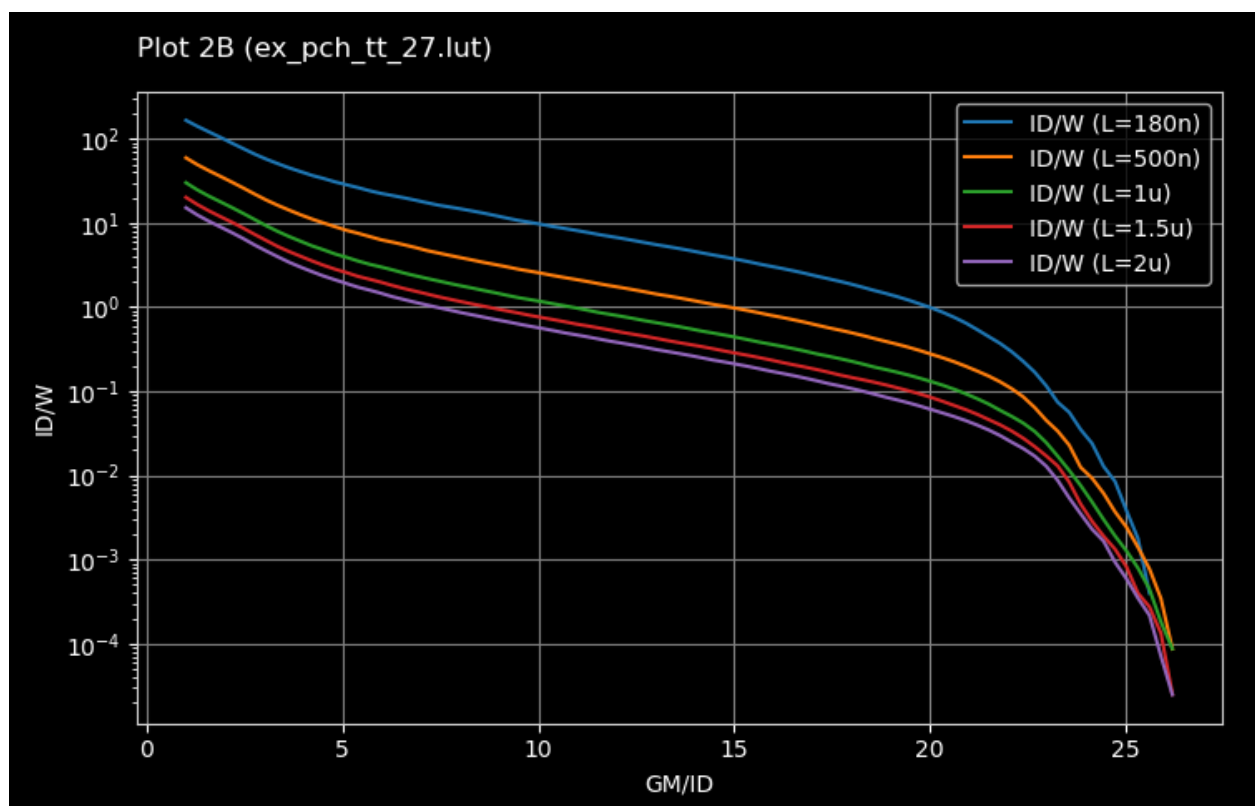
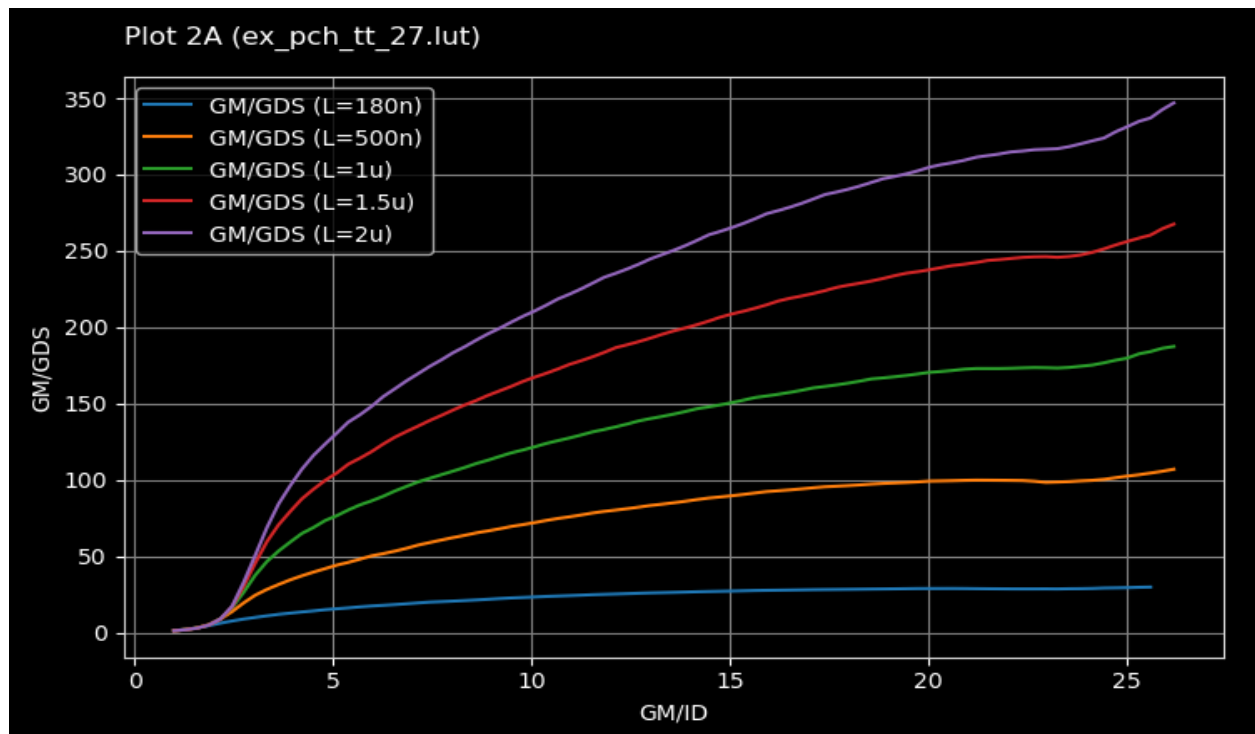
Part 1

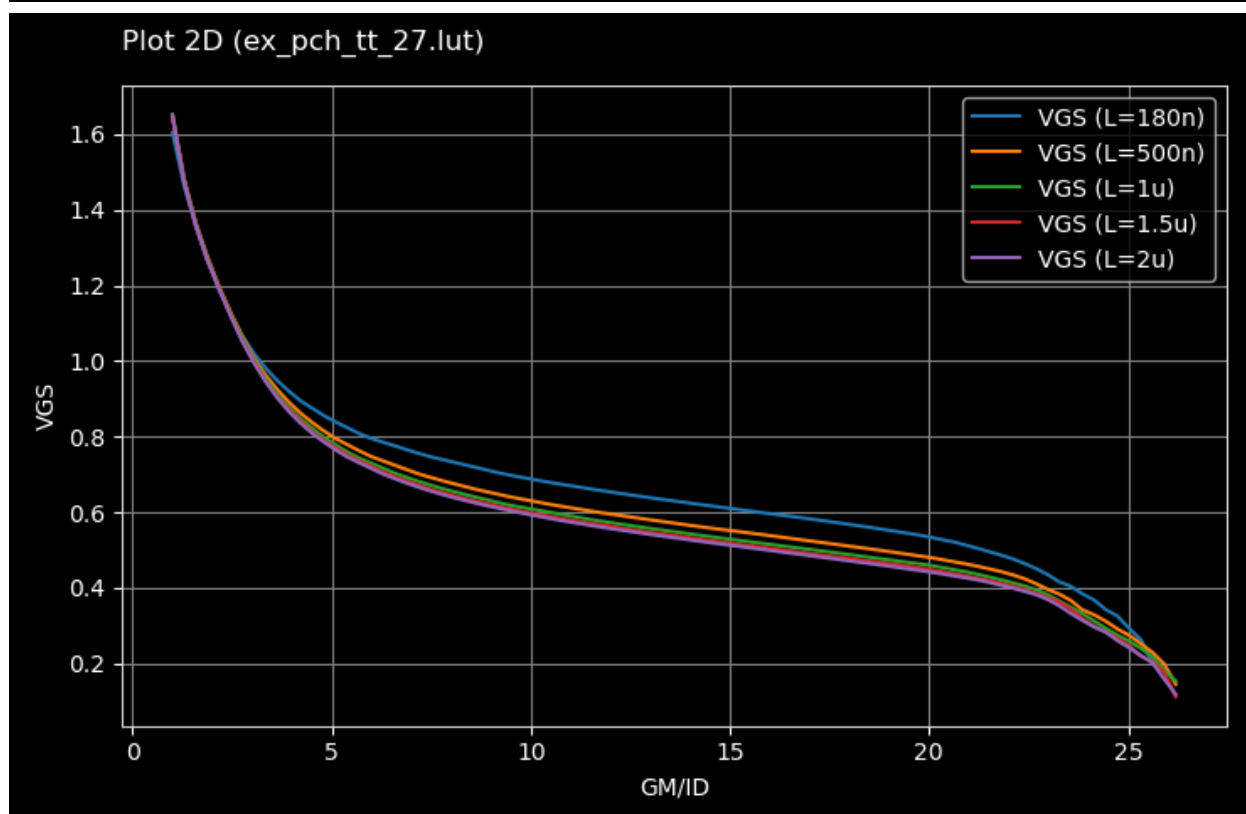
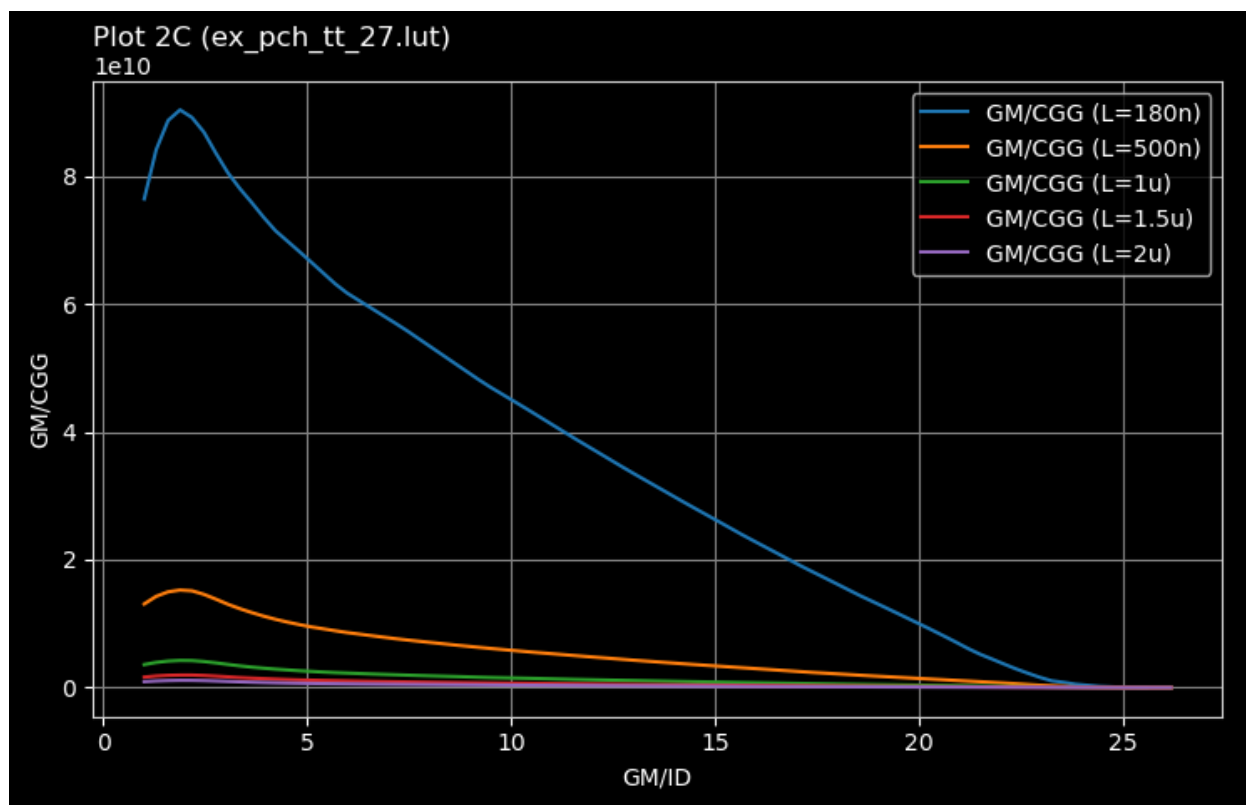
NMOS:





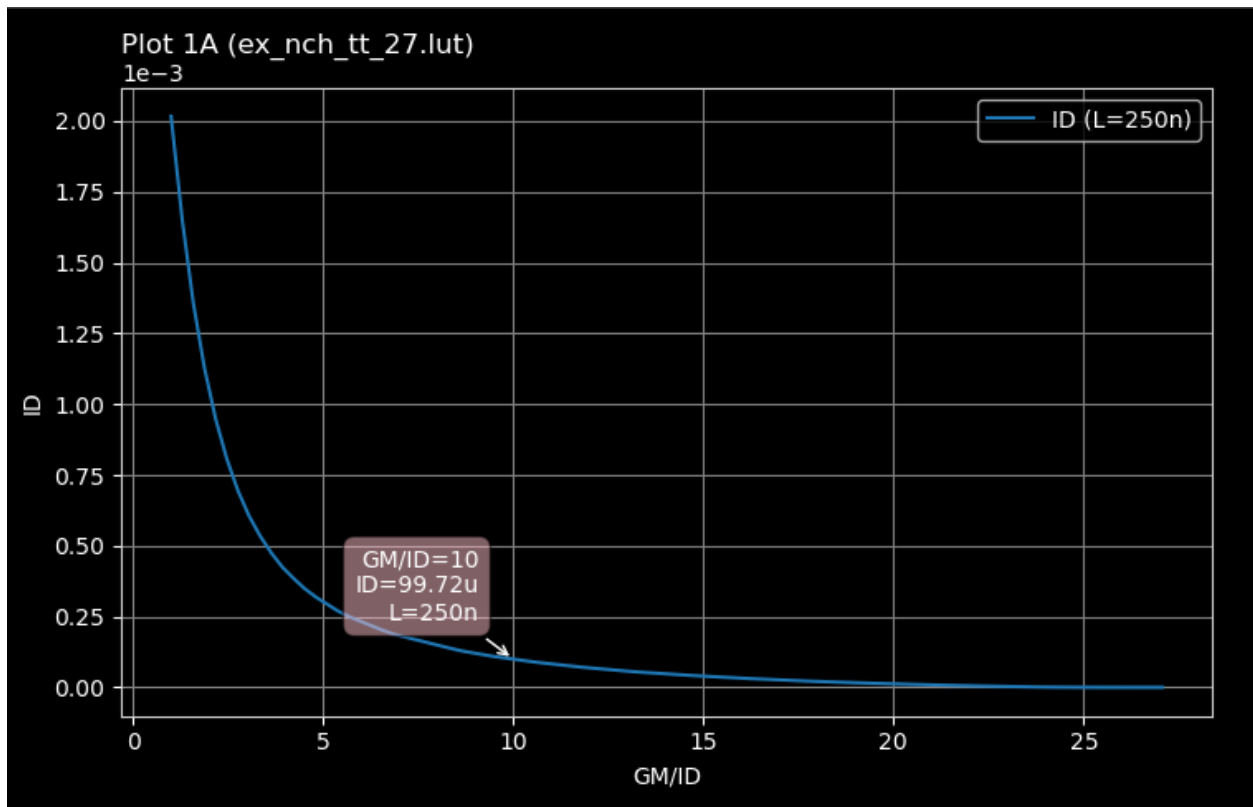
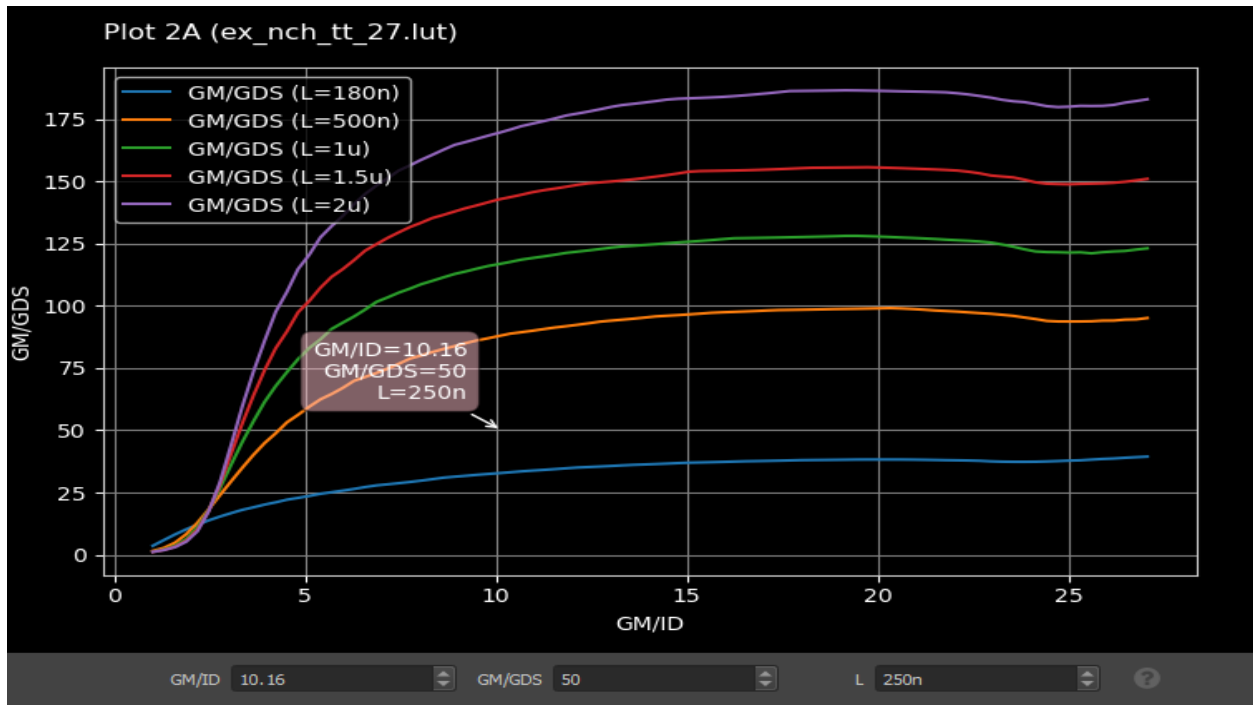
PMOS:

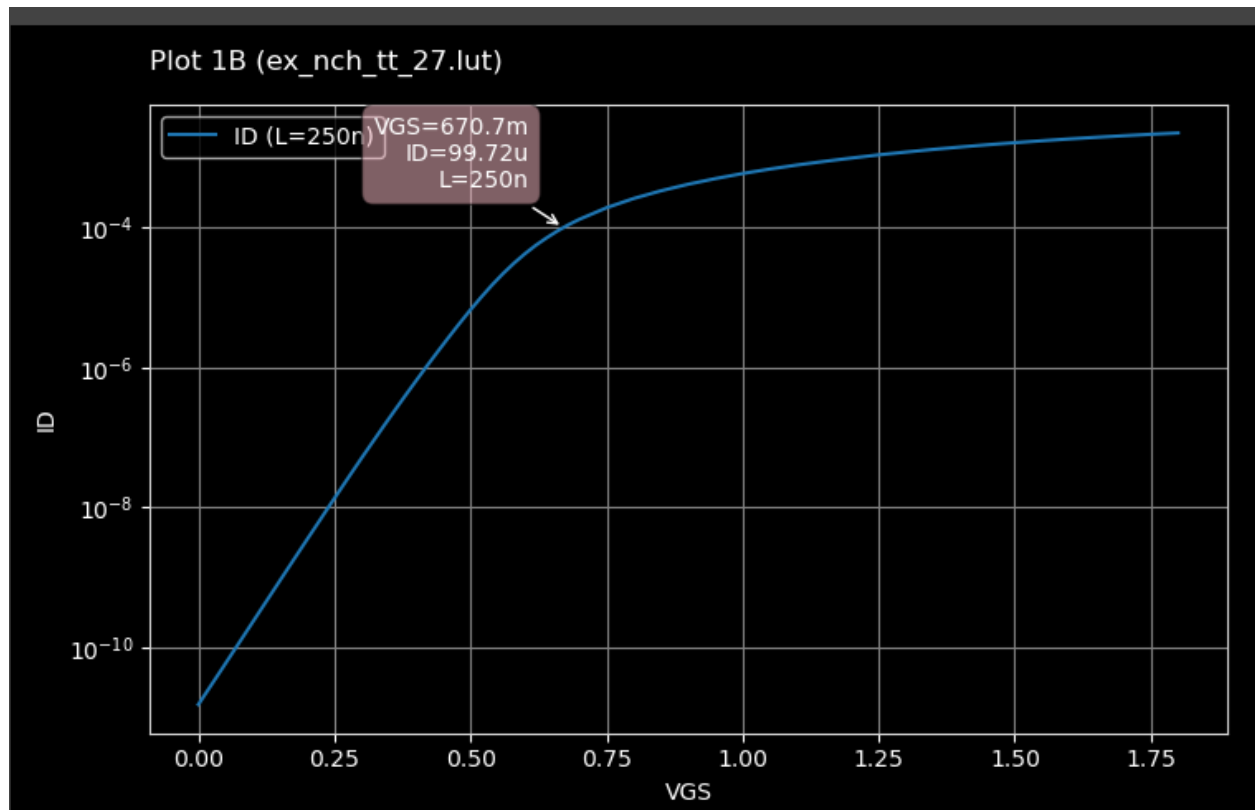




2-

L choice





ID= 99.72 μ A

Vgs = 670.7 mV

3- Lookup Test modifications :

```

itor - C:\Users\DELL\Desktop\Siemens AMS 2025\lab4\lookup_test.m

% Find L that give gm/gds > given value
L_vector = nch.L; % Get the L vector from LUT structure
%Get the gm/gds values vector corresponding to the L_vector
gm_gds_vector = look_up(nch, 'GM_GDS', 'GM_ID', M1.gm_ID, 'VDS', M1.VDS, 'L', L_vector);
% Get the minimum L that gives gm/gds > the given value
% add line to get the minimum L for M1 that gives gm/gds >= M1.gm_gds
valid_indices = find(gm_gds_vector >= M1.gm_gds);
M1.L = L_vector(valid_indices(1));
% Get the current by computing the ID/W and then multiply it by W
M1.ID_W = look_up(nch, 'ID_W', 'GM_ID', M1.gm_ID, 'VDS', M1.VDS, 'L', M1.L);
% add line to get the current of M1
M1.ID = M1.ID_W * M1.W;

% Get the VGS value
% add line to get the VGS value of M1
vgs_vec = nch.VGS;
gm_id_vec = look_up(nch, 'GM_ID', 'VGS', vgs_vec, ...
                    'VDS', M1.VDS, 'L', M1.L);

 [~, idx] = min(abs(gm_id_vec - M1.gm_ID));
M1.VGS = vgs_vec(idx);

% Print the solution
fprintf('Minimum L = %.2g um\n', M1.L);
fprintf('VGS = %.2f\n', M1.VGS);
fprintf('ID = %.2d\n', M1.ID);

```

```

>> lookup_test
Minimum L = 0.26 um
VGS = 0.68
ID = 9.52e-05
fx >>

```

Parameter	Matlab	ADT
L min	0.26 um	0.25 um
VGS	0.68 V	0.6707 V
Id	95.2 uA	99.72 uA

4-

Input pair design

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Step 1 input Pair design

$GBW = \frac{g_m}{2\pi C_l} > \frac{g_m}{I_D} = 15$

$\therefore g_m = 3,14 \times 10^{-4} \text{ S}, I_D = 20,9 \mu\text{A}$

$r_o = \frac{3}{2} \times \frac{A_V}{g_m} = 238,85 \text{ k}\Omega$

$g_{ds} = \frac{1}{r_o} = 4,18 \mu\text{S}$

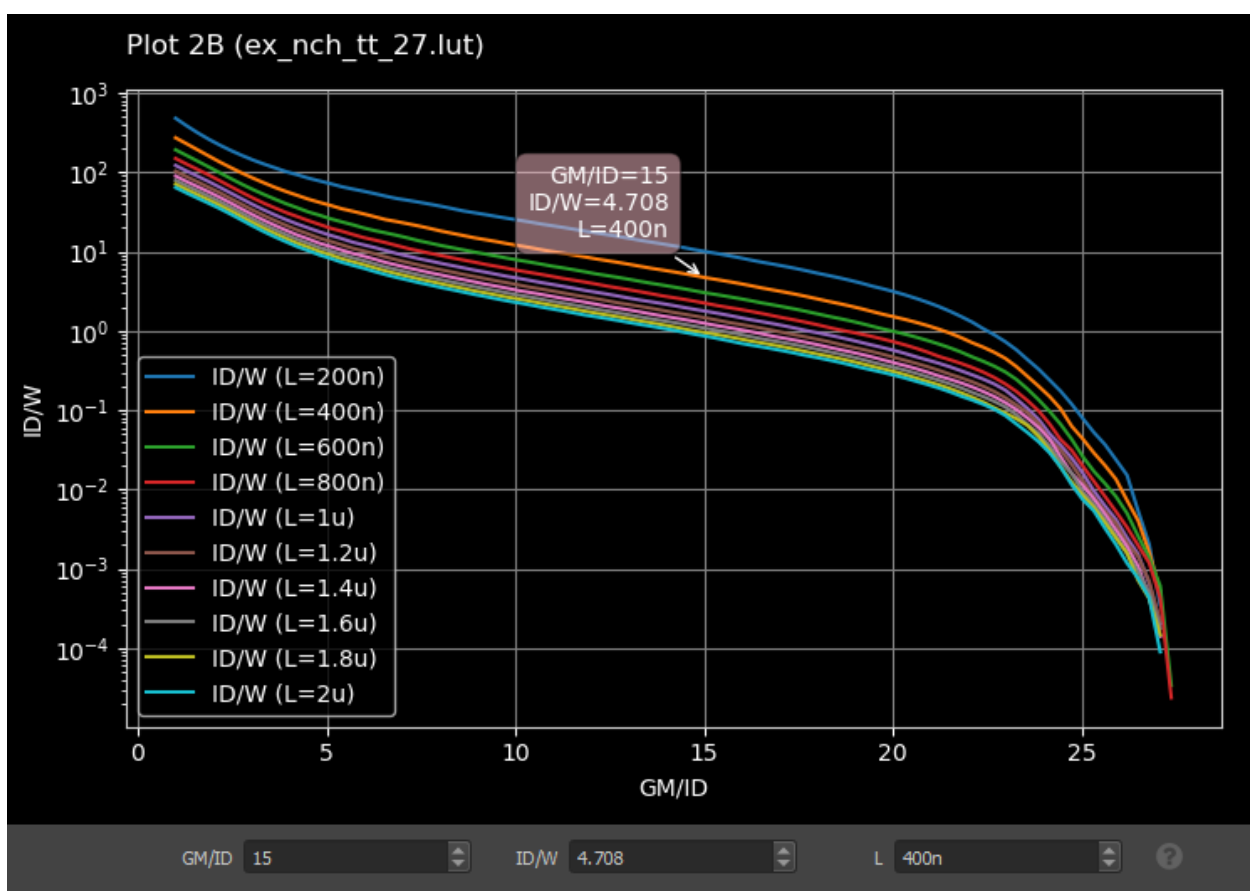
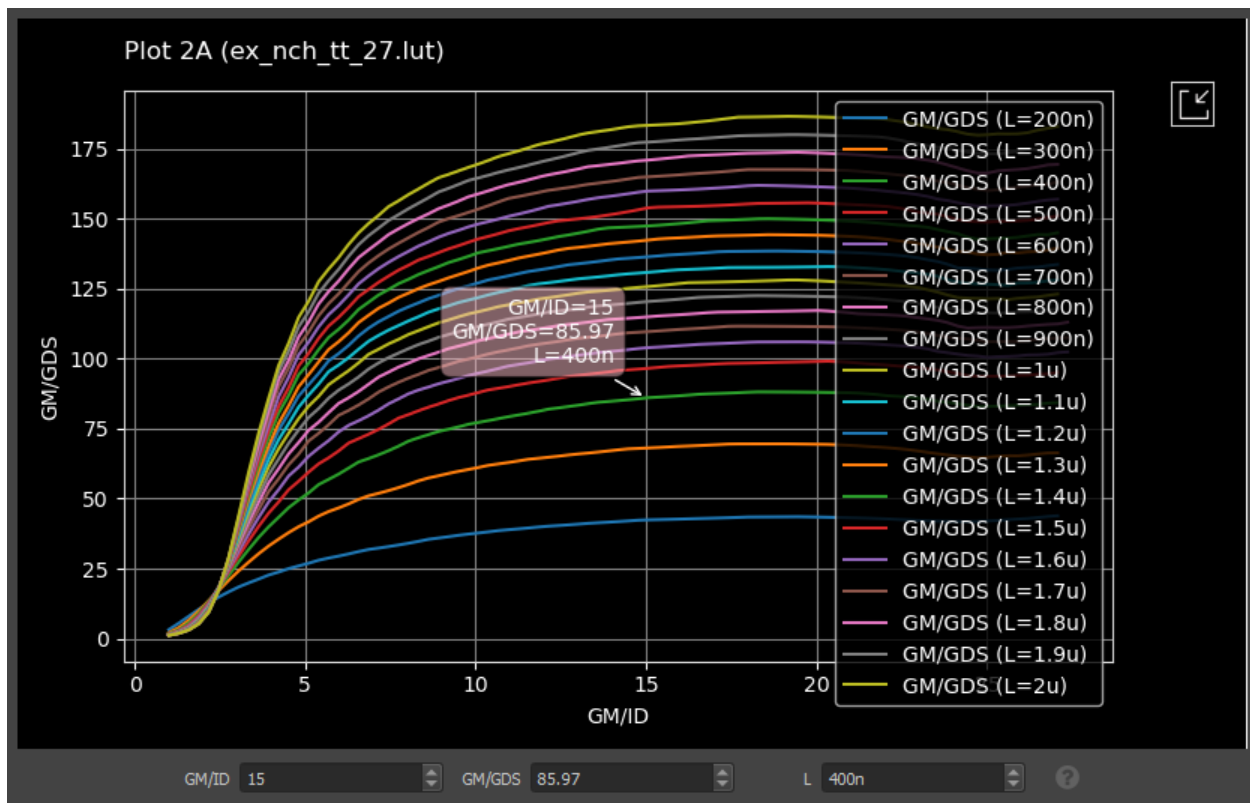
we want $\frac{g_m}{g_{ds}} > \frac{3}{2} \times 50 > 75$

from charts:-

$L = 0,4 \mu\text{m}$

$W = 4,3 \mu\text{m}$

$\frac{I_D}{W} = 4,7$



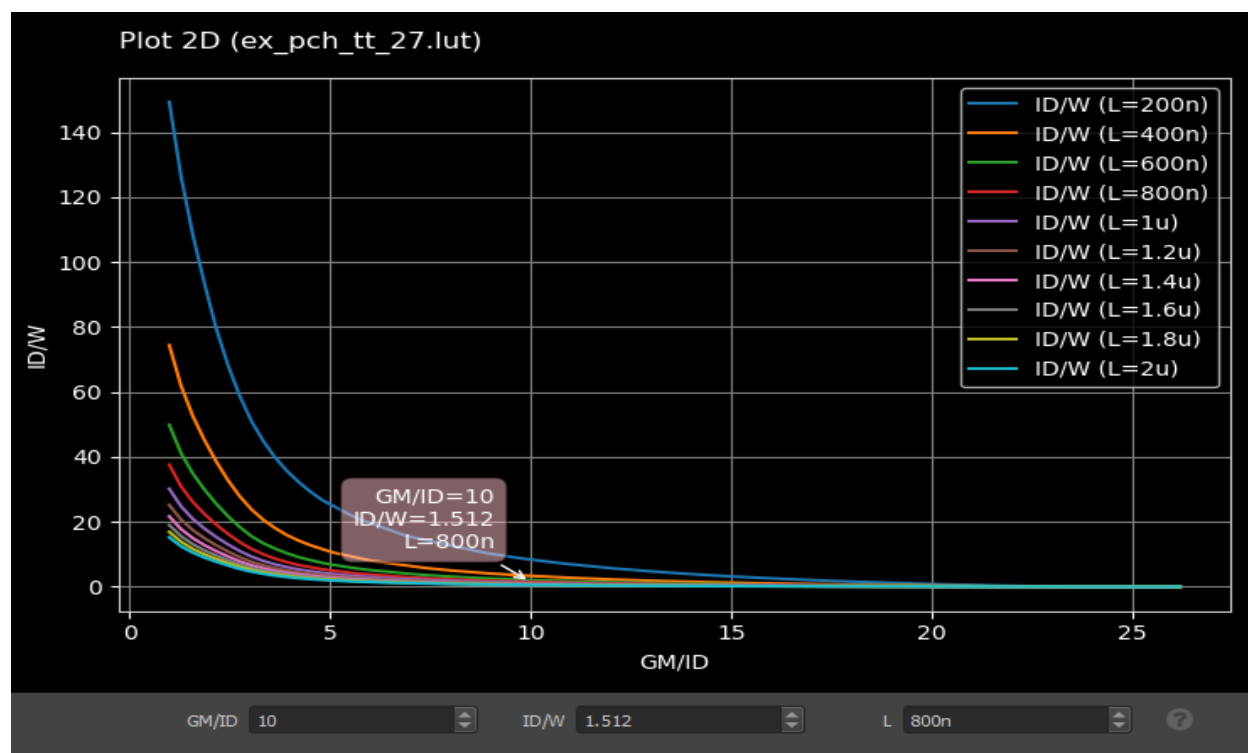
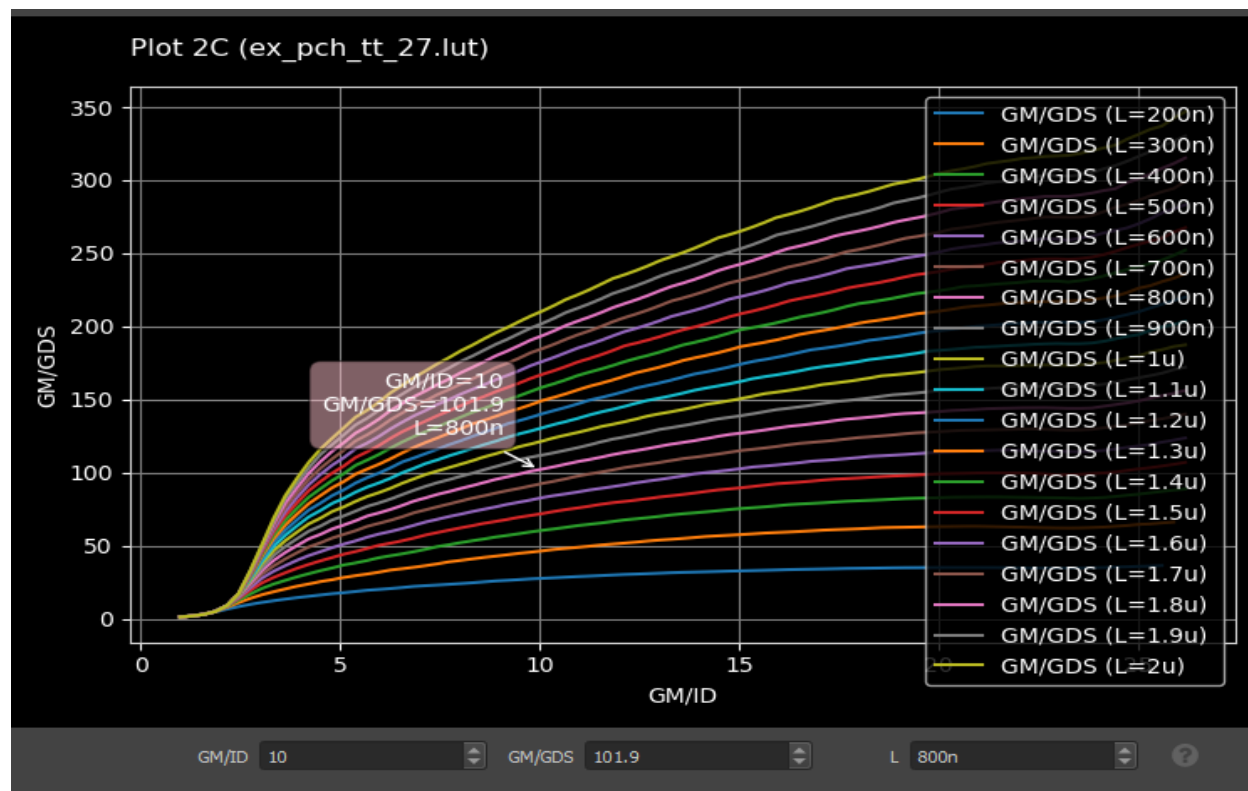
Load design :

Step 2 (current Mirror Load)

$$I_{D2} = I_{D1}, \quad \frac{g_m}{I_D} = 10$$
$$\therefore g_m = 2,09 \times 10^{-4} \text{ S}$$
$$g_{ds2} = \frac{1}{2} g_{ds1} = 2,09 \text{ } \mu\text{S}$$
$$\therefore \frac{g_m}{g_{ds}} = 100$$

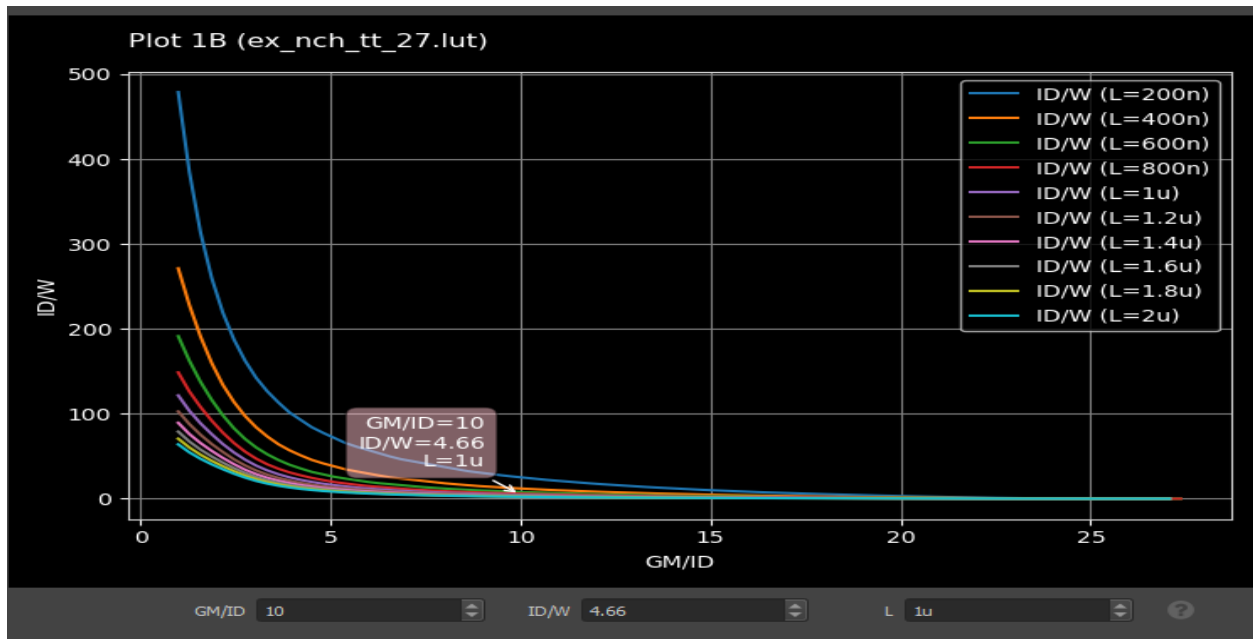
From charts

$$L = 0,8 \text{ } \mu\text{m}, \quad \frac{I_D}{W} = 1,6$$
$$W = 13 \text{ } \mu\text{m}$$



Tail design :

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7 am
Step 3
tail design
assume $\frac{g_m}{I_d} = 10$, $L = 1 \mu m$
 $I_{tail} = 2I_d = 4,188 \times 10^{-5} A$
From chart
 $\frac{I_d}{W} = 4,66$
 $W = 9 \mu m$



gm/ID = 15 for the input pair and gm/ID = 10 for the load and the tail bias (why is this reasonable?)

high gm/Id for the input pair to achieve High gm efficiency, better gain-bandwidth, low power and relatively low gm/Id for load and tail for Smaller area, adequate gm and low channel length modulation , good for current sources

ro of the load is two times ro of the input pair (why is this reasonable?).

PMOS devices have lower mobility, so for the same current, they tend to have wider W, and a longer L . They also tend to have lower λ , so ro is higher.

L= 1um for the tail bias (why is this reasonable?).

High L choice Improves ro and current source quality, helps robustness and matching

DesignOTA.m

```
C designOTA.m
1  function OTA = designOTA(specs)
2  % OTA Synthesis Function
3  % Inputs: specs.GBW, specs.CL, specs.AVDC
4  % Output: OTA structure with sizing and bias info
5
6  % Supply voltage
7  VDD = 1.8;
8
9  % Load lookup tables
10 load 180nch.mat;
11 load 180pch.mat;
12
13 % === Input Pair M1 ===
14 OTA.M1.gm = specs.GBW * specs.CL * 2 * pi;
15
16 % Estimate output resistance from DC gain
17 DC_Gain_mag = 10^(specs.AVDC / 20); % Convert from dB to magnitude
18 Rout = DC_Gain_mag / OTA.M1.gm; % Total output resistance of OTA
19
20 % Assume ro(load) = 5 * ro(input), so:
21 % Rout = (ro_M1 * ro_M3) / (ro_M1 + ro_M3) ≈ ro_M1 * ro_M3 / ro_M3 = ro_M1 / 6
22 % => ro_M1 = 6 * Rout / 5
23 OTA.M1.ro = (3 / 2) * Rout;
24
25 OTA.M1.gds = 1 / OTA.M1.ro;
26 OTA.M1.VDS = VDD / 3; % Assume 1/3rd VDD
27 OTA.M1.gm_gds = OTA.M1.gm / OTA.M1.gds;
28 OTA.M1.gm_ID = 15; % Assumed gm/ID
29
30 % Get drain current from gm and gm/ID
31 OTA.M1.ID = OTA.M1.gm / OTA.M1.gm_ID;
```

```

33 % Search for the minimum L that gives gm/gds >= target
34 L_vector = nch.L;
35 gm_gds_vector = look_up(nch, 'GM_GDS', 'GM_ID', OTA.M1.gm_ID, ...
36 | | | | | | | 'VDS', OTA.M1.VDS, 'L', L_vector);
37 OTA.M1.L = min(L_vector(gm_gds_vector >= OTA.M1.gm_gds));
38
39 % Get ID/W for final W sizing
40 OTA.M1.ID_W = look_up(nch, 'ID_W', 'GM_ID', OTA.M1.gm_ID, ...
41 | | | | | | | 'VDS', OTA.M1.VDS, 'L', OTA.M1.L);
42 OTA.M1.W = OTA.M1.ID / OTA.M1.ID_W;
43
44 % === CM Load M3 ===
45 OTA.M3.ID = OTA.M1.ID;
46 OTA.M3.VDS = VDD / 3;
47 OTA.M3.gm_ID = 10; % Assumption
48 OTA.M3.gm = OTA.M3.gm_ID * OTA.M3.ID;
49
50 % Use ro = 2 * ro_M1
51 OTA.M3.ro = 2 * OTA.M1.ro;
52 OTA.M3.gds = 1 / OTA.M3.ro;
53 OTA.M3.gm_gds = OTA.M3.gm / OTA.M3.gds;
54
55 gm_gds_vector = look_up(pch, 'GM_GDS', 'GM_ID', OTA.M3.gm_ID, ...
56 | | | | | | | 'VDS', OTA.M3.VDS, 'L', L_vector);
57 OTA.M3.L = min(L_vector(gm_gds_vector > OTA.M3.gm_gds));
58
59 % Final sizing of M3
60 OTA.M3.ID_W = look_up(pch, 'ID_W', 'GM_ID', OTA.M3.gm_ID, ...
61 | | | | | | | 'VDS', OTA.M3.VDS, 'L', OTA.M3.L);
62 OTA.M3.W = OTA.M3.ID / OTA.M3.ID_W;
63

```



```

4 % === Tail Transistor M5 ===
5 OTA.M5.L = 1; % Assumption
6 OTA.M5.ID = 2 * OTA.M1.ID; % Sinks current from both M1 and M2
7 OTA.M5.VDS = VDD / 3;
8 OTA.M5.gm_ID = 10;
9
10 OTA.M5.ID_W = look_up(nch, 'ID_W', 'GM_ID', OTA.M5.gm_ID, ...
11 | | | | | 'VDS', OTA.M5.VDS, 'L', OTA.M5.L);
12 OTA.M5.W = OTA.M5.ID / OTA.M5.ID_W;
13
14 % === Common-mode Input Bias ===
15 % Get VGS from gm/ID
16 %OTA.M1.VGS = look_up(nch, 'VGS', 'GM_ID', OTA.M1.gm_ID, ...
17 | % 'VDS', OTA.M1.VDS, 'L', OTA.M1.L);
18
19 vgs_vec = nch.VGS;
20 gm_id_vec = look_up(nch, 'GM_ID', 'VGS', vgs_vec, ...
21 | | | | | 'VDS', OTA.M1.VDS, 'L', OTA.M1.L);
22 [~, idx] = min(abs(gm_id_vec - OTA.M1.gm_ID));
23 M1.VGS = vgs_vec(idx);
24
25 OTA.M1.VG = M1.VGS + OTA.M5.VDS; % DC common-mode input voltage
26
27 end
28

```

DesignOTATest.m

```

C _designOTA_test.m
4 % === SPECS ===
5 AVDC = 34; % DC gain in dB
6 GBW = 100e6; % Gain-bandwidth product in Hz
7 CL = 500e-15; % Load capacitance in Farads
8
9 % Create specs structure
10 specs = struct('AVDC', AVDC, ...
11 | | | | | 'CL', CL, ...
12 | | | | | 'GBW', GBW);
13
14 % Call the OTA synthesis function
15 OTA = designOTA(specs);
16
17 % === Print the results ===
18 fprintf('**** OTA Design ****\n\n');
19
20 fprintf('Input Differential Pair (M1):\n');
21 fprintf('    L = %.2f um\n', OTA.M1.L);
22 fprintf('    W = %.2f um\n', OTA.M1.W);
23 fprintf('    Bias Current = %.2f uA\n', OTA.M1.ID * 1e6);
24 fprintf('    ViCM = %.4f V\n\n', OTA.M1.VG);
25
26 fprintf('Current Mirror Load (M3):\n');
27 fprintf('    L = %.2f um\n', OTA.M3.L);
28 fprintf('    W = %.2f um\n', OTA.M3.W);
29 fprintf('    Bias Current = %.2f uA\n', OTA.M3.ID * 1e6);
30
31
32 fprintf('Tail Current Source (M5):\n');
33 fprintf('    L = %.2f um\n', OTA.M5.L);
34 fprintf('    W = %.2f um\n', OTA.M5.W);
35 fprintf('    Tail Bias Current = %.2f uA\n', OTA.M5.ID * 1e6);

```

Matlab results :

```
NEW TO MATLAB? SEE RESOURCES FOR GETTING STARTED.

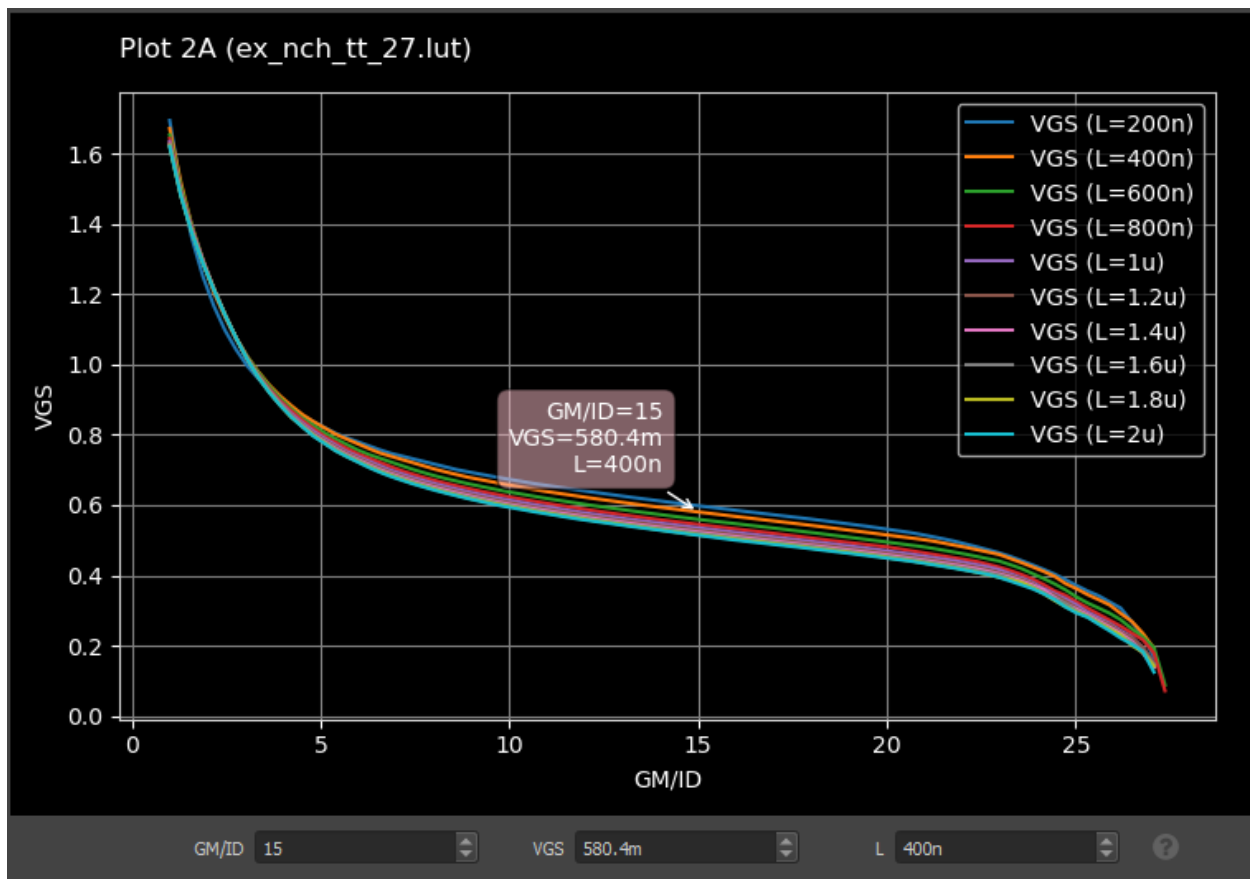
**** OTA Design ****

Input Differential Pair (M1):
  L = 0.34 um
  W = 3.73 um
  Bias Current = 20.94 uA
  ViCM = 1.1750 V

Current Mirror Load (M3):
  L = 0.70 um
  W = 12.09 um
  Bias Current = 20.94 uA

Tail Current Source (M5):
  L = 1.00 um
  W = 9.06 um
  Tail Bias Current = 41.89 uA

fx >>
```



ADT	MATLAB
L1= 0.4 μm	L1= 0.34 μm
W1= 4.3 μm	W1= 3.73 μm
L2 = 0.8 μm	L2 = 0.7 μm
W2 = 13 μm	W2 = 12.09 μm
W3 = 9 μm	W3 = 9.06 μm
I bias = 41.8 μA	I bias = 41.8 μA
VGS = 0.58 V	VGS =0.58 V

7-

Netlist

```

** Circuit Description **

* power supply
VDD 7 0 DC 1.8
* input

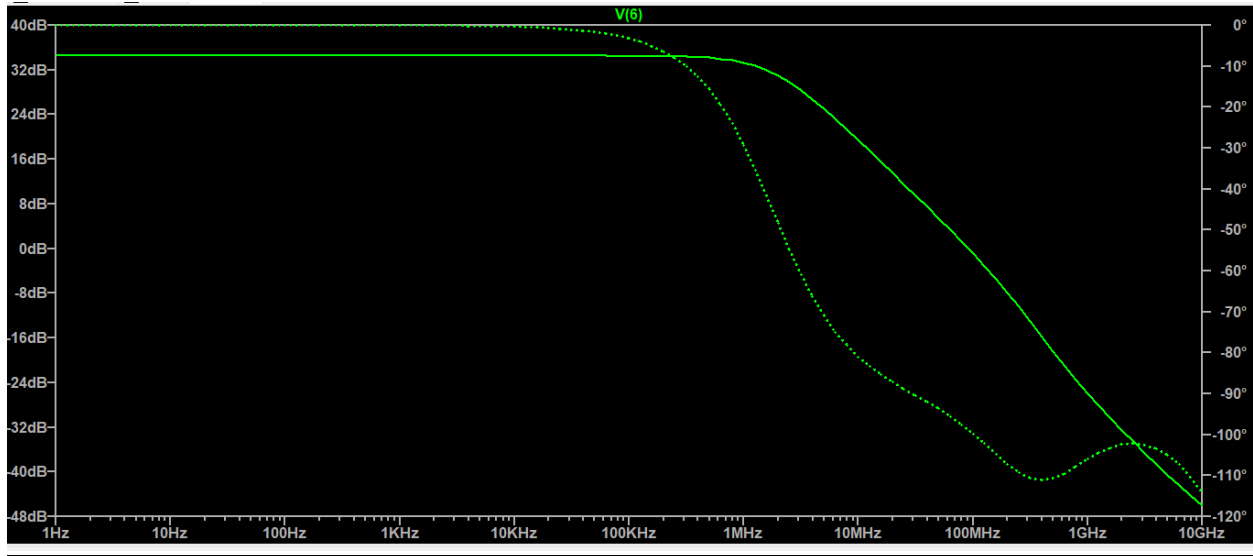
* Add lines here to add the input (voltage) sources
vin1 3 0 DC 1.2 AC 0.5
vin2 4 0 DC 1.2 AC -0.5
* circuit
* 5T OTA
M1 6 4 2 0 nch L=0.4u W=4.2u
M2 5 3 2 0 nch L=0.4u W=4.2u
M3 6 5 7 7 pch L=0.7u W=12u
M4 5 5 7 7 pch L=0.7u W=12u
M5 2 1 0 0 nch L=1u W=9u
CL 6 0 500f
* Current Mirror
M6 1 1 0 0 nch L=1u W=9u
Iref 7 1 41.8u

** Analysis Requests **
.op
.ac dec 10 1 10e9

** Outputs Requests **
*.PROBE
.MEAS AC dc_gain FIND mag(V(6)) AT=1
.MEAS AC gbw WHEN mag(V(6))=1

.END

```



```
dc_gain: mag(V(6))=(34.5071740082dB,0°) at 1
gbw: mag(V(6))=1 AT 92099007.6439
```

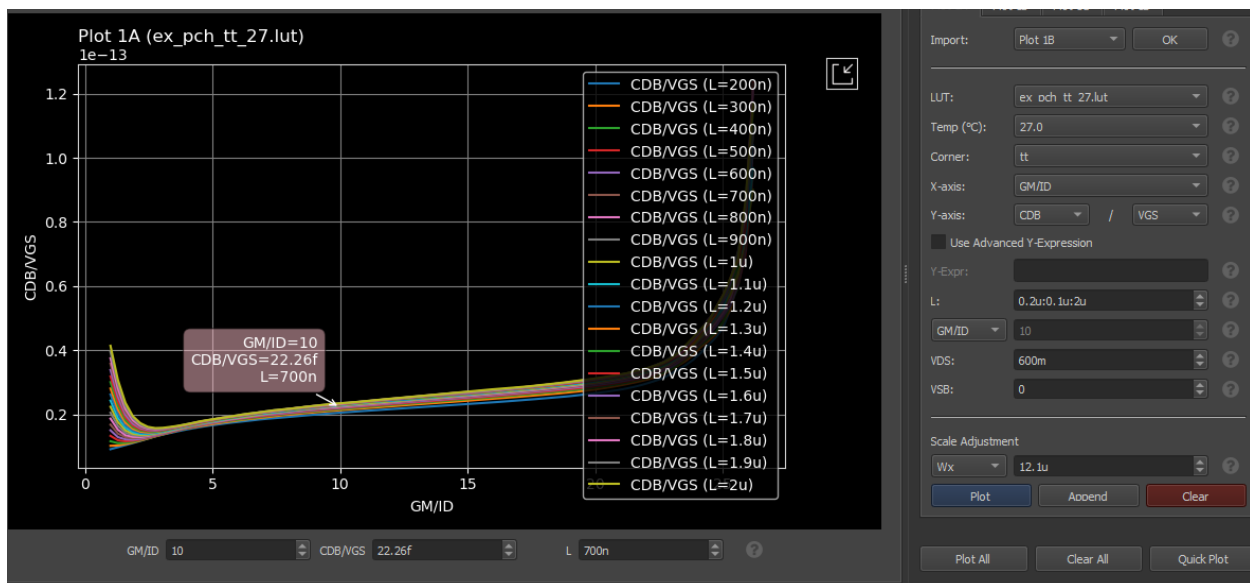
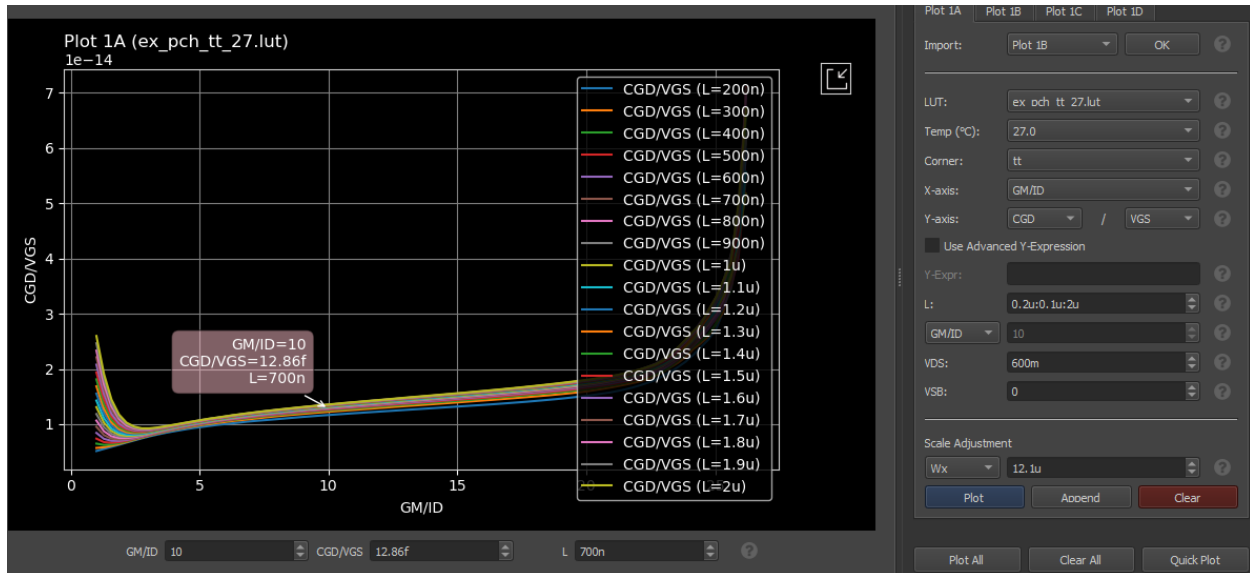
Specs	LTSpice
DC Gain = 34dB	DC Gain = 34.5dB
GBW = 1MHz	GBW = 9.2MHz

The simulator output of our design is nearly acheiving specs but not so accurate as we are ignoring the effect of VDS , self loading and body effect that can make the design more realistic .

Part 2:

To add self loading effect :

$$CDD = CGD + CDB$$



To get CDB and CGD we assume from part 1 that for the load PMOS

VGS= 0.58 V , L = 0.7 μ m , W =12.1 μ m , VDS=0.6 V , GM/ID =10

We get CGD= 7.5 Ff , CDB = 12.9 ff

So CDD = = 7.5 + 12.9 = 20.4 ff

We add CDD to CL and do the analysis again.

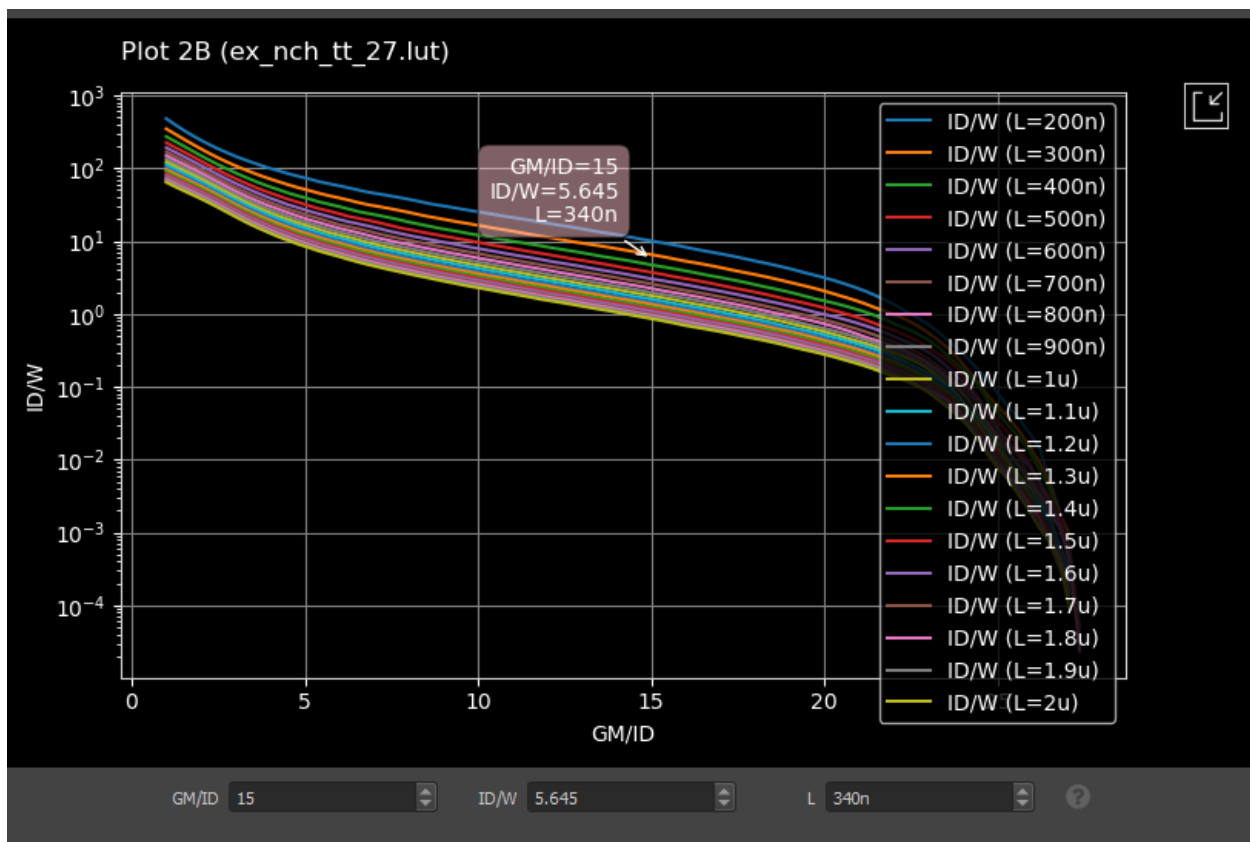
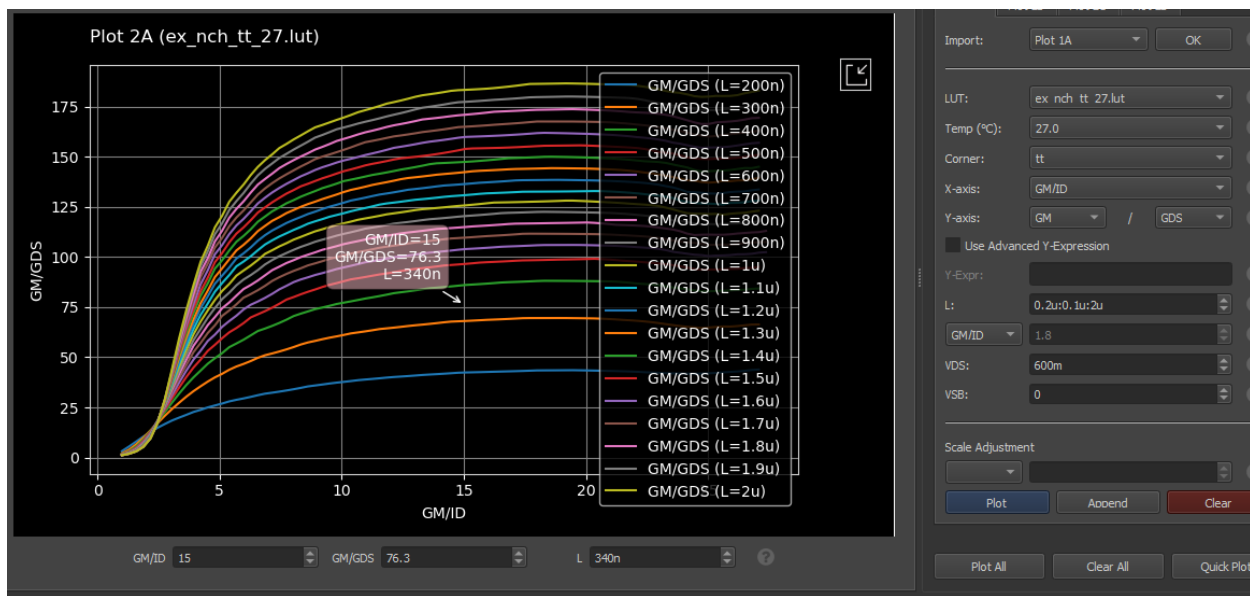
Input pair design:

Step 1

$$C_{L\text{total}} = C_1 + C_{DD}$$
$$g_m = 2\pi \text{GBW} C_{L\text{total}} = 3,26 \times 10^{-4} \text{ S}$$
$$I_D = 2,7 \text{ } \mu\text{A}$$
$$g_{ds} = \frac{1}{r_o} = \frac{2}{3} \times \frac{g_m}{A_V} = 4,346 \text{ } \mu\text{S}$$
$$\frac{g_m}{g_{ds}} = 75$$

\therefore From charts $L = 0,34 \text{ } \mu\text{m}$

$$\frac{I_D}{W} : 5,645 \quad \therefore W = 3,84 \text{ } \mu\text{m}$$



Load design:

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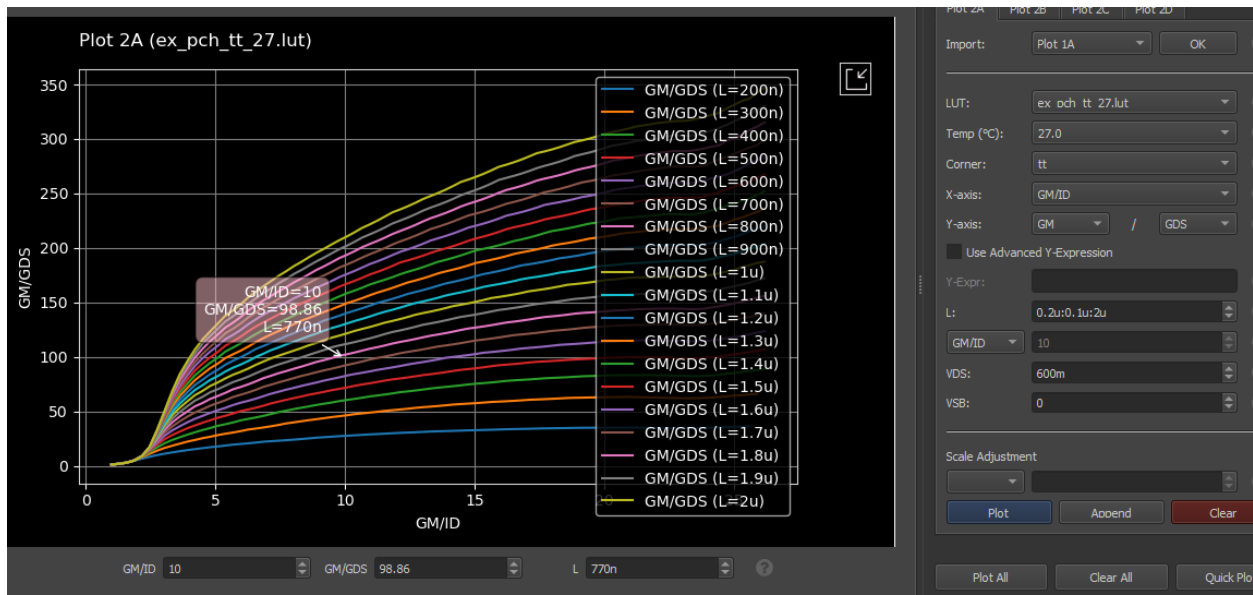
Step 2

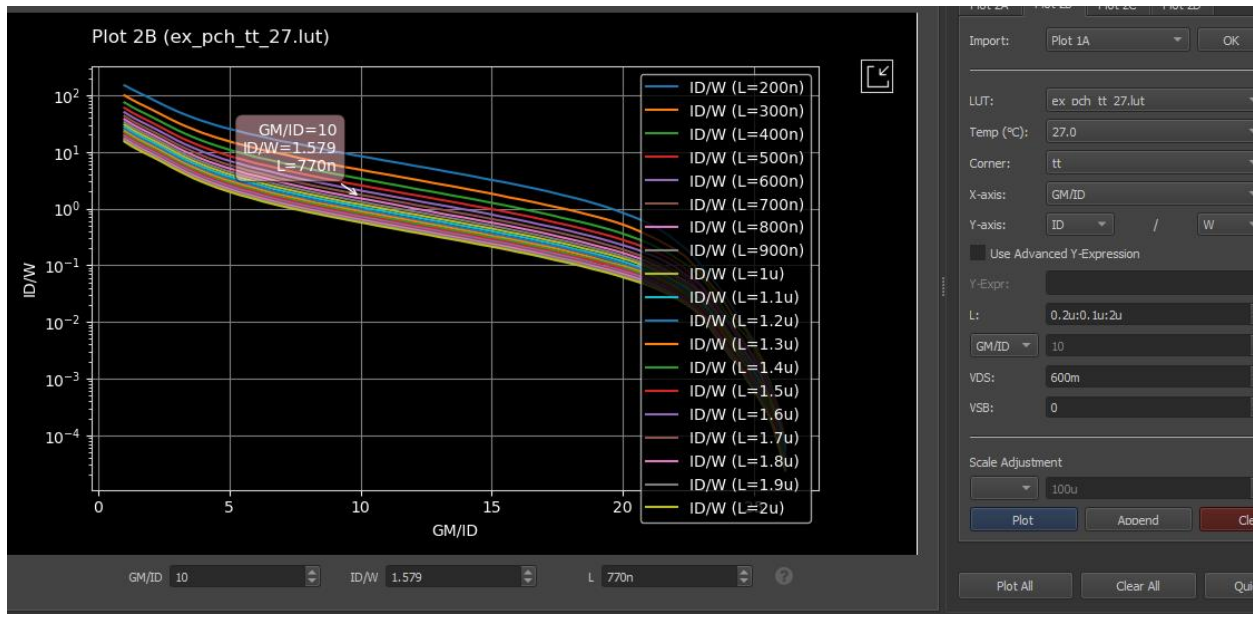
$I_{d1} = I_{d2}$, $\frac{g_m}{I_D} = 10$, $g_{d2} = \frac{1}{2g_{d1}}$

$\therefore g_m = 2,17 \times 10^{-4}$, $g_{dS} = 2,173 \text{ MS}$

$\frac{g_m}{g_{dS}} = 99,86$

$\therefore L = 0,77 \text{ } \mu\text{m}$, $W = 13 \text{ } \mu\text{m}$





Tail current mirror design:

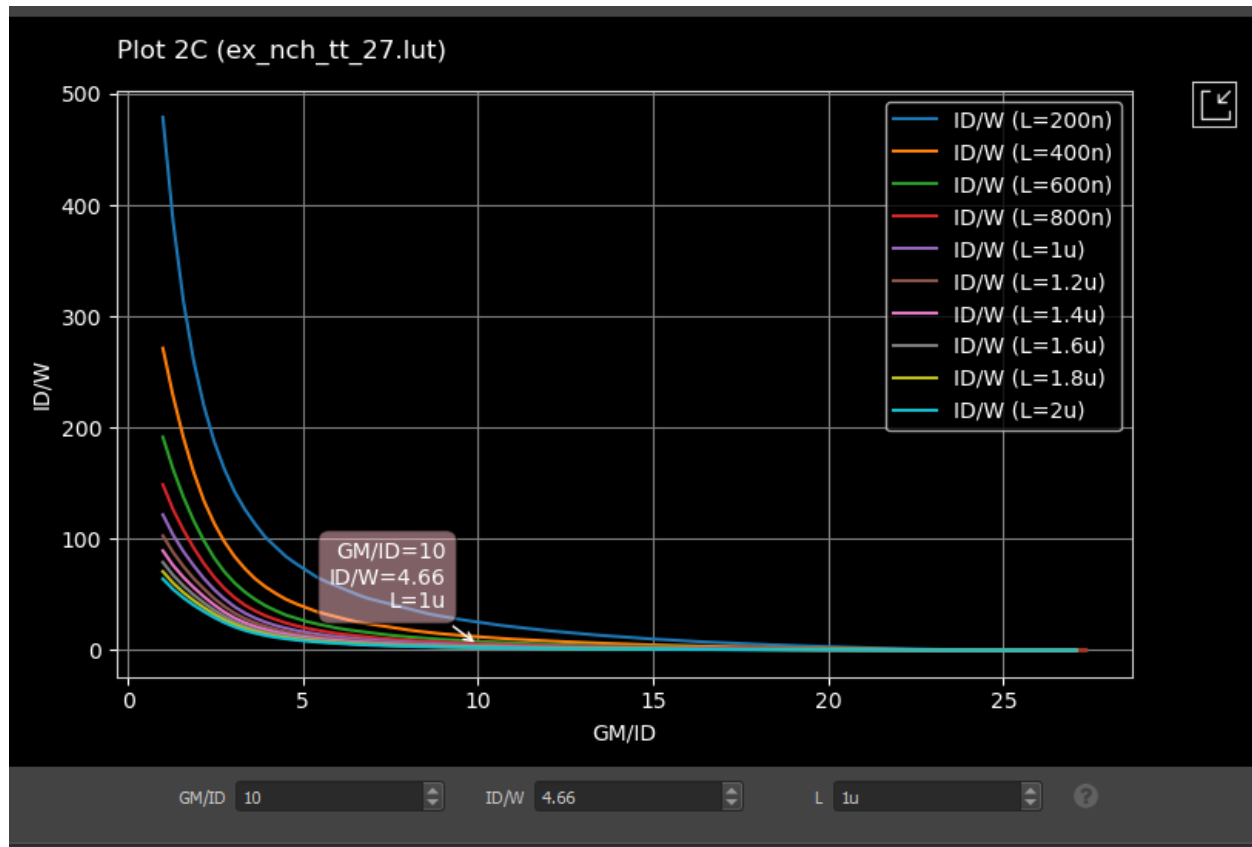
7 am

step 3

$$I_{D3} = 2 I_{D1} = 43,5 \mu A$$

$$\frac{g_m}{I_D} = 10, \quad L = 1 \mu$$

$$W = 9,3 \mu m$$



ADT part 1	ADT part 2
L1= 0.4 um	L1= 0.34 um
W1= 4.3 um	W1= 3.89 um
L2 = 0.8 um	L2 = 0.77 um
W2 = 13 um	W2 = 13 um
W3 = 9 um	W3 = 9.3 um
I bias = 41.8 uA	I bias = 43.5 uA
VGS = 0.58 V	VGS =0.58 V

Matlab function:

```
Cdd_M3 = look_up(pch, 'CDD', 'VGS', 0.58, 'VDS', 0.6, 'L', 0.8);
Cdd_M1 = look_up(nch, 'CDD', 'VGS', 0.58, 'VDS', 0.6, 'L', 0.4);
Cdd_total = Cdd_M3 + Cdd_M1; % One PMOS contributes to output node
CL_total = specs.CL + Cdd_total;
OTA.CL_total = CL_total;
% === Input Pair M1 ===
OTA.M1.gm = specs.GBW * CL_total * 2 * pi;

DC_Gain_mag = 10^(specs.AVDC / 20);
Rout = DC_Gain_mag / OTA.M1.gm;

OTA.M1.ro = (3 / 2) * Rout;
OTA.M1.gds = 1 / OTA.M1.ro;
OTA.M1.VDS = VDD / 3;
OTA.M1.gm_gds = OTA.M1.gm / OTA.M1.gds;
OTA.M1.gm_ID = 15;

OTA.M1.ID = OTA.M1.gm / OTA.M1.gm_ID;
```

```
43 DC_Gain_mag = 10^(specs.AVDC / 20);
44 Rout = DC_Gain_mag / OTA.M1.gm;
45
46 OTA.M1.ro = (3 / 2) * Rout;
47 OTA.M1.gds = 1 / OTA.M1.ro;
48 OTA.M1.VDS = VDD / 3;
49 OTA.M1.gm_gds = OTA.M1.gm / OTA.M1.gds;
50 OTA.M1.gm_ID = 15;
51
52 OTA.M1.ID = OTA.M1.gm / OTA.M1.gm_ID;
53
54 % Find minimum L meeting gm/gds
55 gm_gds_vector = look_up(nch, 'GM_GDS', 'GM_ID', OTA.M1.gm_ID, ...
56 | | | | | 'VDS', OTA.M1.VDS, 'L', L_vector);
57 OTA.M1.L = min(L_vector(gm_gds_vector >= OTA.M1.gm_gds));
58 OTA.M1.ID_W = look_up(nch, 'ID_W', 'GM_ID', OTA.M1.gm_ID, ...
59 | | | | | 'VDS', OTA.M1.VDS, 'L', OTA.M1.L);
60 OTA.M1.W = OTA.M1.ID / OTA.M1.ID_W;
61
62 % === M3 Load (PMOS diode-connected) ===
63 OTA.M3.ID = OTA.M1.ID;
64 OTA.M3.VDS = VDS_M3;
65 OTA.M3.gm_ID = gm_ID_M3;
66 OTA.M3.gm = OTA.M3.gm_ID * OTA.M3.ID;
67 OTA.M3.ro = 2 * OTA.M1.ro;
68 OTA.M3.gds = 1 / OTA.M3.ro;
69 OTA.M3.gm_gds = OTA.M3.gm / OTA.M3.gds;
```

```

gm_gds_vector = look_up(pch, 'GM_GDS', 'GM_ID', OTA.M3.gm_ID, ...
                        'VDS', OTA.M3.VDS, 'L', L_vector);
OTA.M3.L = min(L_vector(gm_gds_vector > OTA.M3.gm_gds));
OTA.M3.ID_W = look_up(pch, 'ID_W', 'GM_ID', OTA.M3.gm_ID, ...
                    'VDS', OTA.M3.VDS, 'L', OTA.M3.L);
OTA.M3.W = OTA.M3.ID / OTA.M3.ID_W;

% === Tail Transistor M5 ===
OTA.M5.L = 1;
OTA.M5.ID = 2 * OTA.M1.ID;
OTA.M5.VDS = VDD / 3;
OTA.M5.gm_ID = 10;
OTA.M5.ID_W = look_up(nch, 'ID_W', 'GM_ID', OTA.M5.gm_ID, ...
                    'VDS', OTA.M5.VDS, 'L', OTA.M5.L);
OTA.M5.W = OTA.M5.ID / OTA.M5.ID_W;

% === VGS and Common-mode bias ===
vgs_vec = nch.VGS;
gm_id_vec = look_up(nch, 'GM_ID', 'VGS', vgs_vec, ...
                    'VDS', OTA.M1.VDS, 'L', OTA.M1.L);
[~, idx] = min(abs(gm_id_vec - OTA.M1.gm_ID));
OTA.M1.VGS = vgs_vec(idx);
OTA.M1.VG = OTA.M1.VGS + OTA.M5.VDS;

```

results:

```

**** OTA Design ****

Input Differential Pair (M1):
    L = 0.34 um
    W = 3.88 um
    Bias Current = 21.80 uA
    ViCM = 1.1750 V

Current Mirror Load (M3):
    L = 0.70 um
    W = 12.59 um
    Bias Current = 21.80 uA
Tail Current Source (M5):
    L = 1.00 um
    W = 9.43 um
    Tail Bias Current = 43.60 uA

```

 >>

MATLAB part 2	MATLAB part 1
L1= 0.34 um	L1= 0.34 um
W1= 3.88 um	W1= 3.73 um

L2 = 0.7 μm	L2 = 0.7 μm
W2 = 12.59 μm	W2 = 12.09 μm
W3 = 9.43 μm	W3 = 9.06 μm
I bias = 43.6 μA	I bias = 41.8 μA
VGS = 0.58 V	VGS = 0.58 V

ADT	MATLAB
L1= 0.34 μm	L1= 0.34 μm
W1= 3.89 μm	W1= 3.88 μm
L2 = 0.77 μm	L2 = 0.7 μm
W2 = 13 μm	W2 = 12.59 μm
W3 = 9.3 μm	W3 = 9.43 μm
I bias = 43.5 μA	I bias = 43.6 μA
VGS = 0.58 V	VGS = 0.58 V

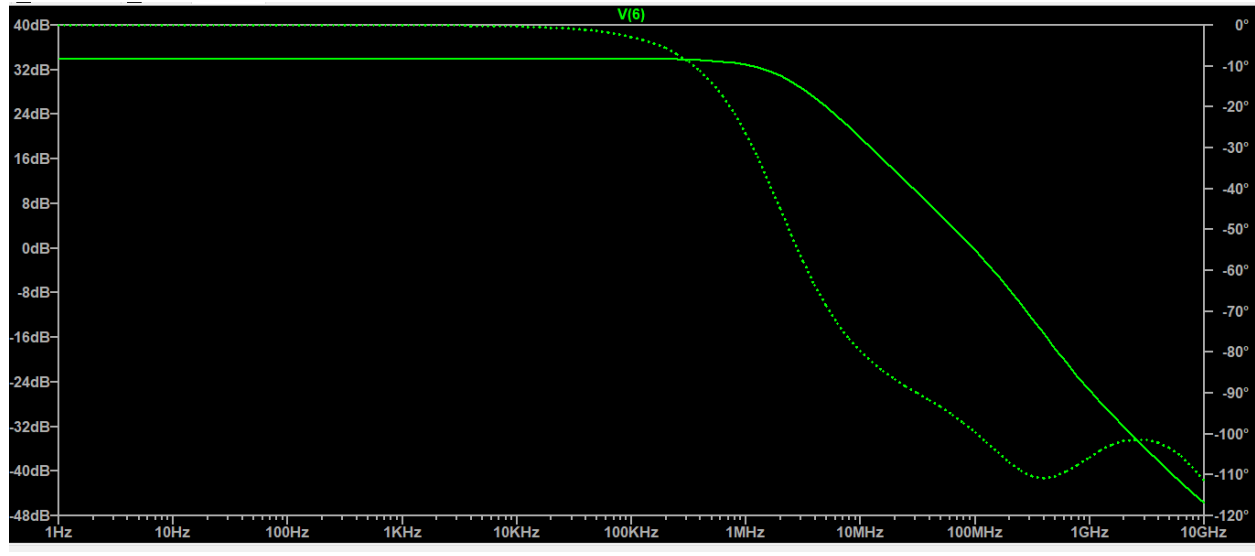
LTSpice:

```

* Add lines here to add the input (voltage) sources
vin1 3 0 DC 1.2 AC 0.5
vin2 4 0 DC 1.2 AC -0.5
* circuit
* 5T OTA
M1 6 4 2 0 nch L=0.34u W=3.9u
M2 5 3 2 0 nch L=0.34u W=3.9u
M3 6 5 7 7 pch L=0.77u W=13u
M4 5 5 7 7 pch L=0.77u W=13u
M5 2 1 0 0 nch L=1u W=9.44u
CL 6 0 500f
* Current Mirror
M6 1 1 0 0 nch L=1u W=9.44u
Iref 7 1 43.65u

** Analysis Requests **
.op
.ac dec 10 1 10e9

```



```
dc_gain: mag(V(6))=(34.0972019245dB,0°) at 1
gbw: mag(V(6))=1 AT 96131037.713
```

Specs	LTSpice
DC Gain = 34dB	DC Gain = 34.09dB
GBW = 1MHz	GBW = 9.6MHz

We can see that the obtained design became more accurate and near to the specs after adding effect of self loading and it could be more accurate if we added effect of body effect and VDS