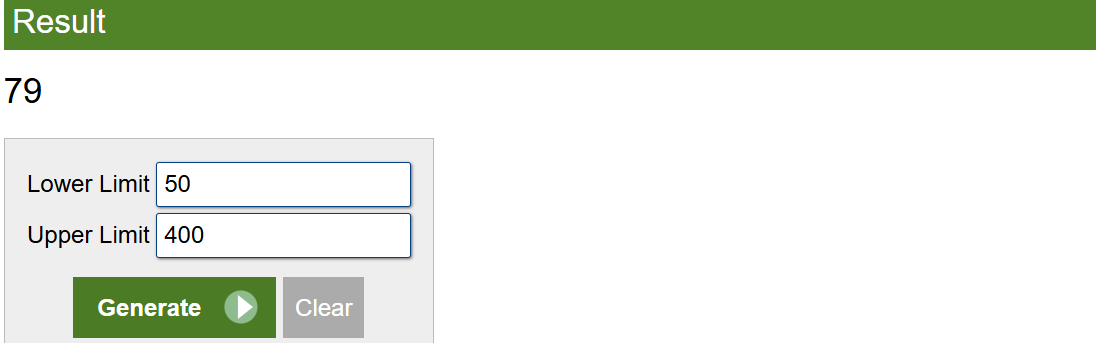
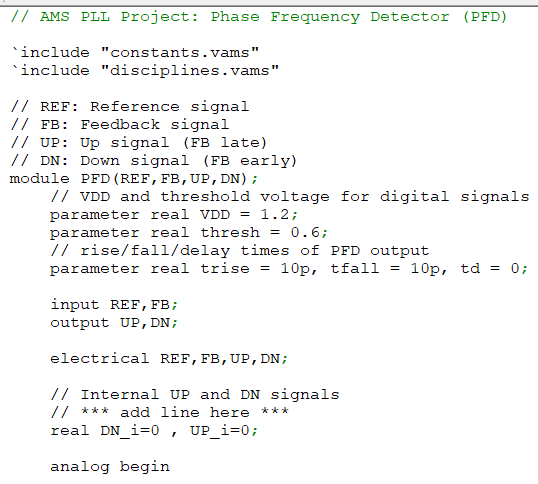
**AMS Course**

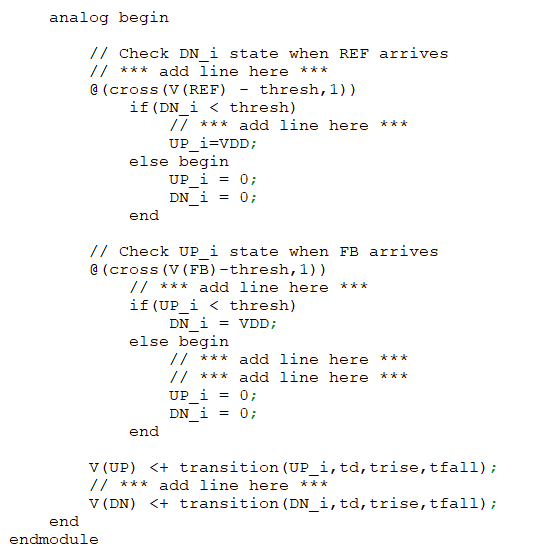
PLL Project

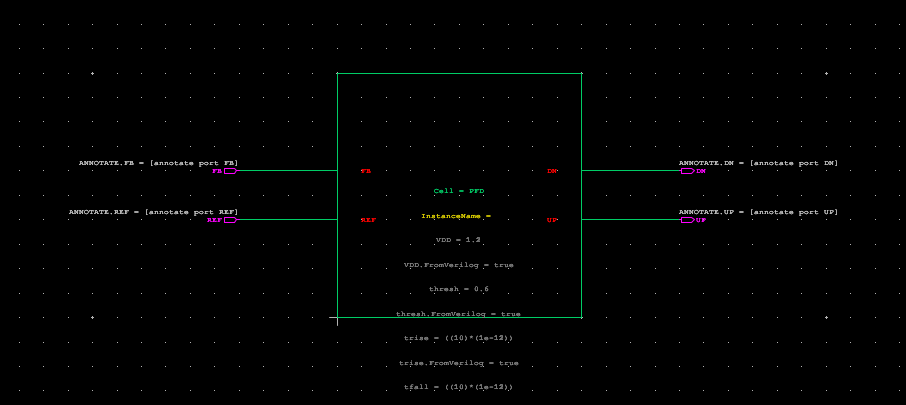


Kvco = 79/100 \*1e9 = 0.79 GHz/V

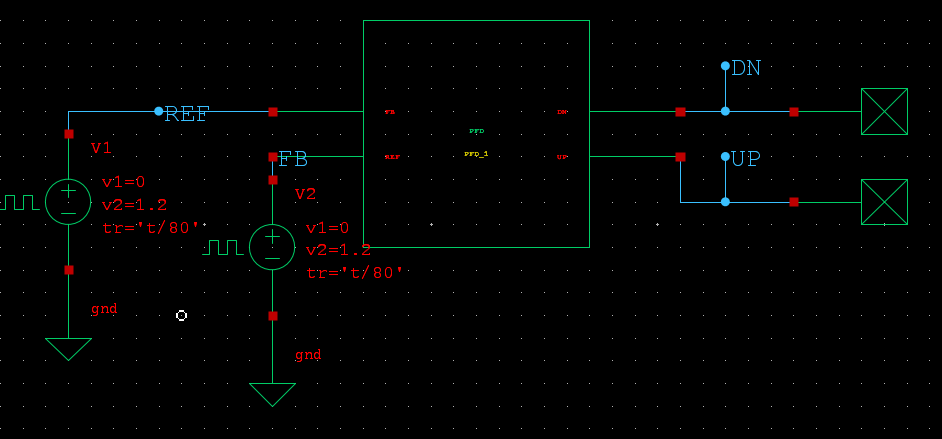
1- PFD Verilog-a model :

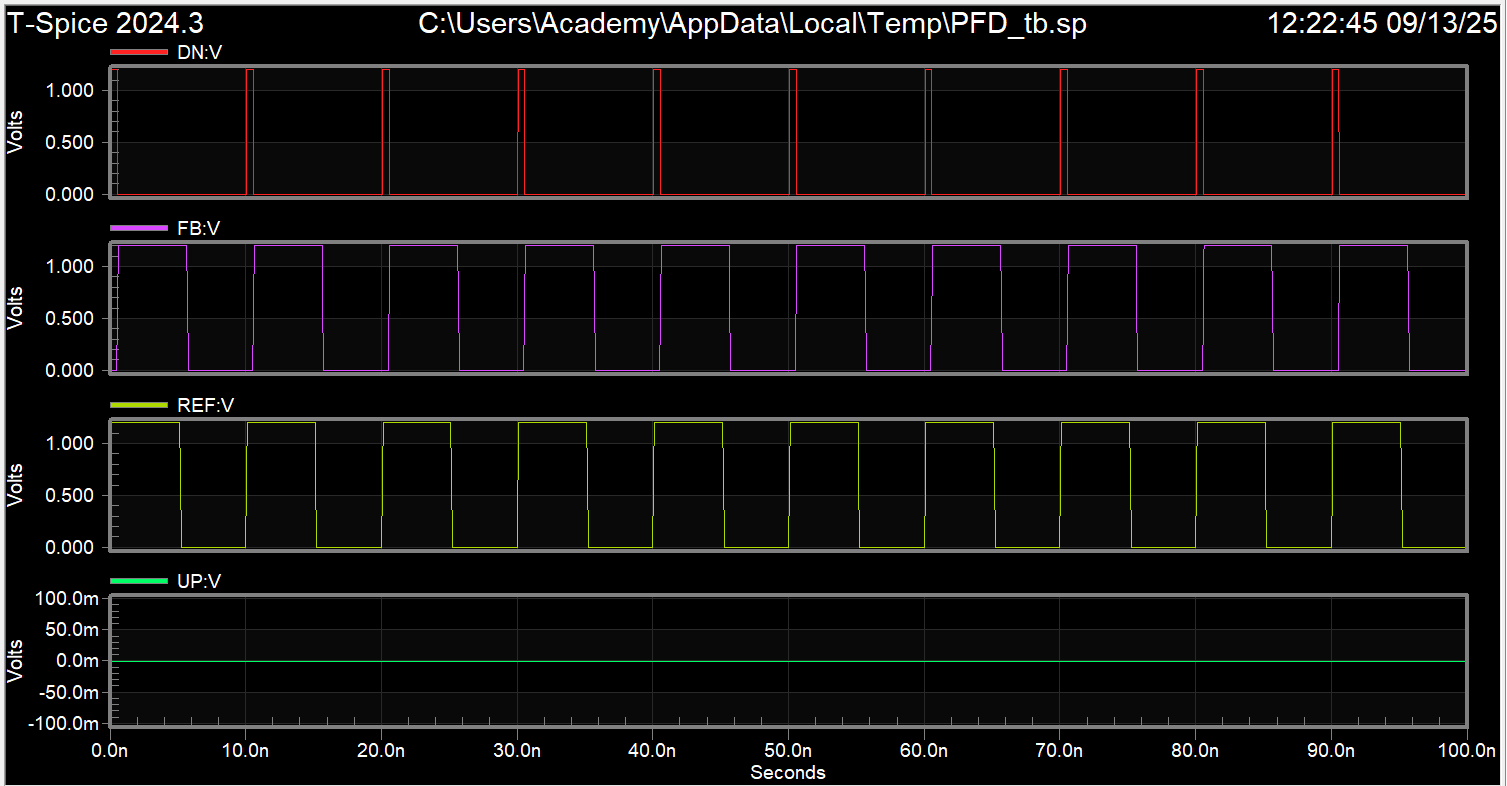




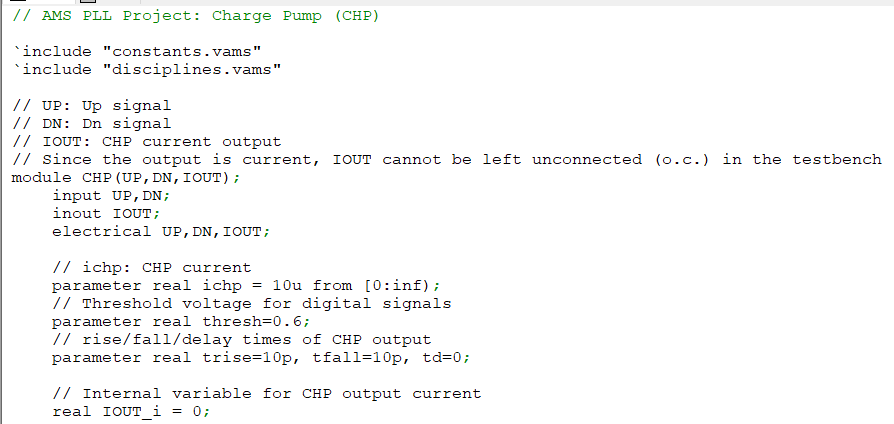


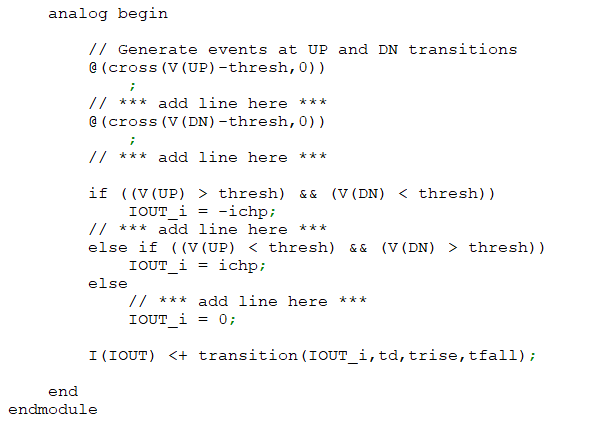
2- PFD testbensh and results:



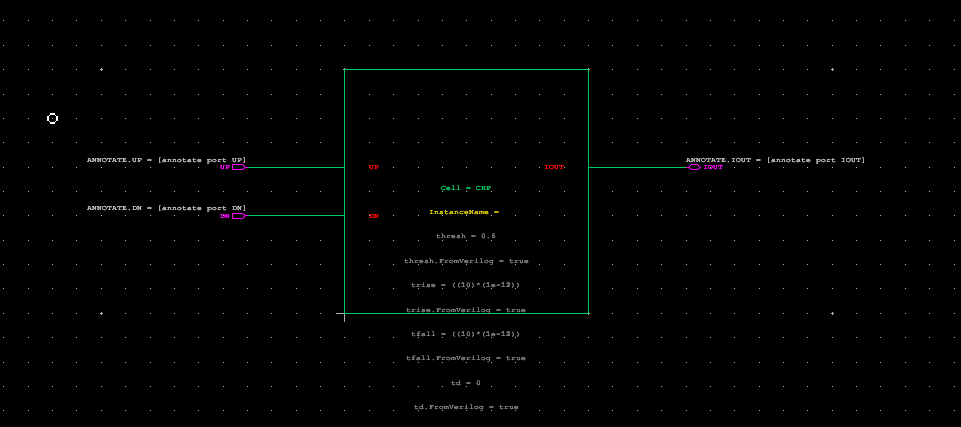


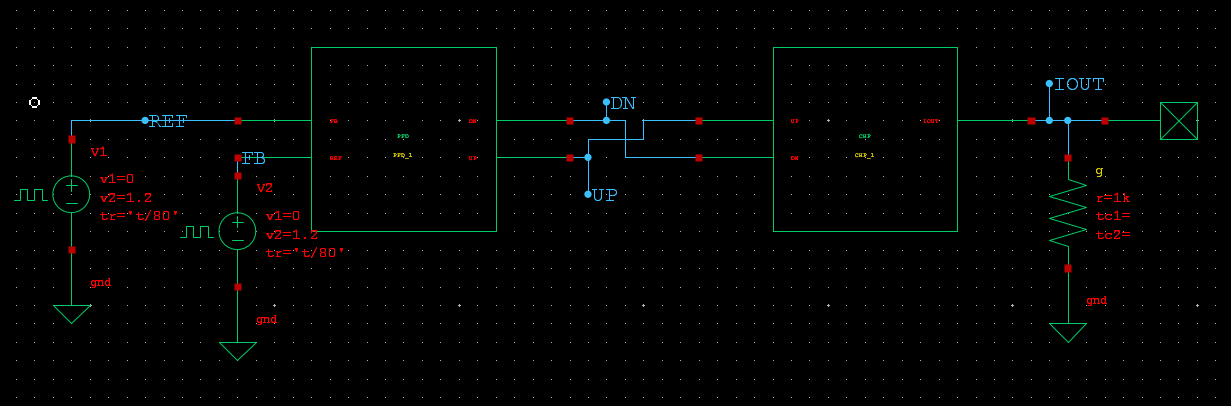
From the charts we can see that we have down pulses due to the leading of REF signal towards the FB signal while the up signal is zero

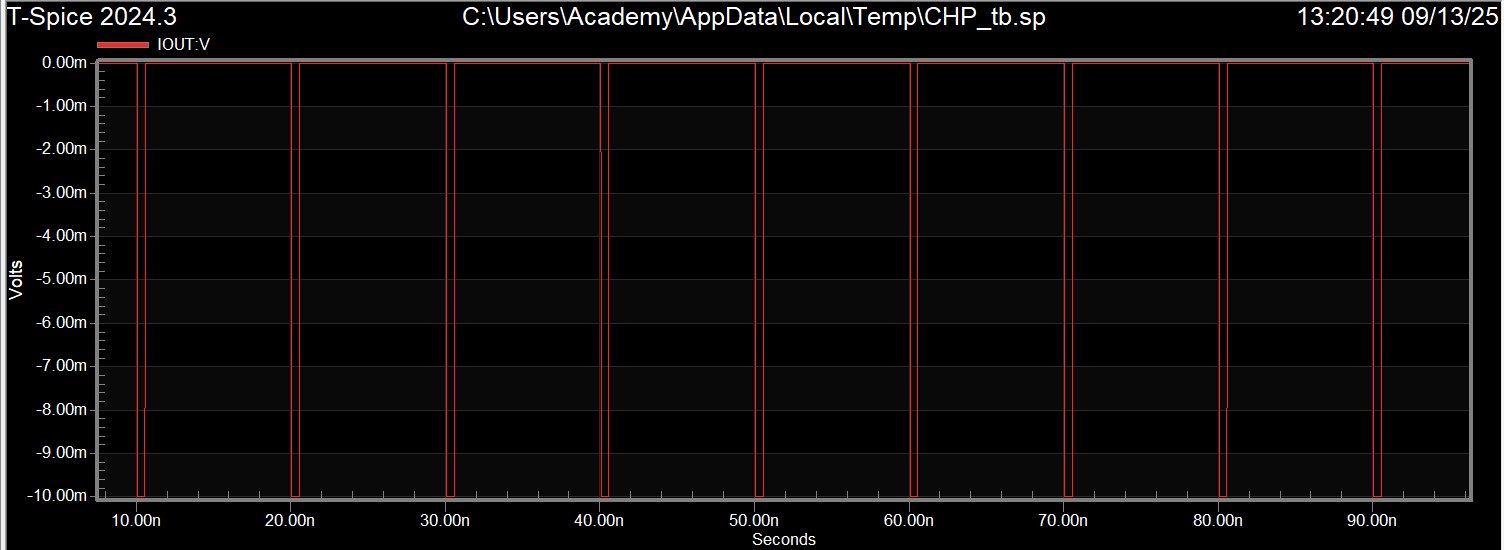
3- CHP Verilog-a model:



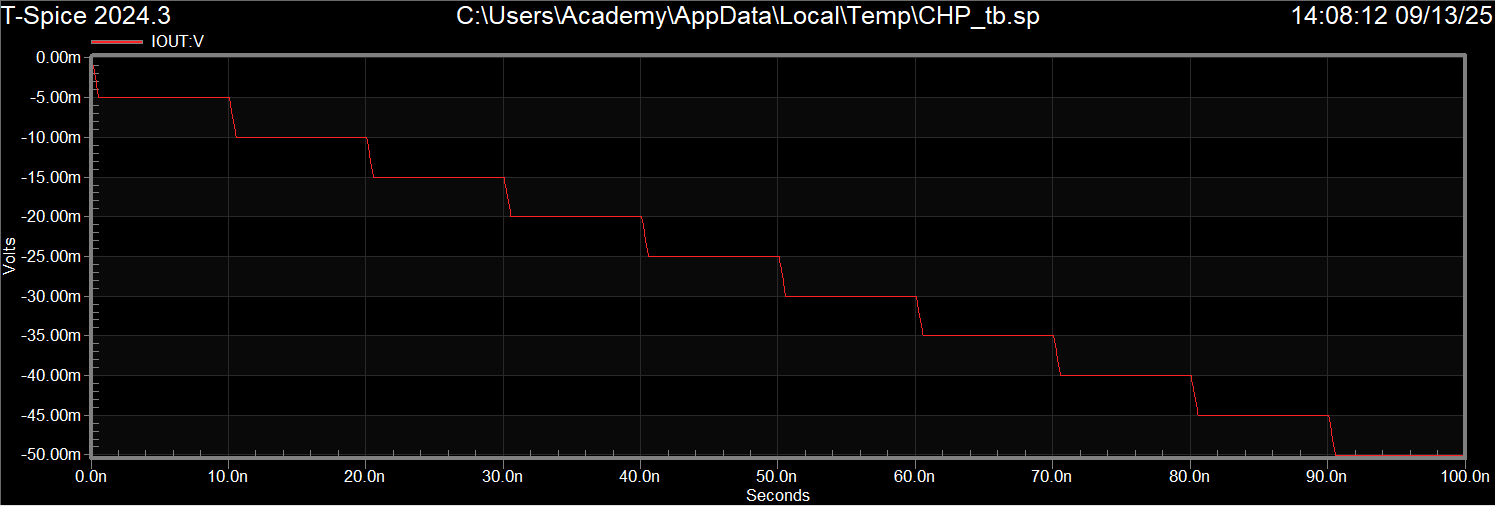
4- CHP testbench and results:







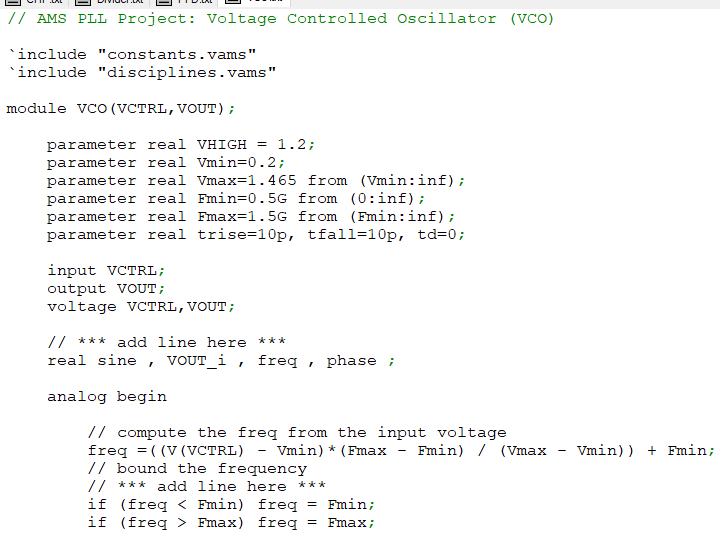
(in case of resistive load )

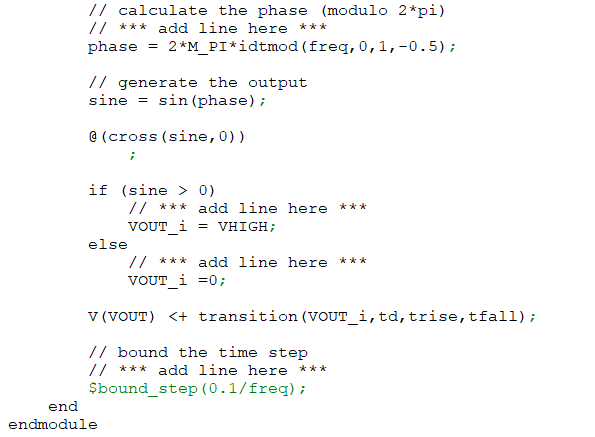


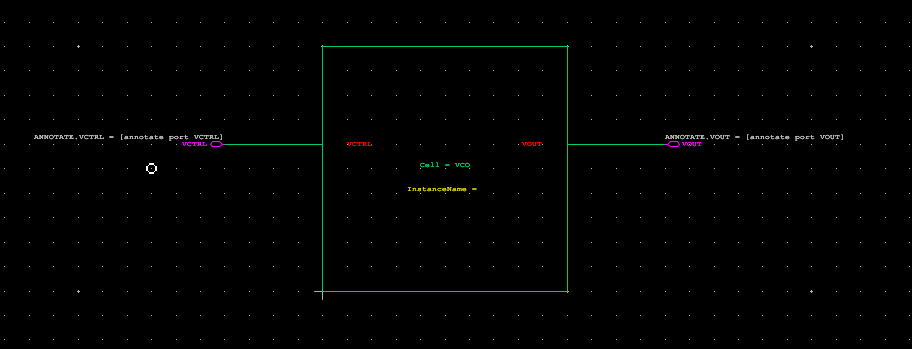
In case of capacitive load

Since feedback leads input voltage , the output current is negative .

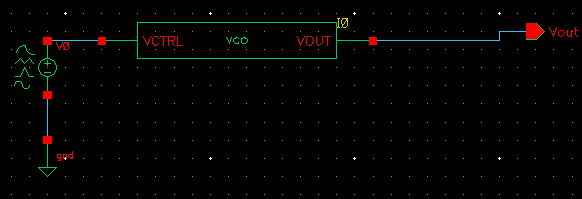
5- VCO Verilog-a model :

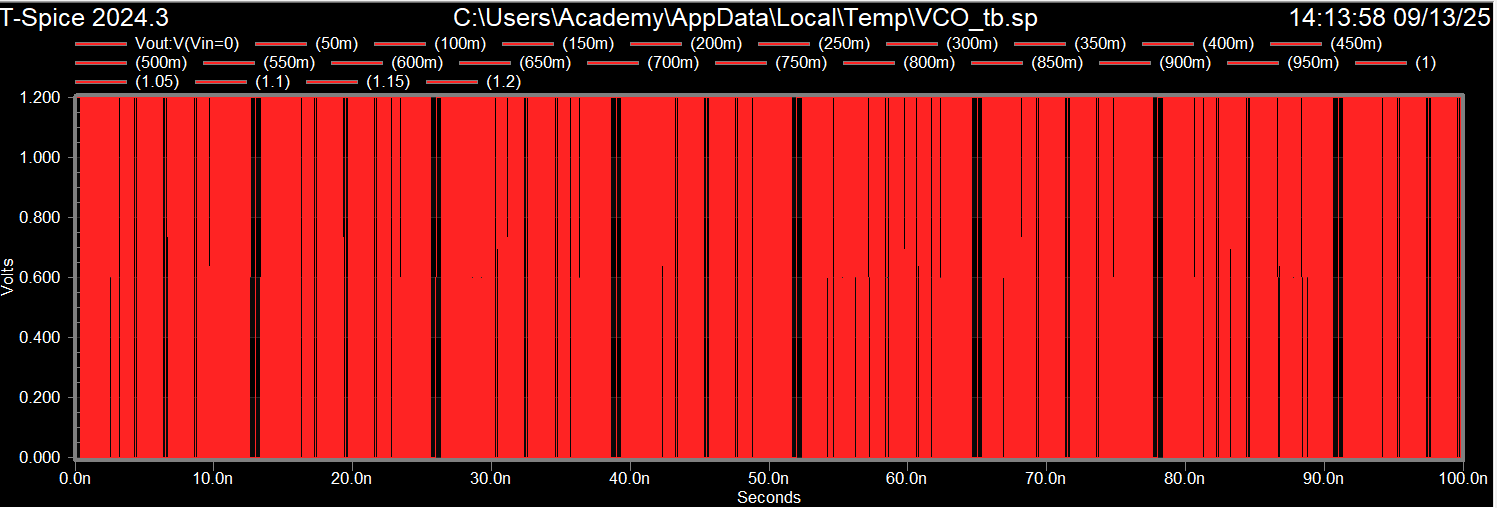


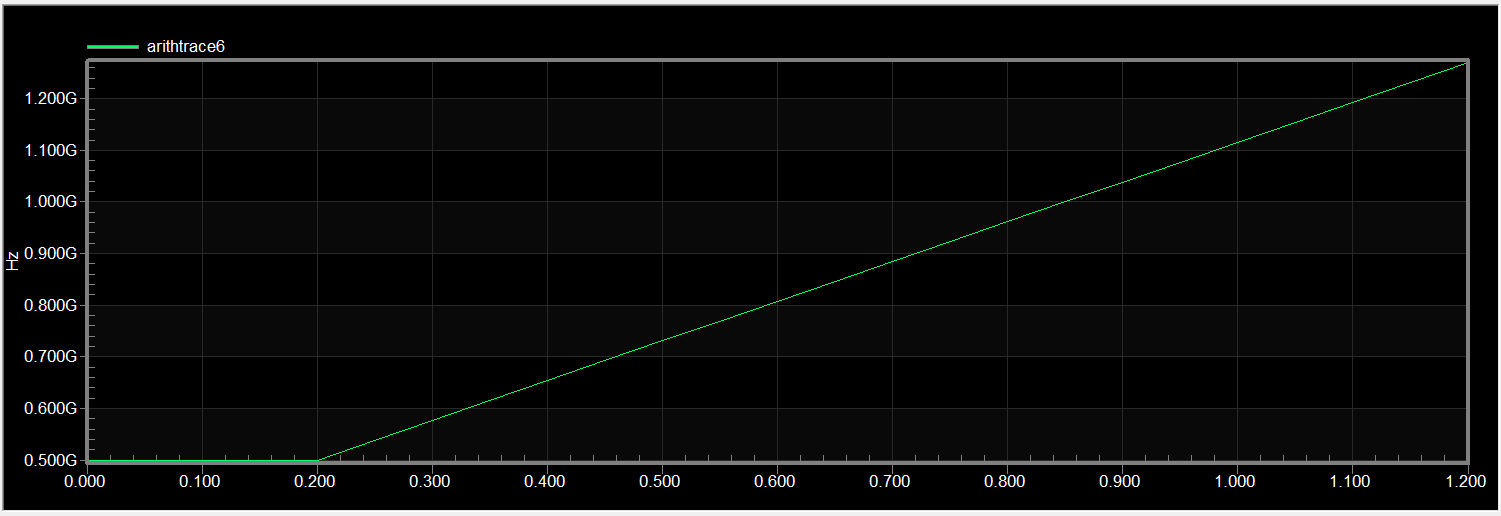


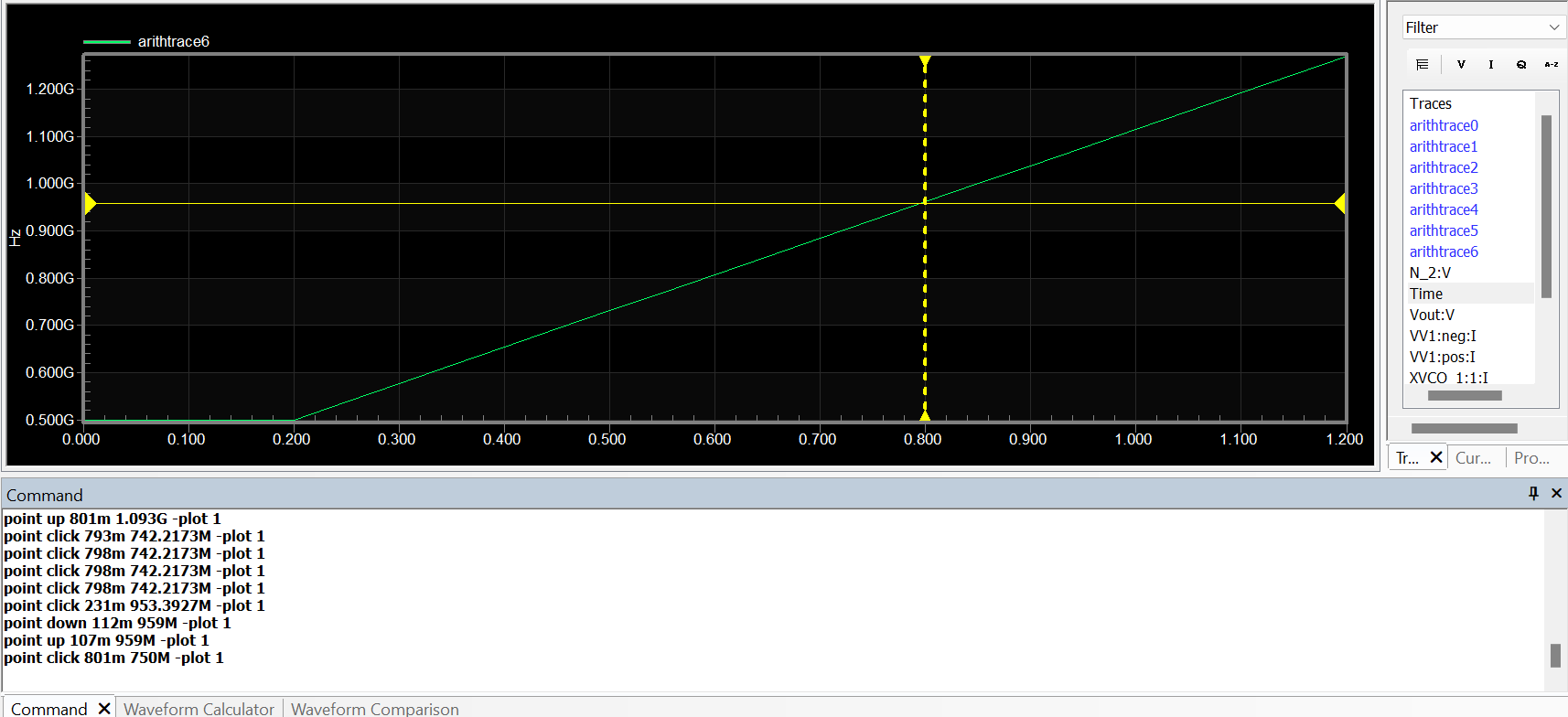


6- VCO testbench and results:



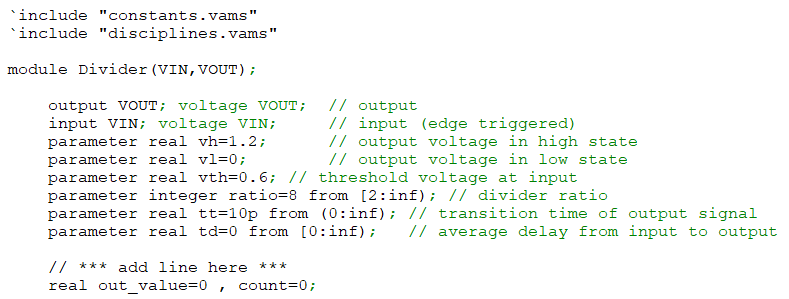


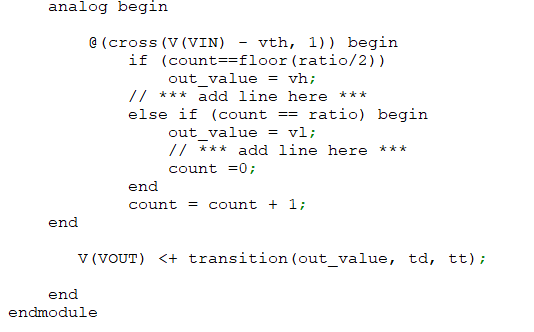




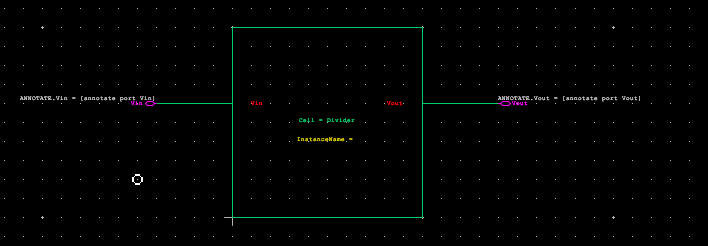
At the desired output frequency (8\*120M = 960 MHz ) , the Vctrl value is nearly 0.79 V

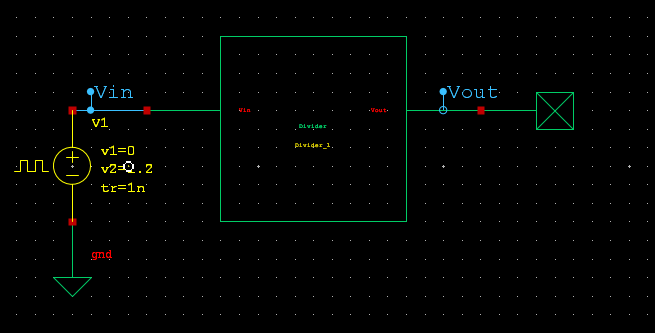
7- DIVIDER Verilog-a model :

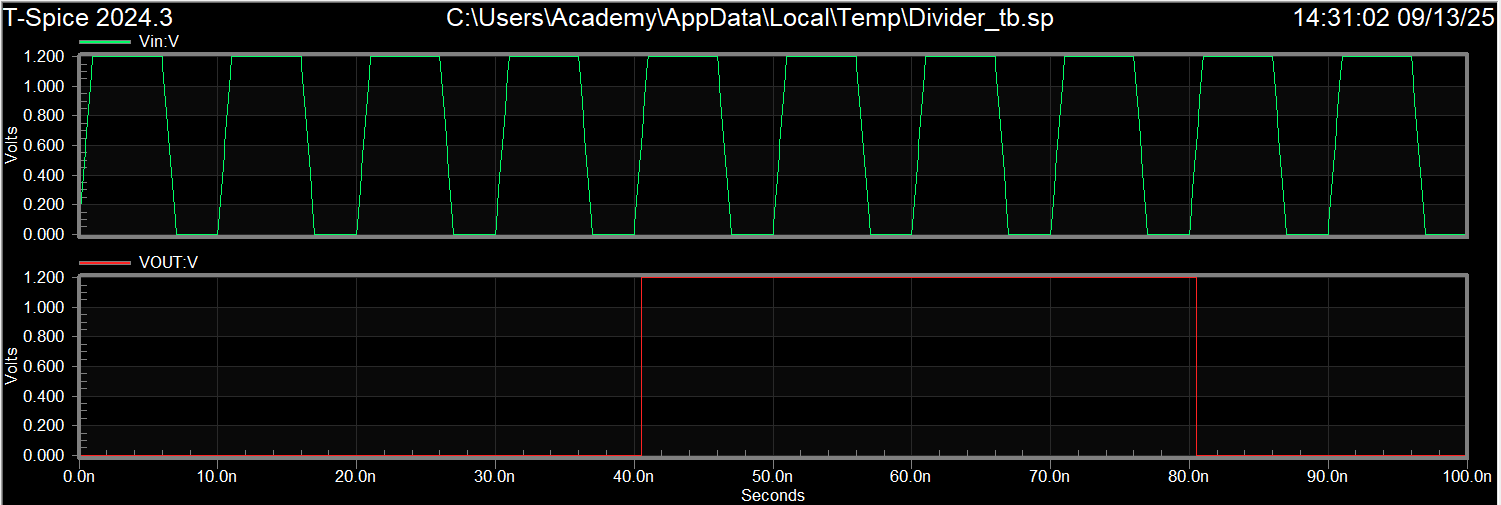




8- Divider testbench and results :

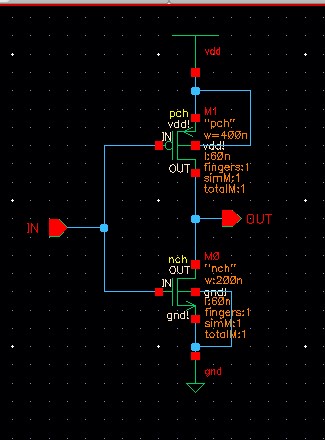




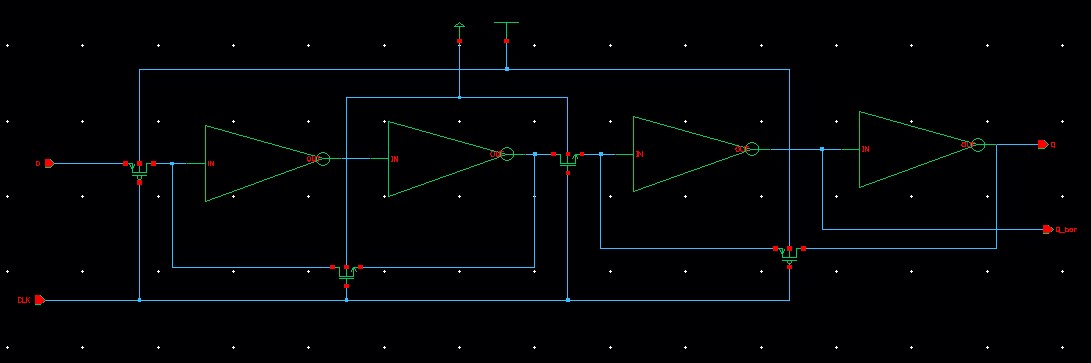


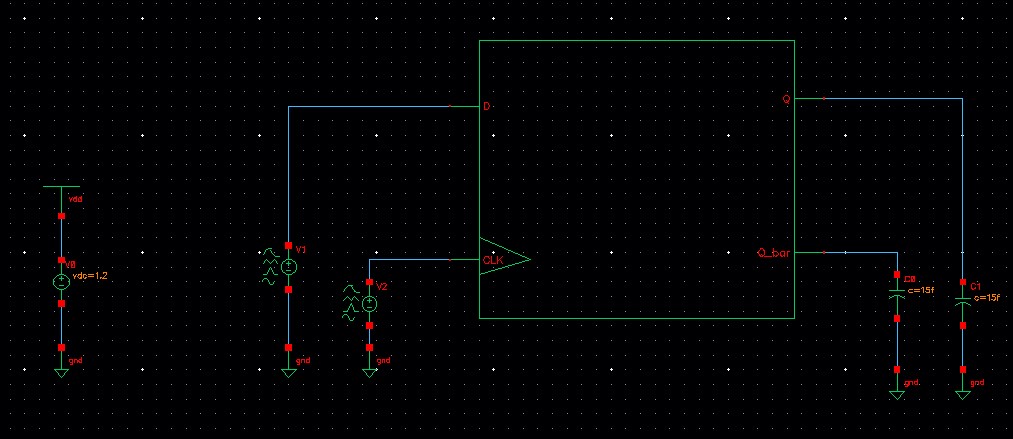
9-

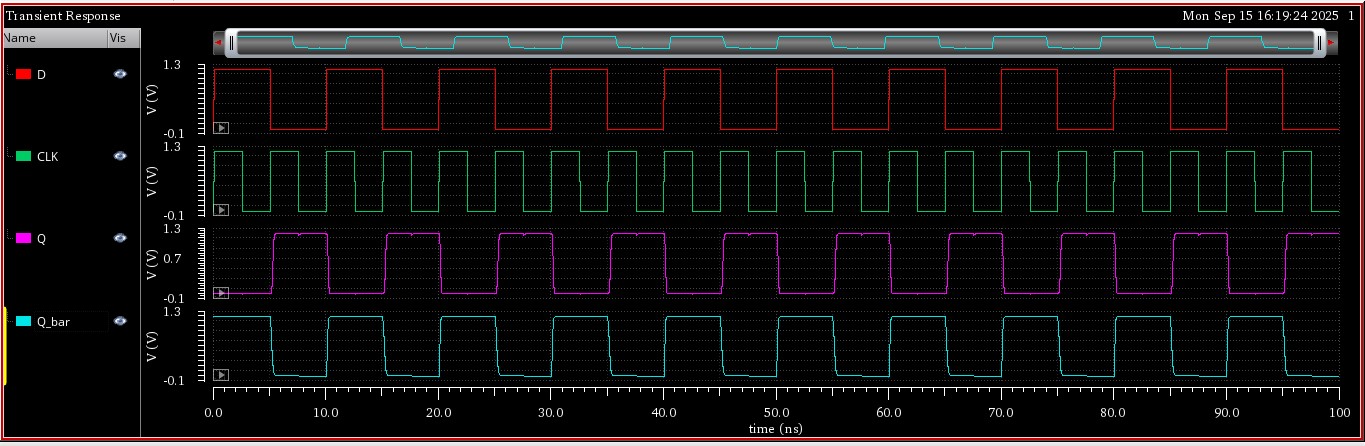
Inverter design



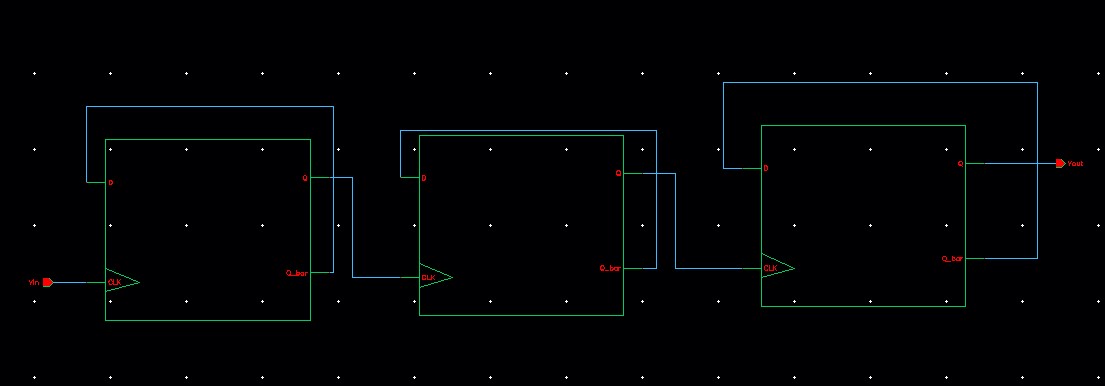
D\_ff design and testbench :

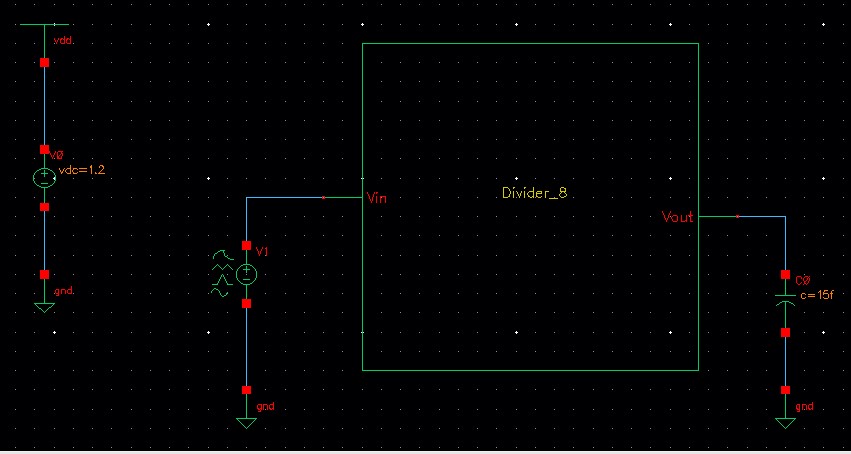


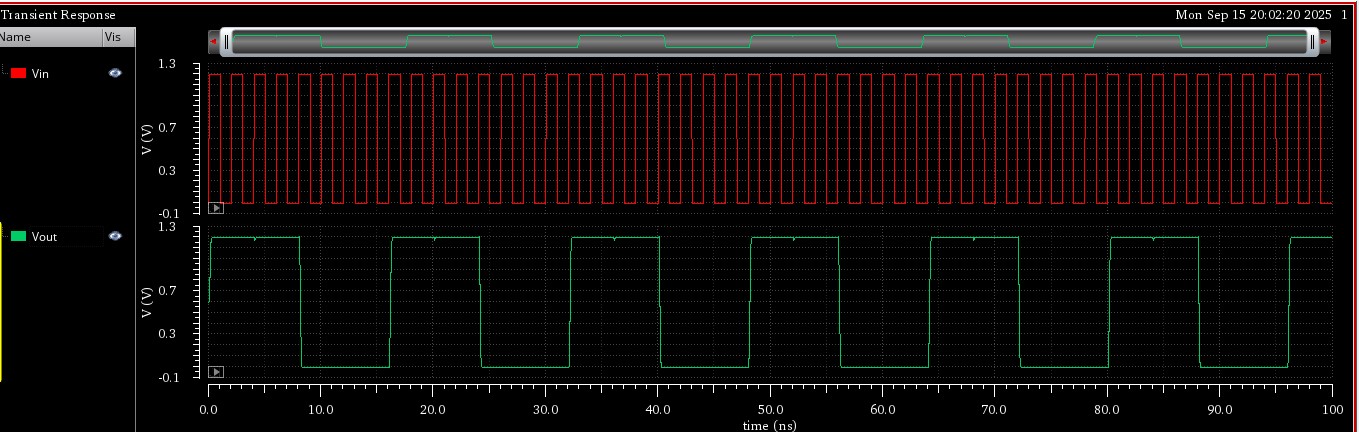




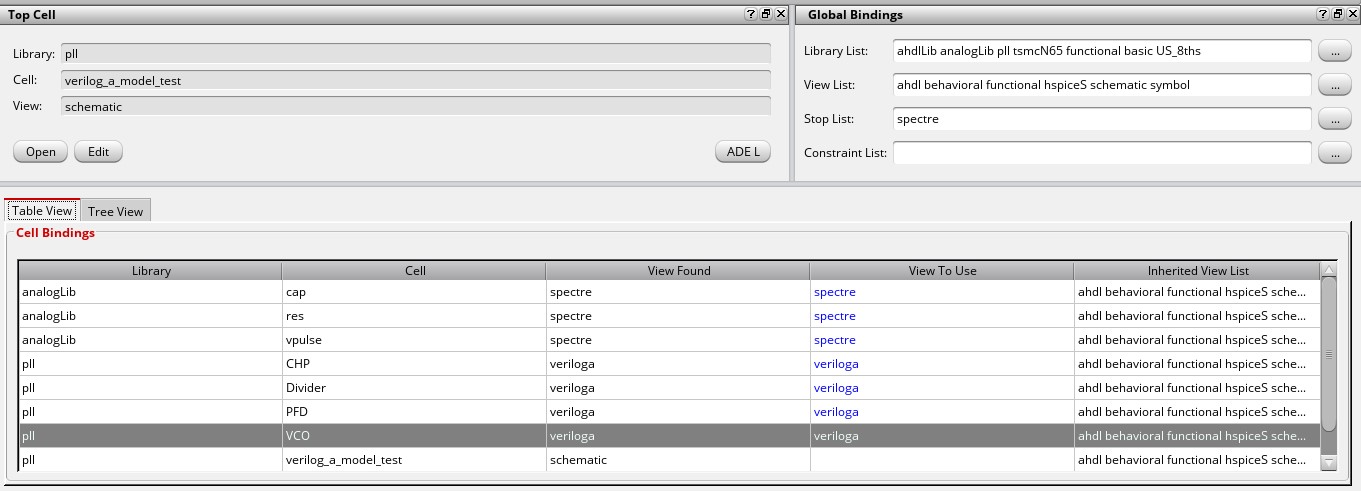
10- transistor level divider design and testbench :

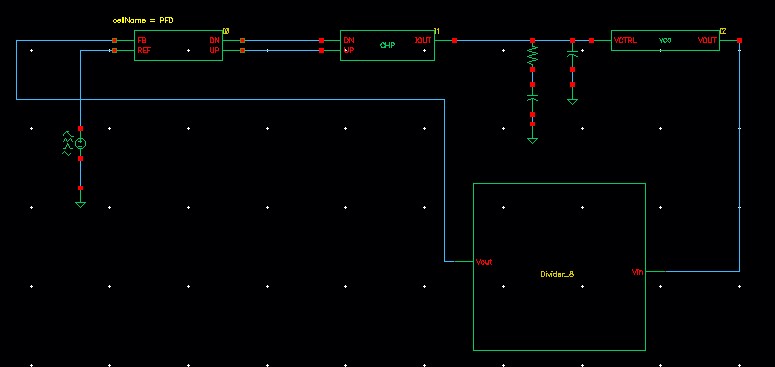


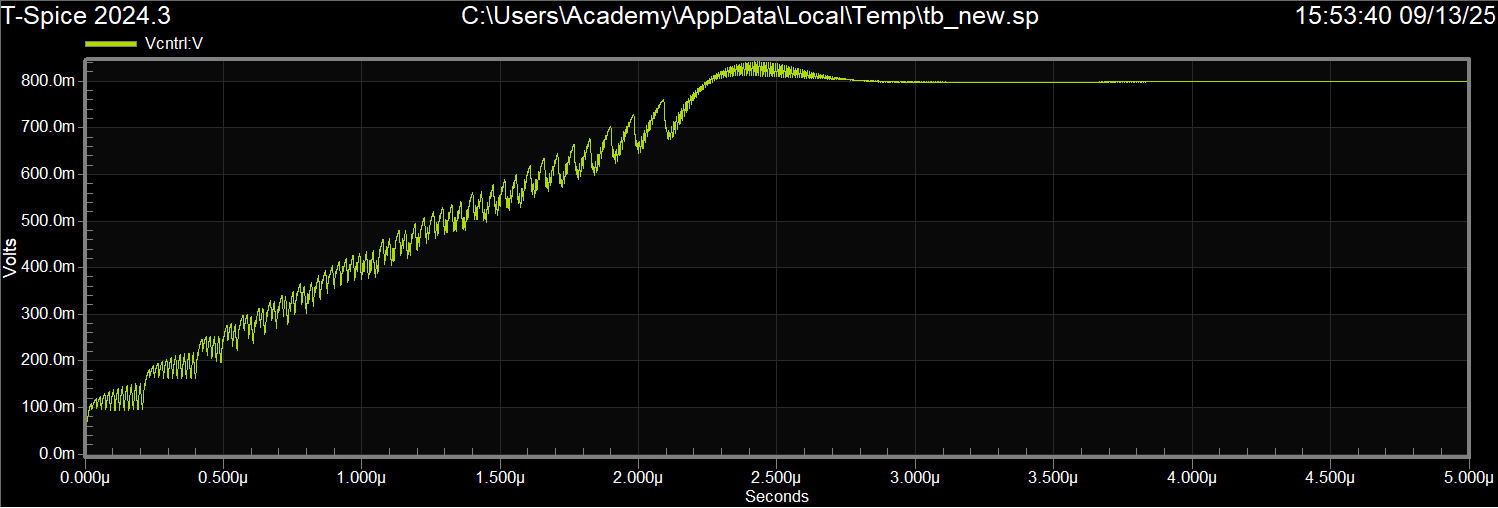


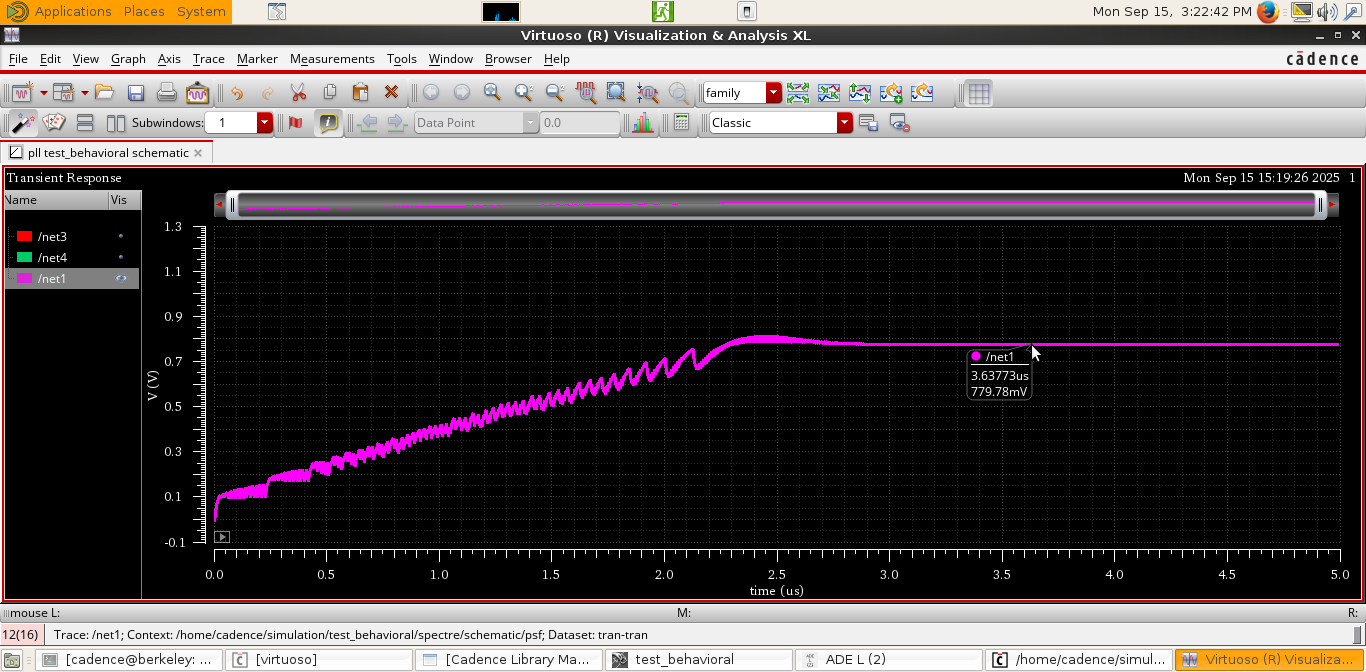


11- pll integration using Verilog\_a models only:









12 – Fout = Kvco \* V + c

For Vmin = 0.2 , Fmin =0.5 GHz , Kvco = 0.79 GHz/V

C= 342e6

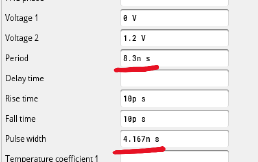
Second substitution when Fout is the required output frequency (960MHz)

960e6 = 0.79 GHz/V \* Vctrl +c

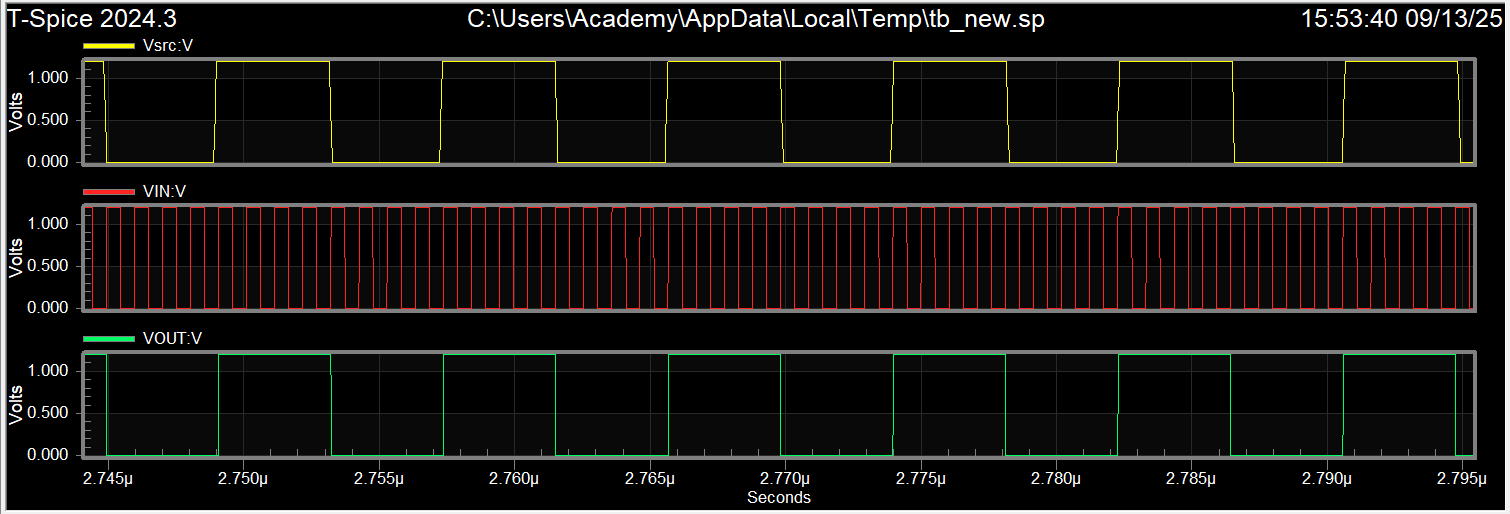
Vctrl = 0.7822 V

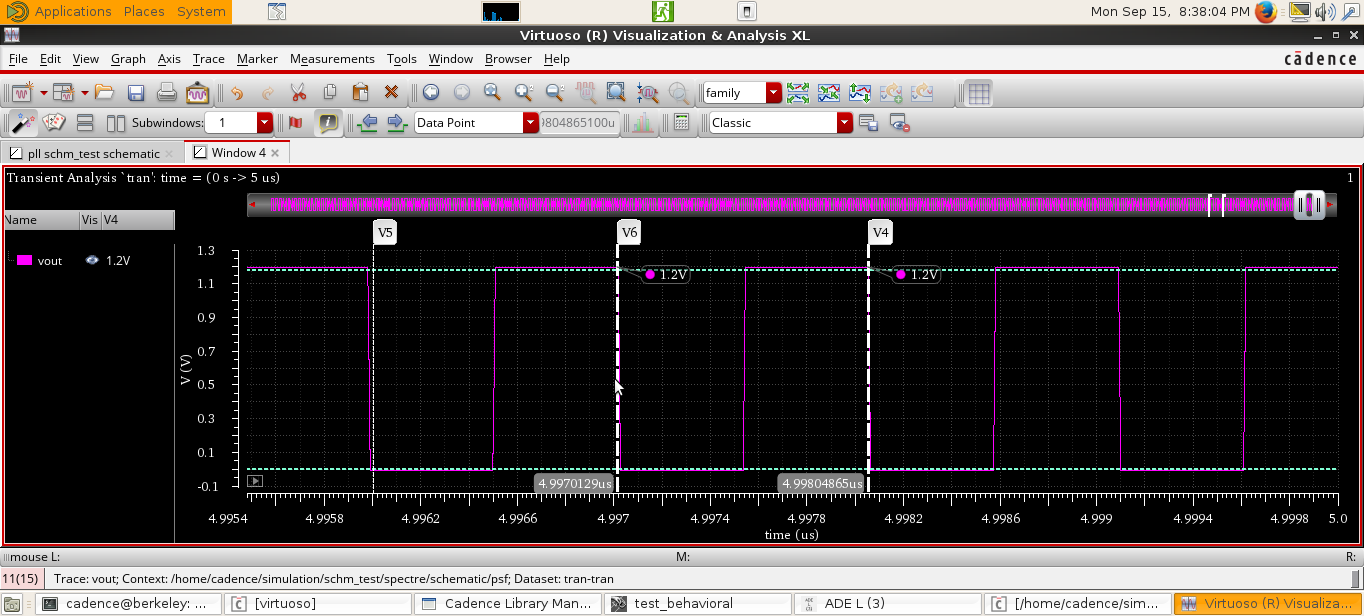
13-

|  |  |
| --- | --- |
| Vctrl simulated | Vctrl analytically |
| 0.779 V | 0.782 V |



there is slightly difference between the two values as the pulse width and period in our simulation are not 100% accurate.

14 - 

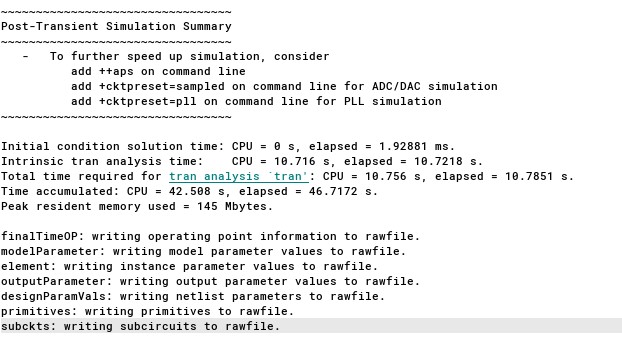
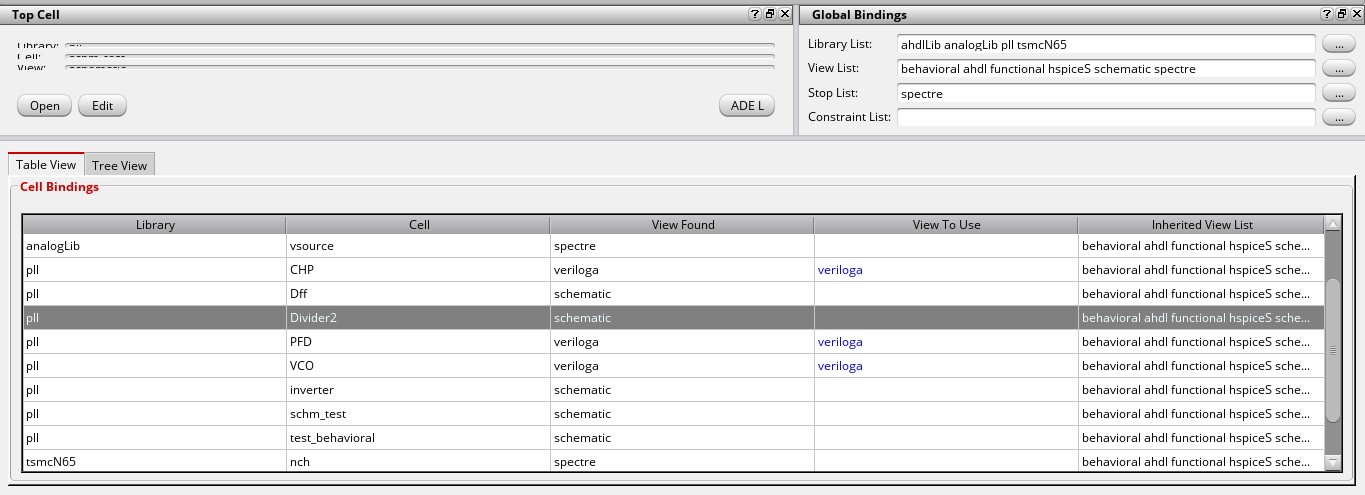
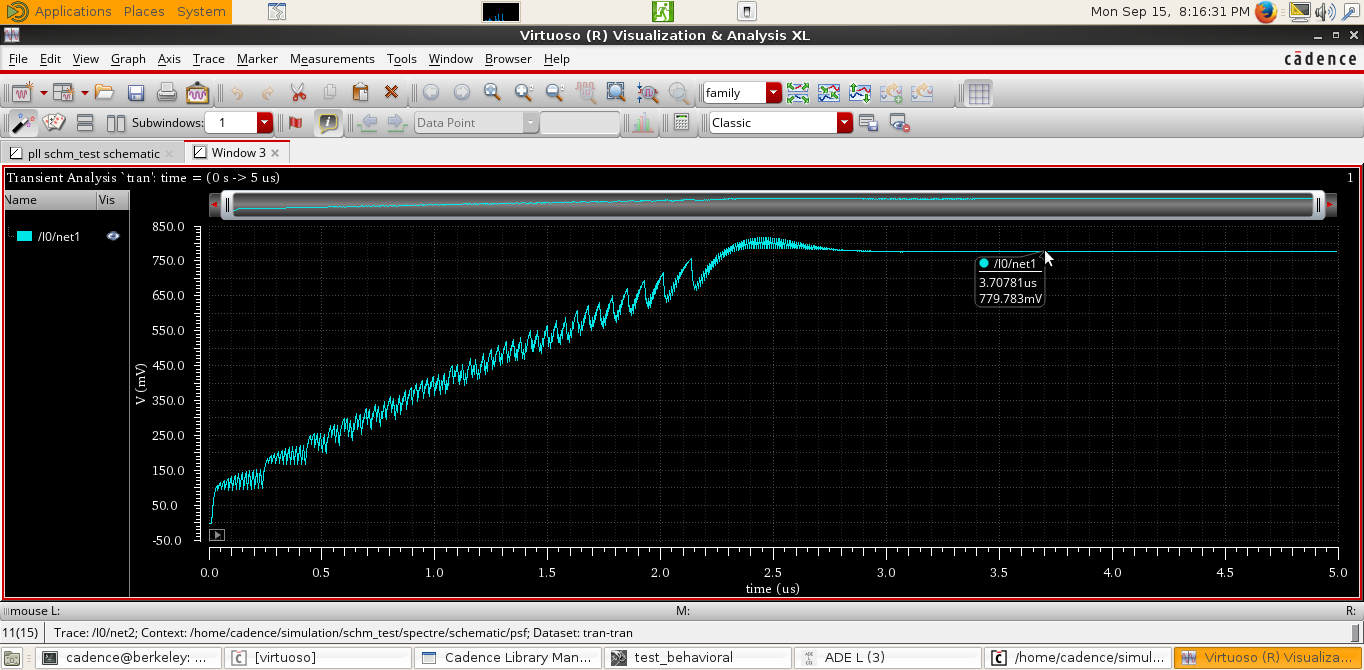
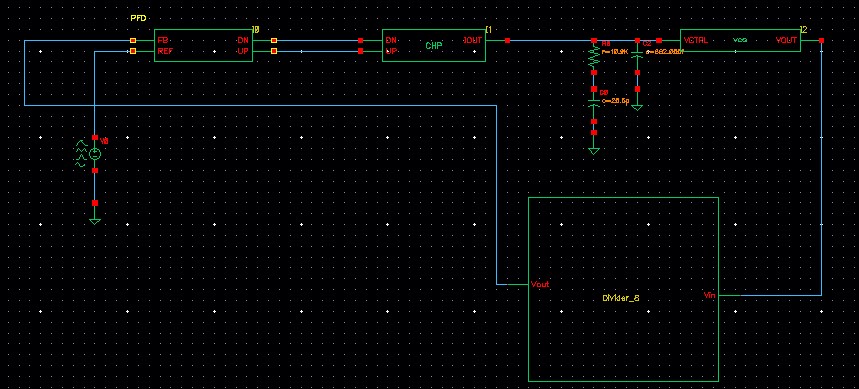


Output frequency = 1/(4.99804865us-4.9970129us) = 965.48 MHz

(not exactly 960MHz because our source period is not accurate 8.3ns)

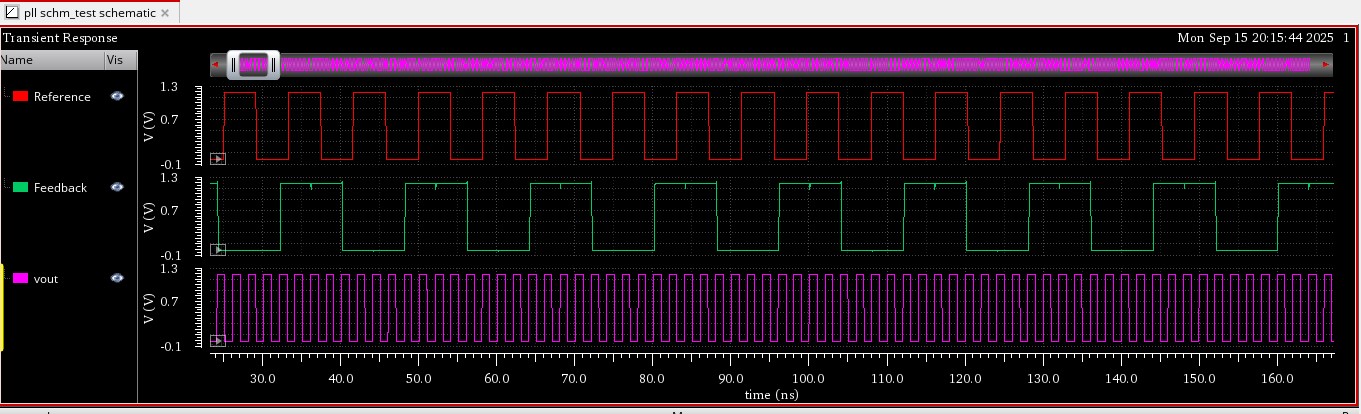
We can see that Vref locks on Vsource with frequency 120MHz and the output frequency is 960MHz .

Note that we had a problem in tanner and needed to switch wiring names so here VOUT represents the feedback and VIN represents the output .

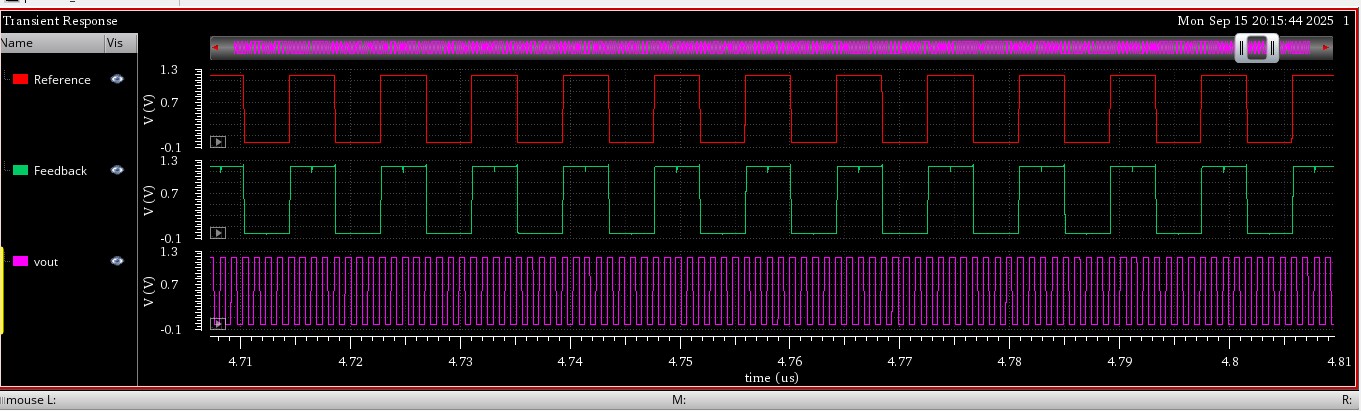
15-16- 17- 

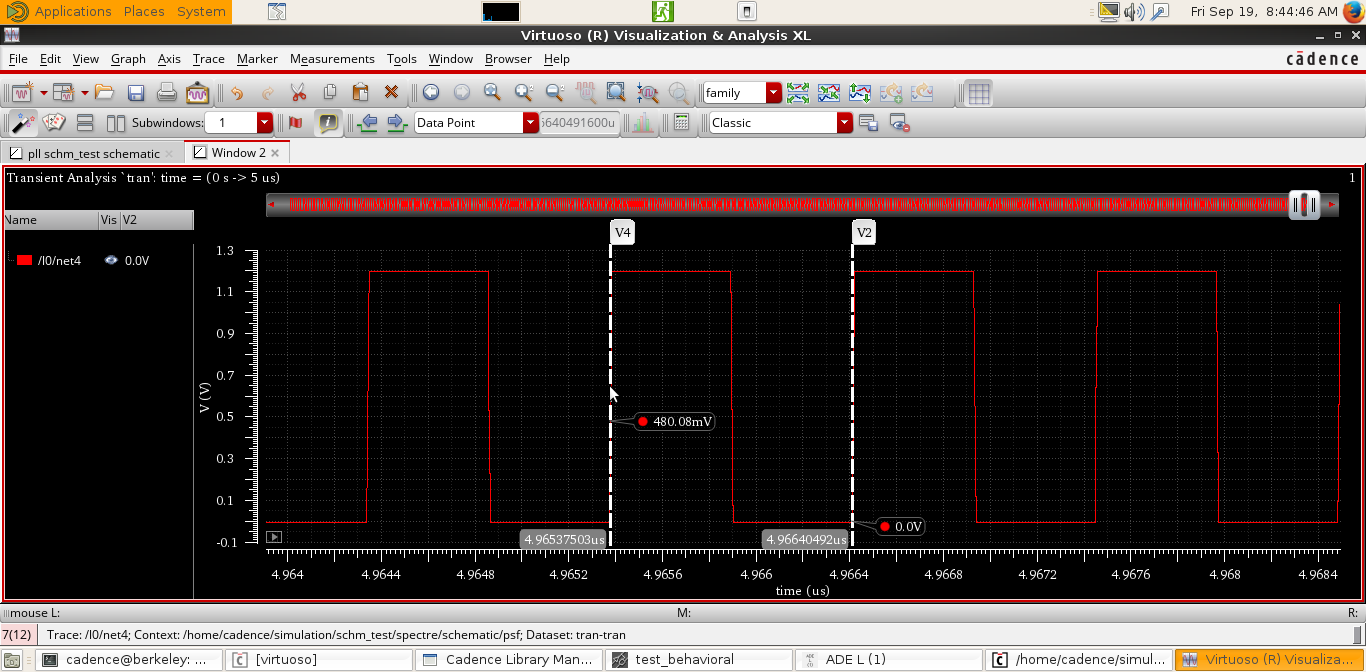
18-

Before lock:



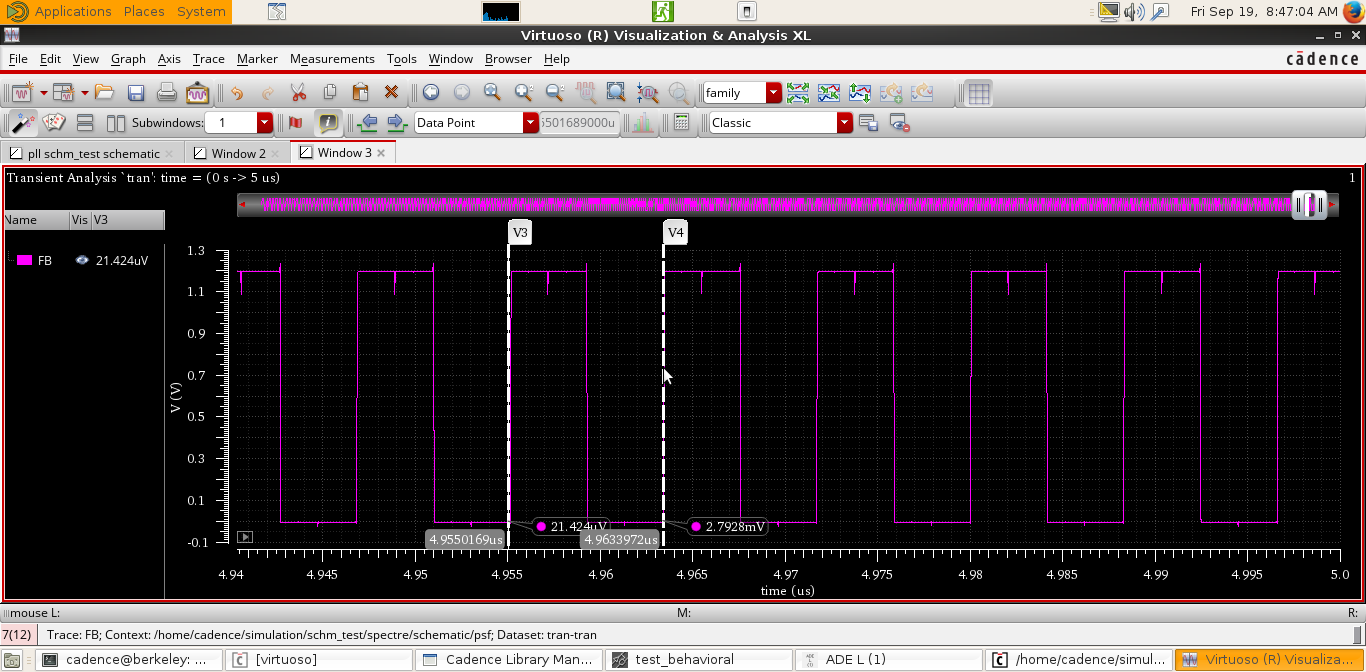
After lock:



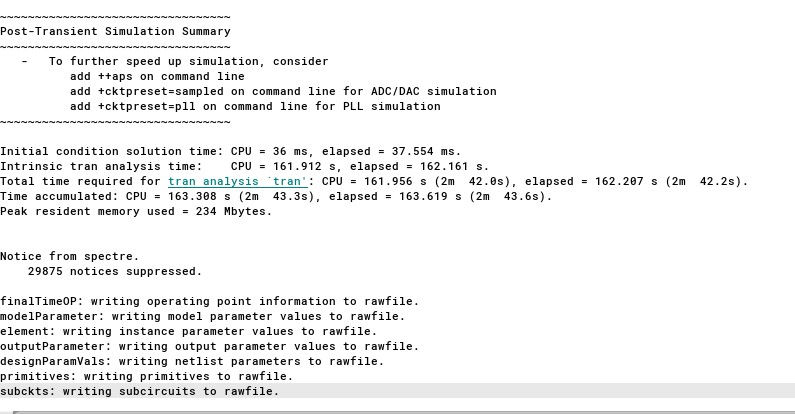
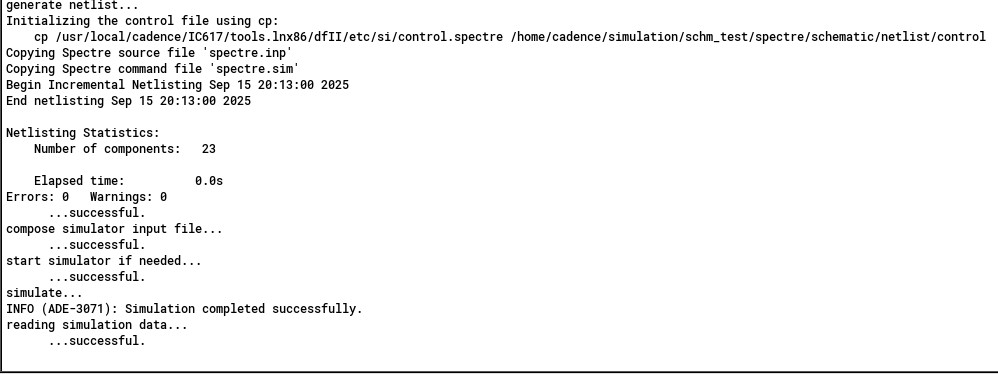


Output frequency = 1/(4.96640492us-4.96537503us) = 970.48 MHz

(not exactly 960MHz because our source period is not accurate 8.3ns)



Feedback lock frequency =1/(4.9633972us-4.9550169us) = 119.4 MHz (not exactly 120MHz ).

19- 

20-

|  |  |
| --- | --- |
| Verilog-A (behavioral model ) | Transistor level model |
| 10 s | 163.6 s |

As expected, the transistor-level simulation requires more time compared to the behavioral-level simulation