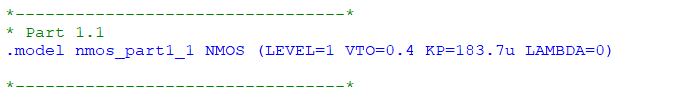
**Lab 3**

**Part 1 (prelab):**

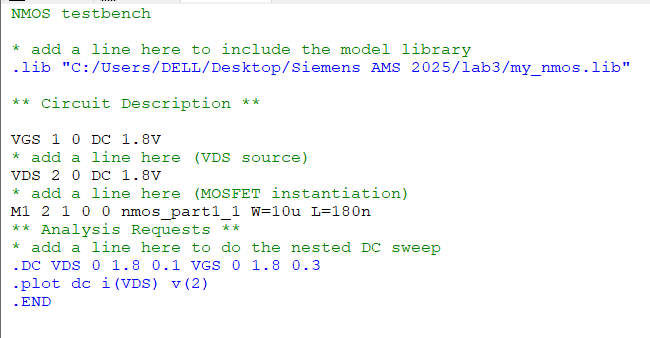
**1-Lib file :**

****

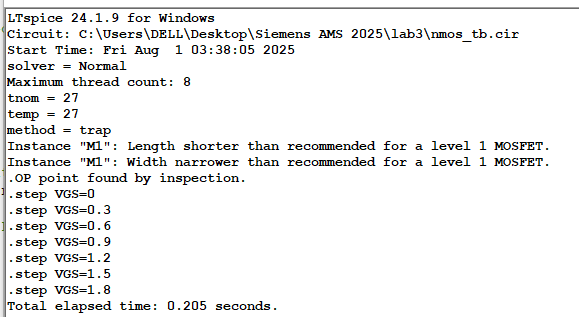
I= 0.5 \*KP\*(w/l)\*(Vgs-VT0)\*\*2

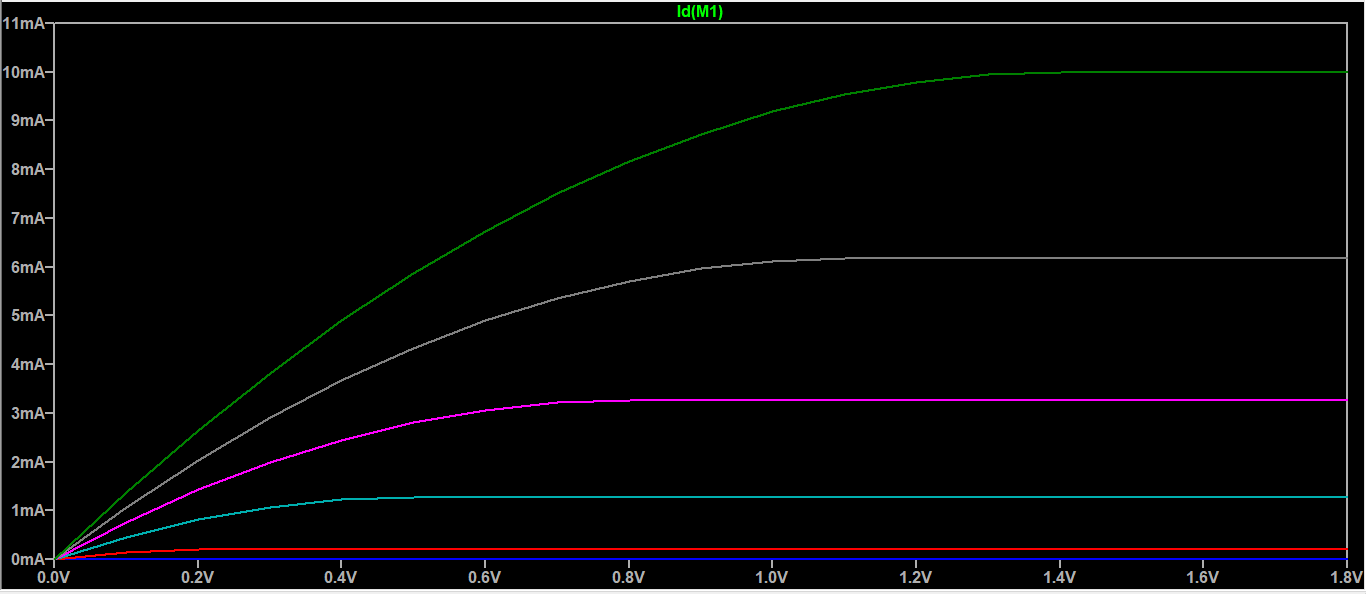
10m=0.5\*KP\*(10/0.18)\*(1.8-0.4)\*\*2 KP = 183.7u

**Netlist :**

****

**Results:**

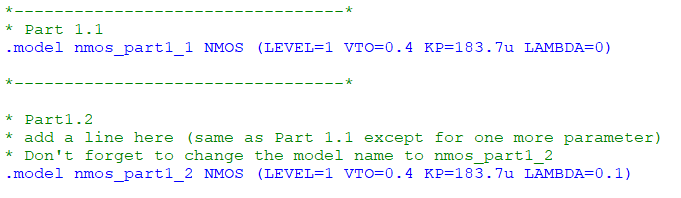
****

****

**Comment:**

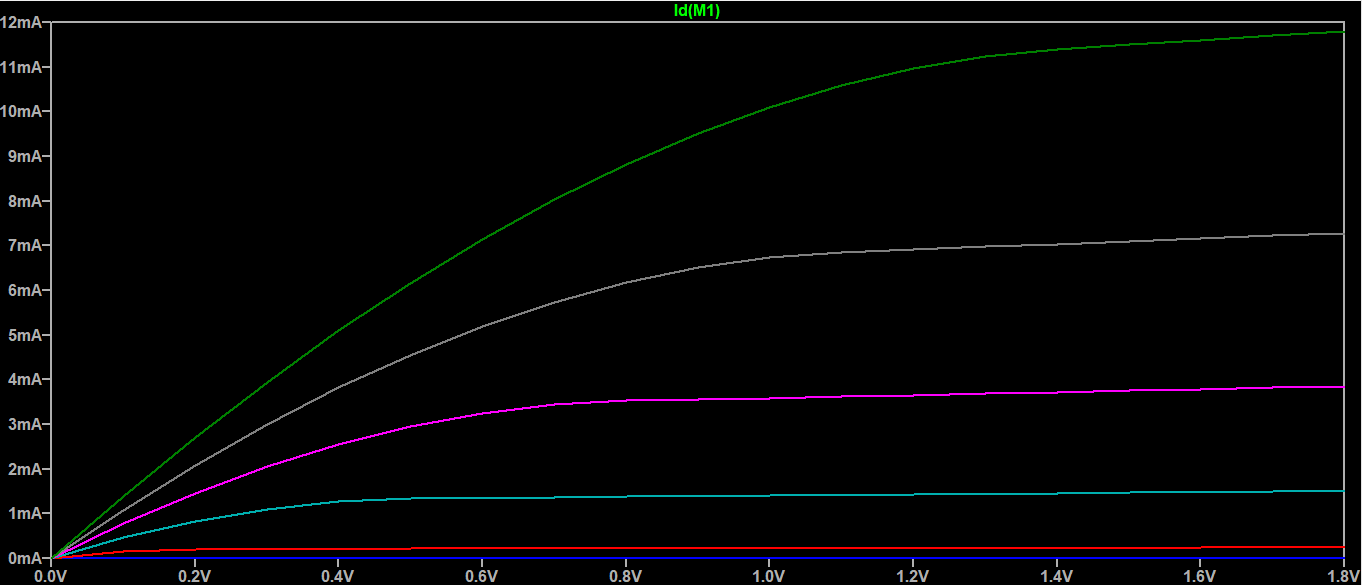
The two warnings are because we are using level 1 model which is used for long and wide channels so the 180nm technology with w=10um is considered small to be used with this model.

**2-Lib file :**

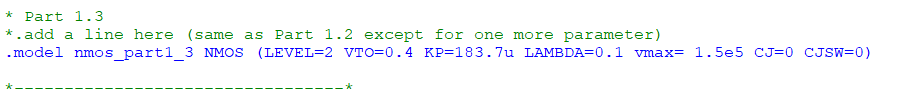
****

Lambda = 1/VA = 1/10 =0.1

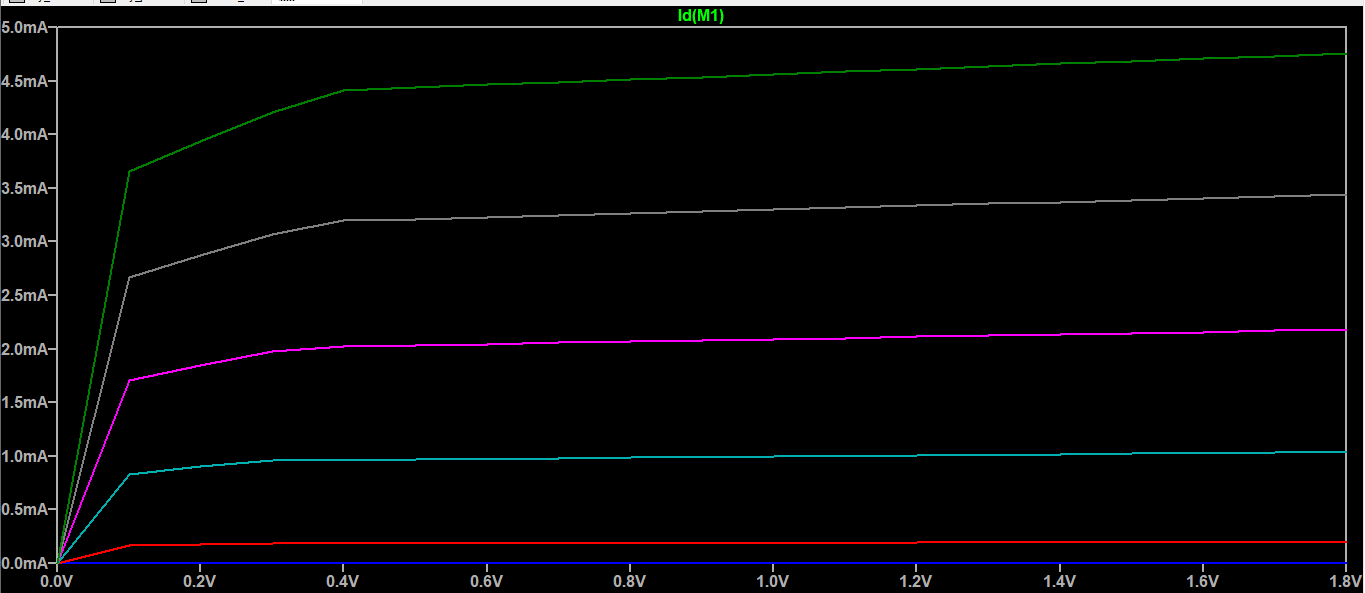
**Simulation:**

****

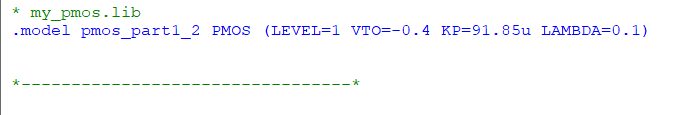
**3-lib file**

****

**Simulation :**

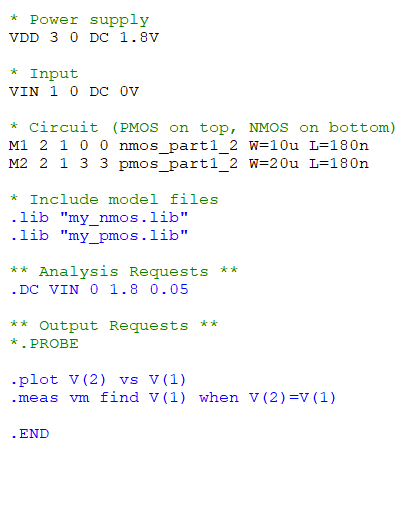
****

**4- lib file :**

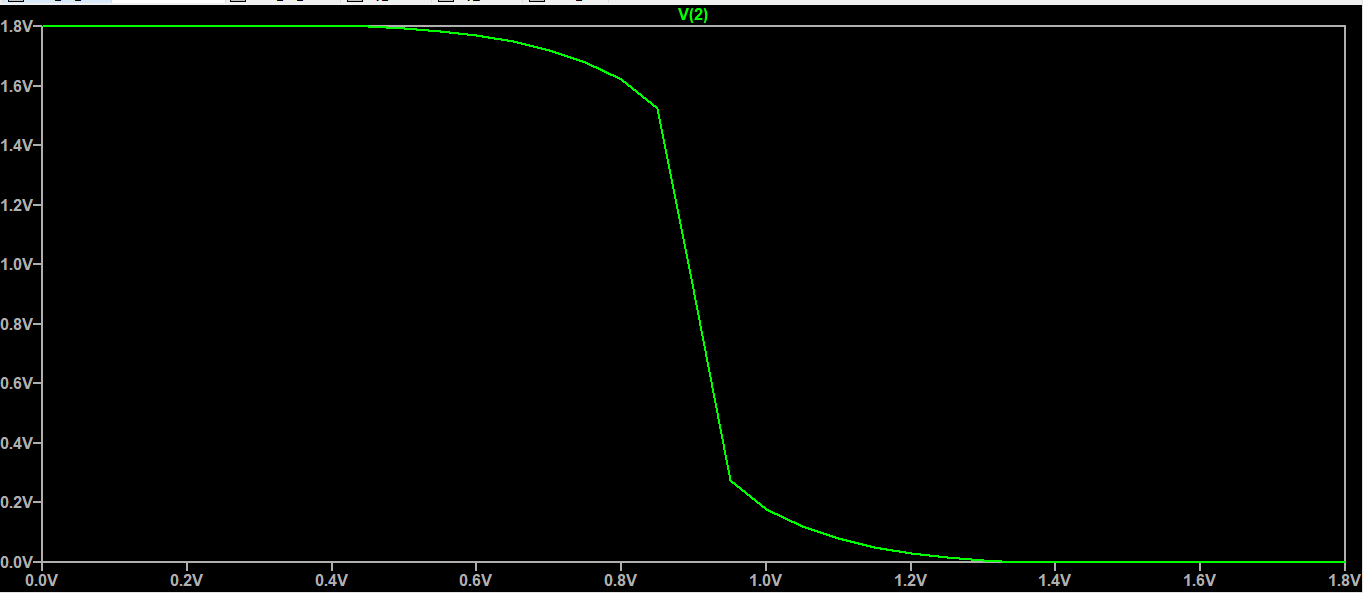
****

**Note:** the vt0 is negative

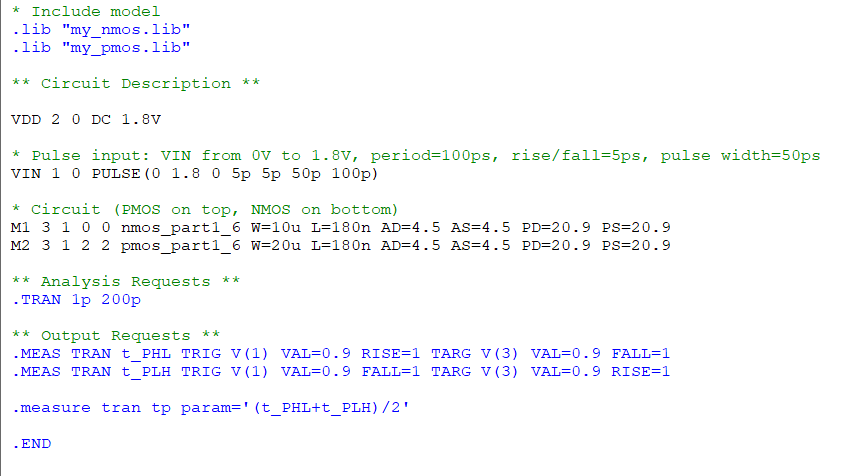
**Netlist:**

****

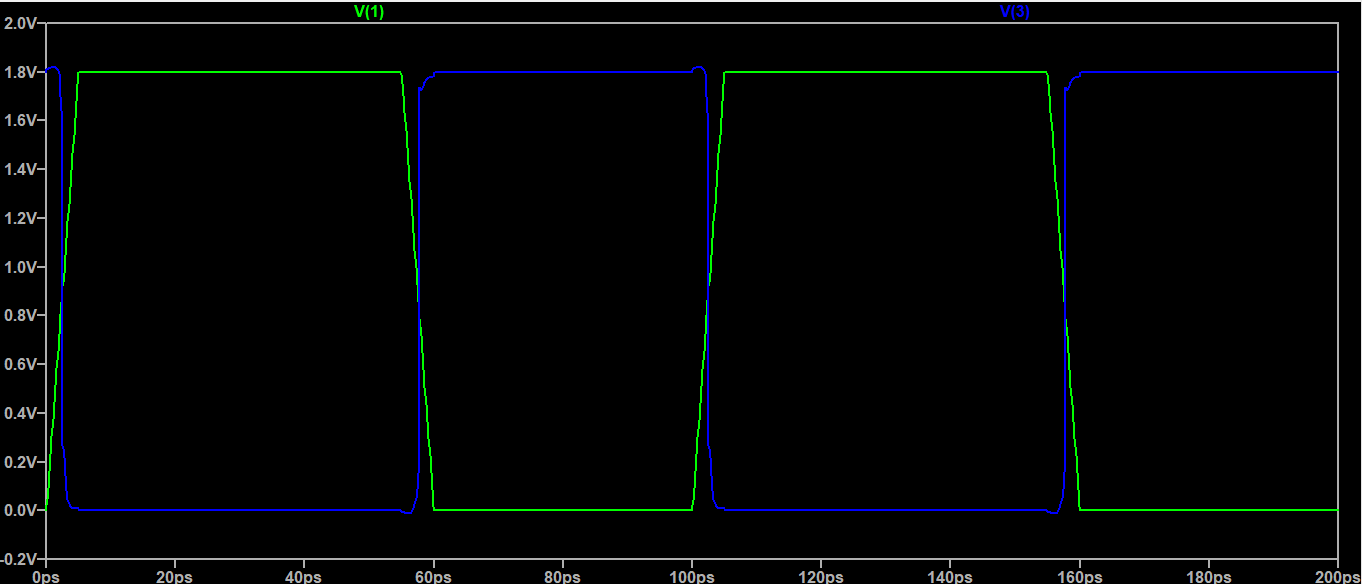
**Simulation:**

****

**5- netlist :**

****

**Simulation:**

****

**Delay measurement :**

****

**6-**

λ = Lmin / 2 → λ = 180nm / 2 = 90nm = 0.09μm

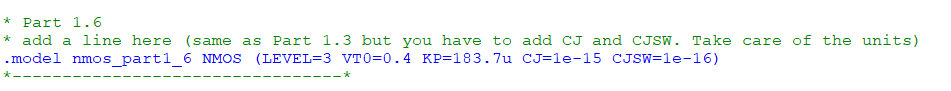
LDIFF = 5 × λ = 0.45μm

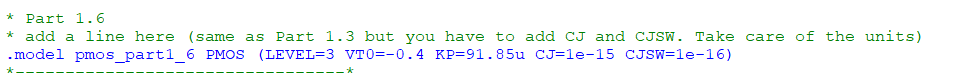
W = 10μm

Junction Area = LDIFF × W = 4.5 μm²

Junction Perimeter = 2 × (LDIFF + W) = 2 × (0.45 + 10) = 20.9 μm

**Model modifications :**

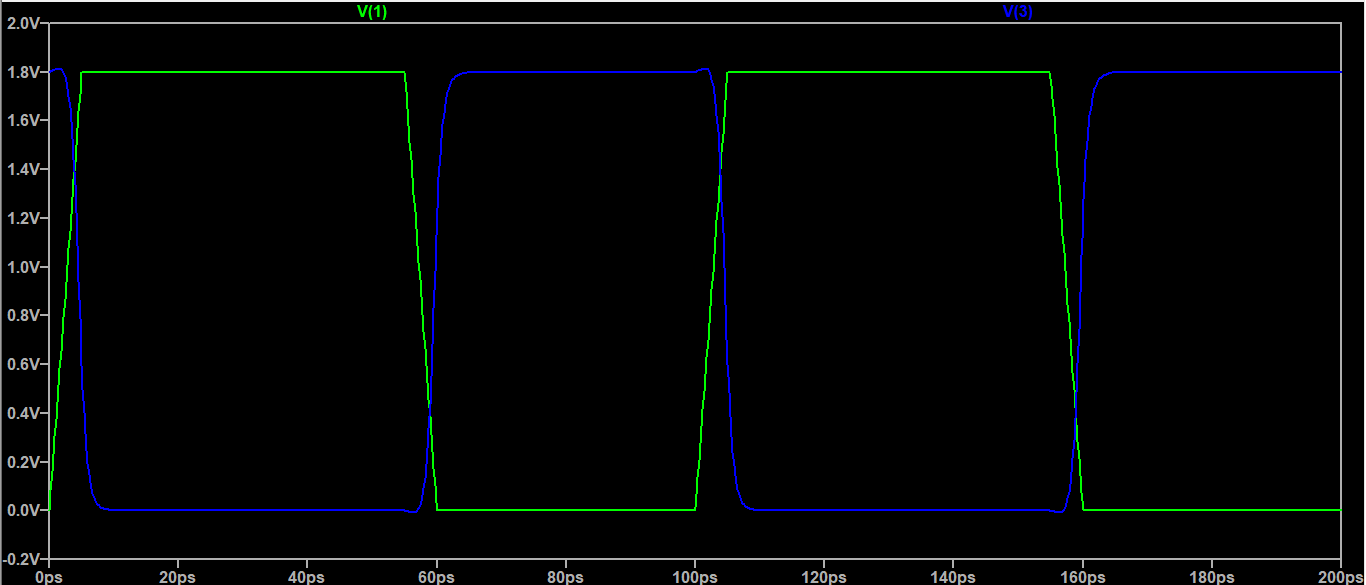
****

****

**Delay measurement :**

****

**Simulation :**

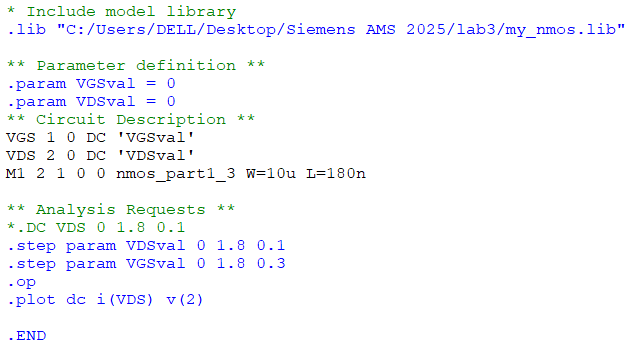
****

We can notice that adding the capacitances effect made the delay much bigger

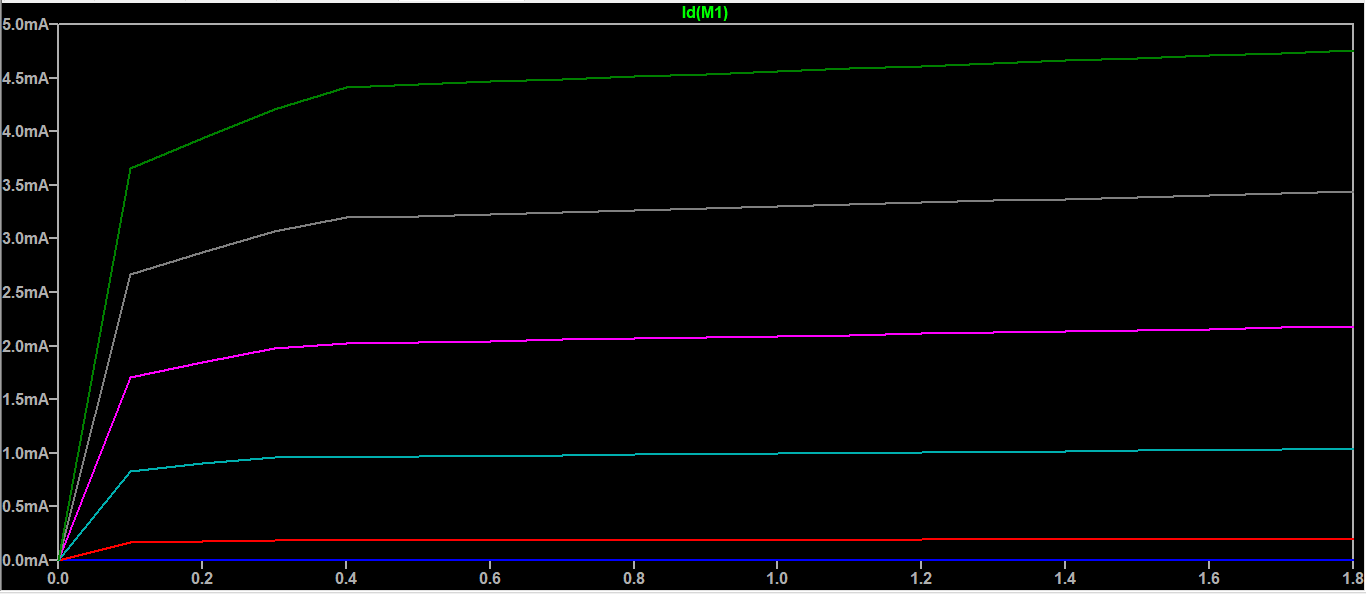
Added effect is ( AD\*CJ , AS\*CJ , PD\*CJSW , PS\*CJSW )

**Part 2:**

1. **nmos\_tb\_param.cir**

****

**Simulation:**

****

**Simulation time for parametric sweep case :**

****

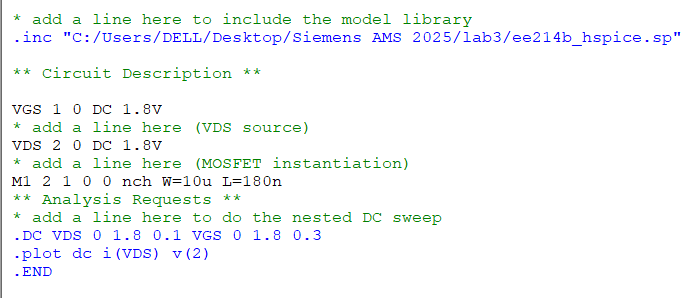
**Simulation time for nested DC sweep case :**

****

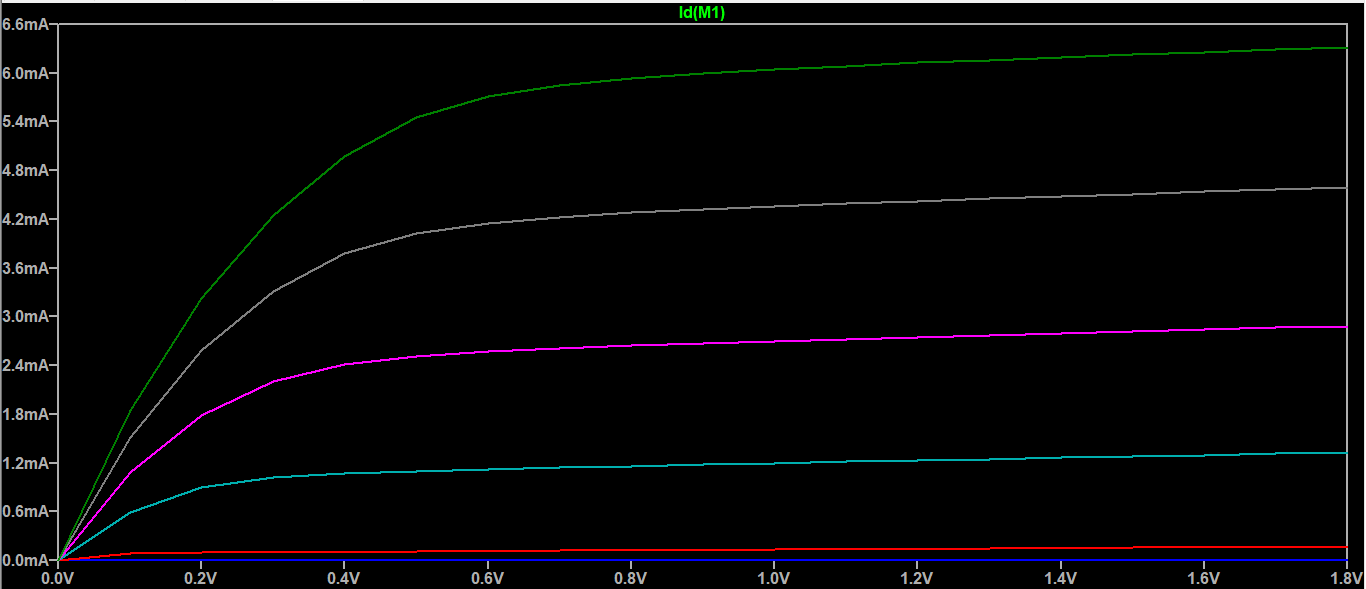
**Comment:**

Although the two cases gives the same simulation results but the parametric sweep takes more time than the nested dc sweep case because in parametric sweep the simulator solves the whole circuit again for each step taken

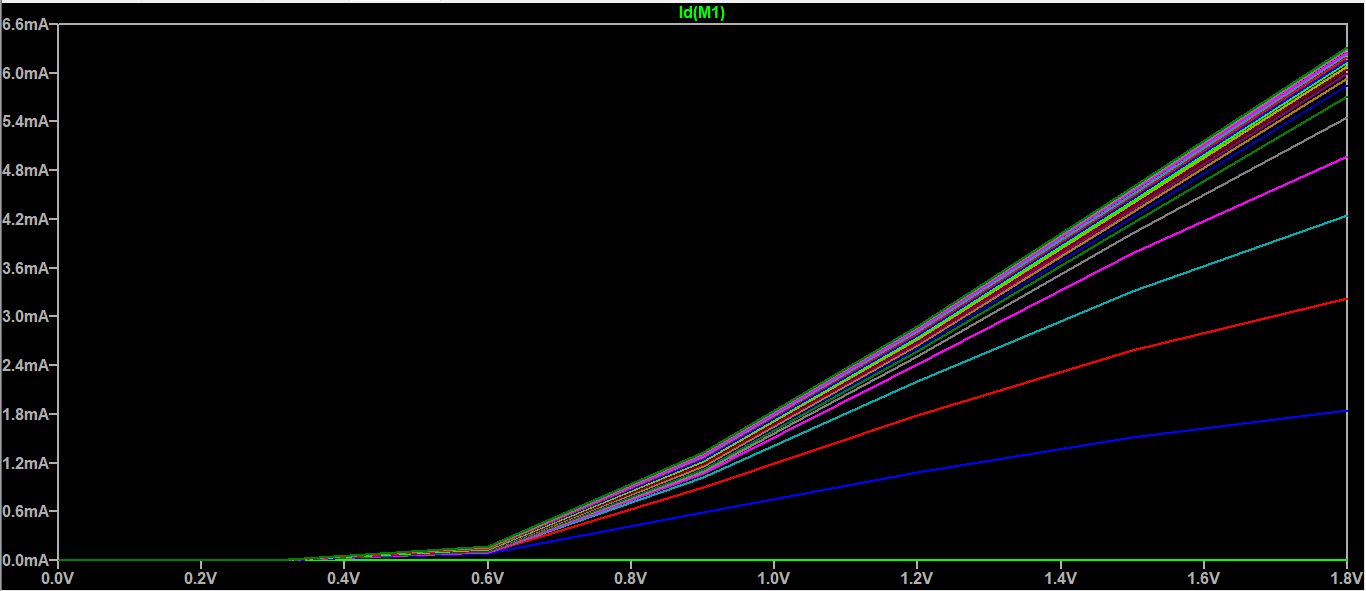
1. netlist :



Simulation: (I vs VDS)



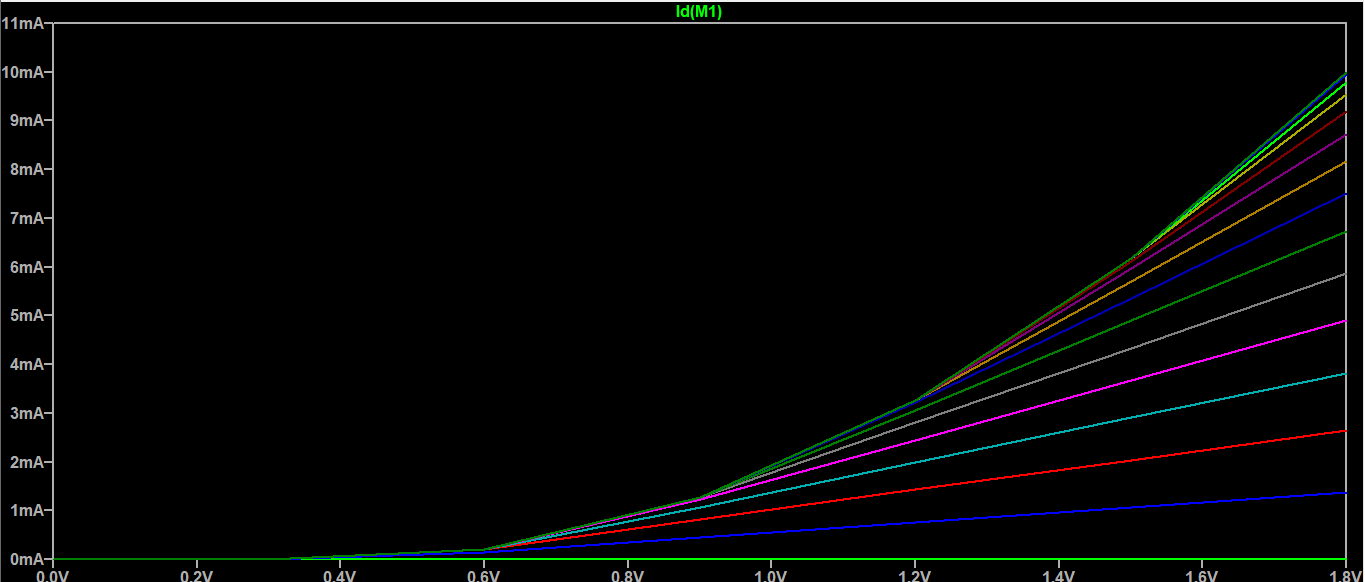
(I vs VGS)



Velocity saturation limitation can be easily observed here.

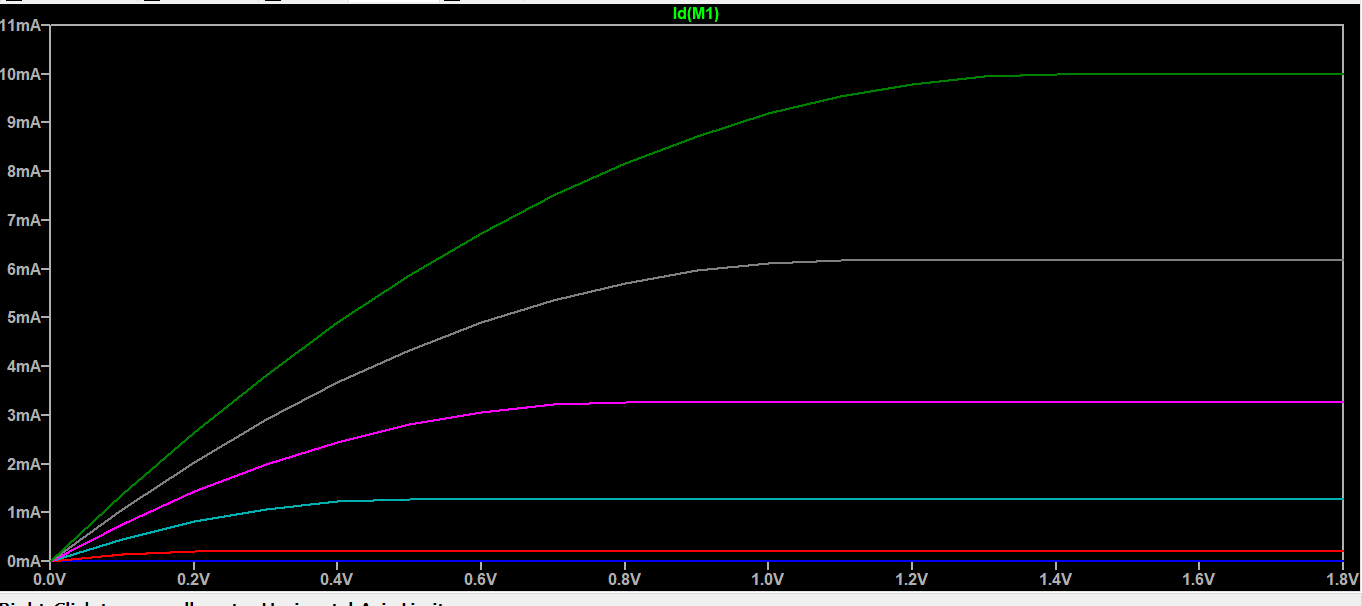
For the level 1 model

I vs VGS



No velocity saturation limitations .

I vs VDS



What version of BSIM is this HSPICE model?

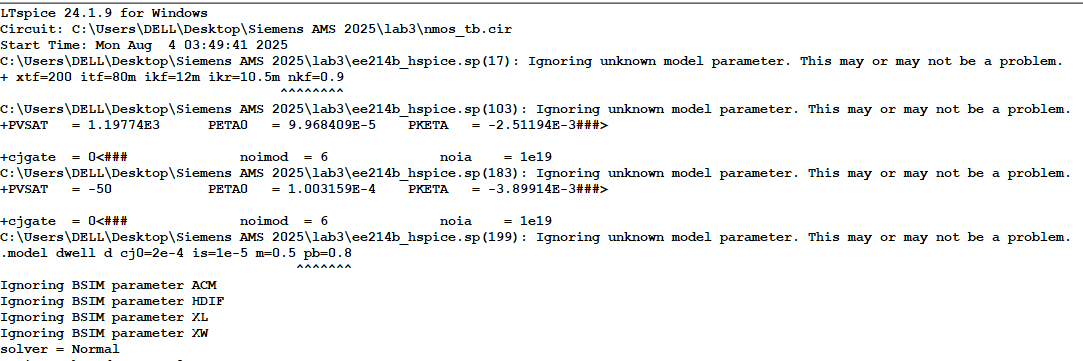
BSIM3 V3.3

How to set the LEVEL parameter appropriately for LTspice in this case?

In LTSpice the model BSIM3 V3.3 corresponds to level 8 so we should set the level parameter LEVEL =8

Compare the results to your LEVEL 1 model.

Velocity saturation limitation can be easily observed for the HSpice model but for level 1 there is no saturation limitation

1. 

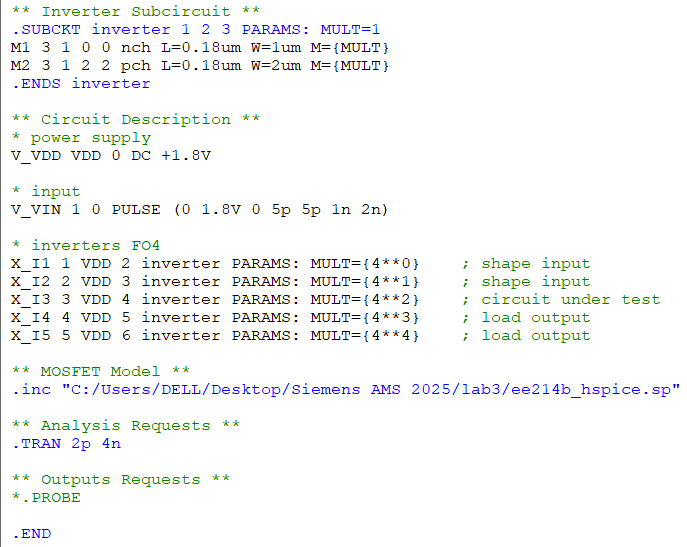
|  |  |  |
| --- | --- | --- |
| Parameter | Meaning | Expected impact |
| ACM | Area Calculation Method: Defines how the area of source/drain junctions is computed | Affects junction capacitance and leakage modeling. |
| HDIF | Source/Drain diffusion height | Affects parasitic resistance and capacitance. |
| XL ,XW | Length/Width offsets to model layout-dependent effects. | Refines effective L and W. |
| cjgate | **Gate-to-body junction capacitance per area** | Impacts input capacitance and delay modeling. |
| noia,noimod | **Noise modeling parameters** | Affects flicker and thermal noise in analog/RF simulation. |
| PVTH0, PKETA | Process variation parameters | Used for modeling process-dependent shifts in threshold, mobility |

|  |  |
| --- | --- |
| Parameter | Value in model |
| ACM | 3 |
| HDIF | 0.32e-6 |
| XL,XW | 0, -1E-8 |
| cjgate | 0 |
| noia | 1e19 |
| noimod | 6 |
| PETA0 | 9.968409E-5 |
| PKETA | -2.51194E-3 |

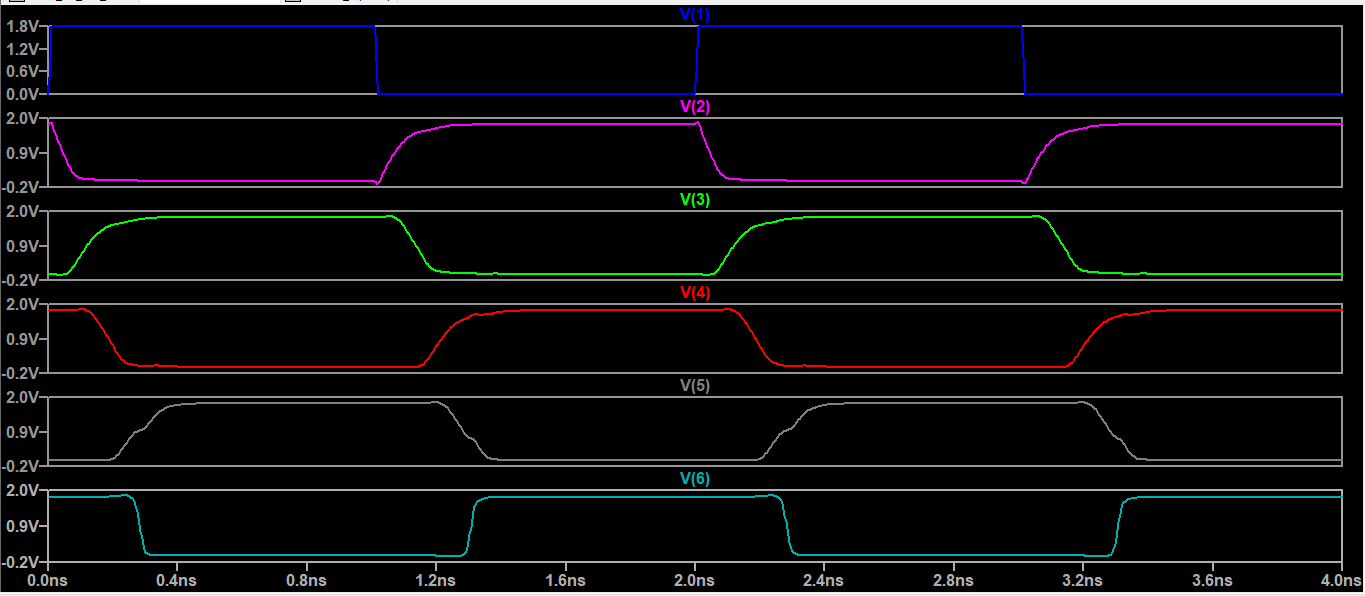
How do you expect they will affect the simulation results?

This can lead to Incorrect Capacitance Modeling , Inaccurate Delay and Slew , Poor Noise Modeling and Neglecting Layout Effects

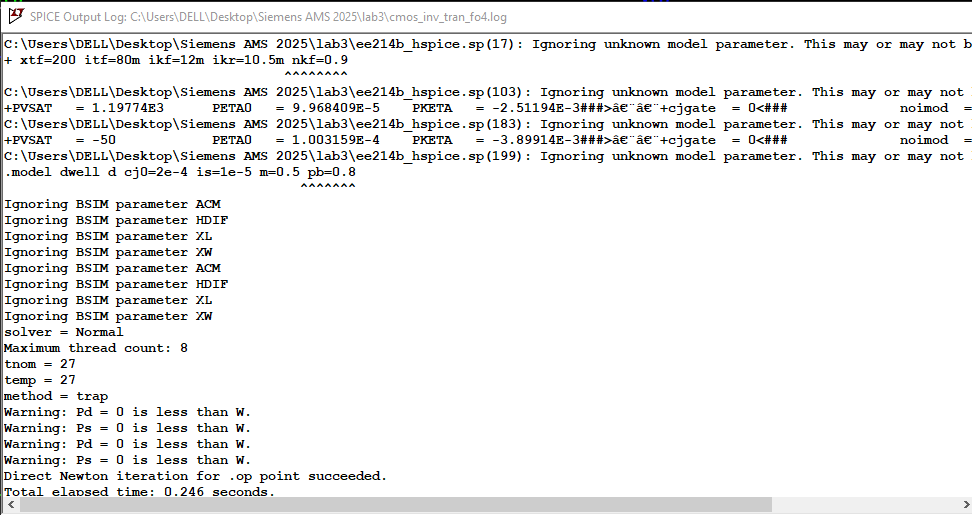
**4-netlist :**

****

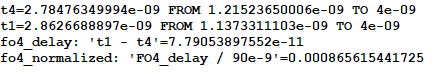
**Simulation :**

****

**Log output :**

****

**Delay measurement:**

****

Fo4 measured delay = 77.905 ps

Lambda = Lmin / 2 = 90 nm

Fo4\_delay normalized = 77.905 / 90 = 0.8656 ps/nm

For the 65nm technology :

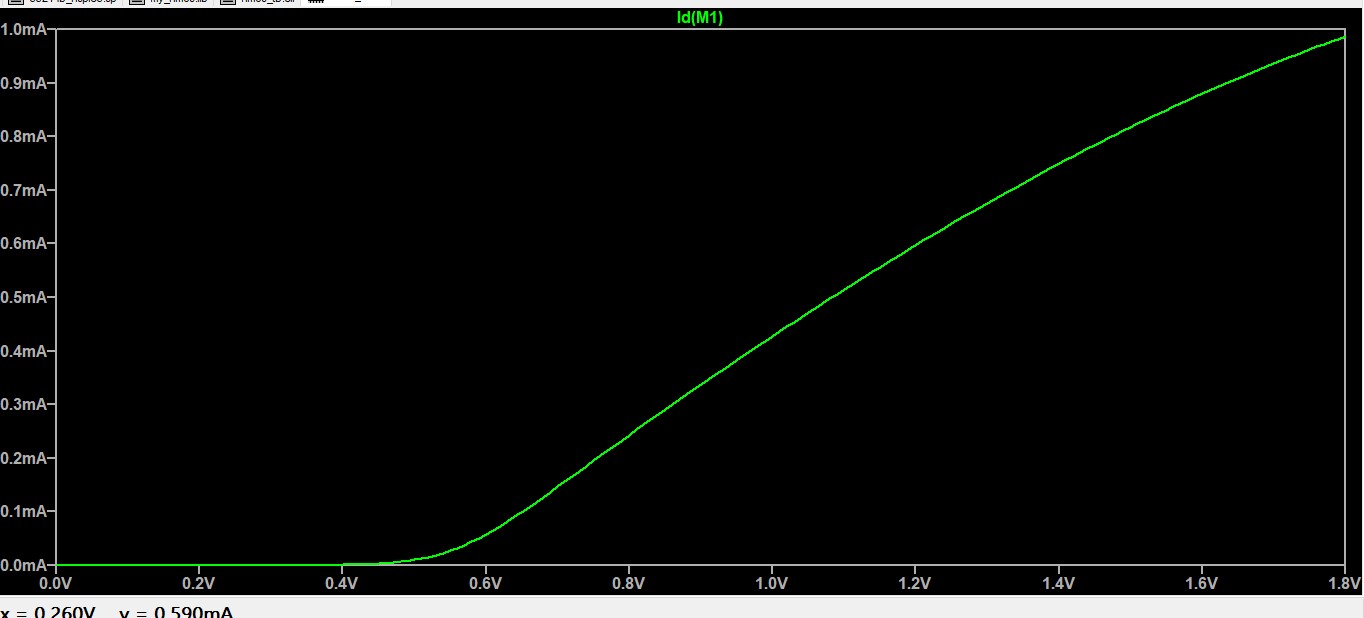
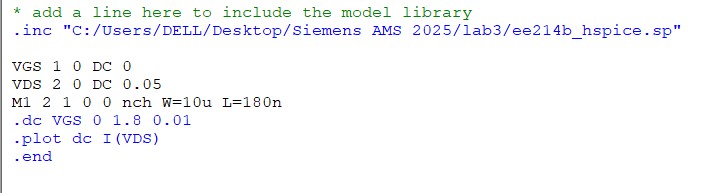
We expect less delay may be in range of 12 -15ps

Lambda = 32.5nm

Fo4\_delay normalized = 12 / 32.5 = 0.369 ps/nm

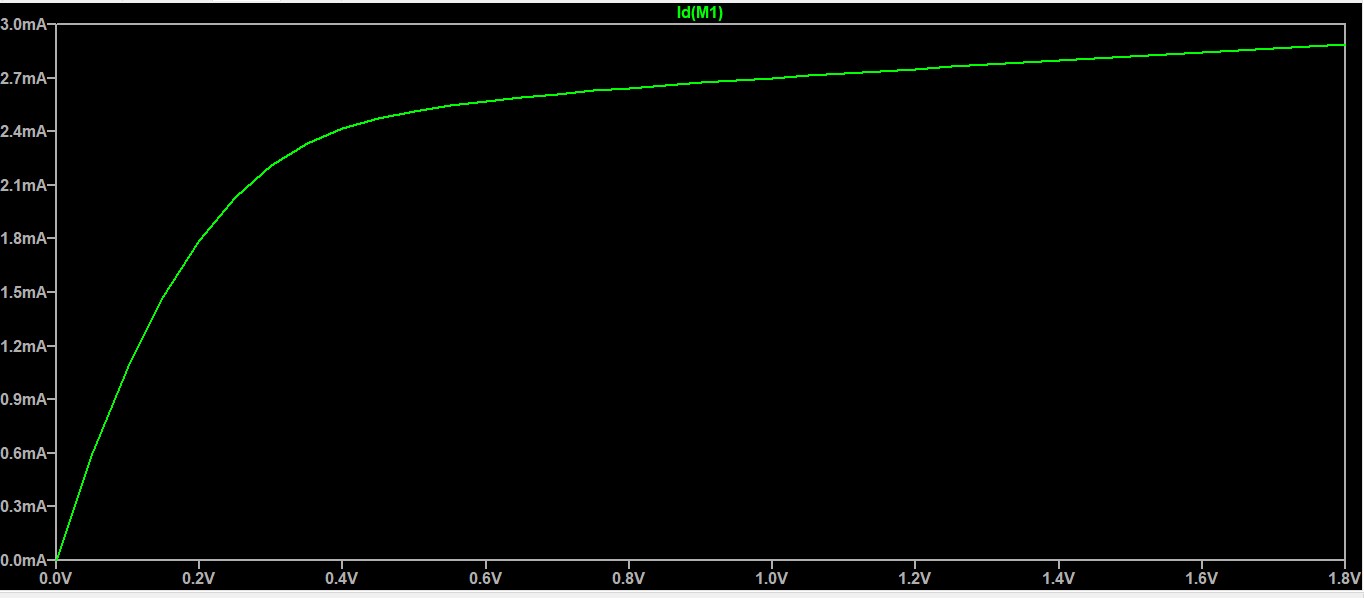
Bonus mearuments :

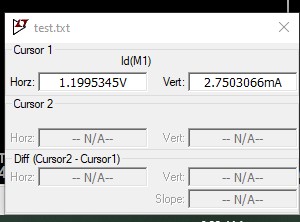
1. Vth



By sweeping vgs with constant small vds we obtain from the curve when we exit the cutoff region (vgs=vth) nearly at 4.3V

1. **LAMBDA**





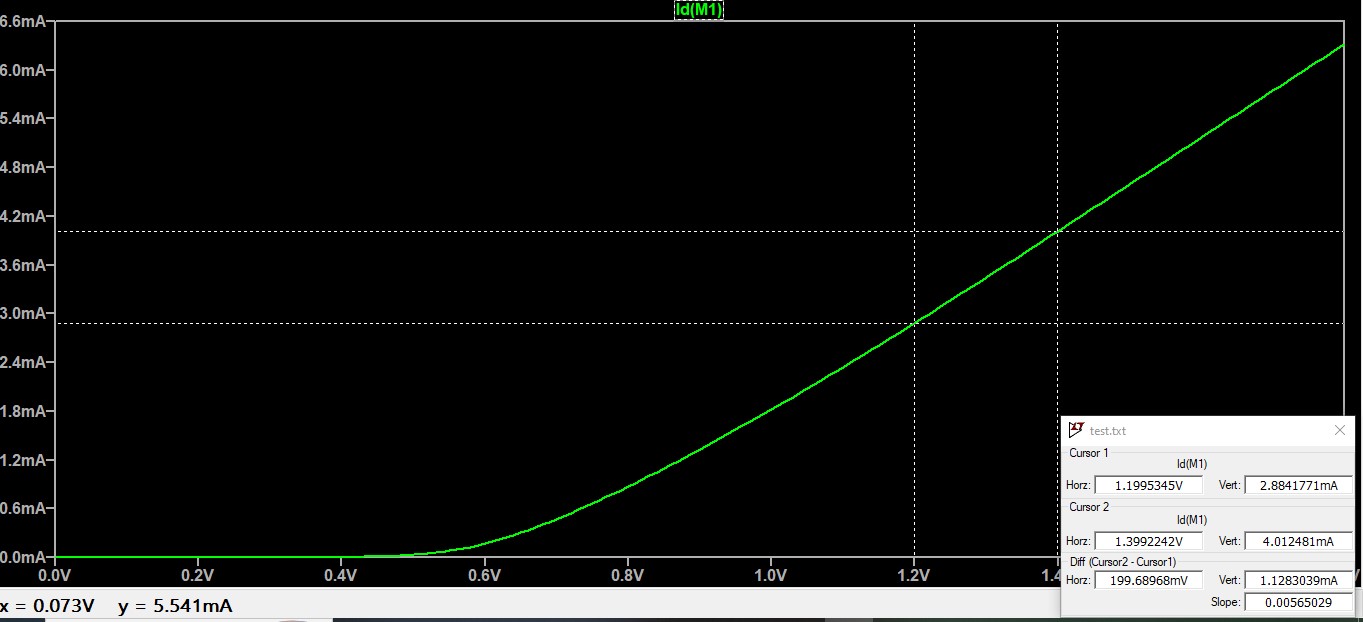
Id= 2.75 mA , Idsat =2.48mA nearly , Vds=1.2 V

Id = Idsat\*(1+lambda\*Vds)

Lambda= 0.08

1. **gm**

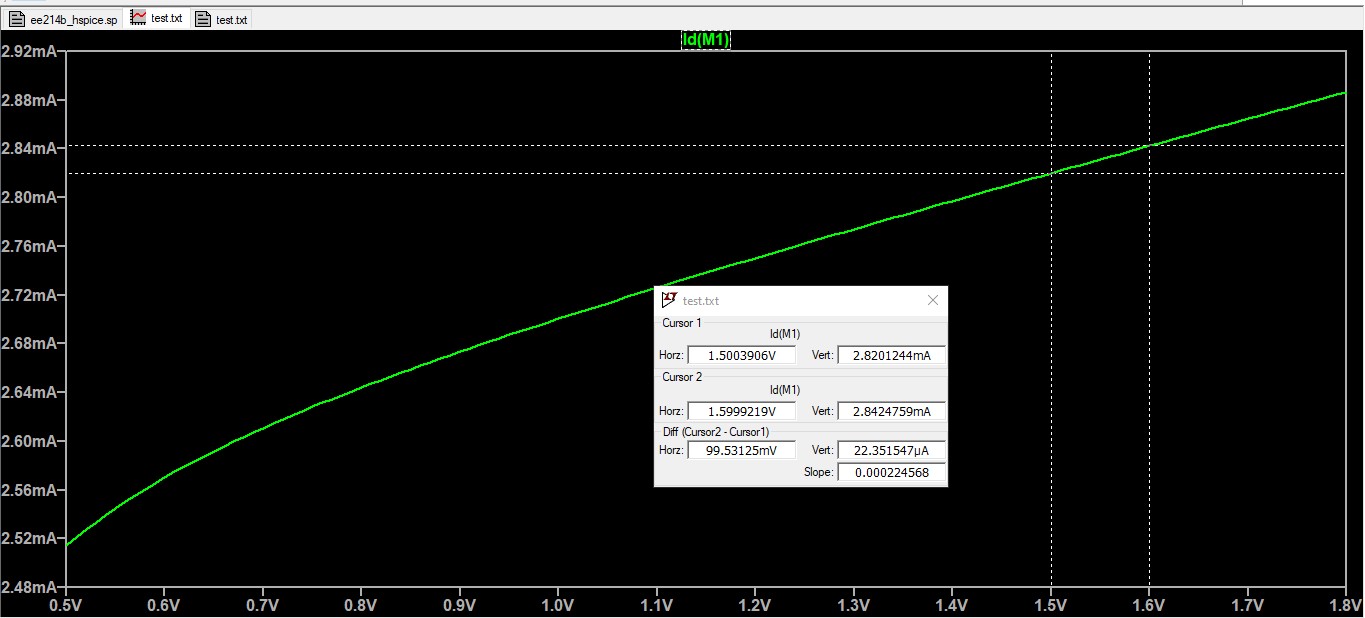
from Id vs VGS curve



gm = slope = = = 5.64 mS

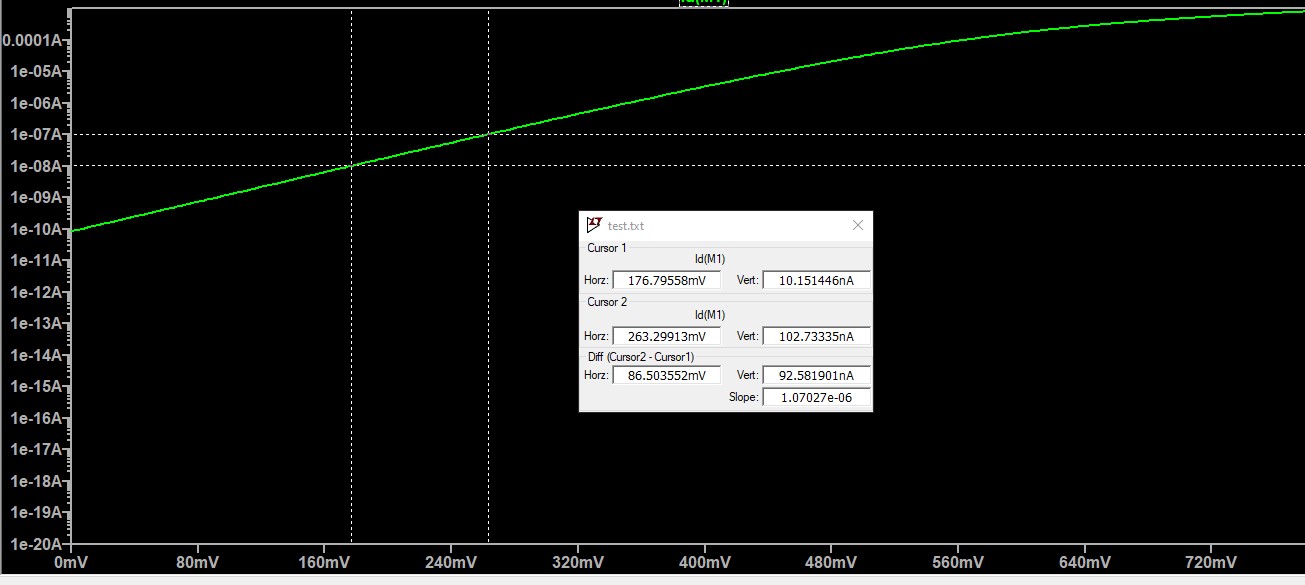
1. **ro**

from Id vs VDS curve



1/ro = slope = = ro = 5 Kohm

1. **Subthreshold Swing**

From Id vs VGS log scale curve 

SS = = \*1000 = 86.5 mV/dec