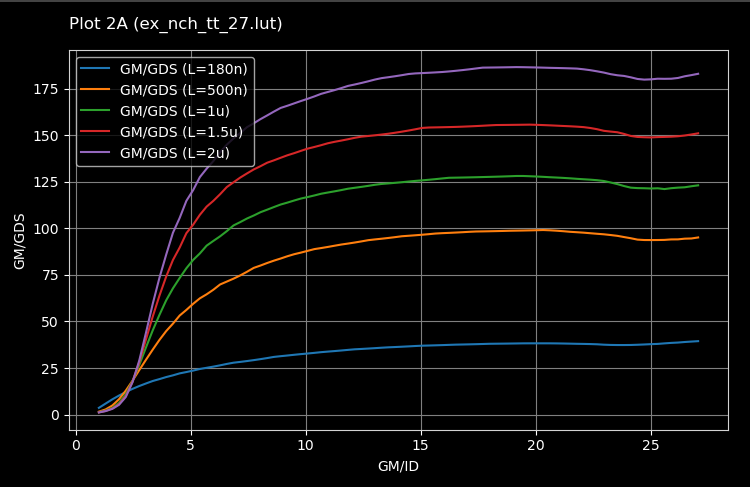
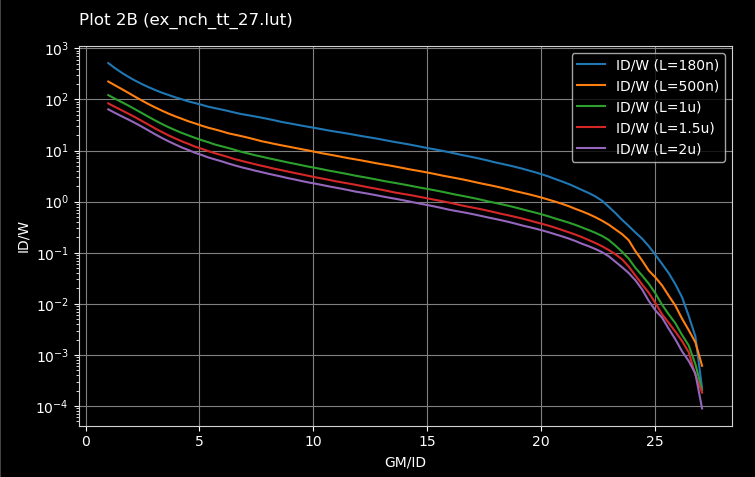
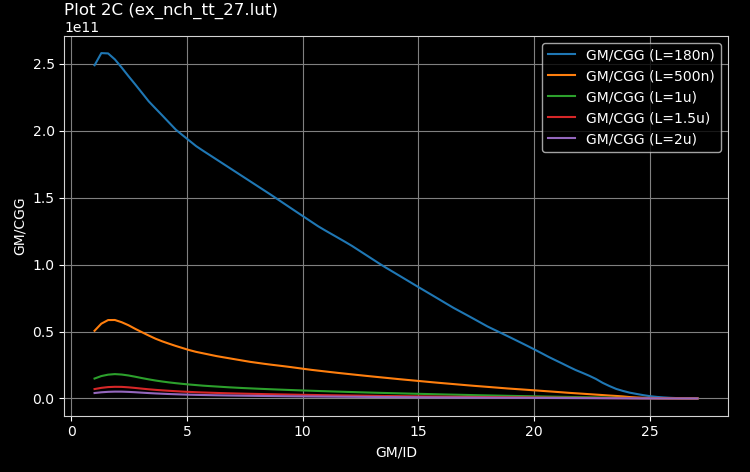
Lab 4

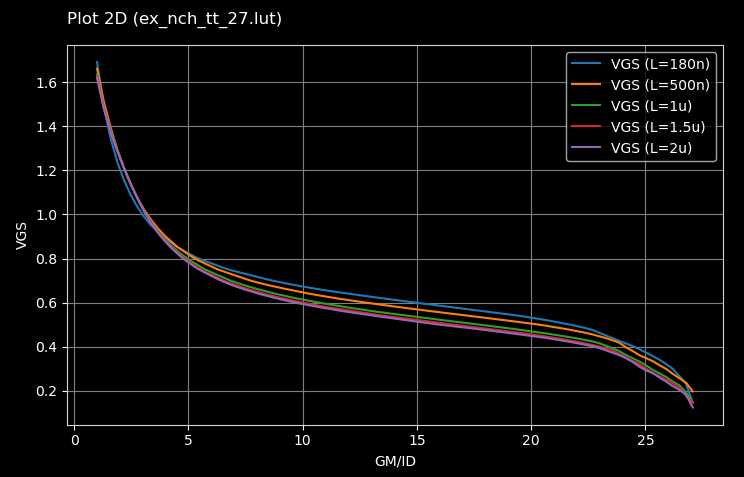
Part 1

NMOS:

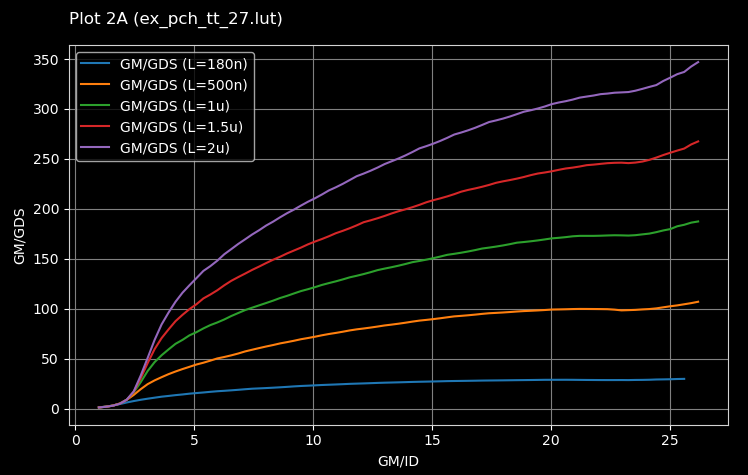


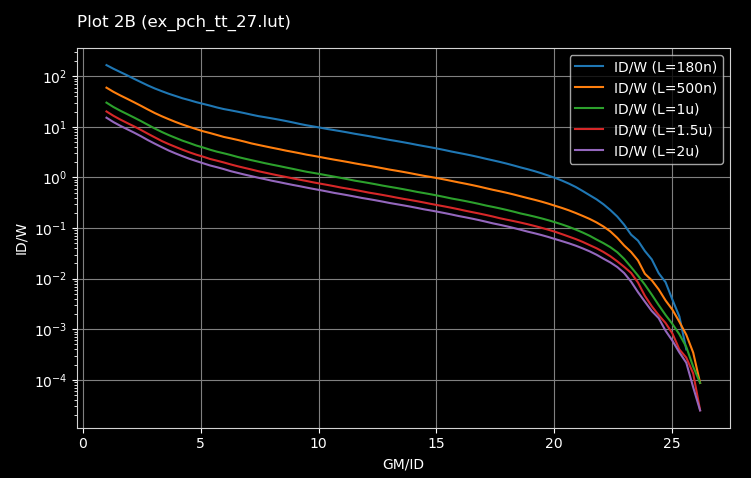


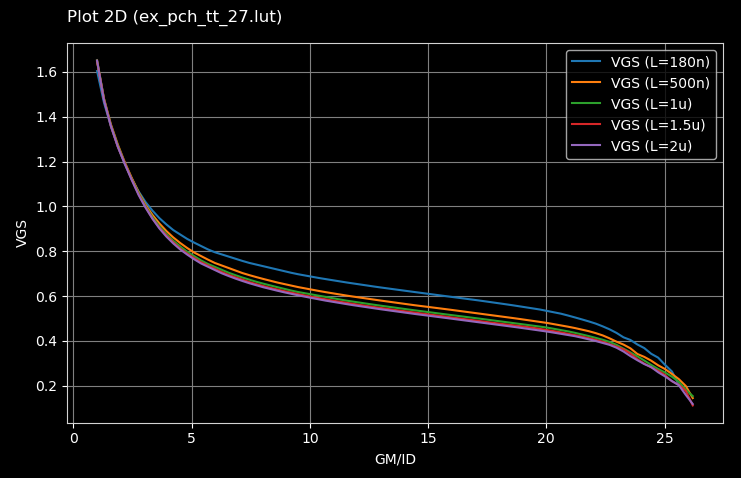
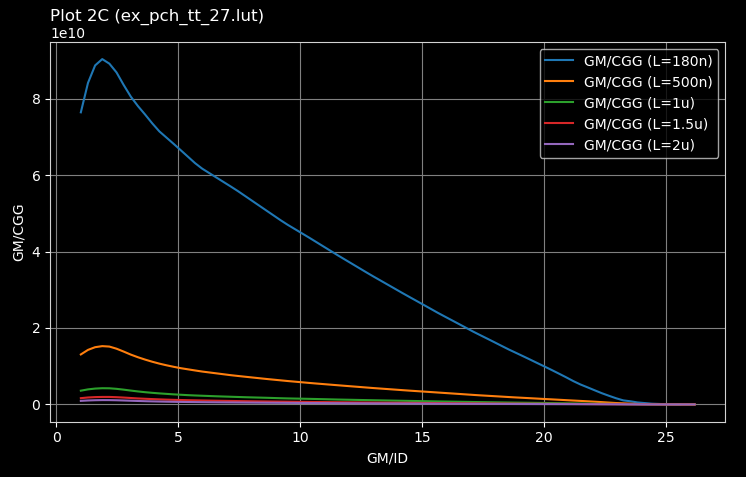




PMOS:

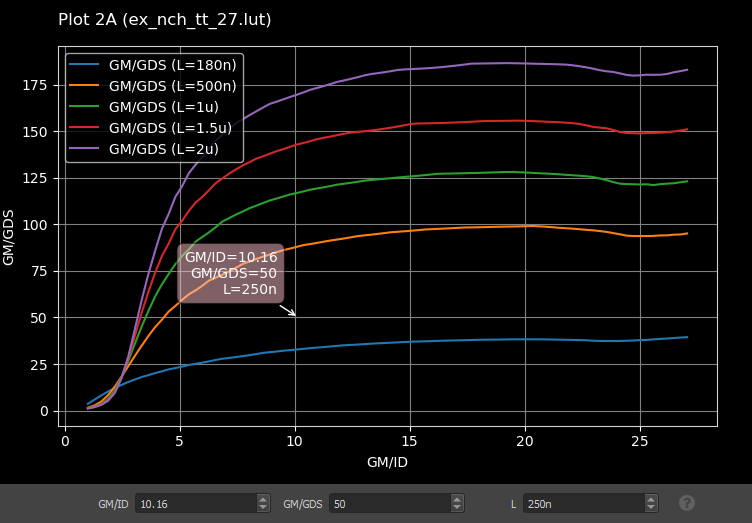


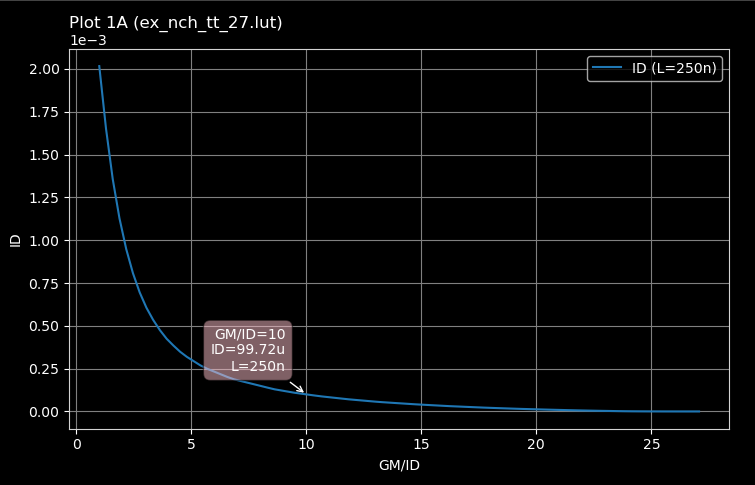


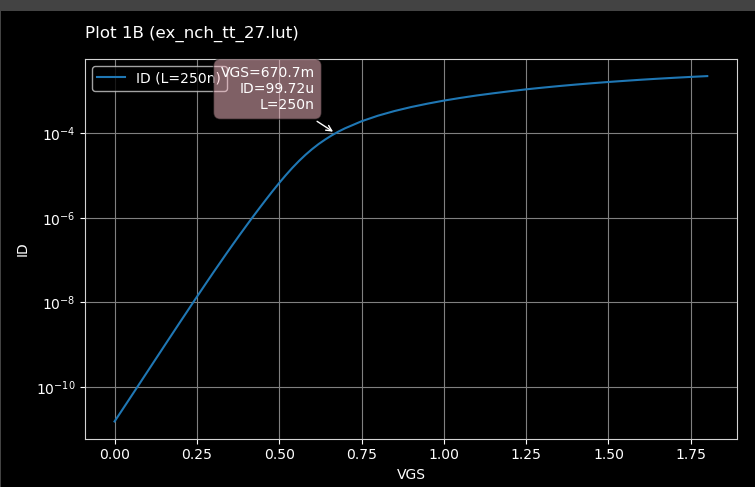


2-

L choice



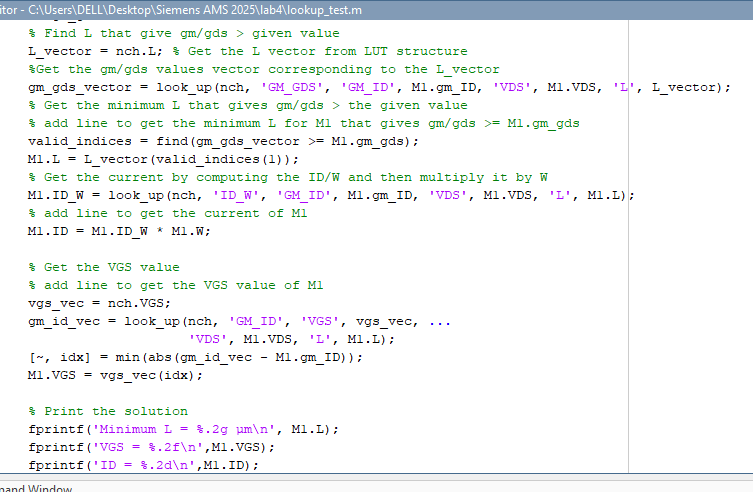


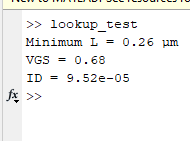


ID= 99.72 uA

Vgs = 670.7 mV

**3- Lookup\_Test modifications :**

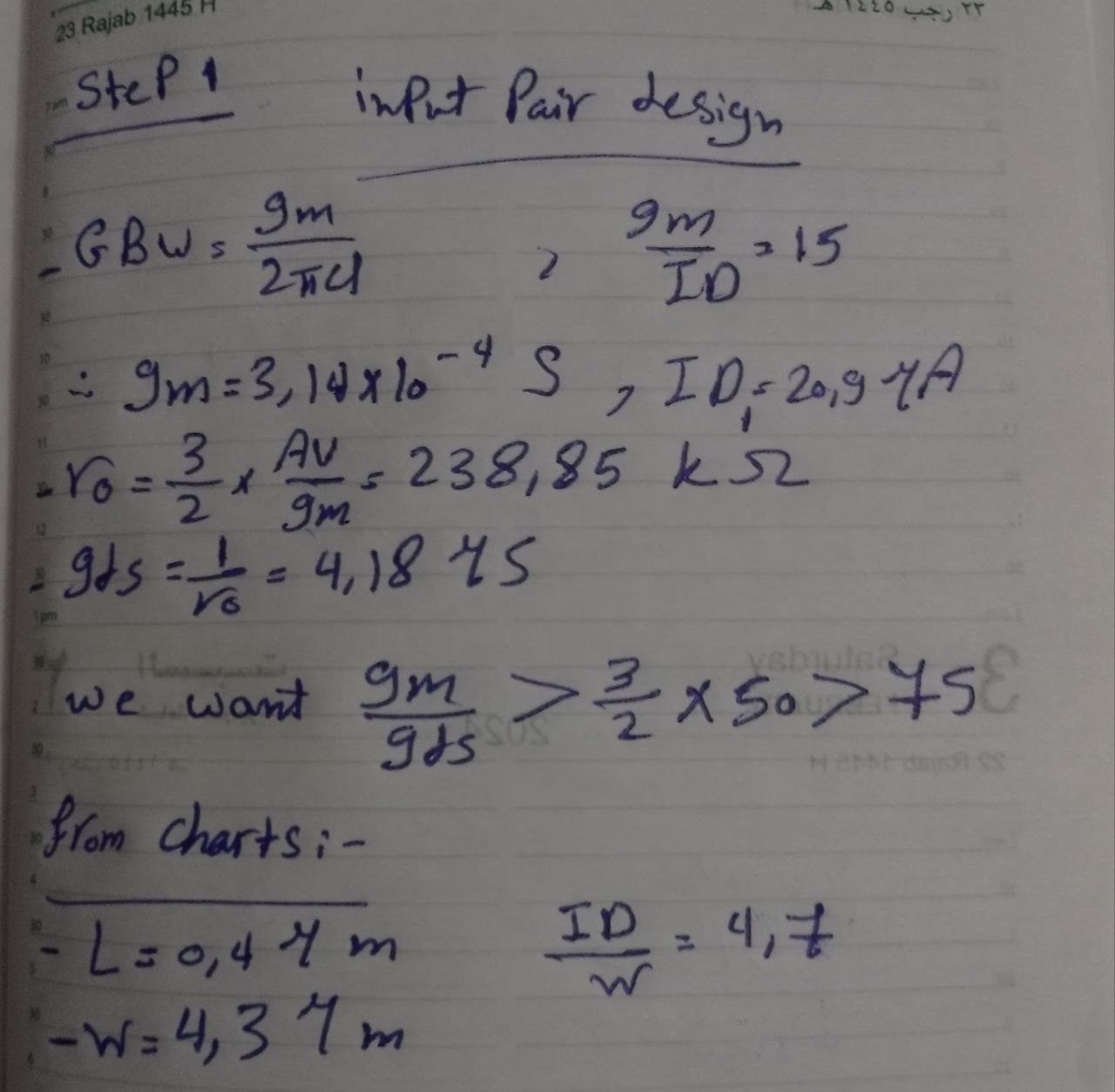
****

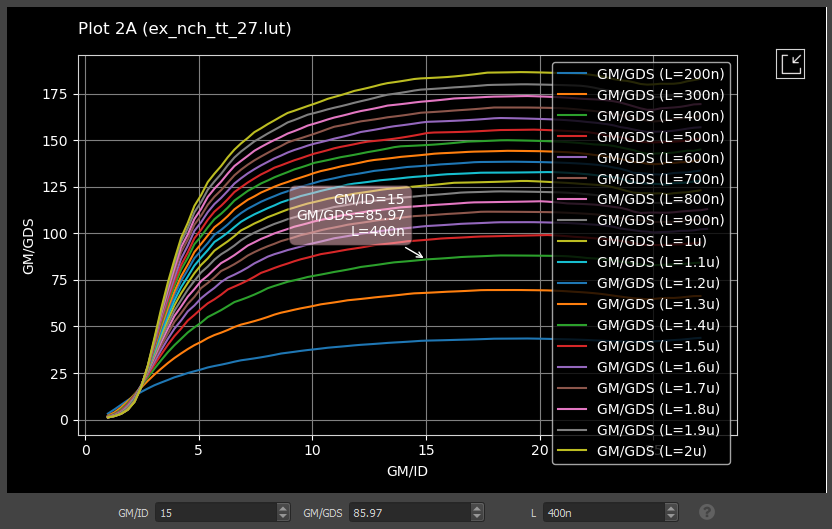


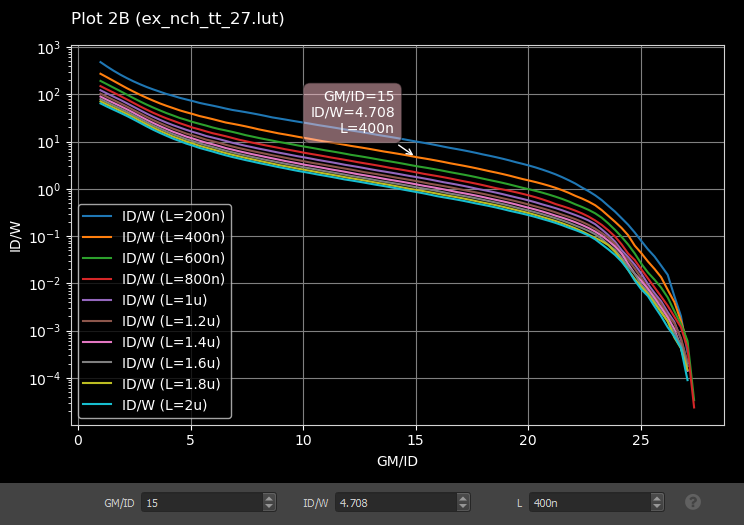
|  |  |  |
| --- | --- | --- |
| Parameter | Matlab | ADT |
| L min | 0.26 um | 0.25 um |
| VGS | 0.68 V | 0.6707 V |
| Id | 95.2 uA | 99.72 uA |

4-

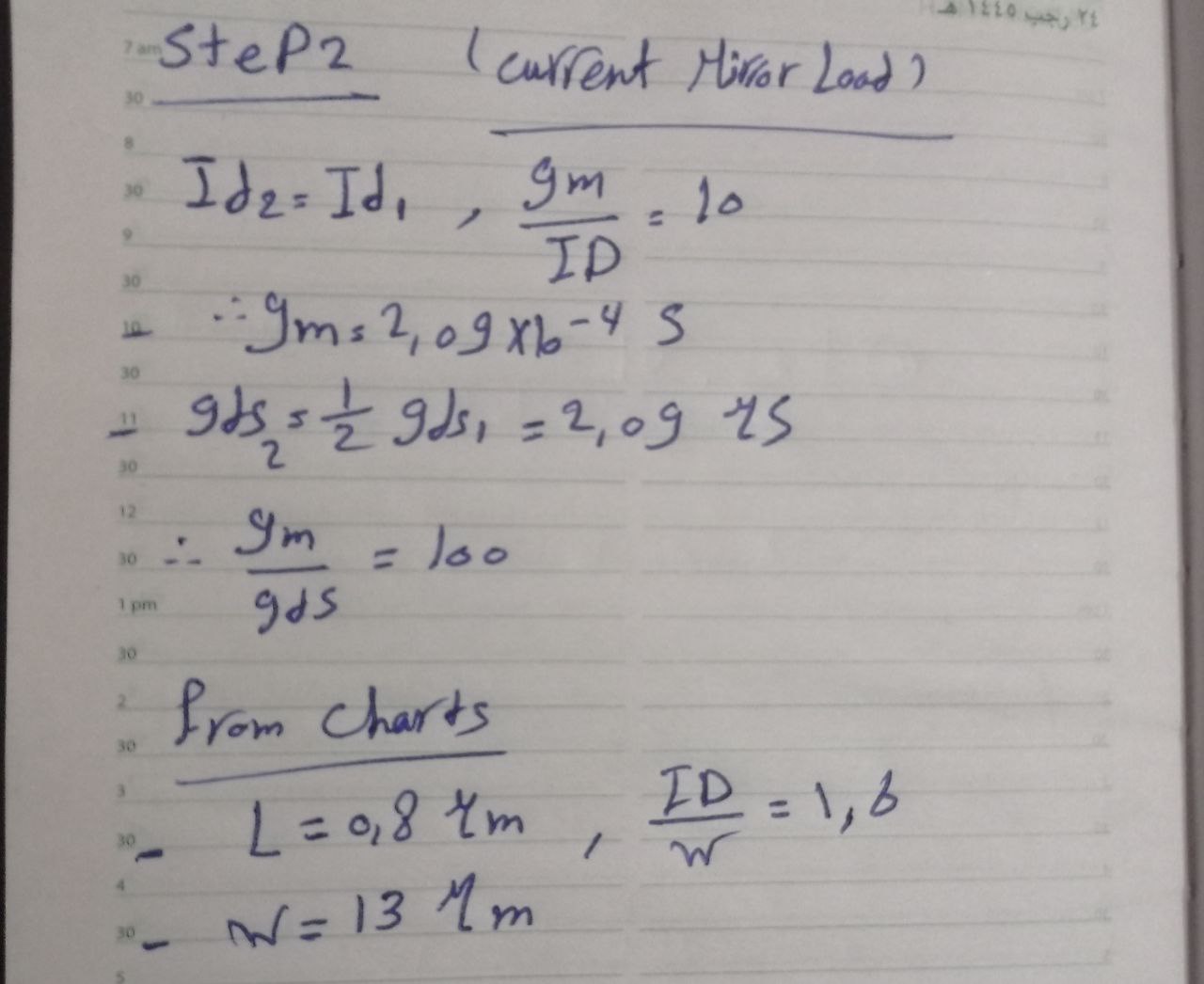
Input pair design

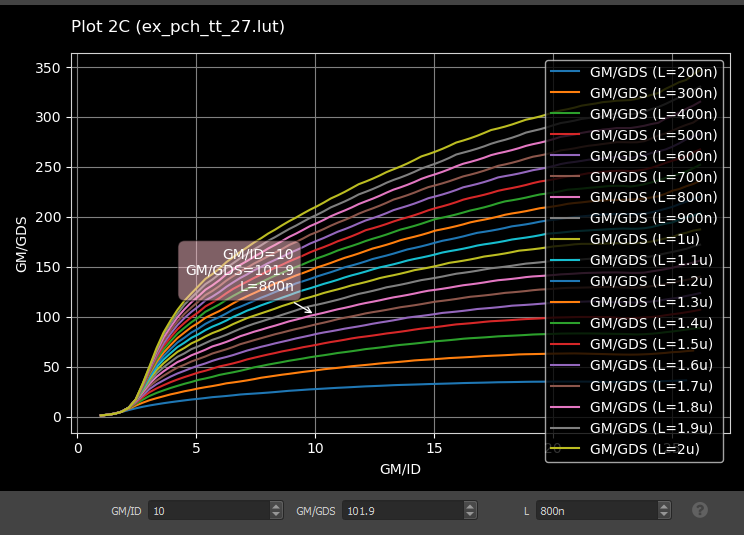


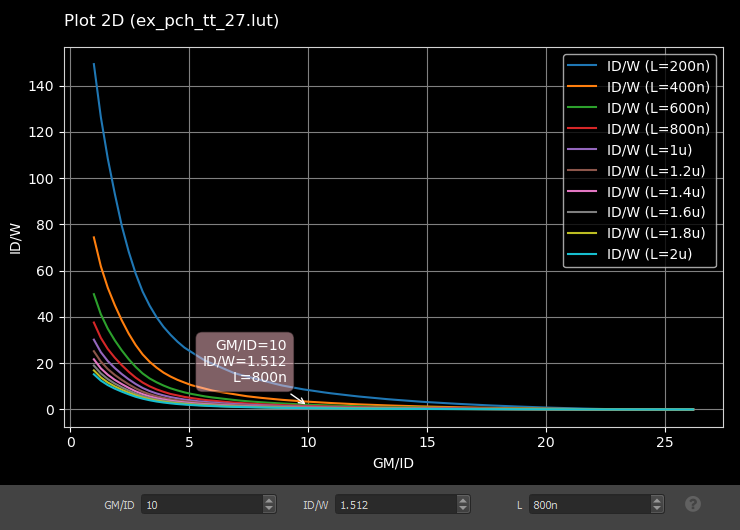




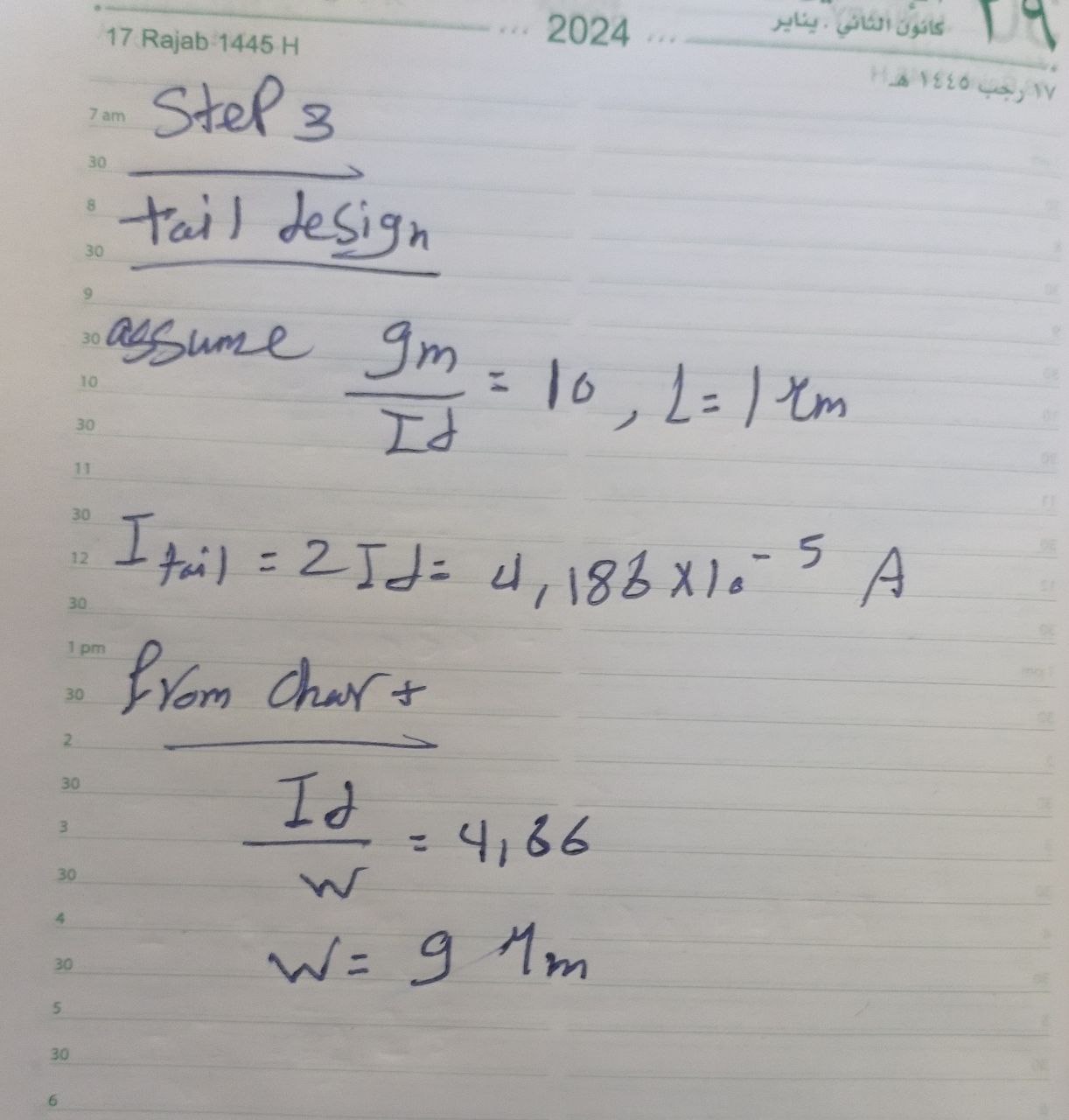
Load design :

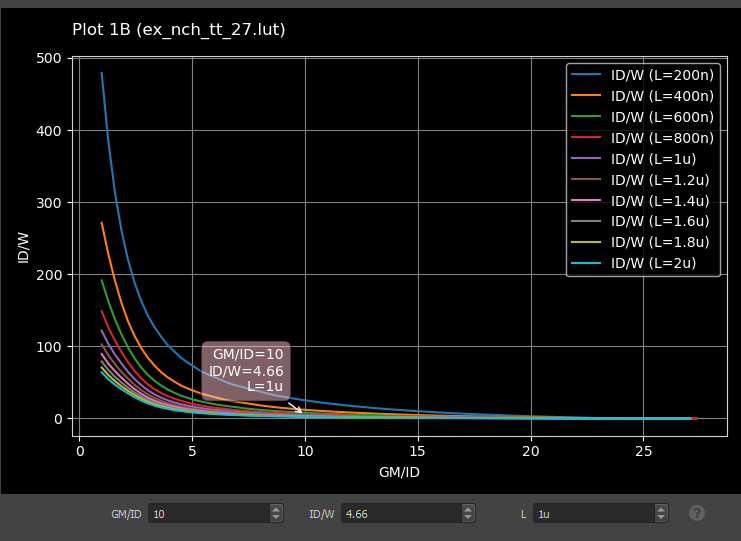






Tail design :





**gm/ID = 15 for the input pair and gm/ID = 10 for the load and the tail bias (why is this reasonable?)**

high gm/Id for the input pair to achieve High gm efficiency, better gain-bandwidth, low power and relatively low gm/Id for load and tail for Smaller area, adequate gm and low channel length modulation , good for current sources

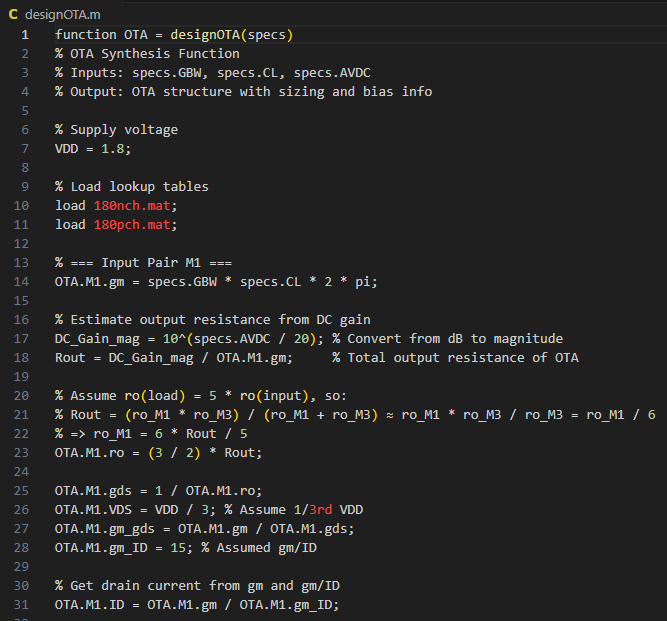
**ro of the load is two times ro of the input pair (why is this reasonable?).**

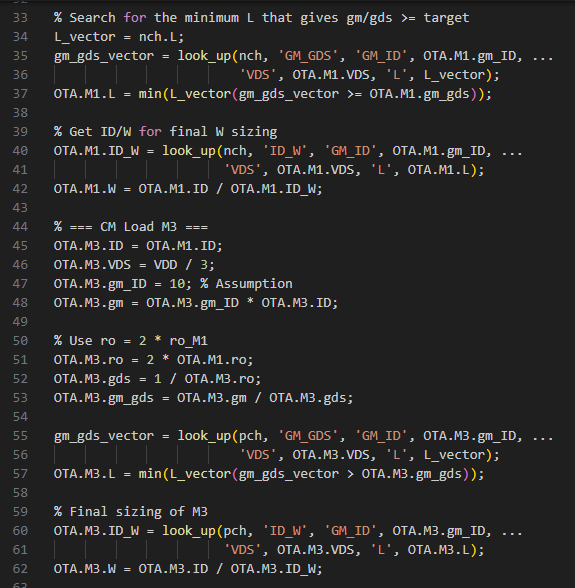
PMOS devices have lower mobility, so for the same current, they tend to have wider W, and a longer L . They also tend to have lower λ, so ro is higher.

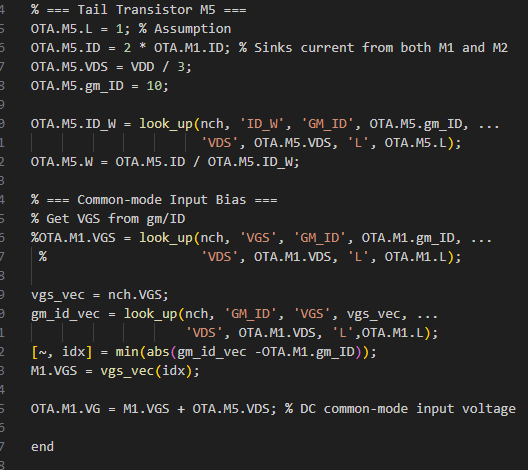
**L= 1um for the tail bias (why is this reasonable?).**

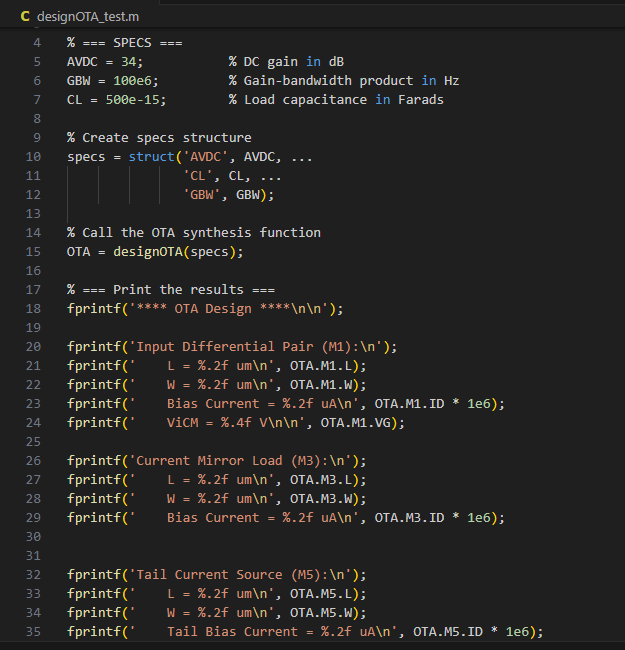
High L choice Improves ro and current source quality, helps robustness and matching

**DesignOTA.m**

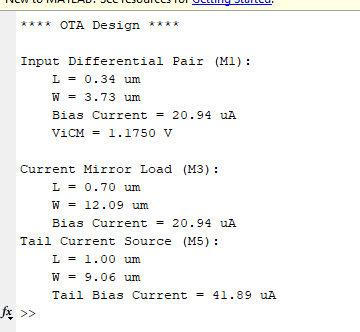


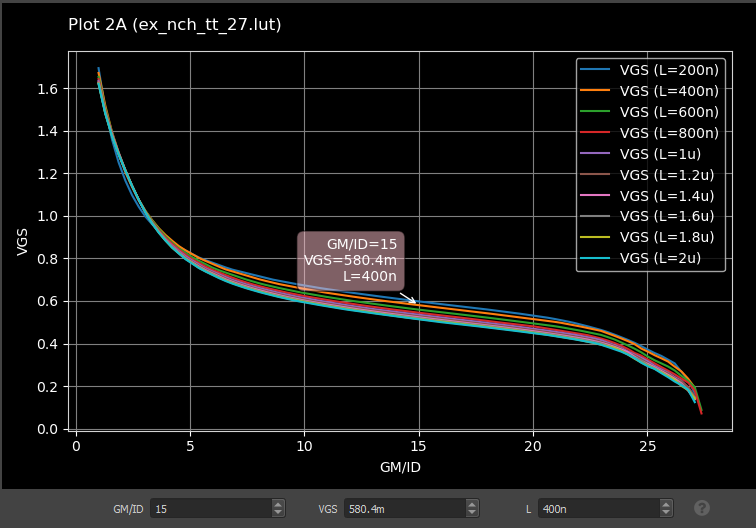


DesignOTATest.m



Matlab results :

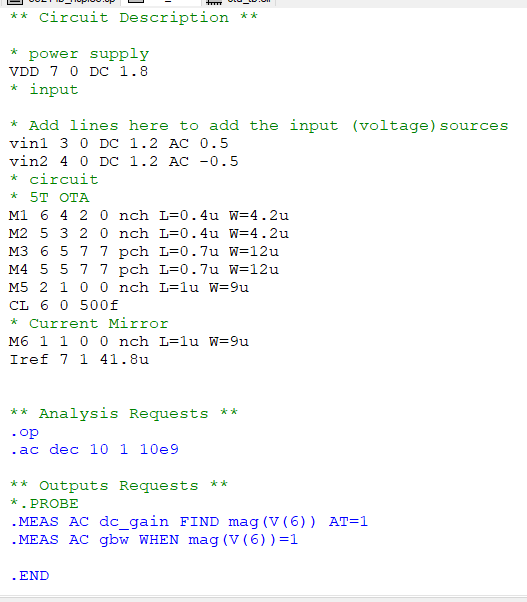


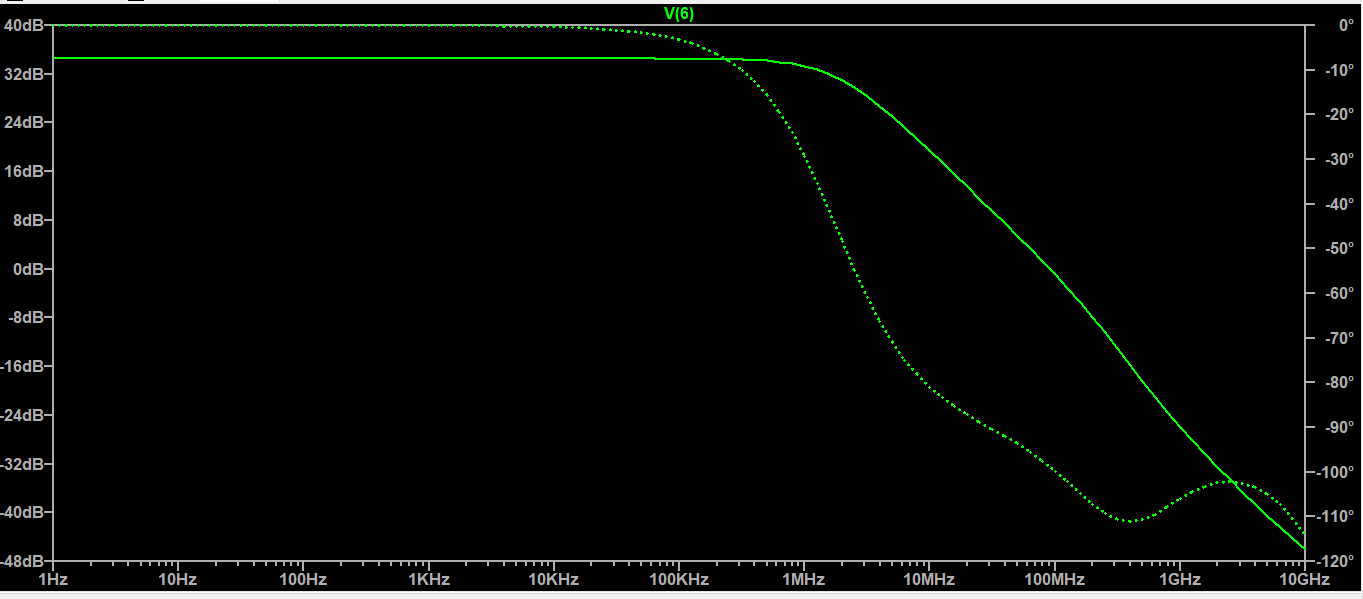


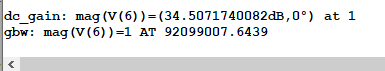
|  |  |
| --- | --- |
| **ADT** | **MATLAB** |
| L1= 0.4 um | L1= 0.34 um |
| W1= 4.3 um | W1= 3.73 um |
| L2 = 0.8 um | L2 = 0.7 um |
| W2 = 13 um | W2 = 12.09 um |
| W3 = 9 um | W3 = 9.06 um |
| I bias = 41.8 uA | I bias = 41.8 uA |
| VGS = 0.58 V | VGS =0.58 V |

7-

Netlist







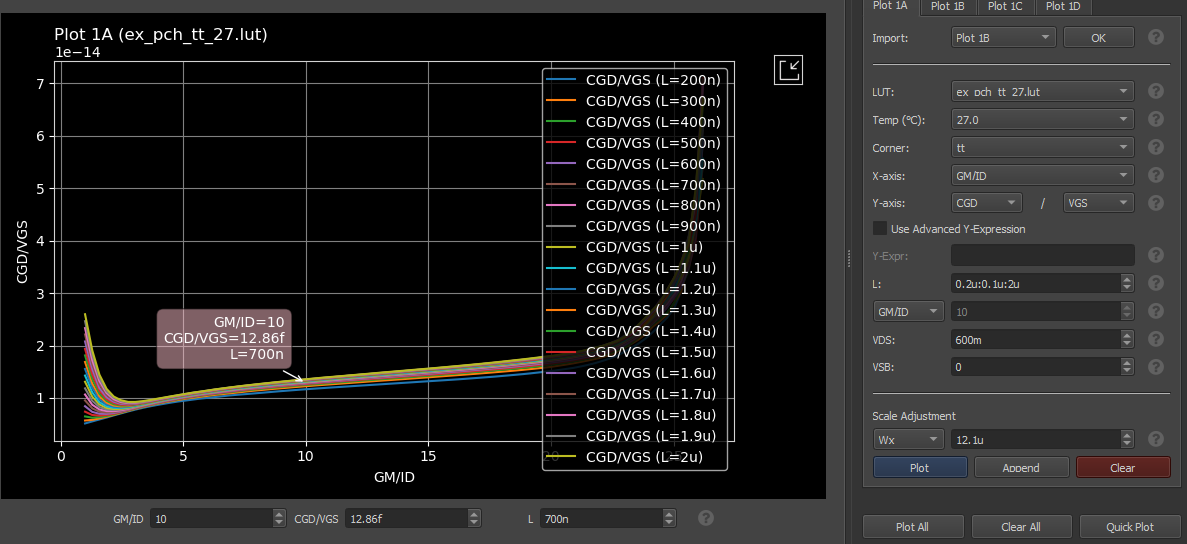
|  |  |
| --- | --- |
| Specs | LTSpice |
| DC Gain = 34dB | DC Gain = 34.5dB |
| GBW = 1MHz | GBW = 9.2MHz |

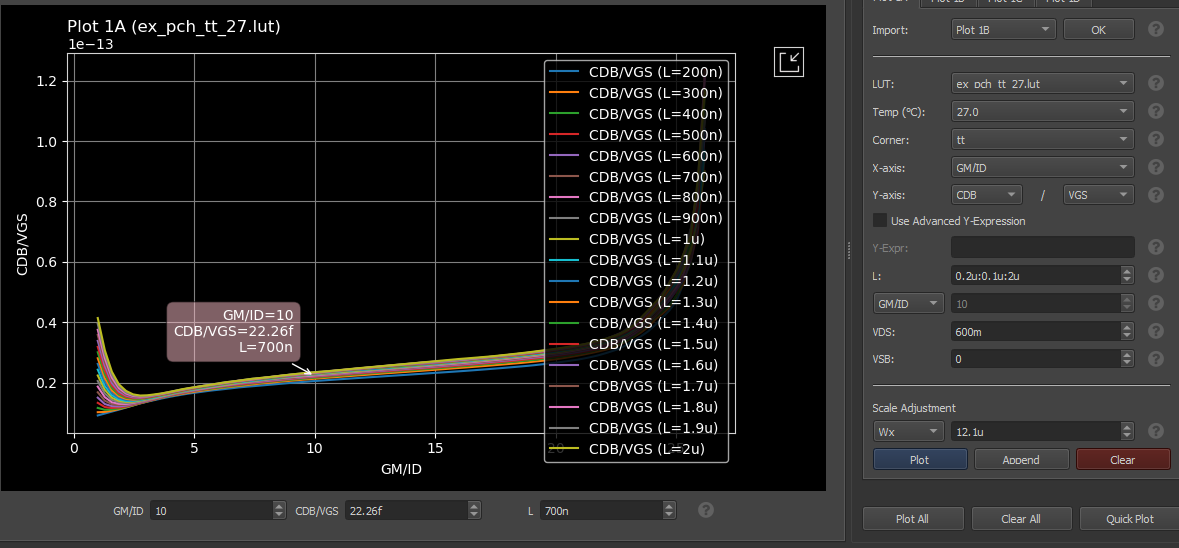
The simulator output of our design is nearly acheiving specs but not so accurate as we are ignoring the effect of VDS , self loading and body effect that can make the design more realistic .

Part 2:

To add self loading effect :

CDD = CGD + CDB





To get CDB and CGD we assume from part 1 that for the load PMOS

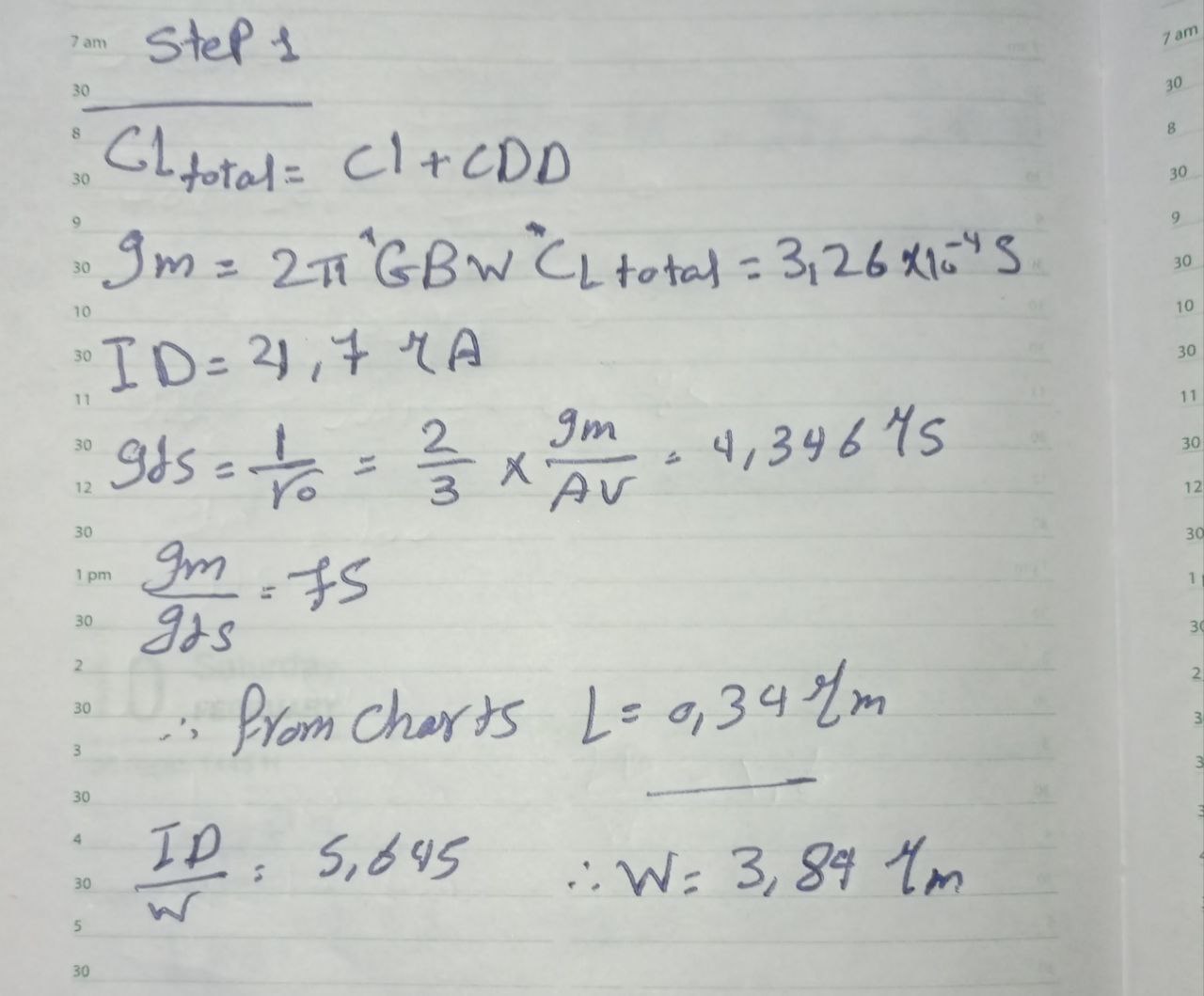
VGS= 0.58 V , L = 0.7um , W =12.1 um , VDS=0.6 V , GM/ID =10

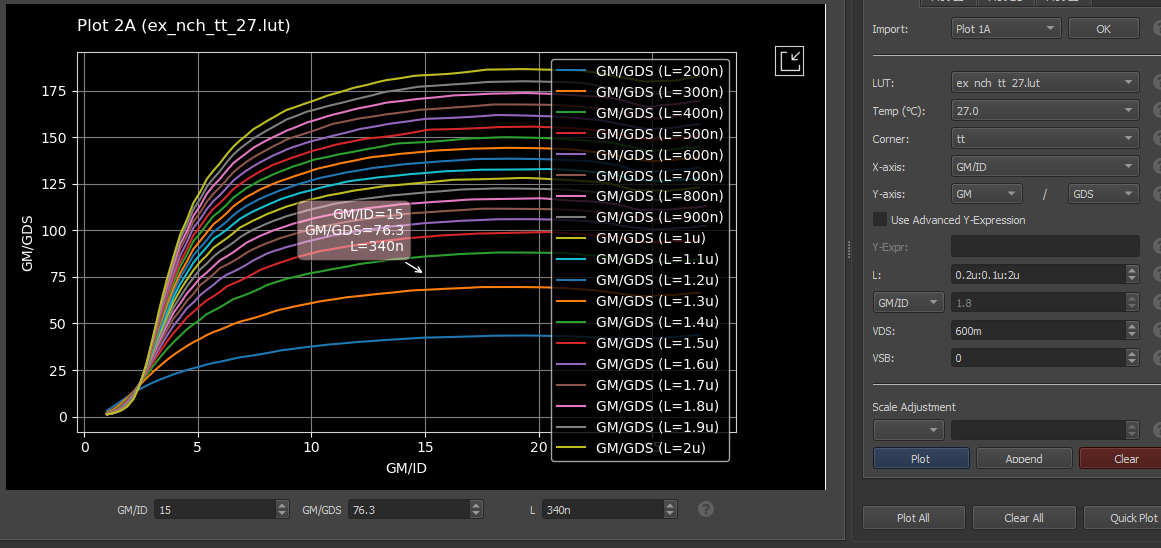
We get CGD= 7.5 Ff , CDB = 12.9 fF

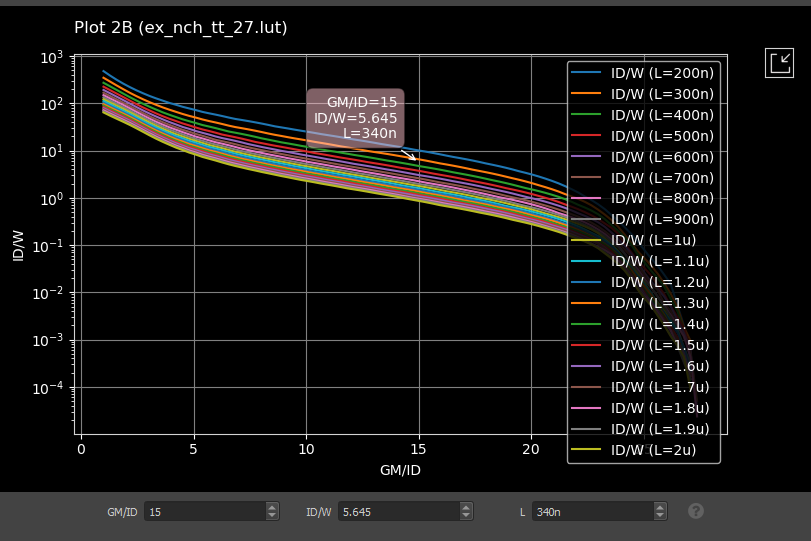
So CDD = = 7.5 + 12.9 = 20.4 fF

We add CDD to CL and do the analysis again.

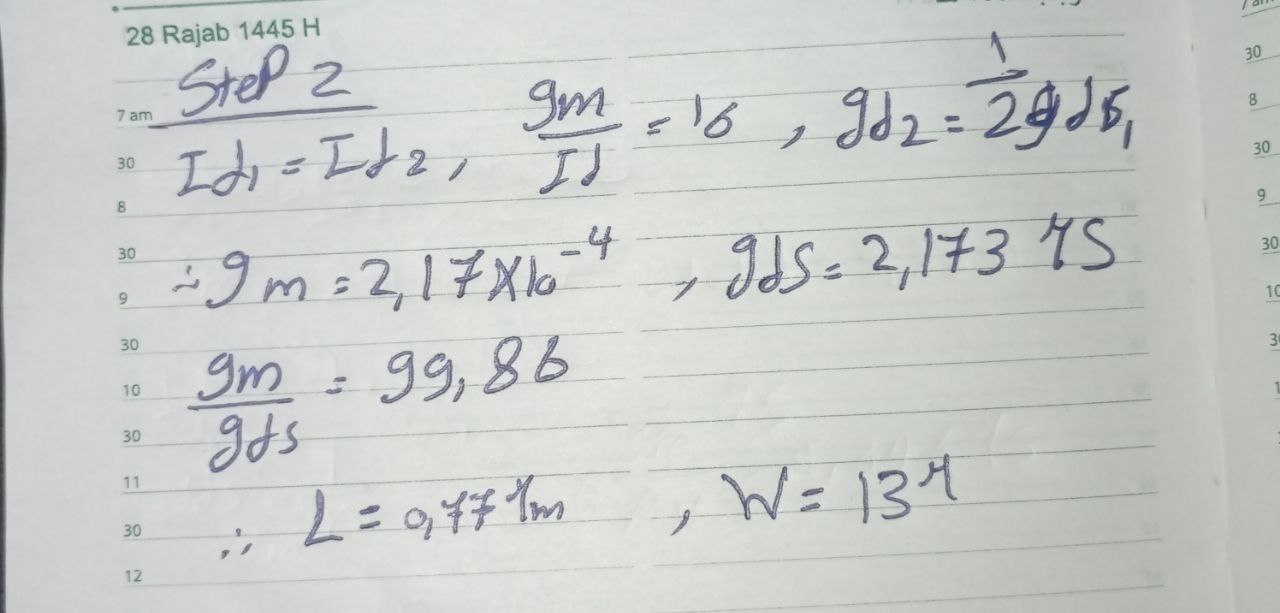
Input pair design:

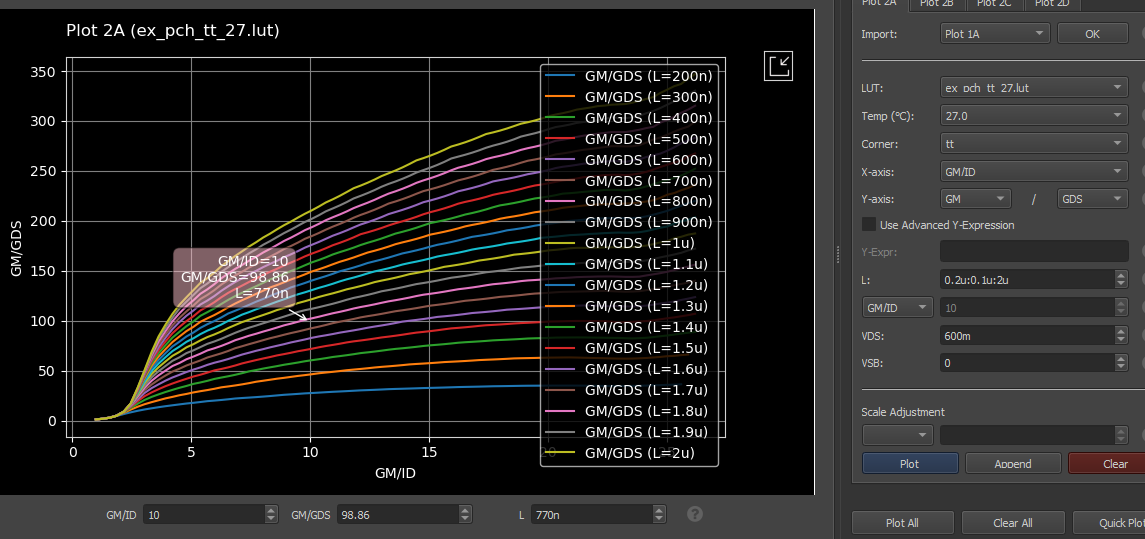


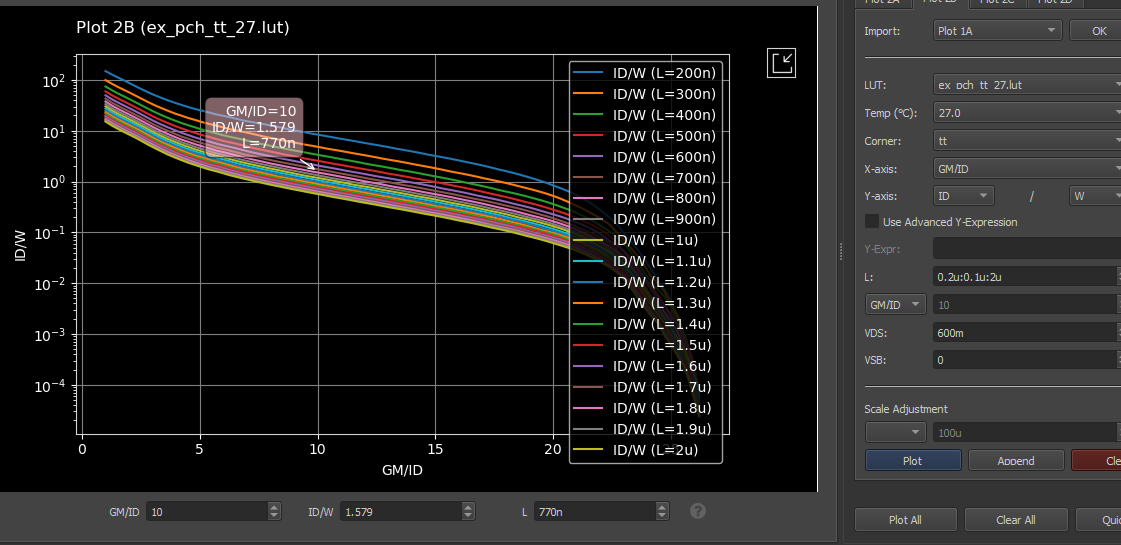




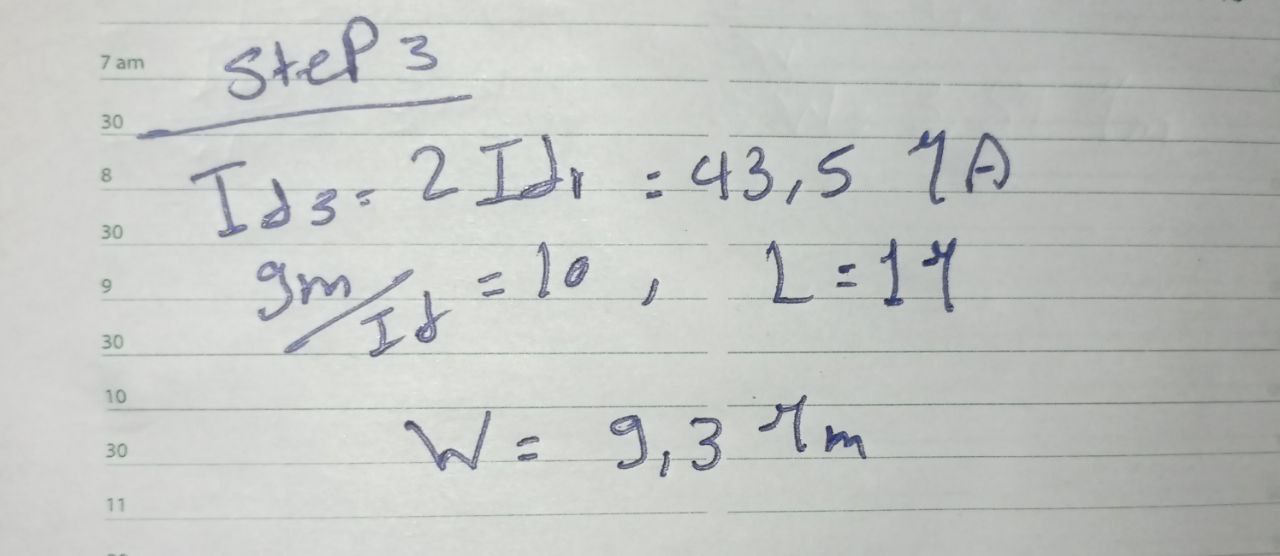
Load design:

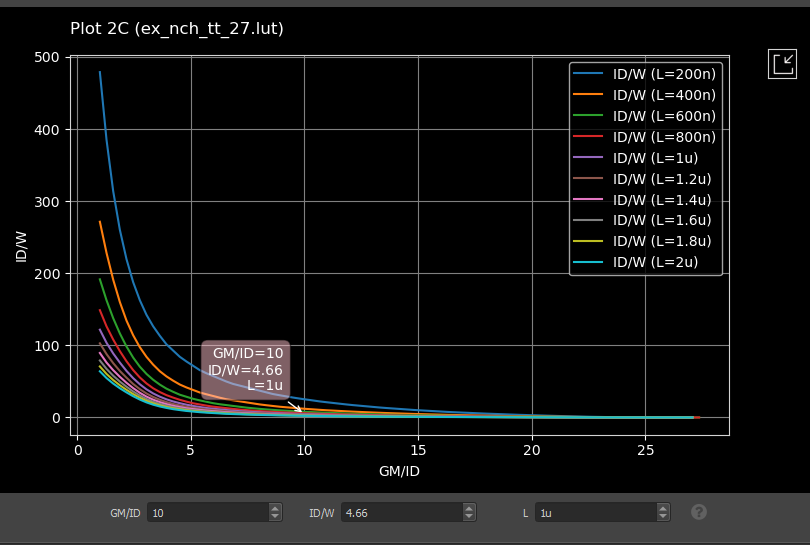






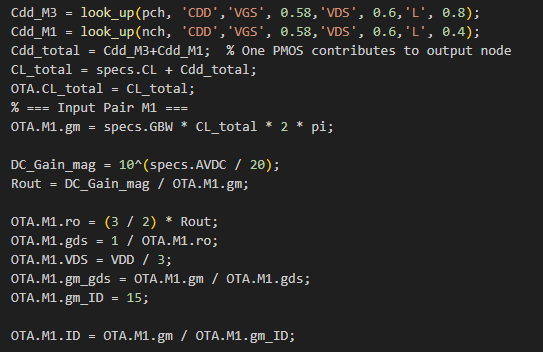
Tail current mirror design:

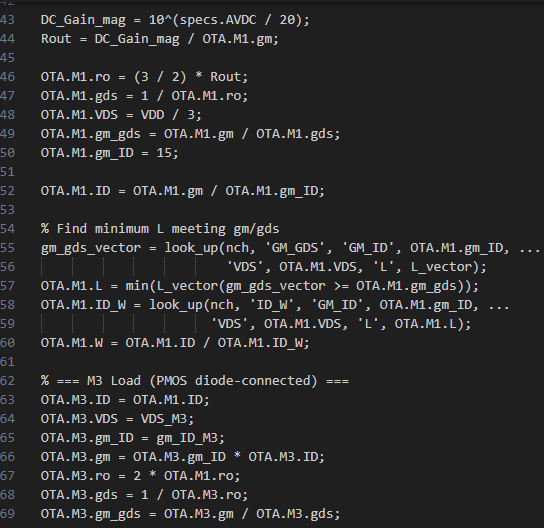


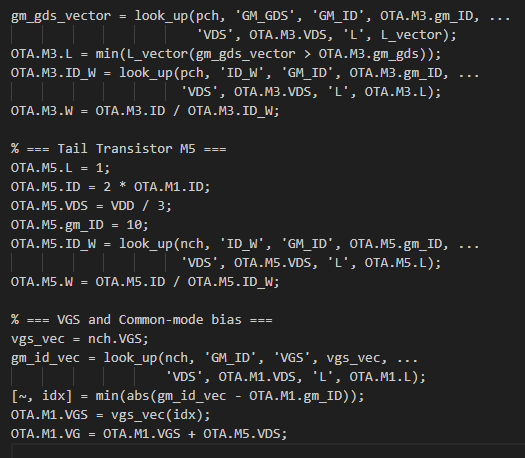


|  |  |
| --- | --- |
| **ADT part 1** | **ADT part 2** |
| L1= 0.4 um | L1= 0.34 um |
| W1= 4.3 um | W1= 3.89 um |
| L2 = 0.8 um | L2 = 0.77 um |
| W2 = 13 um | W2 = 13 um |
| W3 = 9 um | W3 = 9.3 um |
| I bias = 41.8 uA | I bias = 43.5 uA |
| VGS = 0.58 V | VGS =0.58 V |

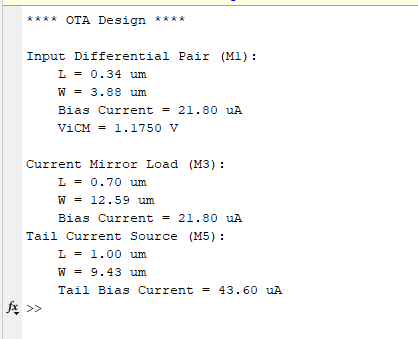
Matlab function:







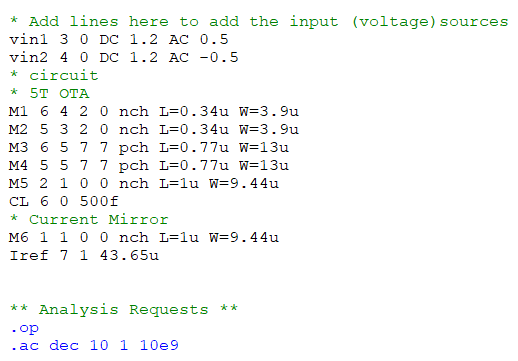
results:

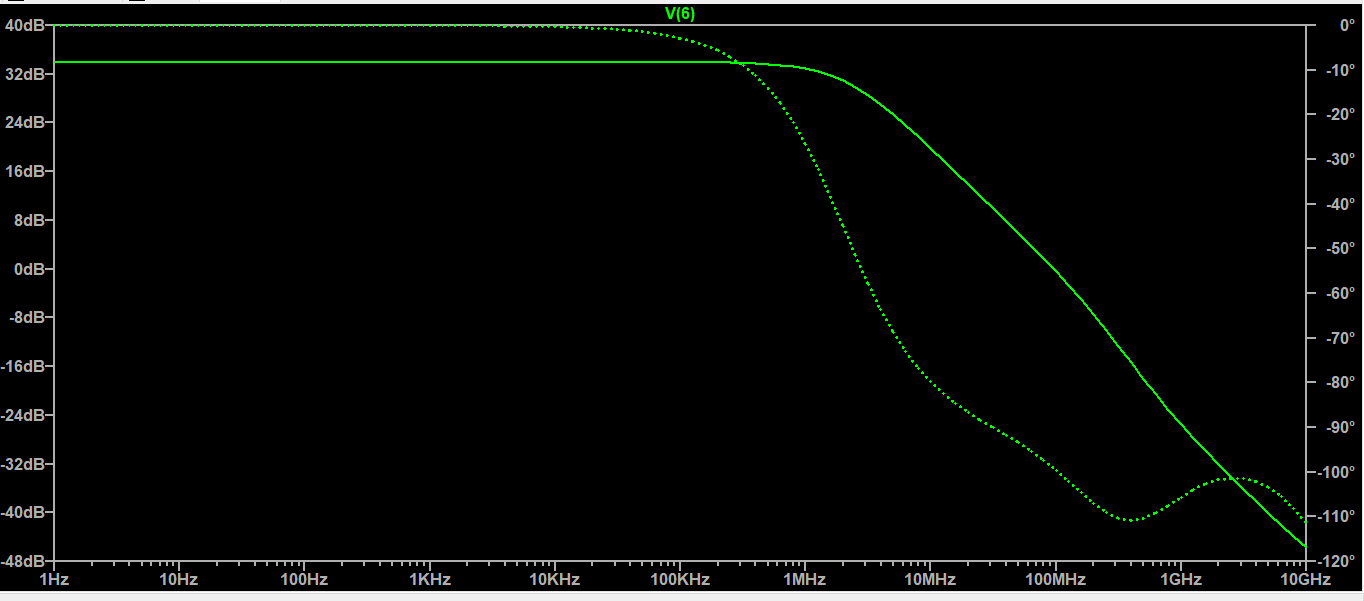


|  |  |
| --- | --- |
| **MATLAB part 2** | **MATLAB part 1** |
| L1= 0.34 um | L1= 0.34 um |
| W1= 3.88 um | W1= 3.73 um |
| L2 = 0.7 um | L2 = 0.7 um |
| W2 = 12.59 um | W2 = 12.09 um |
| W3 = 9.43 um | W3 = 9.06 um |
| I bias = 43.6 uA | I bias = 41.8 uA |
| VGS = 0.58 V | VGS =0.58 V |

|  |  |
| --- | --- |
| **ADT** | **MATLAB** |
| L1= 0.34 um | L1= 0.34 um |
| W1= 3.89 um | W1= 3.88 um |
| L2 = 0.77 um | L2 = 0.7 um |
| W2 = 13 um | W2 = 12.59 um |
| W3 = 9.3 um | W3 = 9.43 um |
| I bias = 43.5 uA | I bias = 43.6 uA |
| VGS =0.58 V | VGS = 0.58 V |

LTSpice:







|  |  |
| --- | --- |
| Specs | LTSpice |
| DC Gain = 34dB | DC Gain = 34.09dB |
| GBW = 1MHz | GBW = 9.6MHz |

We can see that the obtained design became more accurate and near to the specs after adding effect of self loading and it could be more accurate if we added effect of body effect and VDS