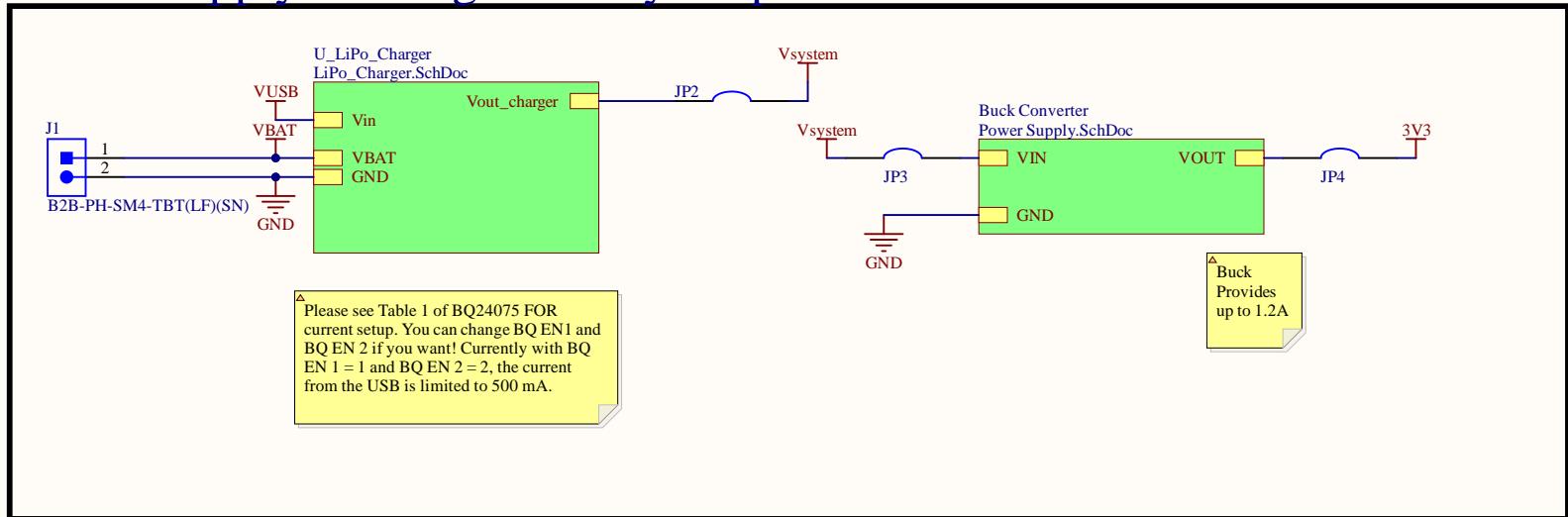


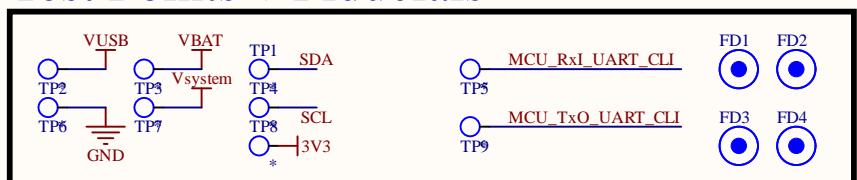
Power Supply - Change me to your power architecture



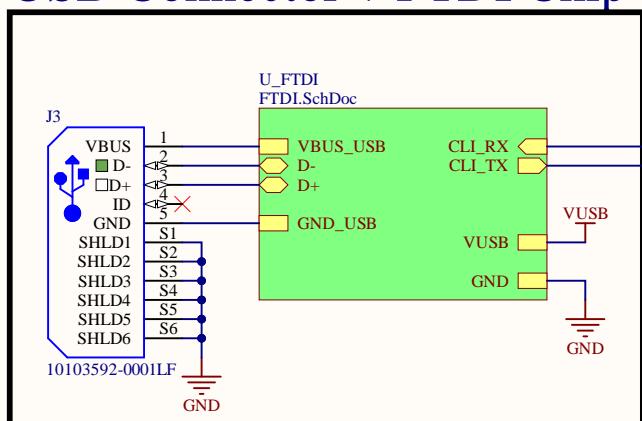
Notes

Section to add version notes or any other general information

Test Points + Fiducials

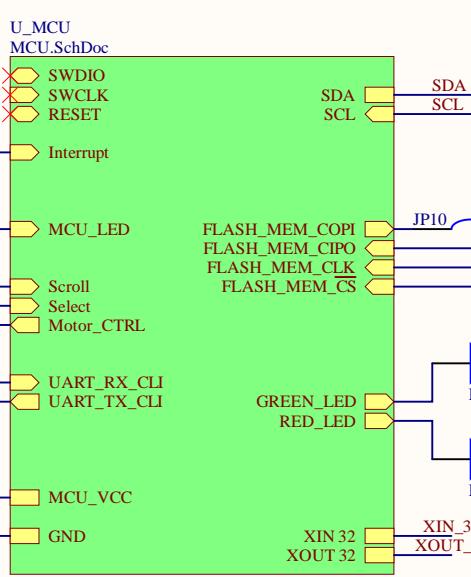


USB Connector + FTDI Chip

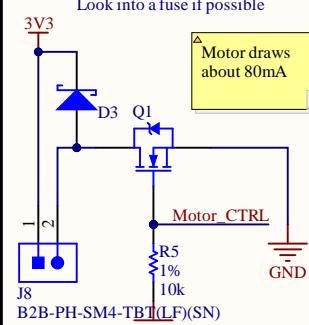
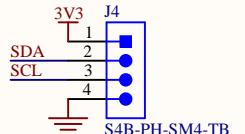


NOTE:
The FTDI Chip is an useful chip that allows us to convert USART messages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board). The FTDI device also contains protection circuitry for the USB.

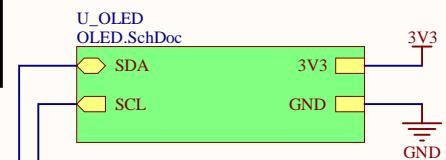
Microcontroller



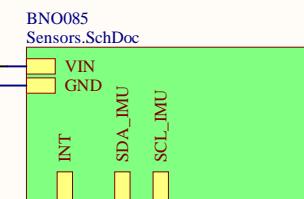
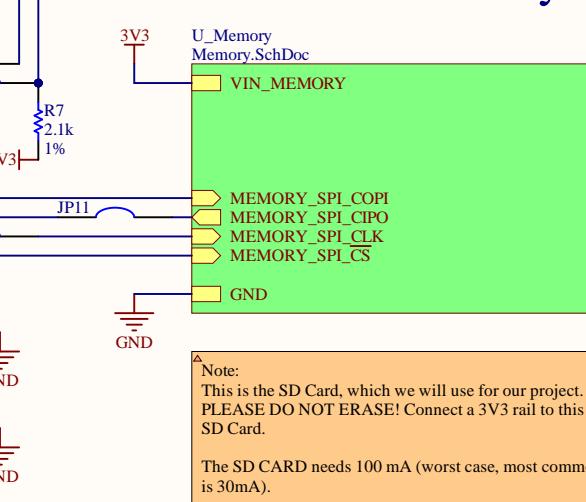
Note: Only the required pins are exposed for the MCU. Remember to add the ports for the pins you need to be exposed!



OLED



SD Card Memory



Title: **Main.SchDoc**

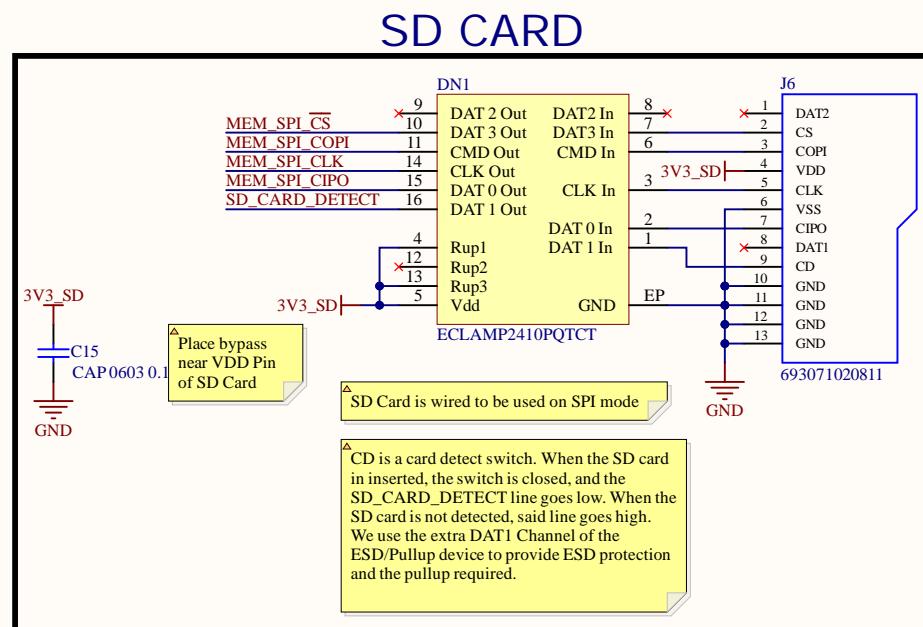
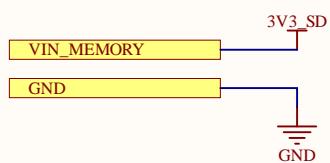
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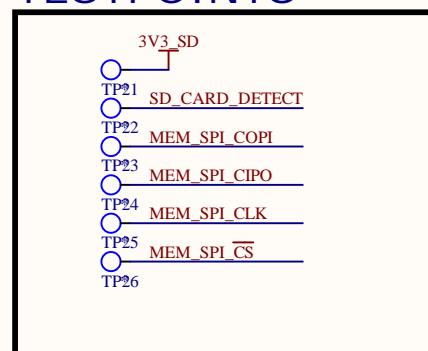
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File: C:\Users\Public\Documents\Altium\BlissAlarm\Main.SchDoc



C

TESTPOINTS



D

Title: **Memory.SchDoc**

Desc:

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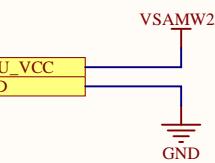
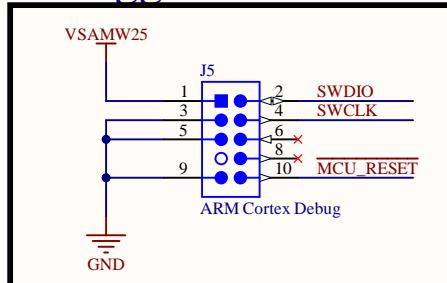
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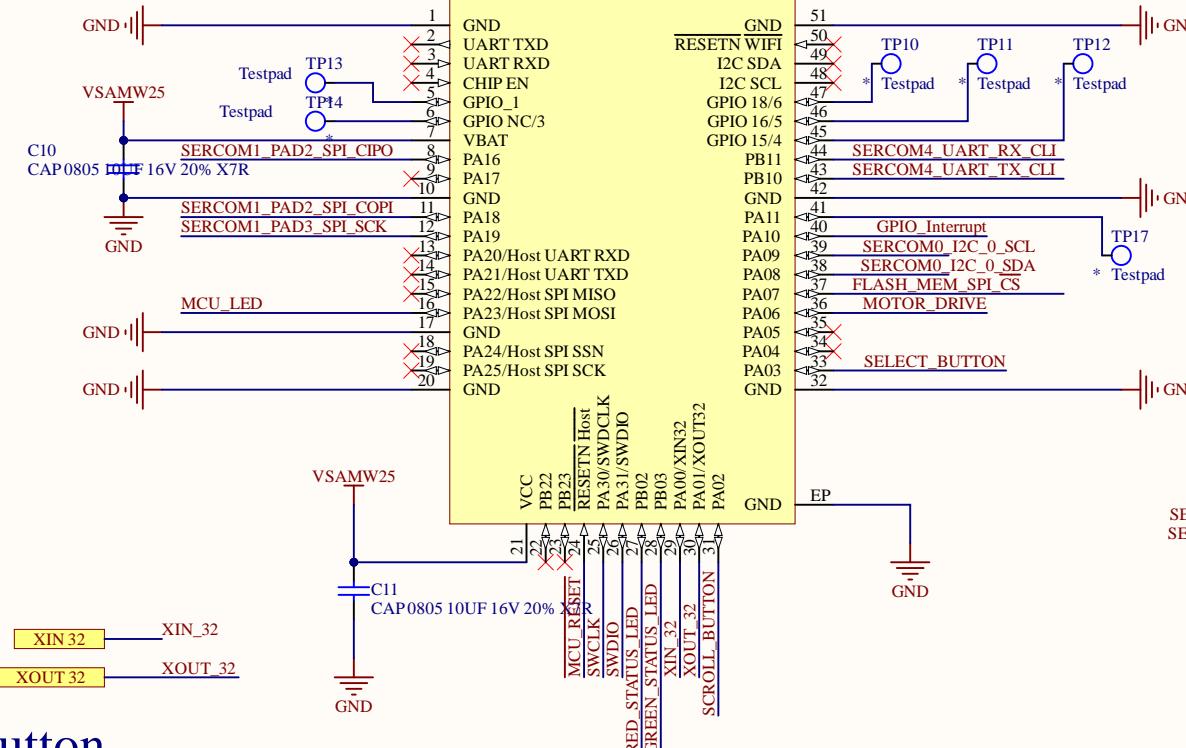
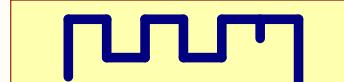
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Electrical and Systems Engineering

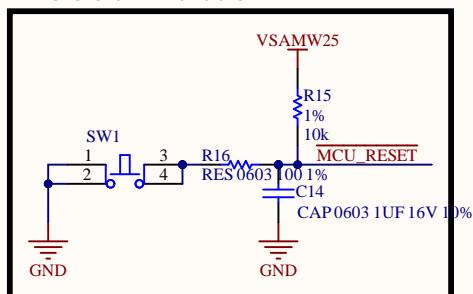
Debugger Port



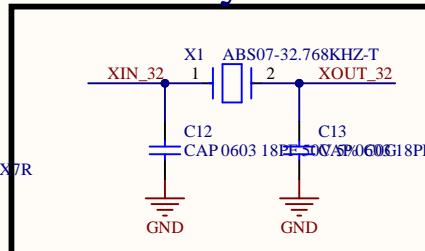
U2 ATSAMW25H18-MR210



Reset Button



32.768 Crystal



△ Calculation of crystal load capacitors:
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$
 $C_{crystal} = 12.5\text{pF}$ (from crystal datasheet)
 $C_{para} = 3.15\text{pF}$ (from MCU datasheet)
 $C_{pcb} = 0.5\text{pF}$ (estimate)
 $C_{ext} = 2 \times (12.5\text{pF} - 3.15\text{pF} - 0.5\text{pF}) = 17.7\text{pF}$

Title: **MCU.SchDoc**

Desc:

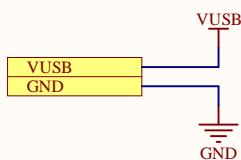
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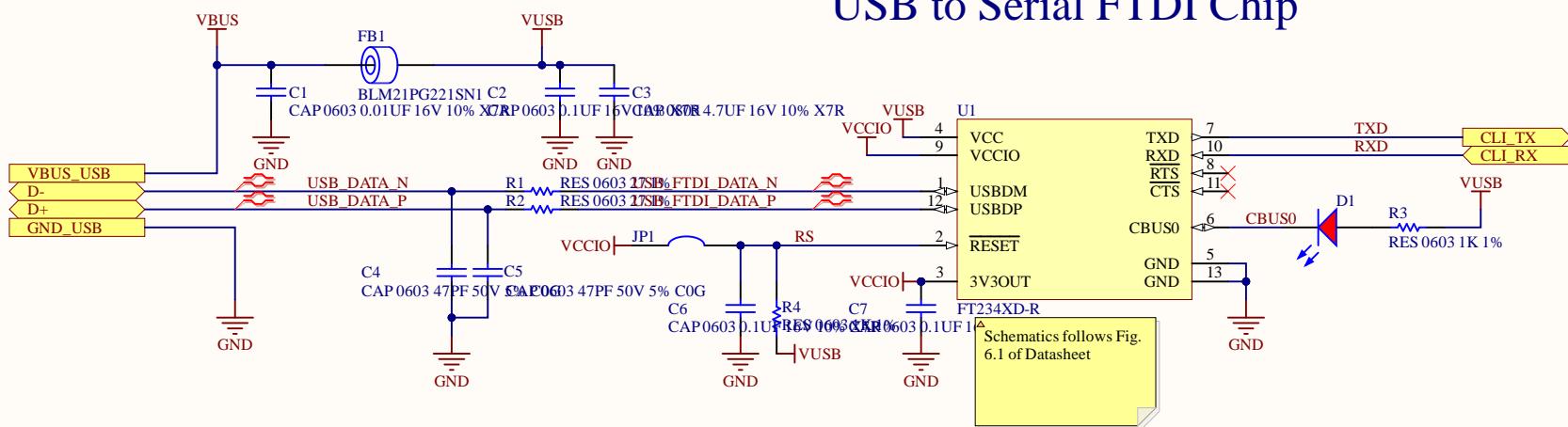
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A

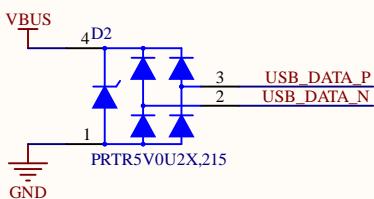


B



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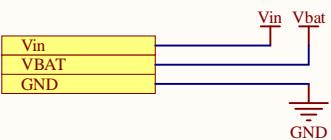
USB ESD Protection



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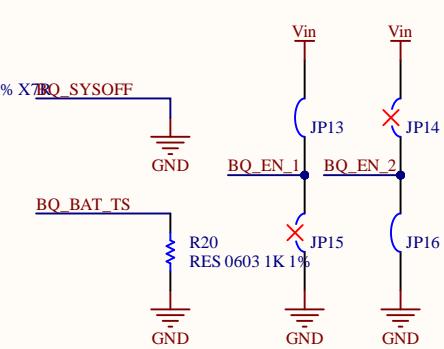
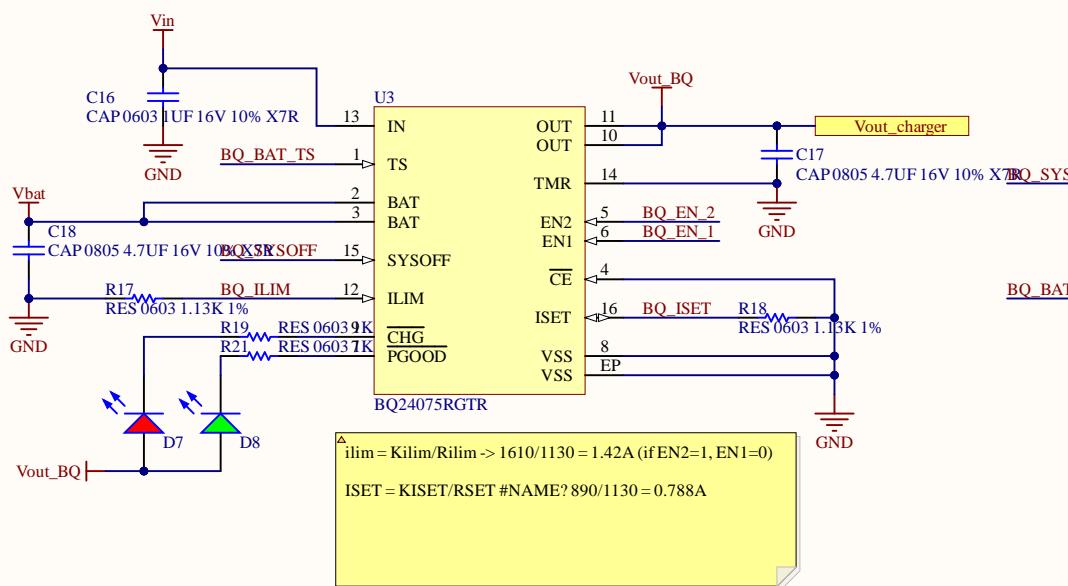
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D

Title: LiPo_Charger.SchDoc

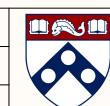
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Date: 10/17/2023 1:38:47 AM AD Ver. 23.8.1.32 Doc. * Sheet 5 of 7

File: C:\Users\Public\Documents\Altium\BlissAlarm\LiPo_Charger.SchDoc



Penn
Engineering
UNIVERSITY OF PENNSYLVANIA

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Electrical and Systems Engineering

A

A

B

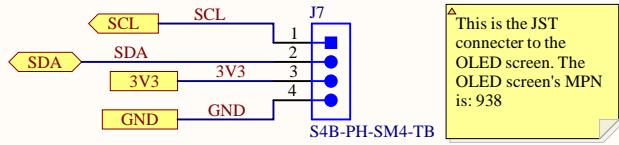
B

C

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D



This is the JST connector to the OLED screen. The OLED screen's MPN is: 938

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Desc:					
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Date: 10/17/2023 1:38:47 AM	AD Ver. 23.8.1.32	Doc. *	Sheet *	of *	www.seas.upenn.edu
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A

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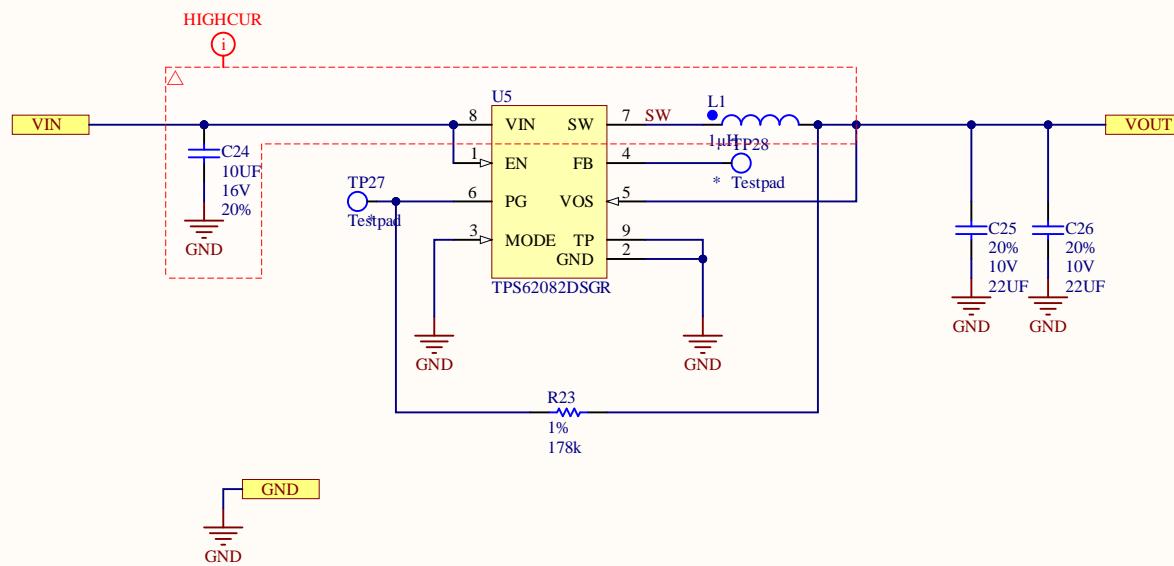
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C

C

D

D



Title: **Power Supply.SchDoc**

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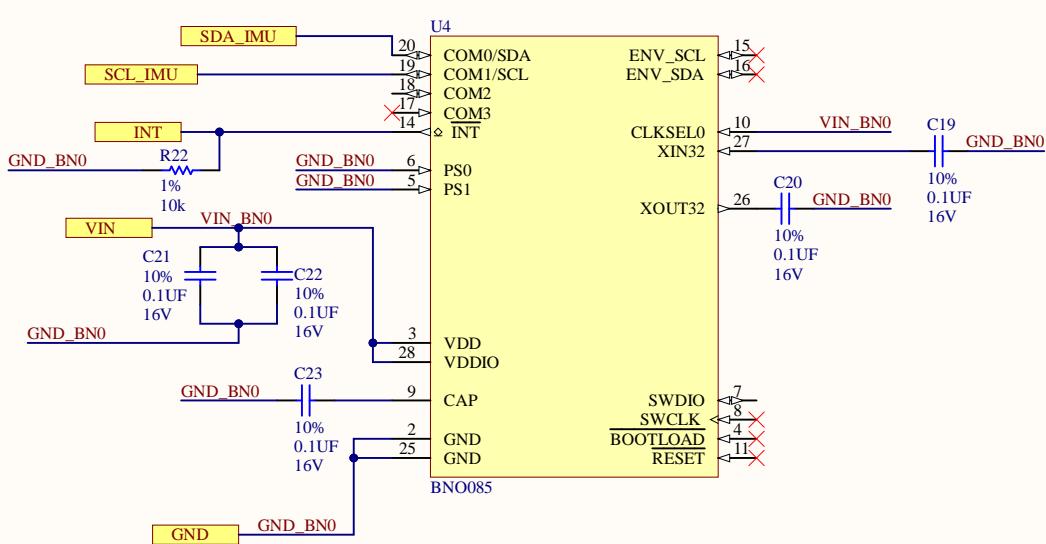
Electrical and Systems Engineering

A

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Title: Sensors.SchDoc		
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VCS: dd06c04858f5c9c244b08896d6ec19e06143508b [No modification]		
Date: 10/17/2023 1:38:47 AM AD Ver. 23.8.1.32 Doc. * Sheet * of *		
File: C:\Users\Public\Documents\Altium\BlissAlarm\Sensors.SchDoc		



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Electrical and Systems Engineering

Manufacturing Notes:

Four (4) Layers

Dimensions: 60mm x 60mm

Thickness: 1.53mm

Material: PP-006; Core-009

All layers are unmirrored - should be able to "see straight through"

Scoring: Yes

Finished Thickness: 1.53mm

Surface Finish: ENIG

Gold Fingers: Yes

Outer Layer Finish Copper: 1oz

Inner Copper: 0.5oz

Number of Holes Per Board: _____

Minimum Hole size: 0.20mm

Minimum Trace (Outer layer): 6mil

Minimum Space (Outer layer): 6mil

Minimum Trace (Inner layer): None (no Trace)

Minimum Space (Inner layer): None (no Trace)

Solder Mask: Yes

Solder Mask Sides: Top and Bottom

Solder Mask Color: Green

Solder Mask Type: LPI

Solder Mask Finish: Standard (Semi-Gloss)

Silk Screen: Yes

Logo Allowed: Silk Screen

Silk Screen Sides: Top and bottom

Silk Screen Color: N/A

Internal Slots: No

Counter Sink: No

Counter Bore: No

Edge Plating: No

Route and Retain: N/A

Scoring: N/A

Controlled Impedance: No

Controlled Dielectric: No

Thru-Hole Via in Pad: No

Thickness Tolerance: +/-10%

UL Marking Required: No

Rohs Marking: No

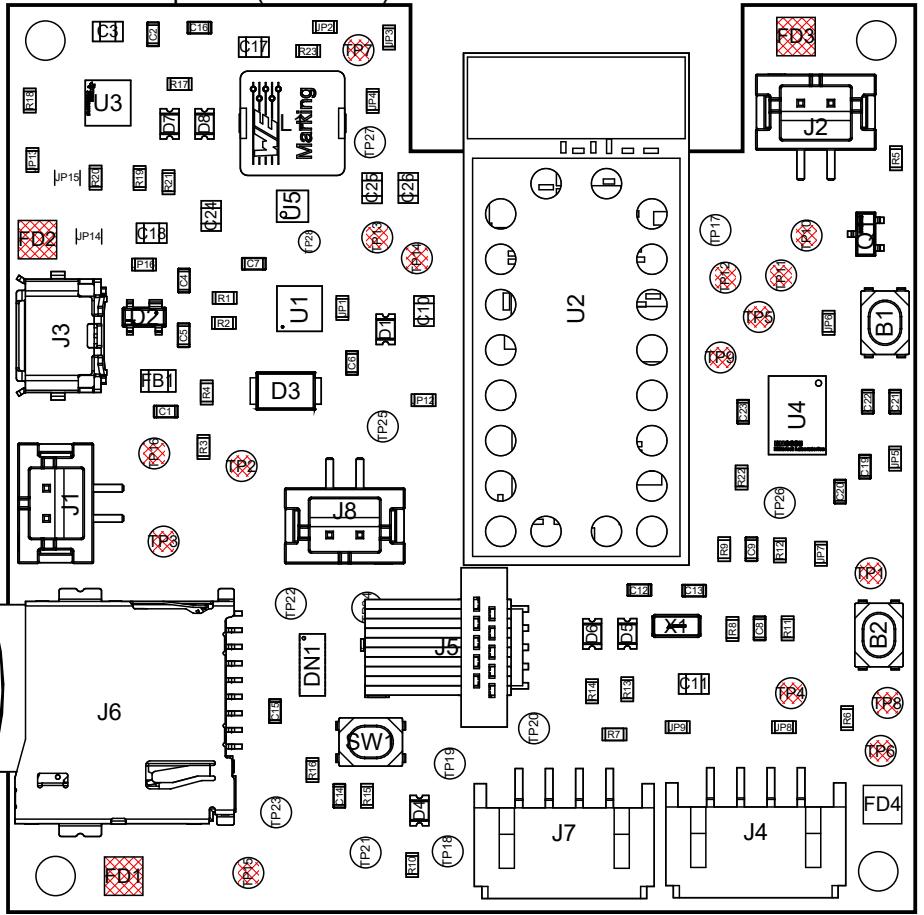
ITAR?: No

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
Surface Material	Top Overlay			Legend	GTO
Copper	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
Prepreg	Top Layer	0.04mm		Signal	GTL
CF-004	GroundPlane	0.33mm	PP-006	Dielectric	
Core	GroundPlane	0.02mm		Signal	G1
CF-004	PowerPlane	0.71mm	Core-009	Dielectric	
Prepreg	PowerPlane	0.02mm		Signal	G2
Copper	Bottom Layer	0.33mm	PP-006	Dielectric	
Surface Material	Bottom Solder	0.04mm		Signal	GBL
	Bottom Overlay	0.03mm	Solder Resist	Solder Mask	GBS
				Legend	GBO

Total thickness: 1.53mm

View from Top side (Scale 2:1)



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CHECKER: =PCB_CHECKER	=PCB_CHECKER		
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ASSY DOC: =DOC_NO_FAB_DWG			
SCH DOC: =DOC_NO_SCH_DWG			
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REV: 1			
SCALE: 1 OF 12	FILE NAME: StarterBoardFabrication.PCBDwf		

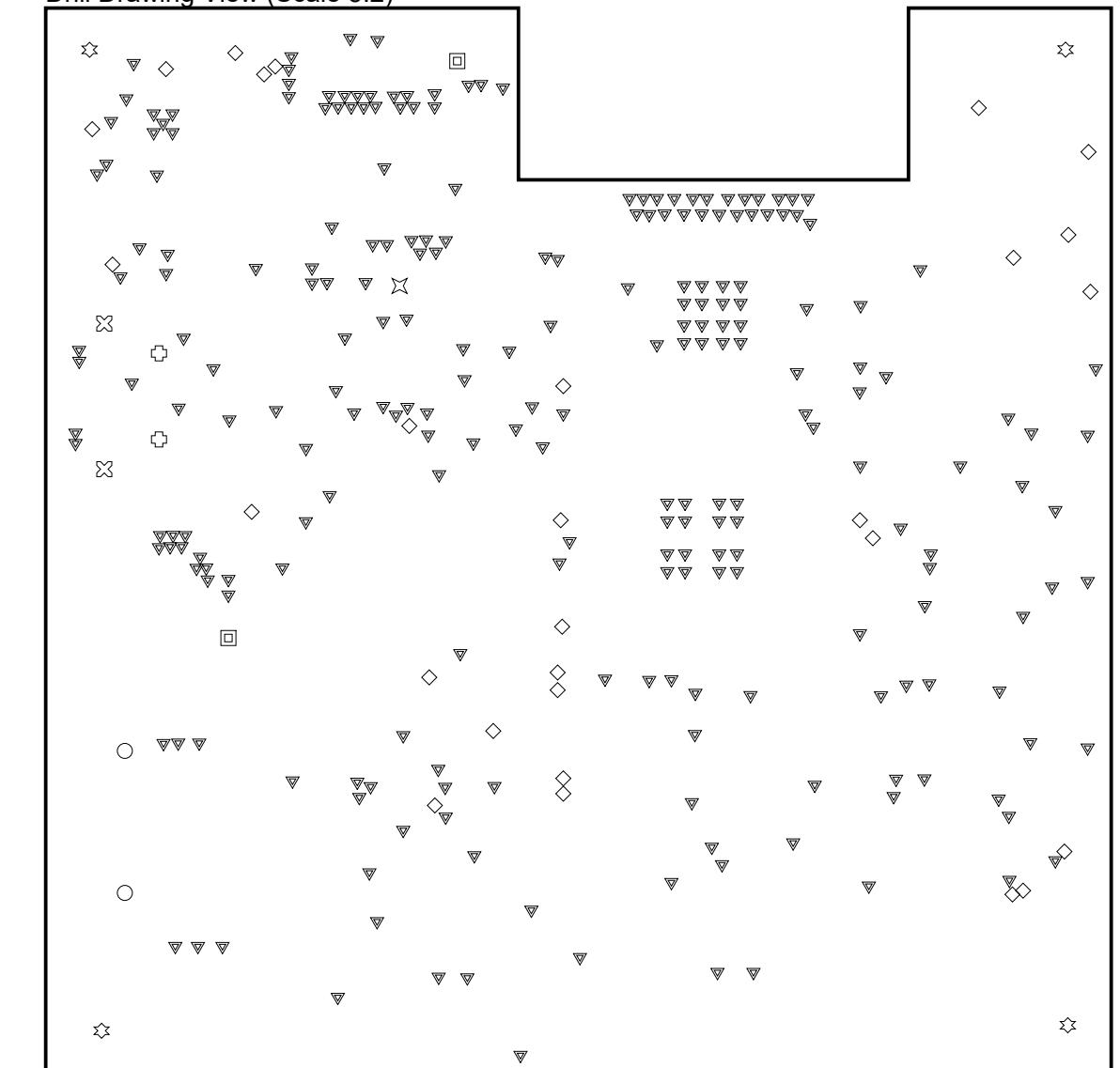
REV STATUS OF SHEETS		REV									
SHEET											

REVISIONS		DESCRIPTION	DATE	APPROVED

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
▽	241	0.20mm	Plated	
◇	28	0.30mm	Plated	
⊛	1	0.38mm	Plated	
✚	2	0.65mm	Plated	
▣	2	0.69mm	Plated	
✖	2	0.70mm	Plated	
○	2	0.90mm	Non-Plated	
⊛	4	2.70mm	Plated	
282 Total				

Drill Drawing View (Scale 5:2)



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APPROVALS DATE

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DESIGNER: =PCB_DESIGNER =PCB_DESIGNER

CHECKER: =PCB_CHECKER =PCB_CHECKER

Reference Documents

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
TM

220 S. 33rd St
Towne Bldg, B11
Philadelphia, PA 19104
USA

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DESIGN ITEM REVISION: .ItemRevision

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REV:

SCALE:

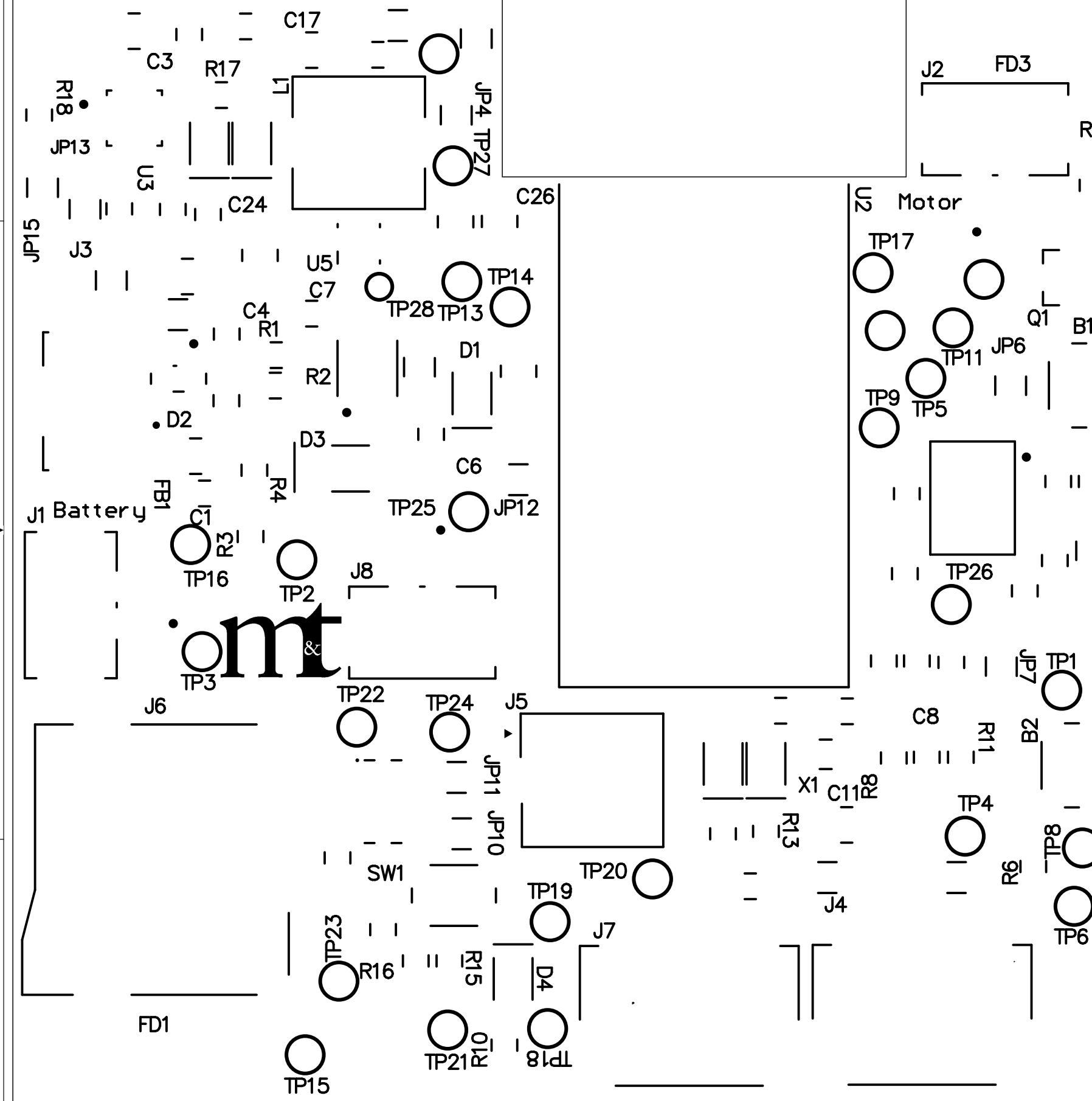
FILE NAME:

StarterBoardFabrication.PCBDwf

2 OF 12



Top Overlay (Scale 4:1)



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APPROVALS	DATE				
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Altium

A

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C

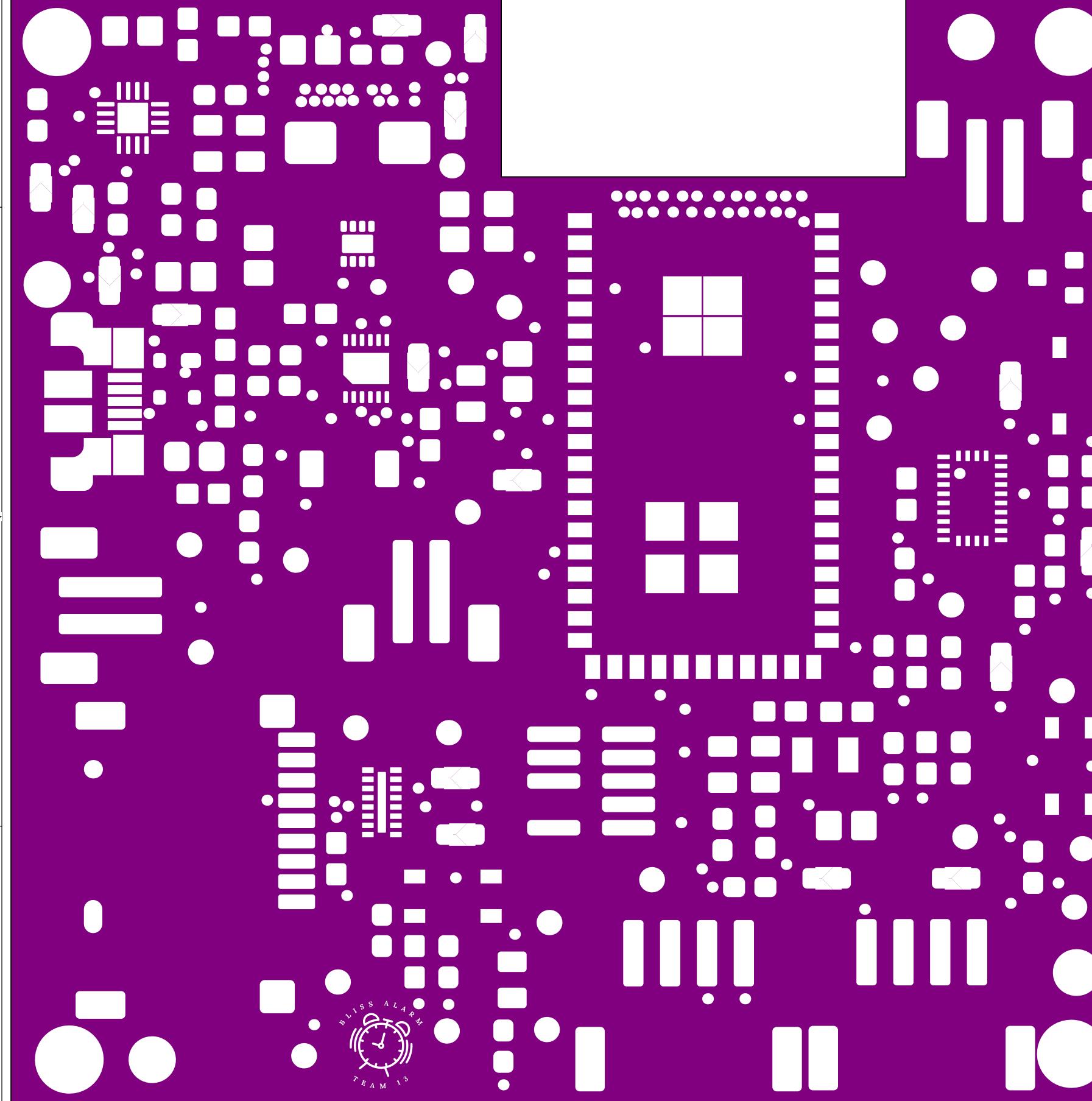
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Top Solder (Scale 4:1)

REV STATUS
OF SHEETSREV
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ZONE	REV

REVISIONS

DESCRIPTION DATE APPROVED

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NEXT ASSY	USED ON	PCB DOC:	=PCB_DWG_NO		
APPLICATION		FILE NAME: StarterBoardFabrication.PCBDwf			SCALE: 4 OF 12

Altium
220 S. 33rd St
Towne Bldg, B11
Philadelphia, PA 19104
USA

DESIGN ITEM: .Item DESIGN ITEM REVISION: .ItemRevision

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SIZE: CAGE CODE: DWG NO: B =CAGE_CO REV:

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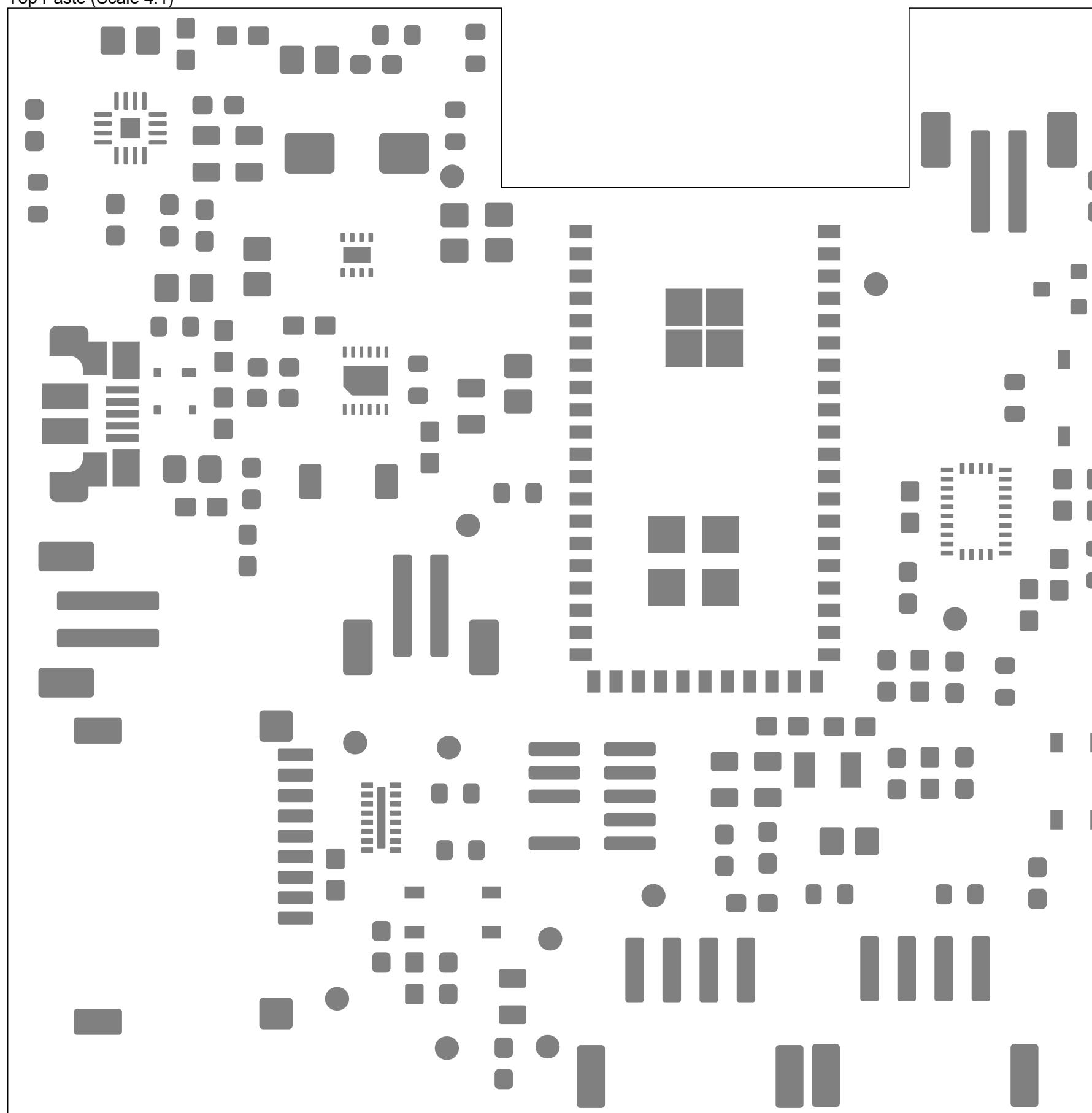
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Top Paste (Scale 4:1)



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Reference Documents

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ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

NEXT ASSY USED ON

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APPLICATION

Altium
TM

 220 S. 33rd St
 Towne Bldg, B11
 Philadelphia, PA 19104
 USA

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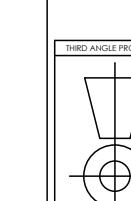
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REV:



SCALE: FILE NAME: StarterBoardFabrication.PCBDwf SHEET: 5 OF 12

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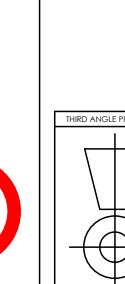
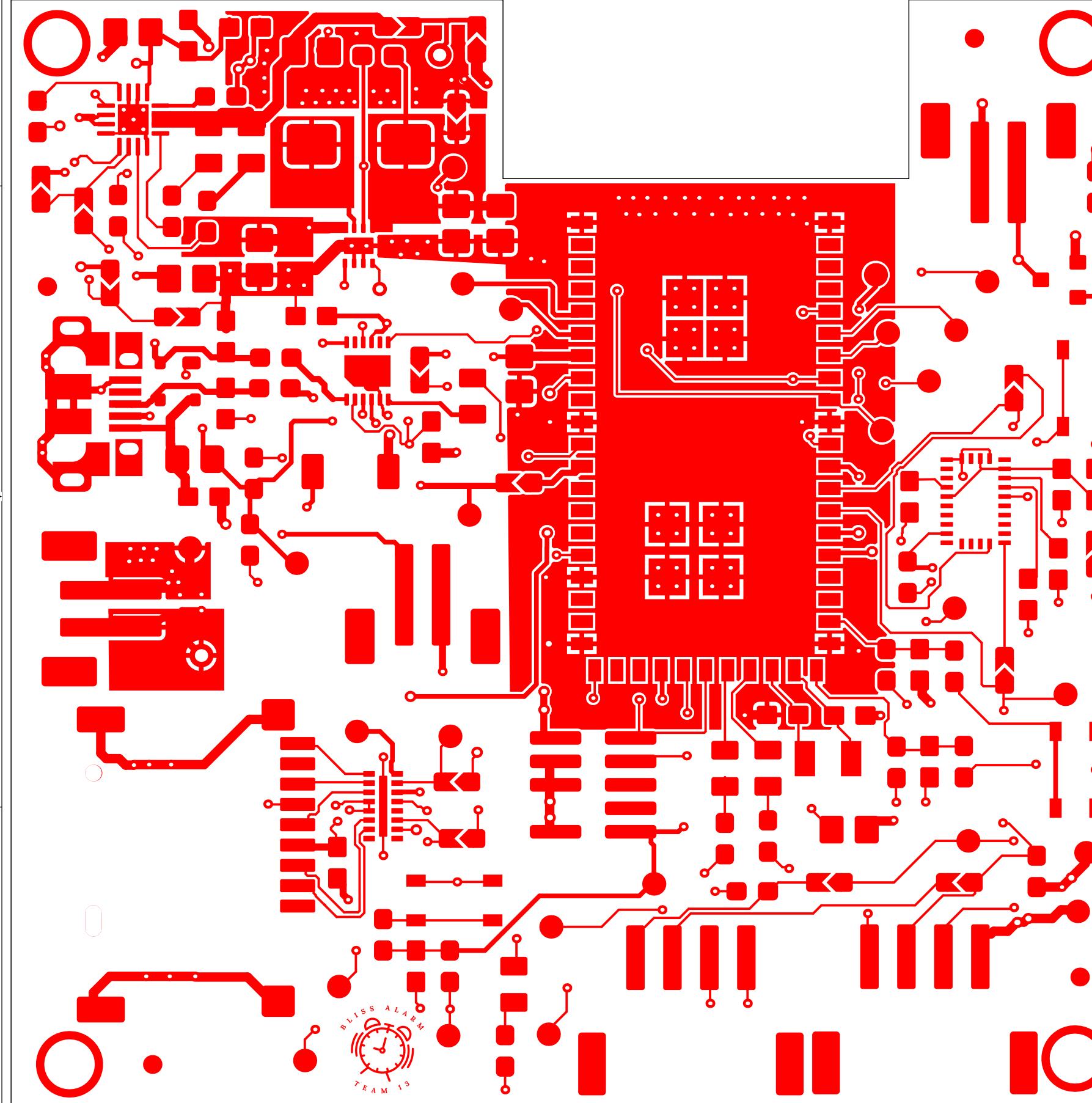
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REV STATUS OF SHEETS	REV		
SHEET			

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REVISIONS		DESCRIPTION	DATE	APPROVED

Top Layer (Scale 4:1)



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APPROVALS DATE

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NEXT ASSY USED ON

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APPLICATION

Altium
TM

 220 S. 33rd St
 Towne Bldg, B11
 Philadelphia, PA 19104
 USA

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SCALE: SHEET: 6 OF 12

A

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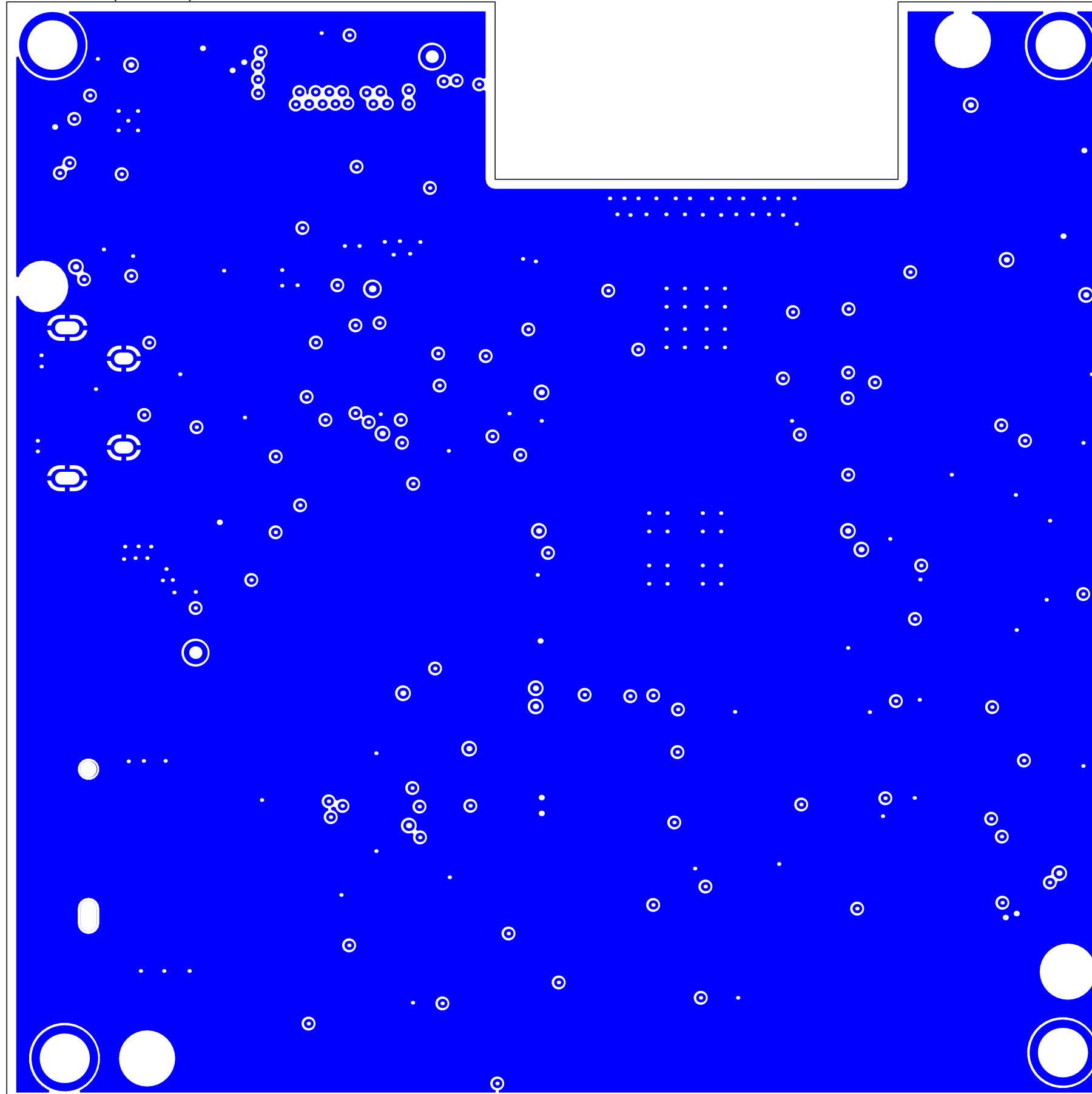
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GroundPlane (Scale 4:1)

REV STATUS
OF SHEETS

SHEET

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REV:

ZONE

REV

REVISIONS

DESCRIPTION

DATE

APPROVED

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SCALE: SHEET: 7 OF 12

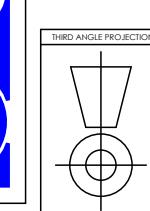
220 S. 33rd St

Towne Bldg, B11

Philadelphia, PA 19104

USA

Altium™



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DWG NO.: =DOC_NO_ASSY_DWG

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REV:

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FILE NAME: StarterBoardFabrication.PCBDwf

SCALE: SHEET: 7 OF 12

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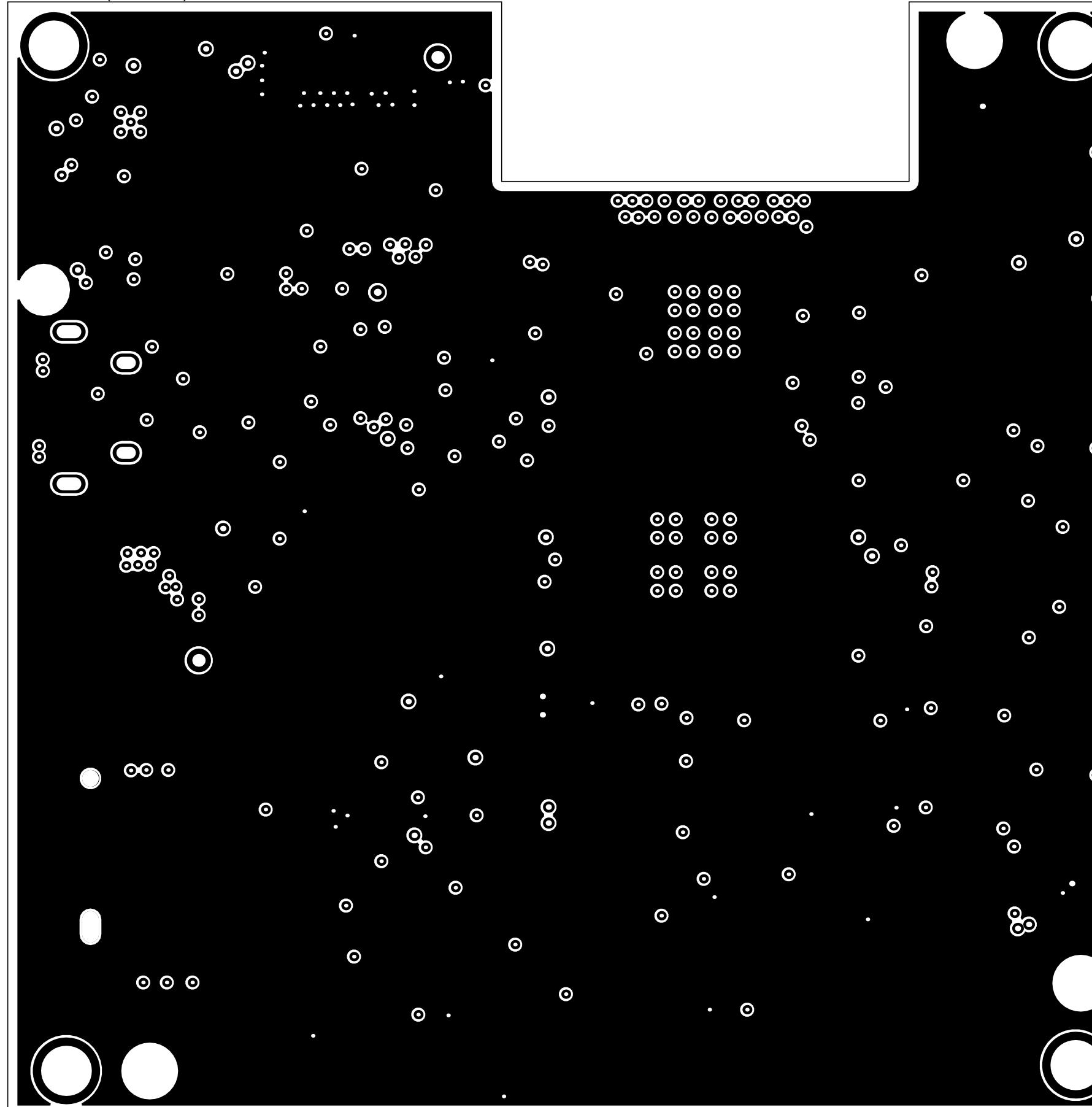
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PowerPlane (Scale 4:1)

REV STATUS
OF SHEETS

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REVISIONS

DESCRIPTION

DATE

APPROVED

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APPLICATION

AltiumTM220 S. 33rd St
Towne Bldg, B11
Philadelphia, PA 19104
USA

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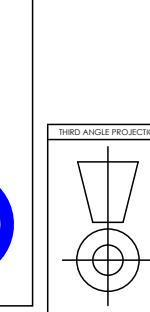
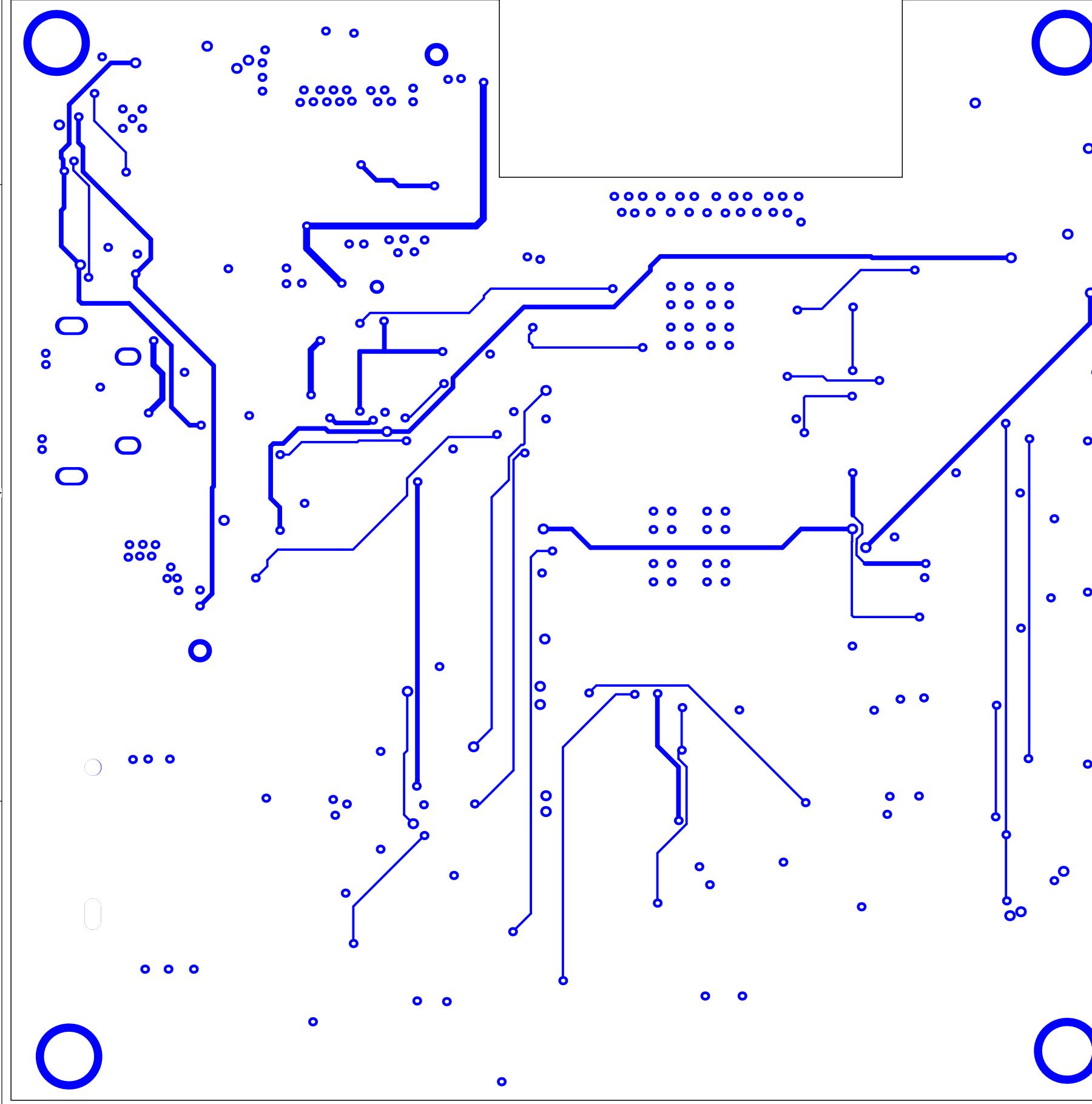
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Bottom Layer (Scale 4:1)



PART NO: =PCB_PART_NUMBER

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USED ON

PCB DOC: =PCB_DWG_NO

APPLICATION

Altium
TM

220 S. 33rd St
Towne Bldg, B11
Philadelphia, PA 19104
USA

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FILE NAME:

StarterBoardFabrication.PCBDwf

SCALE:

9 OF 12

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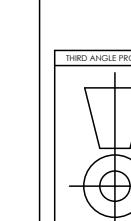
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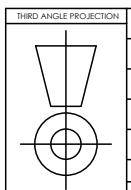
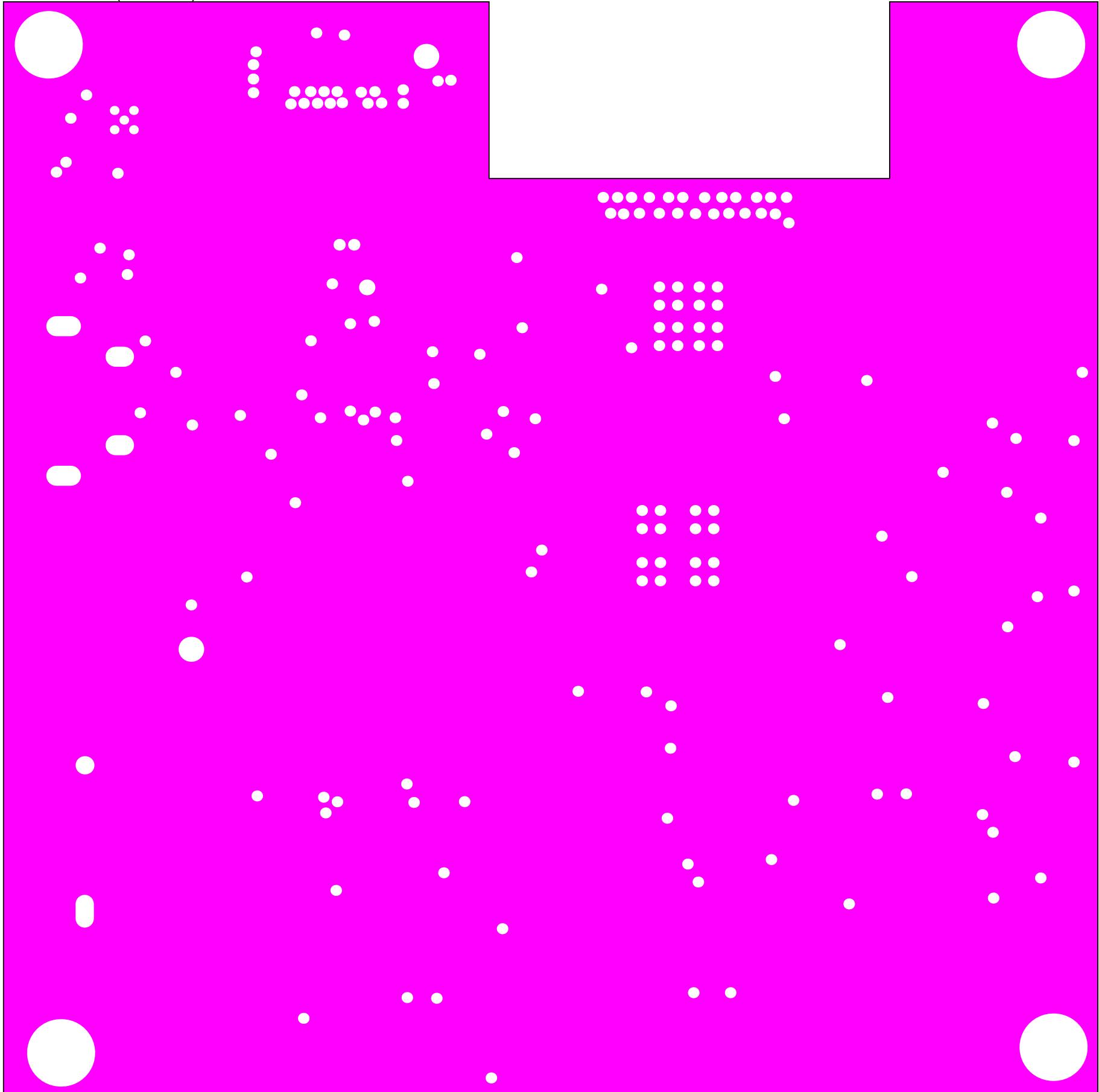
Bottom Paste (Scale 4:1)



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SCALE: FILE NAME: StarterBoardFabrication.PCBDwf			
FILE NAME: StarterBoardFabrication.PCBDwf			
Sheet: 10 OF 12			

Bottom Solder (Scale 4:1)

Bottom Solder (Scale 4:1)



PART NO: =PCB_PART_NUMBER							
APPROVALS	DATE	 TM		220 S. 33rd St			
ENGINEER:	=PCB_ENGINEER					Towne Bldg, B11	
DESIGNER:	=PCB_DESIGNER					Philadelphia, PA 19104	
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SCALE:		FILE NAME:		REV:			
Starts_Pcb_and_Electrization_PCBDesign.dwg				SHEET: 11 OF 12			

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REVISIONS		
DESCRIPTION	DATE	APPROVED

Bottom Overlay (Scale 4:1)



Digitized by srujanika@gmail.com

830

se_Etude_Bijssels



0.0.1 v6

PART NO: PCB PART NUMBER

APPROVALS		DATE
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Altium

220 S. 33rd St
Towne Bldg, B11

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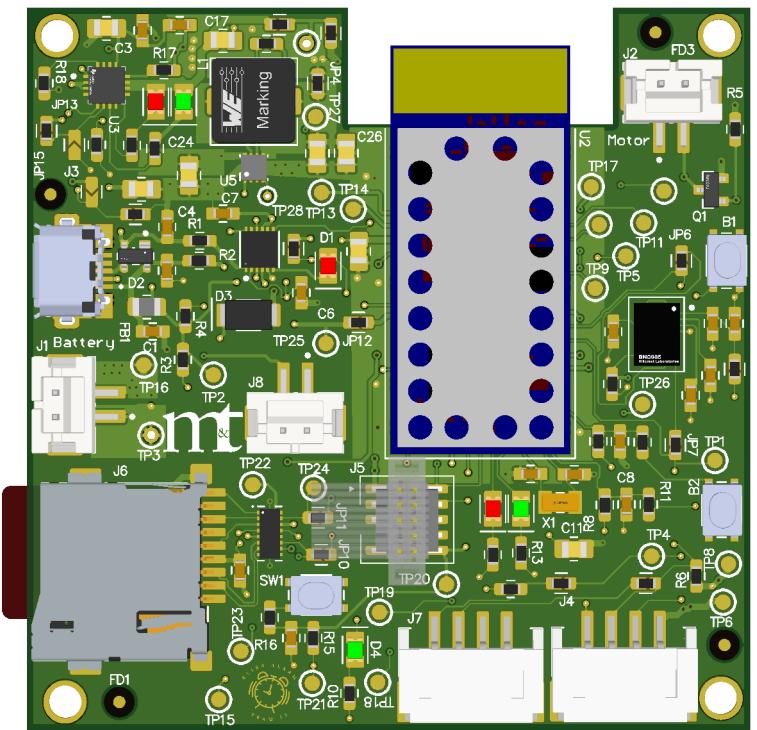
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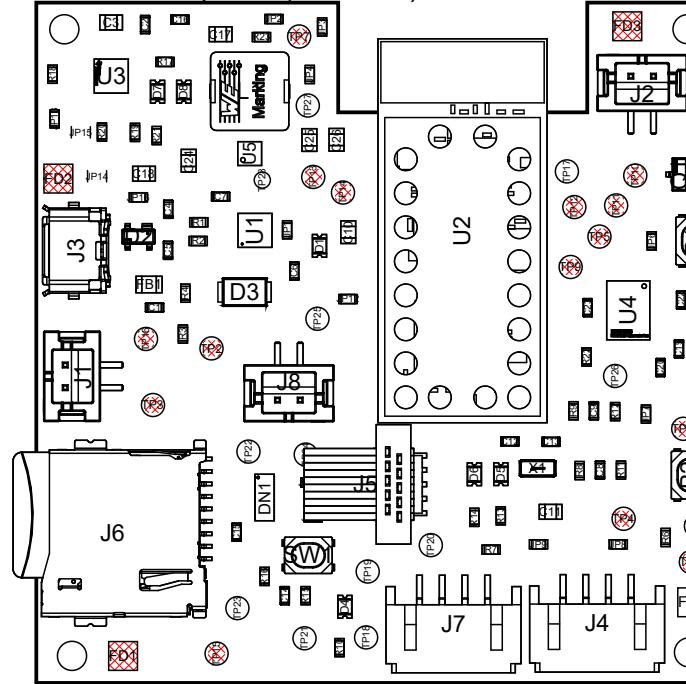
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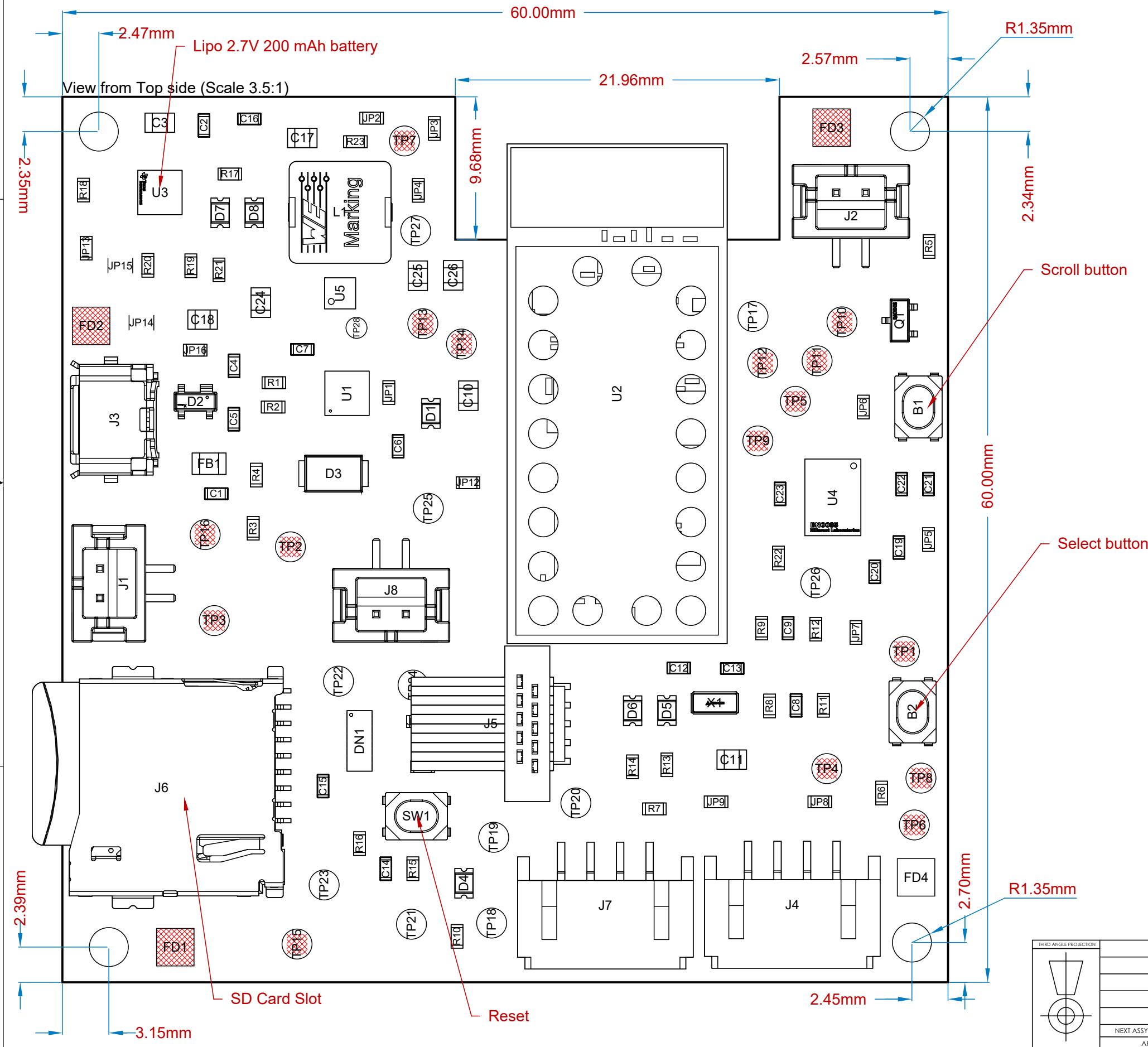
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Realistic View



View from Top side (Scale 3:2)





PART NO. 808 PART NUMBER

DATE			
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WG_NO	StarterBoardAssembly.PCBDwf		

Altium

220 S. 33rd St
Towne Bldg, B11
Philadelphia, PA 19104

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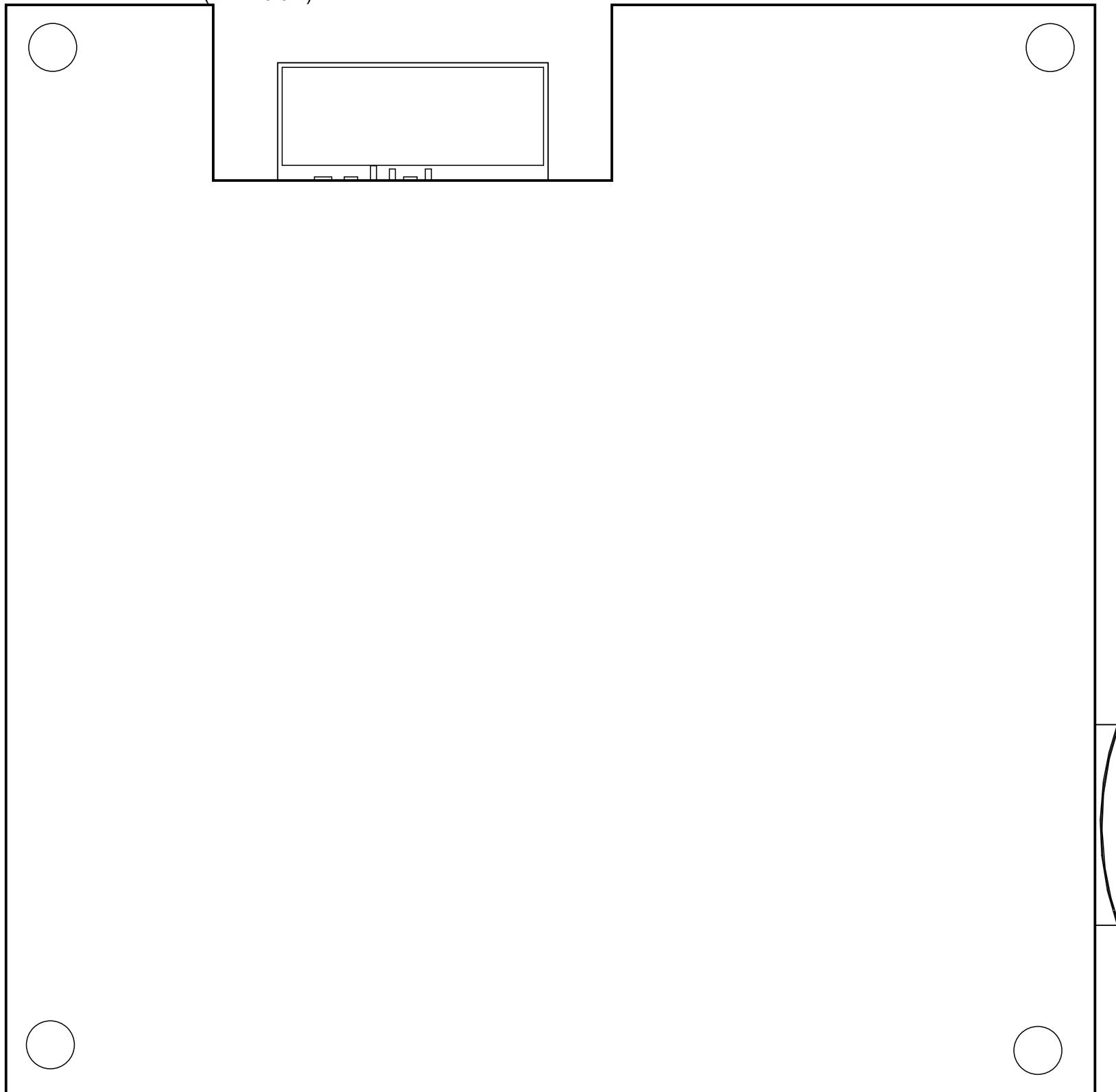
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DWG NO:		=DOC_NO_ASSY_DWG	REV:	.lfe
REV STATUS OF SHEETS	SHEET			

REVISIONS		
DESCRIPTION	DATE	APPROVED

View from Bottom side (Scale 3.5:1)



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ENGINEER: =PCB_ENGINEER	=PCB_ENGINEER		
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APPLICATION			B =CAGE_CO
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