

ECE/CS 552: INTRODUCTION TO COMPUTER ARCHITECTURE

Project Description – Extra Credit

Due on Wednesday, December 12, 2018, 11:59pm

The extra credit components should be implemented atop a working 5-stage pipeline design with caches (Phase 3). Without a working baseline of the mandatory project requirement, no extra credit points will be awarded.

Extra Credit Components

Up to a total of 15 points (out of a total of 100 points on the course) can be potentially obtained by successfully implementing different components of extra credit. The description of different components and their corresponding points are listed below.

Note: for the extra credit portion, you are free to modify your Verilog and violate the 552 rules. For example, you can replace your adder and/or shifter with $+/>>/<<$ operators. However, for your final report and submission, you must maintain and submit a working copy of your Phase 3 rules-compliant Verilog.

1. Successfully synthesizing your design using the Synopsys Design Compiler followed by extracting the synthesized netlist and performing functional simulation by rerunning all the test cases on the post-synthesis netlist. (0-3 points).

Note: Design Compiler can be accessed on the CAE machines using the script from ECE 551 (ask TA).

2. On top of (1), optimizing your design for low area. (0-2 points)

3. On top of (1), optimizing your design for high IPC. (0-2 points)

4. On top of (1), optimizing your design for high IPS (instructions per second); i.e., optimizing your design for both high IPC and high synthesis frequency. (0-2 points)

5. Increase associativity of cache design with LRU (or other) replacement policy. (0-2 points for instruction cache, 0-3 points for data cache)

6. Employing “critical word first” data reads from memory to cache, to service waiting requests early. (0-2 points for instruction cache, 0-3 points for data cache). This will require “hit under miss” behavior so that while your FSM is still filling a previous miss, subsequent instruction fetches, loads, and stores can continue as long as they are to different cache blocks. You must check to see if they are to the same cache block and stall in those cases until the cache block is filled.

7. Branch prediction (0-2 points)

8. *Other optimizations (please discuss with instructor/TA before proceeding).* (0-2 points)

Note: Please talk to the TA before embarking on any of these extra-credit components so as to clearly establish requirements of the extra-credit component.

Submission Requirements

1. You are required to submit a pdf document summarizing your extra-credit design and its differences from the baseline in terms of features, benefits and overheads.

2. You are required to develop one or more test cases, which clearly highlight the benefits of your optimized design, and the results should be shown in the submitted document.

3. You are also required to submit a zipped file containing: all the Verilog files of your design, all test benches used and any other support files.