Parameters

To be defined

Core

number_of_cores

number_of_L2s

number_of_L3s →

target_core_clockrate → system.clk_domain.clock (these are ticks so should be like →

number_cache_levels → if statements

total_cycles → system.cpu.numCycles stats.txt * number of cores

idle_cycles → system.cpu.idleCycles stats.txt * number of cores

busy_cycles → total - idle * number of cores

clock_rate → system.clk_domain.clock and same as earlier

number_hardware_threads → system.cpu.numThreads

fetch_width → system.cpu.fetchWidth

decode_width → system.cpu.decodeWidth

issue_width → system.cpu.issueWidth

commit_width → system.cpu.commitWidth

ALU_per_core → system.cpu.fuPool.FUList0.count (check child for ALU)

MUL_per_core → system.cpu.fuPool.FUList1.count (check child for intMult)

FPU_per_core → system.cpu.fuPool.FUList2-3 but not sure

instruction_buffer_size → system.cpu.fetchBufferSize

ROB_size → system.cpu.numRobs

instruction_window_size →

archi_Regs_IRF_size → system.cpu.numPhysIntRegs

archi_Regs_FRF_size → system.cpu.numPhysFloatRegs

store_buffer_size → system.cpu.SQEntries

load_buffer_size → system.cpu.LQEntries

total_instructions → simInsts stats

int_instructions → ?

fp_instructions → ?

branch_instructions → system.cpu.numBranches

branch_mispredictions → system.cpu.branchPred.condIncorrect

load_instructions → system.cpu.numLoadInsts

store_instructions → system.cpu.numStoreInsts

committed_instructions → system.cpu.committedInsts

committed_int_instructions → system.cpu.commit.integer

committed_fp_instructions → system.cpu.commit.floating

inst_window_reads → system.cpu.intInstQueueReads

inst_window_writes → system.cpu.intInstQueueWrites

inst_window_wakeup_accesses → system.cpu.intInstQueueWakeupAccesses

fp_inst_window_reads → system.cpu.fpInstQueueReads

fp_inst_window_writes → system.cpu.fpInstQueueWrites

fp_inst_window_wakeup_accesses → system.cpu.fpInstQueueWakeupAccesses

int_regfile_reads → system.cpu.intRegfileReads

int_regfile_writes → system.cpu.intRegfileWrites

function_calls → system.cpu.commit.functionCalls

ialu_accesses → system.cpu.intAluAccesses

fpu_accesses → system.cpu.fpAluAccesses

global_predictor_entries → system.cpu.globalPredictorSize

global_predictor_bits → system.cpu.globalCtrBits

chooser_predictor_entries → system.cpu.choicePredictorSize

chooser_predictor_bits → system.cpu.choiceCtrBits

local_predictor_entries → system.cpu.localPredictorSize

local_predictor_size → system.cpu.localPredictorSize

Icache

number_entries → system.cpu.mmu.itb.size

icache_config → (system.cpu.icache.size,
system.cpu.icache.tags.block_size , system.cpu.icache.assoc, 1, 10,
system.cpu.icache.response_latency,
system.cpu.icache.tags.block_size, 0)

buffer_sizes → (system.cpu.icache.mshrs, system.cpu.icache.mshrs,
system.cpu.icache.mshrs, system.cpu.icache.write_buffers)

read_accesses → system.cpu.icache.demandAccesses::total

read_misses → system.cpu.icache.demandMisses::total

Dcache

number_entries → system.cpu.mmu.itb.size

Dcache_config → (system.cpu.dcache.size,
system.cpu.dcache.tags.block_size , system.cpu.dcache.assoc, 1, 10,
system.cpu.dcache.response_latency,
system.cpu.dcache.tags.block_size, 0)

buffer_sizes → buffer_sizes → (system.cpu.dcache.mshrs,
system.cpu.dcache.mshrs, system.cpu.dcache.mshrs,
system.cpu.dcache.write_buffers)

read_accesses → system.cpu.dcache.demandAccesses::total

write_accesses → system.cpu.dcache.WriteReq.accesses::total

read_misses → system.cpu.dcache.ReadReq.misses::total

write misses → system.cpu.dcache.WriteReq.misses::total

BTB (Branch target buffer)

number_of_BTB → usually 1 per core

BTB_config → (system.cpu.branchPred.BTBEntries, system.cpu.branchPred.BTBTageSize, 2, 2, 1, 1)

read_accesses → system.cpu.branchPred.BTBLookups

L2 Config

L2_config → (system.l2cache.size, system.l2cache.block_size, system.l2cache.assoc, 8, 8, system.l2cache.response_laency, system.l2cache.block_size, 0)

buffer_sizes → (system.l2cache.mshrs, system.l2cache.mshrs, system.l2cache.mshrs, system.l2cache.write_buffer)

clockrate → same as system

read_accesses → `system.l2cache.demandAccesses::total`

write_accesses → `system.l2cache.ReadExReq.accesses::total`

read_misses → `system.l2cache.demandMisses::total`

write_misses → `system.l2cache.ReadExReq.misses::total`

L3 Config

L3_config → (system.l3cache.size, system.l3cache.block_size, system.l3cache.assoc, 8, 8, system.l3cache.response_laency, system.l3cache.block_size, 0)

buffer_sizes → (system.l3cache.mshrs, system.l3cache.mshrs, system.l3cache.mshrs, system.l3cache.write_buffer)

clockrate → same as system

read_accesses → `system.l3cache.demandAccesses::total`

write_accesses → `system.l3cache.ReadExReq.accesses::total`

read_misses → `system.l3cache.demandMisses::total`

write_misses → `system.l3cache.ReadExReq.misses::total`

Memory controller

mc_clock → system.mem_ctrl.dram.tCK (needs to be converted), shall be 800MHz

block_size → system.cache_line_size

number_mcs → len(system.mem_ctrl)

memory_channels_per_mc = len(system.mem_ctrl.dram)

number_ranks → `system.mem_ctrl.dram.ranks_per_channel`

req_window_size_per_channel → `system.mem_ctrl.dram.read_buffer_size`

IO_buffer_size_per_channel → `system.mem_ctrl.dram.write_buffer_size`

databus_width → `system.mem_ctrl.dram.device_bus_width` * `system.mem_ctrl.dram.devices_per_rank`