Homework Assignment #13

Modeling and Control of Power Electronics Systems

ECEN 5807

University of Colorado, Boulder

A Computer Server Backplane Power System

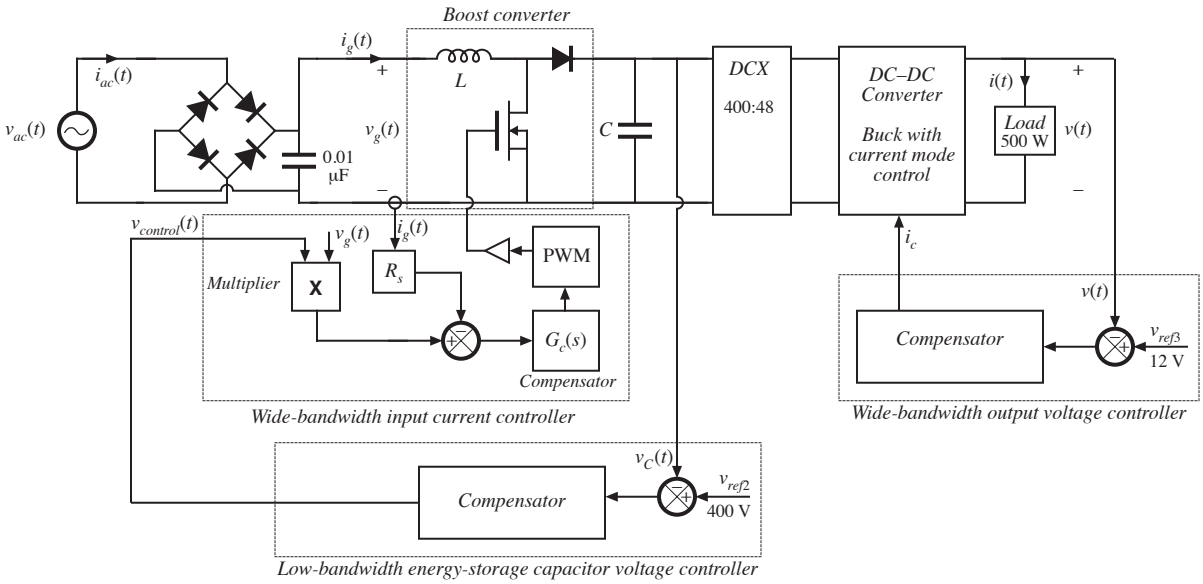

Figure 1 Complete off-line power conversion system.

This problem concerns the modeling and design of the power system of a computer server. The key elements of this system are:

- The 240 Vrms 60 Hz single-phase utility system
- A diode full-wave rectifier
- A boost converter with average current control, a 2.5 mH inductor, and a 100 kHz switching frequency
- A 400 Vdc bus with 220μF bulk energy storage capacitor
- A DC Transformer converter (DCX), having a fixed conversion ratio of 48/400
- A buck DC-DC converter employing a synchronous rectifier and peak current-mode controller. This converter operates with a 200 kHz switching frequency, and includes output filter elements $L = 0.45\mu$H and $C = 680\mu$F.
- A 12 V 500 W DC load

A block diagram of this system is illustrated in Fig. 1. A typical system contains multiple DC-DC converters at the output of the DCX, but for simplicity we consider only one in this problem.

The DC Transformer (DCX) block of this system is a DC-DC converter that has been optimized to operate at a fixed conversion ratio N_{DCX} with very high efficiency. This block is not intended to provide voltage regulation or control. Commercial DCX products are available with 1 MHz switching frequency and approximately 97% efficiency. For this problem, you may model the DCX as a simple fixed ratio dc transformer.

The object of this problem is to model each converter and its control system. Losses may be ignored (you may add some small loss elements if this aids convergence, but this is not required). It is desired to achieve the following minimum performance goals:

- 400 V DC bus returns to steady state within 0.5 sec for part 3 (see part 3 for how this is measured)
- Except for small crossover distortion and transient following the zero crossing, there should be no visible distortion in the ac line current waveform
- Bandwidth of 12 V output voltage regulator loop at least 3 kHz
- All compensators designed such that observed overshoot is less than 20%

You should design and simulate three control loops: the average current controller for the rectifier, the slow voltage control loop to stabilize the 400 V bus, and the fast loop to regulate the dc load voltage. Simple PI controllers are sufficient for these loops, but you may design whatever controllers you prefer. The bandwidths of your control loops must be realistic and may not be greater than 1/5 of the switching frequencies. All pulse-width modulators employ sawtooth waveforms having a peak-to-peak amplitude of 3 volts. All current sensors have gains of 1 volt per ampere. The current-mode controller employs an artificial ramp having a slope given by $m_a = 5A/\mu$sec. You should insert gains as necessary so that your analog control signals are scaled to realistic values on the order of 1 V at the full load quiescent operating point. Please identify the gains that you have included in your Simulink model.

To make your model readable by others, please arrange the high-level simulink model into blocks including the following:

- Boost CCM-DCM model
- Buck CCM-CPM model
- DCX
- Full-wave rectifier
- Average current controller
- Bus voltage controller
- Current mode controller
- Load voltage controller

It is highly recommended that you limit all duty cycles and all PI controller outputs to reasonable ranges. To enable convergence of the simulation of the full-wave rectifier model, you should employ the ode15s solver within Simulink; see the screen shot linked to the hw13 web page for suggested model configuration parameter settings. You will want to adjust the maximum step size to be compatible with the time constants of your design. With correct simulation parameters, you should not see oscillations in the full-wave rectifier model. Several models you may find useful are also linked to this page.

1. **Basic Design**

   Perform a paper (hand) analysis of each of the three loops, at the nominal full-load operating point. You may employ matlab to assist in drawing Bode plots, but this part should be independent of your Simulink model. Design compensators for each loop, and provide Bode plots of the loop gains with crossover frequencies and phase margins identified.

2. **Simulation of Full Load Operation**

   Implement your compensators in a Simulink model of the system, and run a simulation of steady-state operation at full power. You may wish to adjust your compensator parameters to optimize response time and line current harmonics. A small amount of visible crossover distortion in the ac current waveform is acceptable, but otherwise the waveform should appear sinusoidal. Attempt to minimize the time required for the dc bus voltage to reach 400 V. Explain what you did to achieve this. Provide a plot of the following signals:

   - AC line voltage and current
   - 400 V bus voltage
   - Load voltage
   - The duty cycles of each converter

   Your plots should be zoomed so they show approximately two line periods of waveforms, with the system operating close to steady state.

   Hint: can you think of a way to design the slow bus voltage controller so that the bandwidth and phase margin of this loop are maximized yet the 120 Hz variations in $v_{control}(t)$ are kept small?

3. **Simulation of Step Change in Load Power**

   Run a simulation in which the load takes a step change from full power to half power. Provide a plot of the following signals:

   - AC line voltage and current
   - 400 V bus voltage
   - Load voltage
   - The duty cycles of each converter

How large is the peak DC bus voltage during this transient? How long does it take for the average DC bus voltage to return to within 10 volts of the nominal 400 V? Can you design a bus voltage compensator that achieves a time of 0.5 sec without introducing noticable (visible) distortion of the ac line current?