Figure 1. xor instruction during Instruction fetch (IF) cycle.

IR = MEM[PC]

PC = PC+4

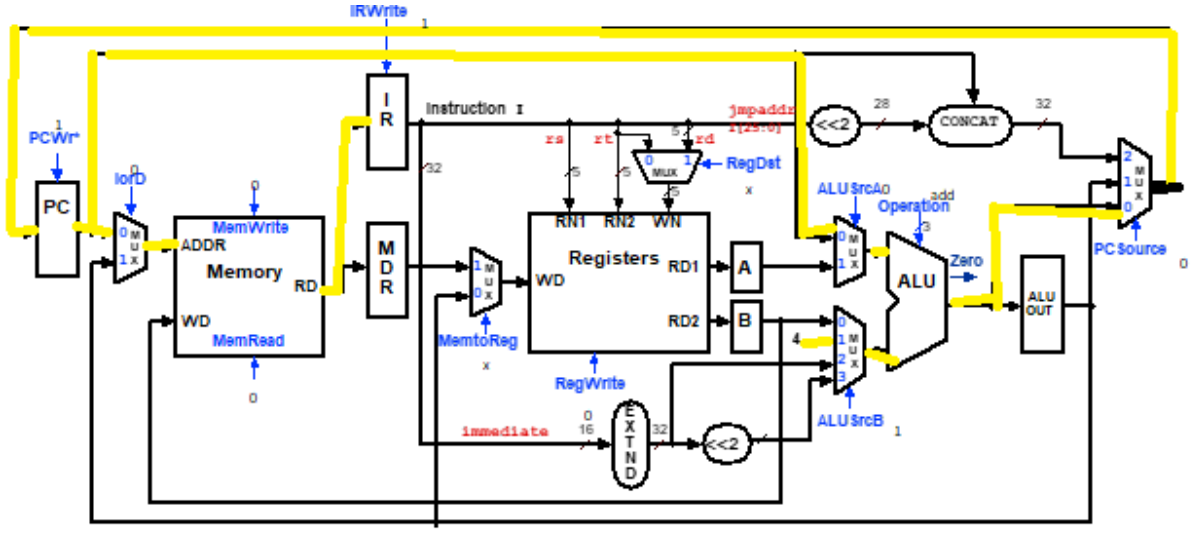

Figure 2. add instruction during Instruction decode (ID) cycle.

A = Reg[IR[25-21]]

B = Reg[IR[20-16]]

ALUOut = PC+(sign_extended (IR[15-0])<<2])

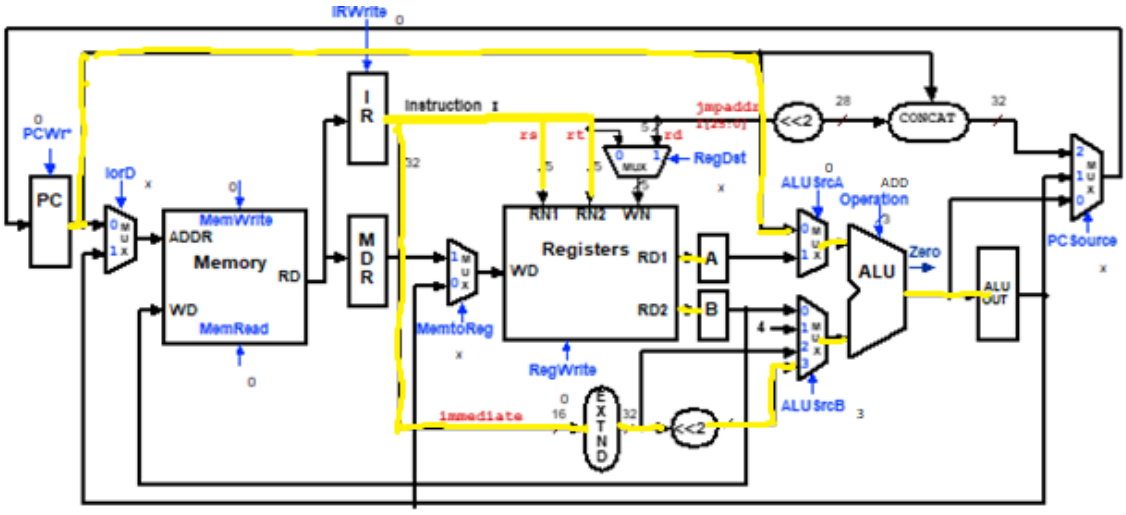

Figure 3. beq instruction during Execution (EX) cycle.

If (A==B), then PC= ALUOut

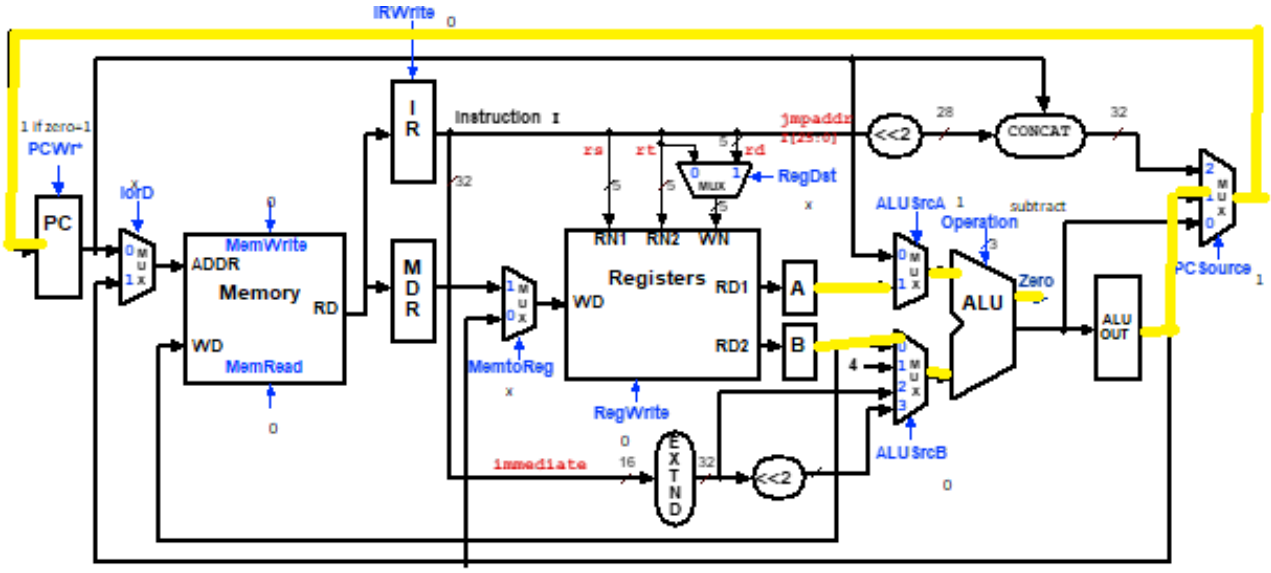

Figure 4. sw instruction during Memory access (MEM) cycle.

MEM[ALUOut]=B

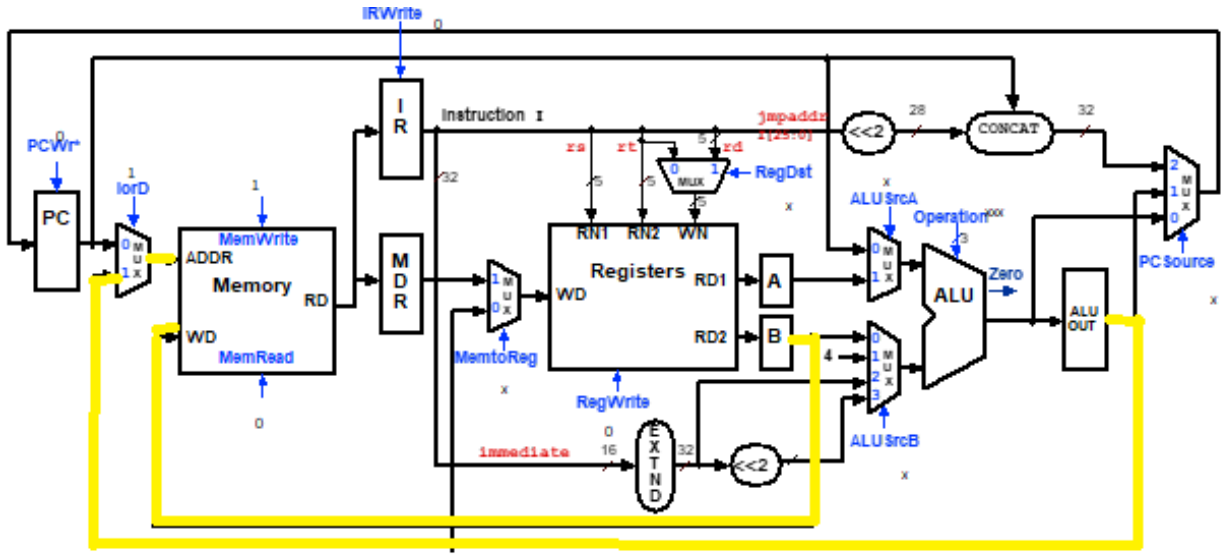

Figure 5. lw instruction during memory read completion cycle.

Reg[IR[20-16]] = MDR