BRAC UNIVERSITY

Department of Computer Science and Engineering

Examination: **MOCK** Mid Term
Duration: 1 Hour 30 Minutes

Semester: Fall 2024
Full Marks: 25

CSE 340: Computer Architecture

Answer the following questions. Show calculations where required.
Figures in the right margin indicate marks. Understanding the question is part of the examination.

Name:	ID:	Section:

1. CO1 **a)** **Define** Instruction Set Architecture and how it impacts performance. 2

b) Suppose a program is running on a PC with 3.2Ghz AMD Ryzen 5 processor. The program consists of 3 major types of instructions. Their instruction counts and CPI are given below:

Instruction Type	Instruction Count($x10^9$)	CPI
Load	3	2.3
Sub	5	?
Add	2	2.0

If the average CPI of the program is 6.3 then **what** is the CPI of the Sub Instruction? 3

c) Based on the results of the SPEC CPU2000 benchmark conducted on an Intel Core i5 13th Gen processor, the system has an average CPI of 2.4 and an instruction count of 5×10E8 . The system completes 5,4000 clock cycles in 12 seconds, and the reference time is 9,650 seconds.

Find the SPEC ratio. Based on your findings, make a comment on the performance of the processor. 3

2. CO2 **a)** **Construct** the equivalent RISC-V code of the following C code and Once you have the RISC-V code, **identify** the instruction format for each instruction: 5

```
if ( A[i] ≤ i){
    A[i+1] = A [B[3]] ;
}
```

Base addresses of array A and B are in register X20 and X21 . Also consider i is in register X22.

b) For the RISC-V assembly instructions below, **what** is the corresponding C/high level statement? 3

```
slli x30, x5, 3
add x30, x10, x30
slli x31, x6, 3
add x31, x11, x31
ld x5, 0(x30)
addi x12, x30, 8
ld x30, 0(x12)
lui x10, 50
addi  x30, x10, 1111
add x30, x30, x5
sd x30, 0(x31)
```

Assume that the variables f, g, h, i, j and k are assigned to registers x5, x6, x7, x28, x29 and x30 respectively. Assume that the base address of the

Arrays A and B are in registers x10 and x11, respectively.

c) **What** is the significance of the funct3 field in terms of Load instruction? 2

d) 2

`Label1:`	For the second SB type instruction calculate the value of the target location, if the PC = 1012 while executing that instruction.
`BNE x24, X25, break`	
`ADD X5, X5, X6`	
`SLLI x22, X22, 3`	
`LH X6, 32(X22)`	
`SD X7, 8(X21)`	
`BEQ x0, x0, Label1`	
`Break:`	

3. CO1, CO2 **Determine** if the following statements are true or false. For any false sentence, write its **correct form**. 1x5

a) Computer A is running Program A, Computer B is running Program B. Both are following the same ISA but CPI for Computer A is 2.4 and CPI for Computer B is 3.

Statement: So, the instruction count will be the same for both the programs. FALSE
Both are different programs.

b) **Statement:** Using the LD instruction we can make a larger jump than BEQ instruction. FALSE
LD instruction only loads values from memories to registers

c) Computer A runs a program in 5s. You want to make the program 5 times faster.
Statement: The new run time for the program would be 1s. TRUE

d) X5 = 5, X6 = 9;

AND X6, X5, X6
ADDI X5, X5, 0

Statement: After running the above mentioned code X5 register will have 5 in it. TRUE

e) As per the functionalities of a register, register X1 is responsible only for storing the return address.
Statement: Addi X1, X1, 5; Following the convention, this code will throw an error. FALSE
Without the X0, no registers are hardcoded to perform only centain tasks.