CSE341

Assignment 02

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Section : 10

Ans. to the ques. no - 01:

(1) logical address (B143 : 5241)

(a) First Physical Address $= (B1430)_h$

Last Physical Address $= (B1430 + FFFF)_h$

$= (C142F)_h$

(b) Fifth Physical Address $= (B1430 + 0004)_h$

$= (B1434)_h$

Last fifth Physical Address $= (B1430 + FFFB)_h$

$= (C142B)_h$

(c) Target Physical Address $= (B1430 + 5241)_h$

$= (B6671)_h$

Ans. to the ques. no - 02:

Physical Address $= (34215)_h$

(-) Offset $= (1252)_h$

Base Address

~~Segment Number~~ $= (32FC3)_h$

MSB ↑ LSB

this ~~segment number~~ Base Address is not acceptable as the LSB value is not equal to 0. If I devide it with $(10)_h$, I find as float number

and a segment number can never be a float number.

Base Address = $(32FC3)_h \div (10)_h$.

= 32FC.3 ← Not acceptable as a segment number.

Ans. to the ques. no - 3 :

$\overline{RD}$ is an active low pin. It means when 0 is provided as input, this pin let microprocessor reads data from memory / IO and when 1 is provided as input, it does not perform its functionality for microprocessor.

$\overline{RD} = \overline{0} = 1$; Active to read data from memory/IO

$\overline{RD} = \overline{1} = 0$; Inactive.

Ans. to the ques. no 4.:

An active high performs its functionality when given 1 as an input.
For example: ALE is an active high pin. This means, when
ALE = 1, it indicates an address is available on bus and
ALE = 0, it remains inactive.
This is no one of the example of an active high pin. The active high pin mostly remains active when given 1 and inactive when given 0.

Ans. to the ques. no-05:

Clock cycle = 6

Duty Cycle = 25%

Clock Rate, $f = 20 \times 10^6$ Hz

(i) Clock Pulse, ~~$T = 5 \times 10^{-8}$~~ $T = \frac{1}{f} = \frac{1}{20 \times 10^6} = 5 \times 10^{-8}$ sec.

(ii) Time needed for a complete bus cycle = $T \times$ Clock cycle

$= 5 \times 10^{-8} \times 6$

$= 3 \times 10^{-7}$ sec.

(iii) Logical High on one clock cycle, $(T_{ON}) = \frac{25}{100} \times T$

$= \frac{25}{100} \times 5 \times 10^{-8}$

$= 1.25 \times 10^{-8}$ sec.

(iv) Logical High on one bus cycle $= T_{ON} \times 6$

$= 1.25 \times 10^{-8} \times 6$

$= 7.5 \times 10^{-8}$ sec.

(v) Logical Low for one clock cycle, $(T_{off}) = \left(1 - \frac{25}{100}\right) \times T.$

$= \left(1 - \frac{25}{100}\right) \times 5 \times 10^{-8}$

$= 3.75 \times 10^{-8}$ sec.

(f) Logical Low for one bus cycle, $(T_{OFF}) = 3.75 \times 10^{-8} \times 6$ s

$= 2.25 \times 10^{-7}$ sec

Ans. to the ques. no - 6 :

Duty cycle, T_{ON} = 25 ns

total time for one bus cycle = 250ns

Clock cycle = 8

$\therefore$ Duty cycle = $\frac{25 \times 8}{250}$

$= 0.8$

Ans. to the ques. no-7:

ⓐ MOV [3214h], BL

⇒ Here, $A_0 = 0$, as the starting address is even and

$\overline{BHE} = 1$, as we are working with 1 byte (8 bit) data, no need to store the data on odd bank.

ⓑ MOV AX, [1234h]

⇒ Here, $A_0 = 0$, as the starting address is Even, and

$\overline{BHE} = 0$, the reason is, ~~even if~~ we are working with 2 byte (16 bit) data, so we need to store the lower bits on even/low ~~data~~ bank and the higher bit on odd/High bank.

ⓒ MOV CH, [1234h]

⇒ Here, $A_0 = 0$, as the starting address is Even, and

$\overline{BHE} = 1$, as we are ~~going to~~ working with 1 byte (8 bit) data, no need to store on odd/High bank.

ⓓ MOV [5413h], DL

⇒ Here, $A_0 = 1$, as the starting address is Odd, and

$\overline{BHE} = 0$, as we are working with 1 byte odd data, we need to store it on odd/High bank.

And. to the ques. no- 8:

ⓐ This timing diagram is for the Read cycle.

ⓑ The reason behind M/$\overline{IO}$ pin being twisted around [both one and ~~a~~ zero] like that is, the value of passing M or $\overline{IO}$ both happens within the same pin and we are not certain in which ~~time the~~ passes according to specific time. So, we use this twisted patten so that both address and data can pass accordingly.

ⓒ If the ALE pin was high in T_3 (third clock cycle), it would be a problem, Because ALE pin enables the passing of address which needs to be passed at T_1 (First clock cycle); ~~so if we~~ The reason is, the both data and address passes through the AD pin and data specifically passes on the T_3 clock cycle. Now, if both address and data are enable to pass on the third clock cycle, it will create a conflict whether the address or data should be passed on T_3 (Third clock cycle).

(d) The number of clock cycles will increase upto two clock cycle until the ready pin is ~~actived~~ activated. So, the ~~is~~ last cycle will not be 4 anymore.

BONUS:

~~The DT/$\overline{R}$ pin~~

The $\overline{RD}$ pin lets the microprocessor to read data from memory/$\overline{IO}$; whereas the DT/$\overline{R}$ pin ensures the direction of flow through the transceiver. The transceiver ensures the flow of data from microprocessor to ~~memory~~ memory/$\overline{IO}$ or viceversa.