SRAM NMOS Inverter Proposal

Group Number: 2
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Parameter	Value	Reasoning/Method to Achieve
VDD	1.8 V	Skywater 130nm NMOS transistors are 1v8
Kn (Cox,μn)	TBD	To produce Kn we'd need to read through the PDK and check for the spice info of the transistor we wanna use.
Vth	TBD	This can be found through the PDK when we select our transistor type, being an SVT 1v8 nmos.
Speed	20ns	This speed is meant to represent the maximum write time seeing writing should take longer than reading on average.
Gain	TBD	This would be dependent on how we design our inverter and how we would modify it to affect its gain.
W/L Ratios		
• Access Transistor	W/L = 2	Sized for adequate write capability while maintaining read stability
• Pull-down Transistor	W/L = 3	Pull-down must be stronger than access transistor to prevent read disturb and maintain stored logic levels
Pull-down Resistance	50 kΩ	Starting point for resistance value. Will require optimization to balance noise

		margin vs. power consumption trade-offs
Write Margin	> 200 mV	Minimum voltage margin required for reliable write operations. To be verified through DC sweep simulation of write operation
Static Noise Margin (SNM)	100-200 mV	Target noise immunity for stored data. Measured using butterfly curve method: DC sweep applied to storage nodes to determine maximum tolerable noise before bit-flip

Calculation Parameters (Kn and Vth)
The transconductance parameter Kn and the voltage threshold Vth are necessary to determine MOSFET characteristics which we can find through the skywater 130nm PDK. Kn will help us determine the current-driving capability of our transistors and it will matter for Noise margins of SRAM cells. While the threshold voltage Vth is required to determine when our transistors will turn on and what our logic levels will look like before we begin SPICE simulations.

W/L Ratio Design
The width-to-length ratios for our transistors need to be decided in order to ensure a balance of read/write stability and area efficiency. The access transistors being W/L=2 is sized that way to allow it to be capable enough of writing while not strong enough to cause the pull-down transistor to be disturbed during reading due to DC noise. The pull-down transistor needs to be W/l=3 in order to be stronger than the access creating a ratio of 1.5, this ratio will then help us ensure that the voltage can remain stable by checking for Vq and see what it needs to fall under. We can potentially reduce or increase these ratios based on how much area we want to cover or to deal with parasitic capacitance.

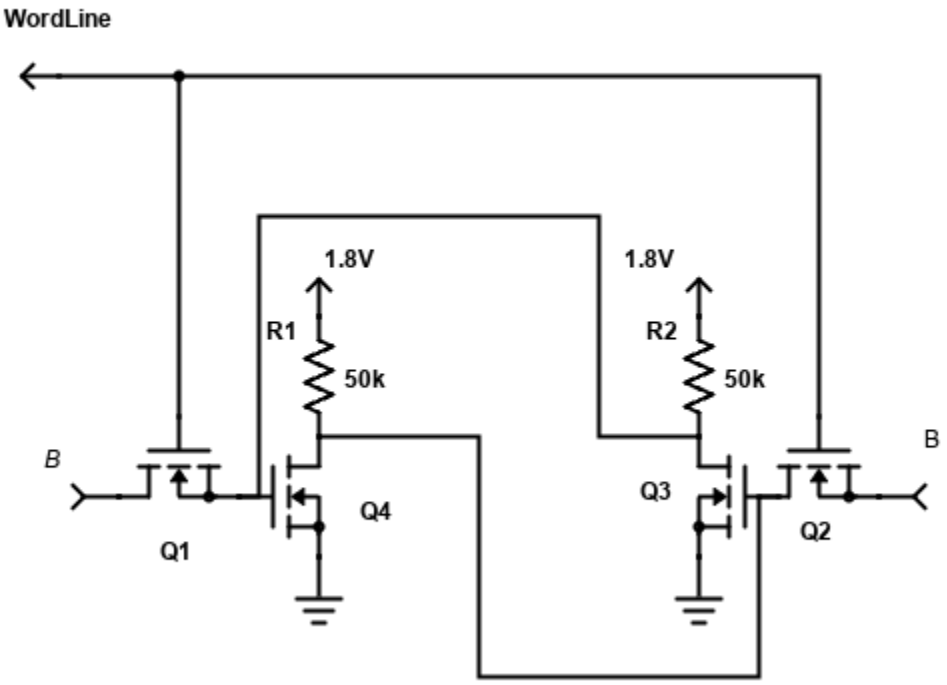
Resistance Selection
Currently we chose 50kΩ pull-down resistance values, this is mainly a placeholder until we do further testing to determine what is the resistance we want to aim for. Seeing the higher the resistance the lower power is consumed, but at the same time it causes SRAM to take longer when it comes to twitching due to a larger RC time constant. Lower values might allow for faster switching speed and potential making it better at handling noise. It will be modified based on our SNM requirements.

Write Margin Analysis
We are going to need to see how stable our cell is and how reliably it can be programmed in the worst-case situation. This will be done by storing a ‘1’ in our cell. We would begin a write operation having our Wordline on Vdd, but our bitline will be swept from 0V to Vdd. Through this

we can determine the minimum voltage we would need in order to flip the bit. Currently 200mV is a placeholder.

Static Noise Margin

The static Noise Margin will help us determine how much DC noise that can be applied to our bit cell, specifically at the storage nodes before they flip. This is necessary to determine how robust our system is. We will do this by applying a voltage source at the outputs of both inverters and produce a DC sweep for each noise from 0V to Vdd. We will then plot a curve of the Voltage at one inverter output against the other and determine the SNM through measuring either one of the squares formed by that method. We are aiming for 100-200mv..



Timeline

- Design & Simulation
    - Topology and starting sizes
    - Test benches
    - First numbers for the table
- Physical Layout & Parasitics
    - 6T Layout
    - Plan access fets and bitline
- Interfacing to other RAM components
    - bitline interfacing

    - wordline timing
    - sense amp
    - write-driver

Design & Simulation (2-3 weeks total):

- Week 1
    - Setting up software (magic and spice)
    - Reading up Sky130 PDK
    - Investigate transistor properties through simulation of Ids vs Vgs to determine transistor properties
- Week 2
    - Setting up circuit model in Spice
    - Simulating Inverter designs and determining resistor value and W/L of inverter transistor size.
    - Simulating Storage Cell for Static Noise Margin and modifying W/L appropriately based on the achieved noise and resistor value
- Week 3
    - Setting up Bit cell Spice model
    - Testing W/L of access transistors and determining Write Margin through that
    - Adding in Capacitors to the circuit and testing out Bit cell delay when reading and writing