Mountain Falls

The Wide Band Transistor Amplifier

ENGR 346 - Design Challenge II (DC2)

The second design challenge assigned in ENGR 346 explored the analysis and design of the wide band transistor based signal amplifier. The design challenge defined specifications for the given input and the necessary output to design for. An amplifier was developed to meet those specifications. The process will be discussed in this report.

Introduction

For DC2, the task was to design a wide band transistor based amplifier that could take a low voltage of $25mV_{0p}$ with 500 Ohms of input resistance and to amplify it to produce a $1v_{0p}$ signal across a 1k Ohm load. The amplifier design was to have a low frequency cut off at 100Hz and a high frequency cut off at 10MHz. The input signal source was specified to only be capable of providing currents less than or equal to 5 microamps. The last requirement is that the final design must not include any integrated circuits or operational amplifiers. The maximum voltage rails available were positive and negative 9v sources.

Background

Transistor amplifiers are prevalent throughout the world of electronics and, though their significance was not initially recognised, the invention of the transistor in 1947 led to great leaps and bounds in the possibilities of electrical inventions. In DC2 the transistor is used to amplify small signals of wide band width across a load. Transistors are commonly used for such applications. There are many amplifying configurations for transistors though the simplest fall prey to a frequency reducing effect known as the miller effect. Because of internal capacitance transistor amplifier designs can lose bandwidth due to an inverse relationship between bandwidth and gain. For DC2 a design was chosen using the cascode amplifier configuration. This configuration combines a common collector amplifier with a common base amplifier which successfully reduces the miller effect allowing for higher frequency functionality.

Theory Analysis/Modeling:

First a circuit was designed to meet the specifications listed in the introduction. The finalized design is shown in Figure 1 for reference throughout the analysis.

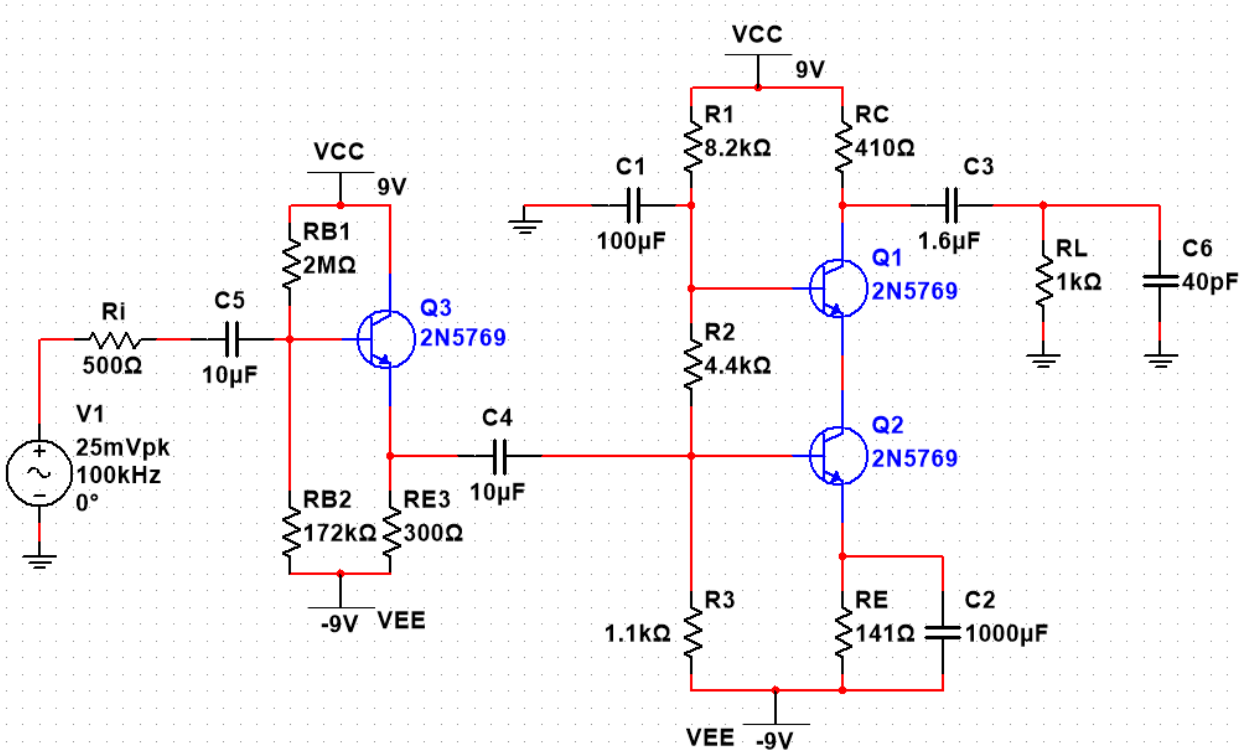


Figure 1: Final Circuit Design

It can be seen in Figure 1 that the design uses 3 BJT transistors in a two stage amplifier circuit. The second stage is a cascode amplifier that completes the bulk of amplification and inverts the signal as a byproduct of the common emitter Q2. The first stage emitter follower Q3 slightly reduces voltage gain but significantly increases input resistance which reduces input current. This first stage was necessary to keep the input current beneath the 5 uA maximum input current requirement. The low frequency cut off is defined by the various coupling capacitors throughout the circuit. These values were tinkered with in the simulation software multisim to achieve the low frequency cut off of 100Hz. The high frequency cut off is defined by the low pass filter created by the parallel connection of RL and C6. The value of C6 was calculated in the theoretical analysis but changed slightly to produce the desired high frequency corner of 10MHz. The 2N5769 transistor was selected for its 500MHz cut off frequency. This transistor has a Beta of 78 which is moderately low but a necessary trade off to achieve the desired frequency response.

Theoretical Analysis:

Before the circuit was simulated, analysis was conducted to find component values. It is important to note for the following analysis that beta will be assumed to be constant and collector and emitter current will be assumed to be equal on the grounds that **β+1** is negligible. First it was deduced that the total voltage gain would have to be 40. After this was determined the cascode configuration was chosen due to its moderate gain and wide band frequency response. Then due

to the maximum input current of 5 uA the first stage common collector was chosen to reduce input current with its high input impedance.

The analysis began with the design of the cascode amplifier. First the values shown in Figure 2 were selected for the DC biasing characteristics. For theoretical analysis a V_{CC} of 18 was used though in the simulated circuit the rails are set to +9v and -9v. This choice was made to increase the ease of the calculation. I_C was first chosen at 4 mA but later adjusted to 5.32 mA to achieve the desired voltage gain. The large V_{CE1} and V_{CE2} were chosen to increase linearity and give ample room for voltage swing to avoid nonlinear regions on the cascode's IV curves.

$I_C = 0.00532$

-10

$V_{CC} = 18$ $V_{E1} = 0.75$

-10 -10

$V_{CE2} = 9.07$ $V_{BE} = 0.7$

-10 -10

$V_{CE1} = 6$ $\beta = 78$

Figure 2: Stage 2 cascode Selected Values

After the initial values were selected the other component values were calculated. The resistor labels match with their positions in Figure 1. R_3 was kept an order of magnitude smaller than $\beta * R_E$ to keep the current into the bases of the transistors negligible compared to the currents in R_1, R_2, and R_3. This allowed for the assumption that the base resisters formed an ideal voltage divider to be close to accurate. This estimate substantially reduced complexity in the DC biasing analysis without compromising accuracy too seriously. These calculations can be seen in figure 3. After the resistors were calculated to adhere to the biasing scheme for the selected collector current values were calculated for the AC analysis and gain equations. The final gain equations for stage 1 can be found in Figure 4. The gain of the cascode had to be higher than the requirement of 40 to account for gain lost in the emitter follower (common collector).

$$I_{R3} = \frac{V_{R3}}{R_3}$$

$I_{R3} = 0.00131863247863$

$$R_E = \frac{V_{E1}}{I_C}$$

$R_E = 140.977443609$

$$V_{R3} = V_{E1} + V_{BE}$$

$V_{R3} = 1.45$

$$R_2 = \frac{V_{R2}}{I_{R3}}$$

$R_2 = 4360.57816956$

$$V_{B1} = 1 + 0.7$$

$V_{B1} = 1.7$

$$V_{R2} = V_{B2} - V_{B1}$$

$V_{R2} = 5.75$

$$R_1 = \frac{V_{R1}}{I_{R3}}$$

$R_1 = 8190.30334457$

$$V_{B2} = V_{E1} + V_{CE1} + V_{BE}$$

$V_{B2} = 7.45$

$$V_{R1} = V_{CC} - V_{R2} - V_{R3}$$

$V_{R1} = 10.8$

$$V_C = V_{E1} + V_{CE1} + V_{CE2}$$

$V_C = 15.82$

$$V_{R3} = V_{E1} + V_{BE}$$

$V_{R3} = 1.45$

$$R_3 = \frac{1}{10}\beta(R_E)$$

$R_3 = 1099.62406015$

$$R_C = \frac{V_{CC} - V_C}{I_C}$$

$R_C = 409.77443609$

Figure 3: Stage 2 cascode value calculations

$R_L = 1000$

−10 1000

$V_F = 100$

−10 100

$V_T = 0.025$

$$R_i = \frac{R_{E3}R_{CCout}}{R_{E3} + R_{CCout}}$$

$R_i = 52.6629217478$

$$r_{pi} = \frac{\beta + 1}{g_m}$$

$r_{pi} = 371.240601504$

$$g_m = \frac{I_C}{V_T}$$

$g_m = 0.2128$

$$R_B = \frac{R_2 R_3}{R_2 + R_3}$$

$R_B = 878.171992481$

$$A_{mid} = g_m^2 \cdot \left(\frac{R_C R_L}{R_C + R_L}\right)\left(\frac{r_{pi}}{g_m r_{pi} + 1}\right)\left(\frac{R_{Bllrpi}}{R_i + R_{Bllrpi}}\right)$$

$A_{mid} = 50.8232679462$

Figure 4: Stage 1 gain calculations

The final calculated voltage gain for the cascode was about 50 while taking the output resistance from the first stage (R_{CCout}) into account. Before this resistance was known an estimate of 300 was used. Values were recalculated to the final values after stage 1 was designed.

Before the total gain could be calculated the second stage values were chosen for the emitter follower configuration. The chosen values can be seen in Figure 5. These values were chosen to keep the base current (I_{B3}) below 5 uA, hence a base current of 4 uA was designed to allow some breathing room. R_{E3} was chosen to be 300 because this low value kept output resistance to a minimum which increased the gain of the stage 2 cascode. The same transistor as the first stage was used as Q3, the 2N5796. This choice was made again due to its wide band frequency characteristics. The rest of the values to achieve the desired base current were calculated from the chosen values using the formulas shown in Figure 6. It is important to note that $R_{1//3}$, and $R_{4//L}$ are values used to represent the parallel combinations of R_1 with R_3 and R_4 with R_L respectively. The Gain for this stage was then calculated giving the expected less than unity voltage gain and high current gain.

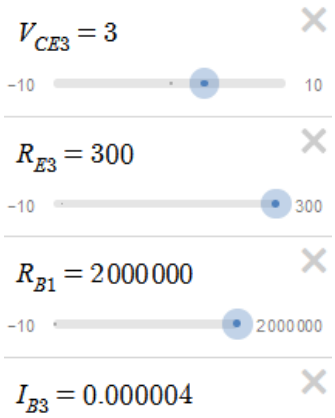


Figure 5: Stage 2 selected values

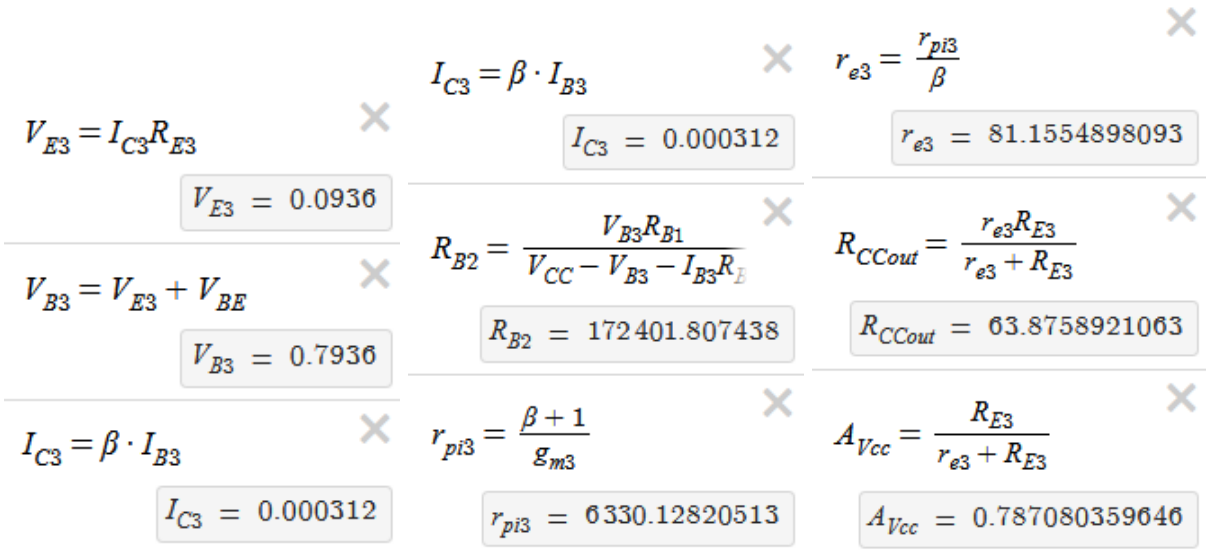
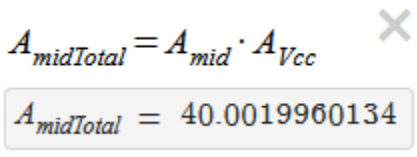


Figure 6: Stage 1 Common Collector value calculations



Once the gain equations for the first and second stages of the circuit were calculated, the total gain could be found. The total gain calculations can be seen in Figure 7.

Figure 7: Final Gain Calculations

$$C_6 = \frac{1}{f_h R_L} \cdot \frac{1}{2\pi}$$

$$C_6 = 1.5915494309 \times 10^{-11}$$

$$f_h = 10000000$$

Figure 8; Low pass filter calculation

The high frequency corner of the chosen transistors was well above 10MHz and thus a low pass filter to attenuate the signals above the desired frequency range was necessary. The estimation calculation used to find the capacitor value can be seen in Figure 8. The final value seen in Figure 1 was found by varying the value while simulating the frequency response til the corner frequency was very close to 10MHz. After the calculations were finalized input and out resistances were calculated. Those calculations and values can be seen in figure 9.

$$R_{input} = \left(\frac{1}{R_{B1}} + \frac{1}{R_{B2}} + \frac{1}{\beta r_{e3} + \beta R_{B1}} \right)^{-1}$$

$$R_{input} = 158558.68325$$

$$R_{output} = \frac{\left(g_m^2 \cdot \left(\frac{R_C R_L}{R_C + R_L} \right) \left(\frac{r_{pi}}{g_m r_{pi} + 1} \right) \left(\frac{R_{Bllrpi}}{R_i + R_{Bllrpi}} \right) \right)}{\frac{\left(g_m^2 \cdot \left(\frac{r_{pi}}{g_m r_{pi} + 1} \right) \left(\frac{R_{Bllrpi}}{R_i + R_{Bllrpi}} \right) \right)}{R_L}}$$

$$R_{output} = 290666.666667$$

Figure 9; Input and output resistance calculations

Modeling:

At this point the circuit was simulated to see how the theoretical results matched the simulated values. The current value out of the input that can be seen in Figure 8 is in the nano order of magnitude and is thus well below the absolute maximum for the input signal.

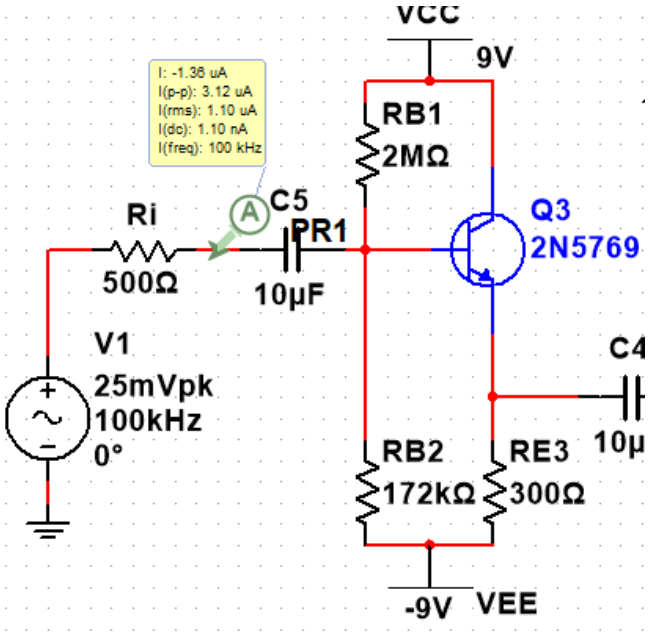


Figure 10: DC measurement simulation

Next the frequency responses and gain were tested. Figure 9 shows the input signal compared to the output signal. For this test 100kHz was chosen due to it being well into the midband of the frequency range. The -1.032v output over the -0.0241v input shows a gain of 41.82. It is important to note that the positive peaks of the output voltage are acting nonlinearly. This is likely due to nonlinearities introduced in the cascode.

Figure 11: Graphical representation of the input (shown in blue on channel 1) compared to the output (shown in red on channel B)

The Bode plot of the circuit output can be seen in Figure 10. The mid band rests at about 31dB at 100Hz the signal is close to 3dB down as shown in the figure. The high frequency cut off at 10MHz is also very close to 3dB down as shown in the figure. This shows that the amplifiers frequency response was designed for successfully.

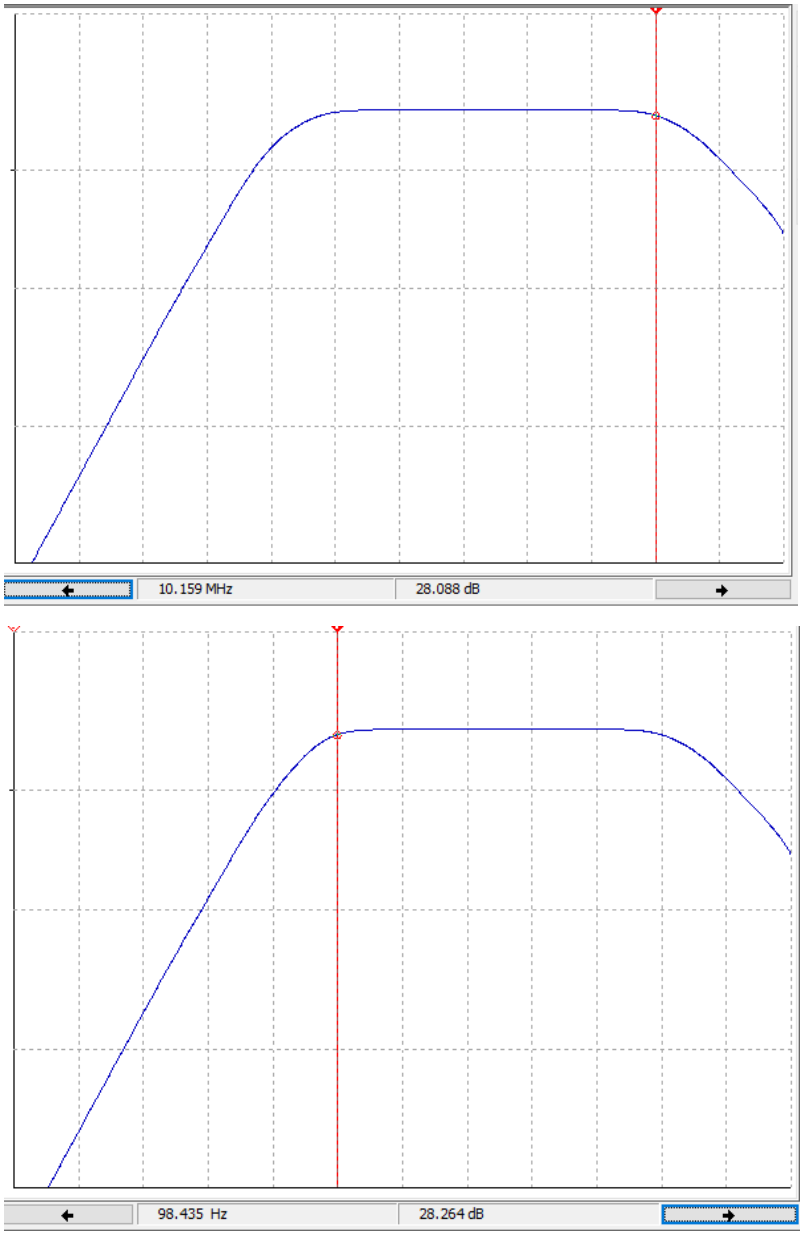


Figure 12: Bode Plot of output signal frequency response

Discussion and Conclusion

As shown in the virtual modeling of the final circuit design the design produced successfully achieved the requirements set by DC2. The output signal showed the required gain of 40, and did so over the required frequency band from 100Hz to 10MHz. The input current was successfully kept below 5 uA.

The design did not act as expected on the positive peaks of the output signal. Somewhere within the cascode stage of the amplifier nonlinearity was introduced into the gain equation. An attempt was made to design this out of the circuit by raising the collector emitter voltages of the transistors in the cascode but this had no noticeable effect. Various other component values were varied to find the culprit of the nonlinearity but nothing seemed to affect the positive half of the output signal. The high frequency corner of the output signal created by the high pass filter did not match the value estimated with the simple low pass filter calculation. This was because the internal capacitance of the transistors was not taken into account. This estimate turned out to be close and using the simulation as a guide a passable value was found.

Summary and Next Steps

The results of the design challenge are satisfactory though the nonlinearity issue remains unsolved. A mistake was made when designing for the low input current due to the incorrect assumption that base current and input current are equivalent. Luckly, they correlate though the input current is much lower due to the input resistance of the amplifier. Thus, designing for a low base current did have the desired effect even though the initial thought was incorrect. In the future input current can be designed for more directly. In future designs nonlinear in the cascode could potentially be corrected by using transistors with higher linearity in beta and other IV characteristics.

Acknowledgements

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References

Digikey.com - Datasheets for the 2N5769 and component prices

The George Washington University School of Engineering and Applied Sciences -
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https://www2.seas.gwu.edu/~ece20/spring15/labs/tutorials/ECE_2115_Tutorial_6_Designing_a_Common_Collector_Amplifier.pdf

Microelectronic Circuits
by Adel S. Sedra; Kenneth C. (KC) Smith; Tony Chan Carusone; Vincent Gaudet

Appendices

Data Sheet for 2N5769 found at:

https://www.mouser.com/datasheet/2/68/2n5769_pn2369a-1518585.pdf

Table 1: Bill of Materials

Part	Quantity	Unit Price
2N5769	3	$4.24
1600nF Ceramic Capacitor	1	$0.10
40pF Ceramic Capacitor	1	$0.10
100uF Electrolytic Capacitor	1	$0.34
1000uF Electrolytic Capacitor	1	$0.66
10uF Ceramic Capacitor	2	$0.10
Common resistors Carbon Film	8	$0.12
Total Circuit Cost	-	$15.20