CmpE 124 Project 2: Signal Generator Tests AND, OR, XOR

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***Abstract*—Building and demonstrating the uses of the 74LS163 as a signal generator for combinational circuits.**

I. Introduction

THE purpose of this lab is to create a basic counter and use it as a signal generator for a combinational circuit. The counter, as well as, the adder are one of the most fundamental components of the computer. Being to keep count and keep count allows a computer or system designer to do a lot of things. One such purpose is to generate the signals needed to test the min-terms of a combinational circuit up to 4 inputs. In this project, the q0 and q1 signals will be used as the inputs for a SN74LS00N (NAND Gate), a SN74LS02N (NOR Gate), and a SN74LS86N (XOR), to see if the output matches the device's function for each min terms.

II. Design Methodology

A. Parts List

- HP 54603B Oscilloscope
- 8x 10KΩ Resistor
- 4x 390Ω Resistor
- 4x LEDs
- 10Mhz Crystal
- One Pole Double Throw switch
- 10pF ceramic capacitor
- SN74LS00N
- 2x SN74LS04N
- SN74LS02N
- SN74LS86N
- SN74LS163N

B. Truth Tables

TABLE I: 74LS00 NAND Gate Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

TABLE II: Outputs per stage of 74LS163

stage	q0	q1	q2	q3	rco
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
10	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

TABLE III: 74LS02 NOR Gate Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

TABLE IV: 74LS86 XOR Gate Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

C. Original and Derived Equations

SN74LS00N: $Y = \overline{ab}$
SN74LS02N: $Y = \overline{a + b}$
SN74LS04N: $Y = \overline{a}$
SN74LS86N: $Y = \overline{a}b + \overline{b}a$

D. Schematics

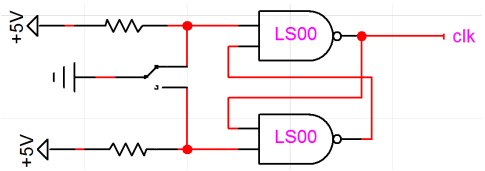

Fig. 1: RS Latch schematic circuit for manual clock.

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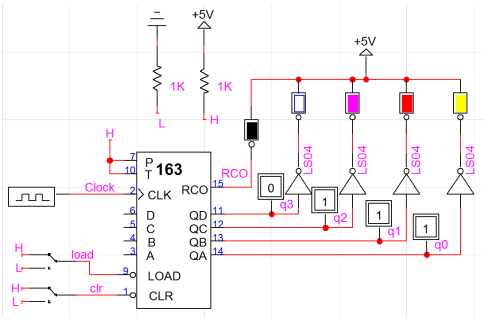

Fig. 2: Schematic of LS163 Circuit outputs connected to LEDs.

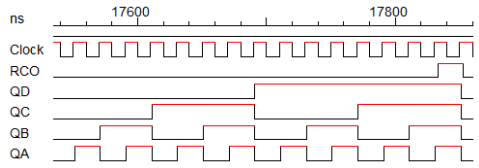

Fig. 3: Expected LS163 Circuit outputs signals.

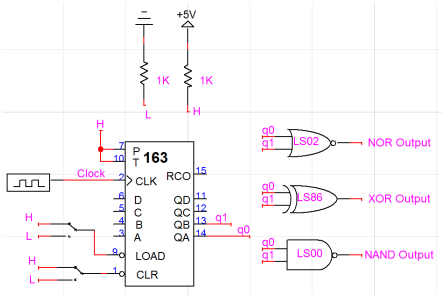

Fig. 4: Schematic for LS163, using inputs q0 and q1 for LS00 (NAND), LS02 (NOR), and LS86 (XOR).

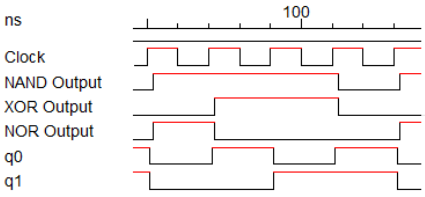

Fig. 5: Expected signal output from LS00, LS02, and LS86.

III. TESTING PROCEDURES

Step 1:
Connect latch to 74LS163 and toggle switch to see if LED indicators are counting in binary.

Step 2:
Measure clock signal by itself and show that is has a frequency of 10MHz.

Step 3:
Connect clock output signal to 163 and use oscilloscope probe to show output of clock against the output of q0, q1, q2, and q3 of 74LS163.

Step 4:
Use q0 and q1 outputs from 74LS163 and connect them to 74LS00, 74LS02, 74LS86 gates and show output on oscilloscope against clock signal.

Step 5:
Use q0 and q1 outputs from 74LS163 and connect them to 74LS00, 74LS02, 74LS86 gates and show output on oscilloscope against clock signal.

IV. TESTING RESULTS

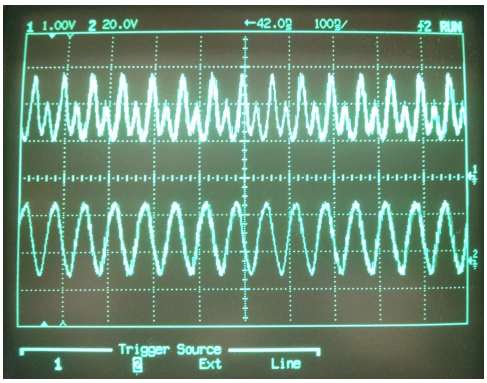

Fig. 6: Clock And LS163 q0 Signals.

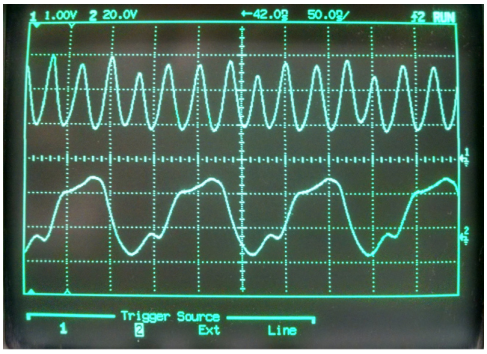

Fig. 7: Clock And LS163 q1 Signals.

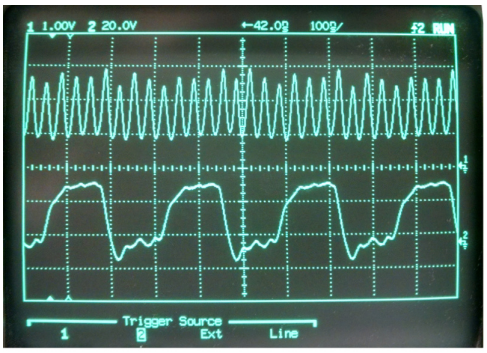

Fig. 8: Clock And LS163 q2 Signals.

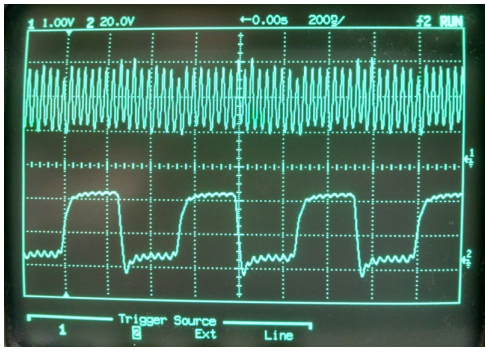

Fig. 9: Clock And LS163 q3 Signals.

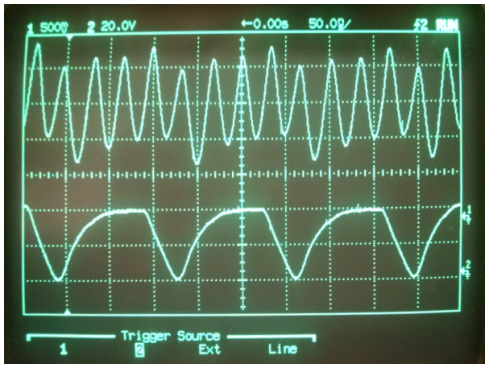

Fig. 10: Clock And LS00 Output Y1 Signal. q0 and q1 are connected to 74LS00 Input A1 and B1 Inputs receptively.

Fig. 11: Clock And LS02 Output Y1 Signal. q0 and q1 are connected to 74LS02 Input A1 and B1 Inputs receptively.

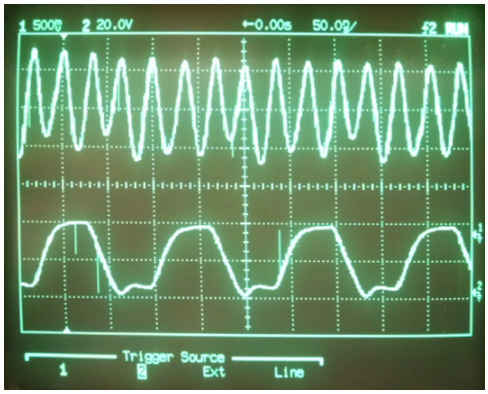

Fig. 12: Clock And LS86 Output Y1 Signal. q0 and q1 are connected to 74LS86 Input A1 and B1 Inputs receptively.

V. CONCLUSION

Despite the fact that the clock signal looks like a sine wave, the clock signal is still registering on the 74LS163. The aside from the outputs suffering from in circuit transients q0, q1, q2, q3 all look like and agree with their LogicWorks counter parts. The outputs of the 74LS00, 74LS02 and 74LS86 also match their LogicWorks counter parts as well.

The 74LS00's output is low only when both outputs are high which happens at clock the 4th rising edge. The 74LS02's output is only high only when both outputs are low which happens at clock the 1st rising edge. The 74LS86's output is high only when both outputs are differnt which happens at the clock's the 2nd and 3rd rising edge.

A. Problems Encountered

Some of the issues encountered in this lab were the result of bad sizing of the loading capacitor for the 10MHz crystal. Originally I used a 100pF cap for the crystal but this resulted in strange behaviour in the 163, such as the clock being triggered from a falling and a rising edge. So a 10pF cap resulted in a more stable waveform. With this change, the clock signal looks like a sine wave.

VI. APPENDICES AND REFERENCES

Not Applicable.