Ameba-Z DEV01 User Manual

This document defines pin out of Ameba-Z DEV01 demo board.

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1. Hardware block diagram

- IC: RTL8710B
- Module HDK version: HDK-XXXX
- DEV HDK version: RTL-AMEBAZ_DEV01_1V0

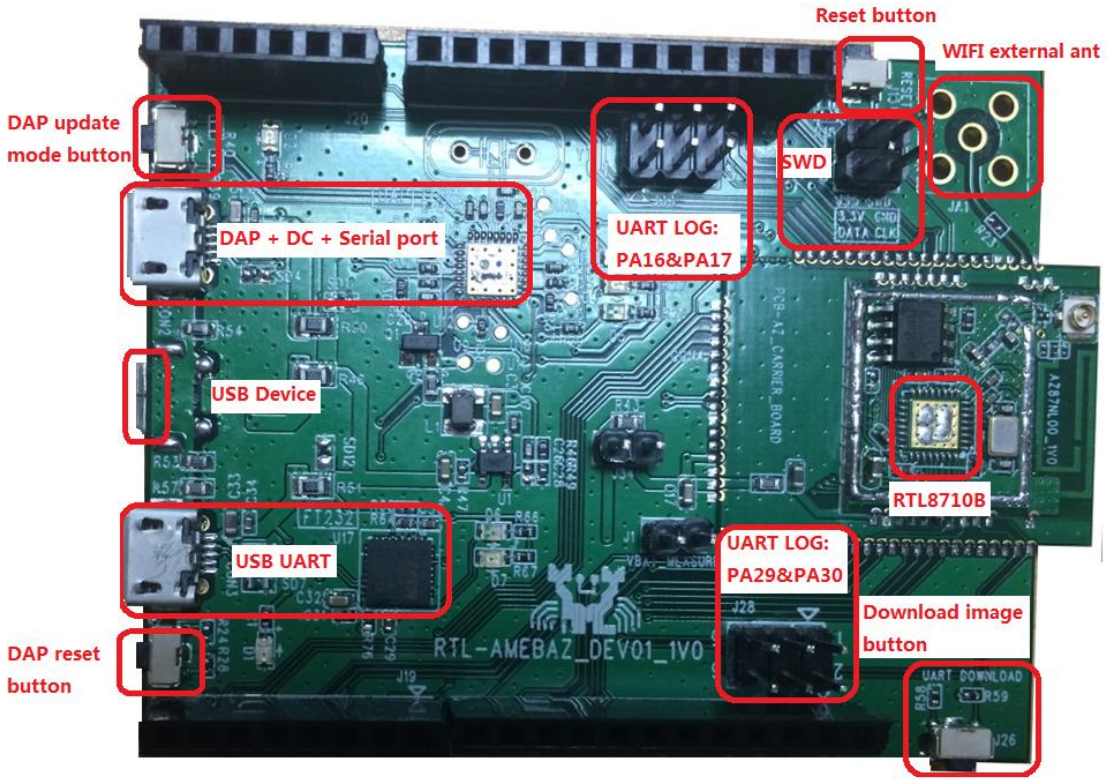


Figure 1 Ameba-Z DEV Diagram

2. System requirements

- Windows PC(XP,Vista,7)
- USB type

3. Pin mux Alternate Functions

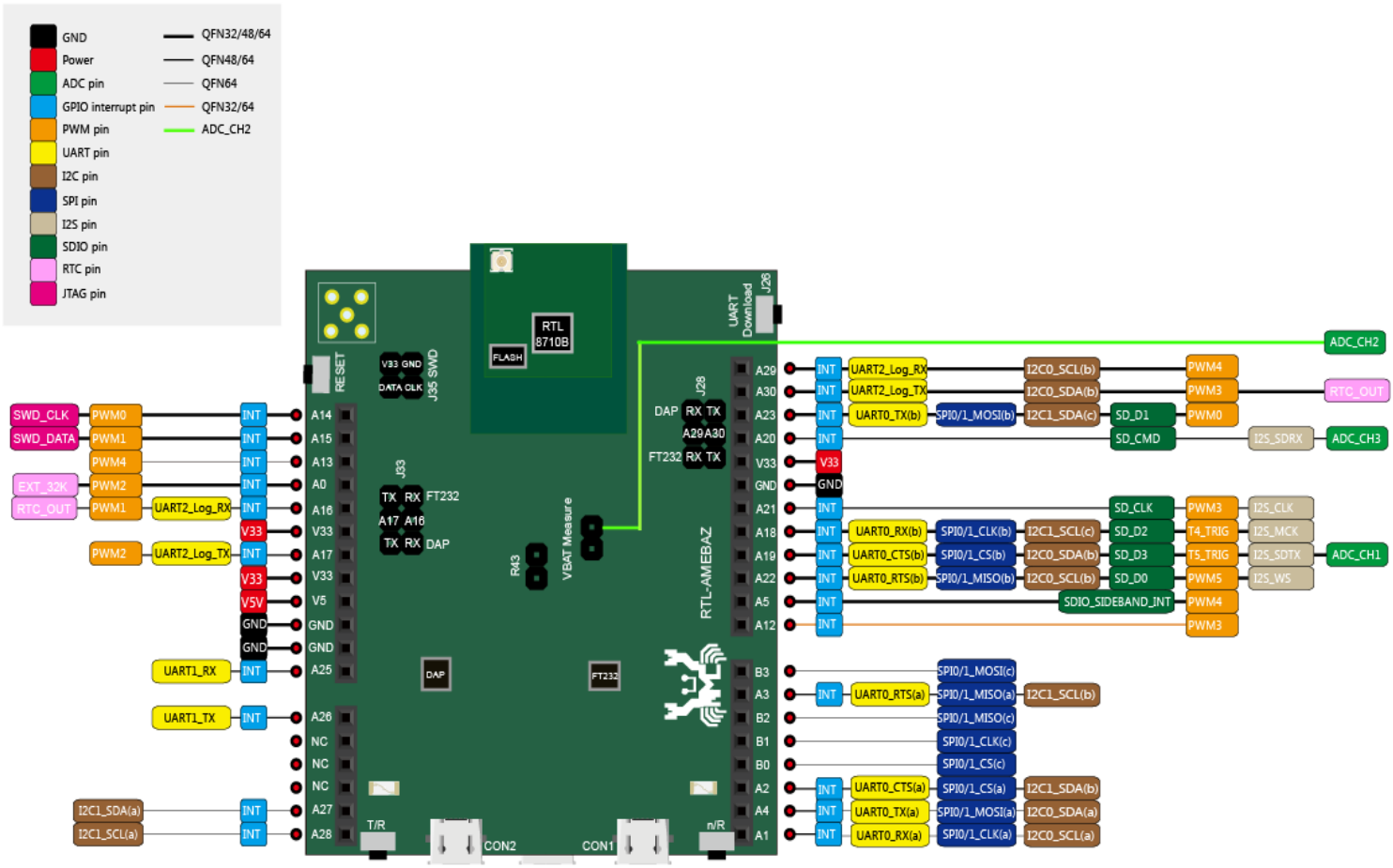
3.1. Pin mux table

Table 1 Ameba-Z pin mux table

QFN68 8711BG	QFN48 8711BN	QFN32 8710BN	GPIO	UART	SPI Master	SPI Slave	SPI Flash	I2C	SDIO	PWM/ TIMER	EXT32K	I2S	Others
✔	✔	✔	PA_14							PWM0	SWD_CLK		
✔	✔	✔	PA_15							PWM1	SWD_DATA		
✔			PA_13							PWM4			
✔	✔	✔	PA_0							PWM2	ext_32K		
✔	✔		PA_16	UART2_log_RXD						PWM1	RTC_OUT		
✔	✔		PA_17	UART2_log_TXD						PWM2			
✔	✔		PA_25	UART1_RXD									
✔	✔		PA_26	UART1_TXD									
✔			PA_28					I2C1_SCL					
✔			PA_27					I2C1_SDA					
✔		✔	PA_12							PWM3			
✔	✔		PA_4	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C0_SDA					
✔	✔		PA_1	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C0_SCL					
✔	✔		PA_2	UART0_CTS	SPI1_CS	SPI0_CS		I2C1_SDA					
✔	✔		PA_3	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C1_SCL					
✔	✔	✔	PA_6				SPIC_CS		SD_D2				
✔	✔	✔	PA_7				SPIC_DATA1		SD_D3				
✔	✔	✔	PA_8				SPIC_DATA2		SD_CMD				
✔	✔	✔	PA_9				SPIC_DATA0		SD_CLK				
✔	✔	✔	PA_10				SPIC_CLK		SD_D0				
✔	✔	✔	PA_11				SPIC_DATA3		SD_D1				
✔	✔	✔	PA_5						SDIO_SIDEBAND_INT	PWM4			WAKEUP_1
✔	✔	✔	PA_18	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C1_SCL	SD_D2	TIMER4_TRIG		I2S_MCK	WAKEUP_0

QFN68 8711BG	QFN48 8711BN	QFN32 8710BN	GPIO	UART	SPI Master	SPI Slave	SPI Flash	I2C	SDIO	PWM/ TIMER	EXT32K	I2S	Others
✔	✔	✔	PA_19	UART0_CTS	SPI1_CS	SPI0_CS		I2C0_SDA	SD_D3	TIMER5_TRIG		I2S_SD_TX	ADC1
✔	✔		PA_20						SD_CMD			I2S_SD_RX	ADC3
✔	✔		PA_21						SD_CLK	PWM3		I2S_CLK	
✔	✔	✔	PA_22	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C0_SCL	SD_D0	PWM5		I2S_WS	WAKEUP_2
✔	✔	✔	PA_23	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C1_SDA	SD_D1	PWM0			WAKEUP_3
✔			PB_1		SPI1_CLK	SPI0_SCK							
✔			PB_0		SPI1_CS	SPI0_CS							
✔			PB_2		SPI1_MISO	SPI0_MISO							
✔			PB_3		SPI1_MOSI	SPI0_MOSI							
✔			PB_4								SWD_CLK	I2S_MCK	
✔			PB_5								SWD_DATA	I2S_SD_TX	
✔			PA_24									I2S_SD_RX	
✔			PA_31									I2S_CLK	
✔			PB_6									I2S_WS	
✔	✔	✔	PA_30	UART2_log_TXD				I2C0_SDA		PWM3	RTC_OUT		
✔	✔	✔	PA_29	UART2_log_RXD				I2C0_SCL		PWM4			

3.2. Pin out reference



4. Features

Table 2 Ameba-Z Features

Feature list			*QFN68 RTL8711BG*	*QFN48 RTL8711BN*	*QFN32 RTL8710BN*
Integrated core	Core type		ARM CM4F		
	Core clock maximum freq.		125MHz		
Memory	Internal ROM		512KB		
	Internal SRAM		256KB		
	External FLASH		128MB		
FPU	Float process unit		Yes		
SWD/JTAG			SWD		
Backup register	Backup register for power save		16B		
Boot Reason			Yes		
F/W protection			Yes		
Read protection	RAM read protection		4KB		
WIFI	802.11 B/G/N		Yes		
BOR	BOR Detection		Yes		
peripherals	UART	Normal-UART	2	2	1
		Log-UART	1	1	1
	SPI Master	Max. 31.25Mbps	1	1	1
	SPI Slave	Max. 31.25Mbps	1	1	1
	I2C	Max. 400Kbps	2	2	2
	ADC	VBAT	1	0	1
		Thermal	1	1	1

Feature list			***QFN68 RTL8711BG***	***QFN48 RTL8711BN***	***QFN32 RTL8710BN***
		Normal	2	2	0
	GDMA	2*6 channels	2	2	2
	GPIO	IN/OUT/INT	39	26	17
	I2S		1	1	0
	RTC	D/H/M/S	1	1	1
		OUTPUT	1	1	1
	Timer	Basic timer use 32K	4	4	4
		Advanced timer use XTAL	2	2	2
	PWM	OUTPUT	6	6	6
		INPUT Capture	2	2	2
	WDG		1	1	1
	USB device		1	0	0
	SDIO 2.0 Device		1	1	1
External 32K	External 32K		1	1	1
Dsleep Wakepin	Deep sleep wake pin		4	4	4
Package	trays and tape-in-reel		(8x8mm^2)	(6x6mm^2)	(5x5mm^2)
Part Number			RTL8711BG	RTL8711BN	RTL8710BN

5. Hardware configuration

5.1. LOGUART PIN SEL

Table 3 Ameba-Z LOGUART EFUSE

	EFUSE	*LOGUART PIN*
EFUSE NOT PG	EFUSE 0x19[6]=0	GPIOA_29 & GPIOA_30
EFUSE PG	EFUSE 0x19[6]=0	GPIOA_29 & GPIOA_30
	EFUSE 0x19[6]=1	GPIOA_16 & GPIOA_17

5.2. SWD & LOGUART

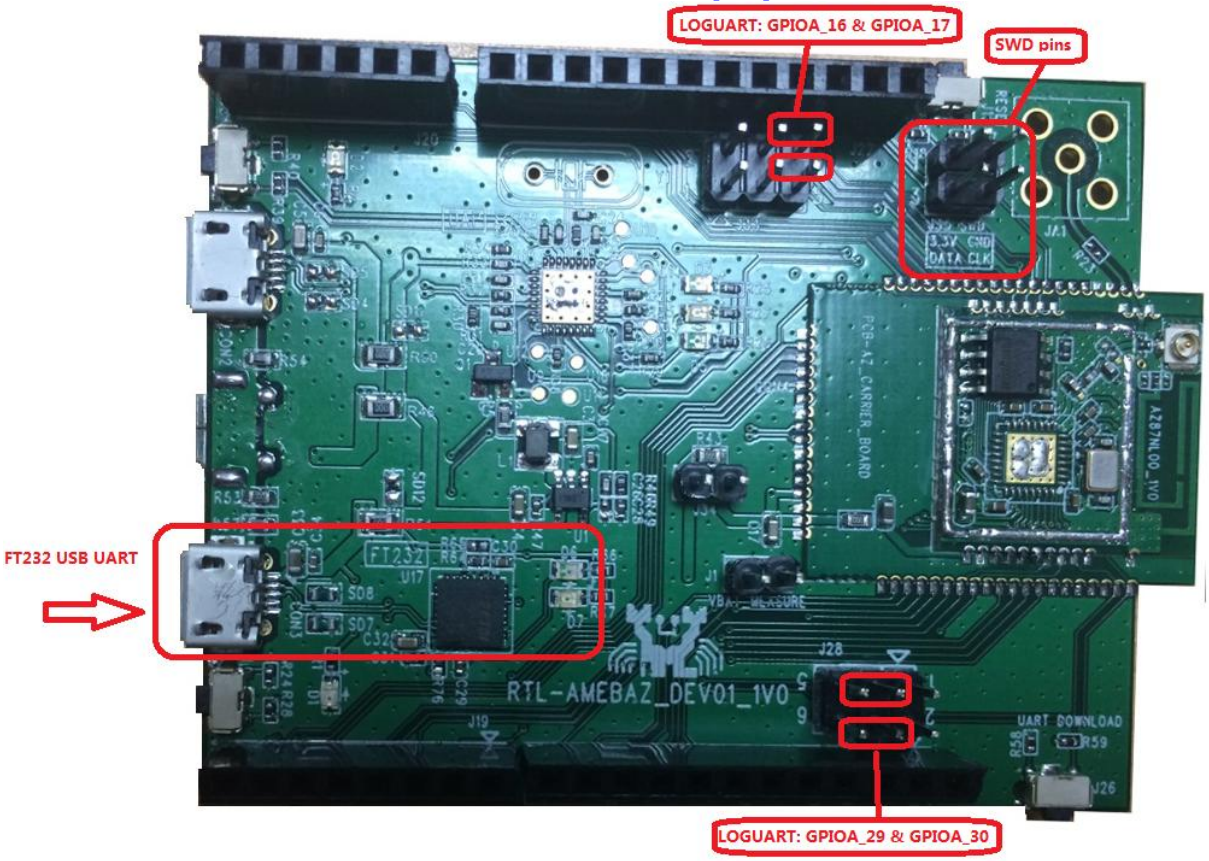


Figure 2 Ameba-Z SWD & LOGUART

5.3. CMSIS-DAP & LOGUART

RTL-AMEBAZ_DEV01 supports CMSIS-DAP debugger. It requires installing "serial to USB driver" at first. Serial to USB driver can be found in tools\serial_to_usb\mbedWinSerial_16466.
Connect board to the PC with micro-USB cable.

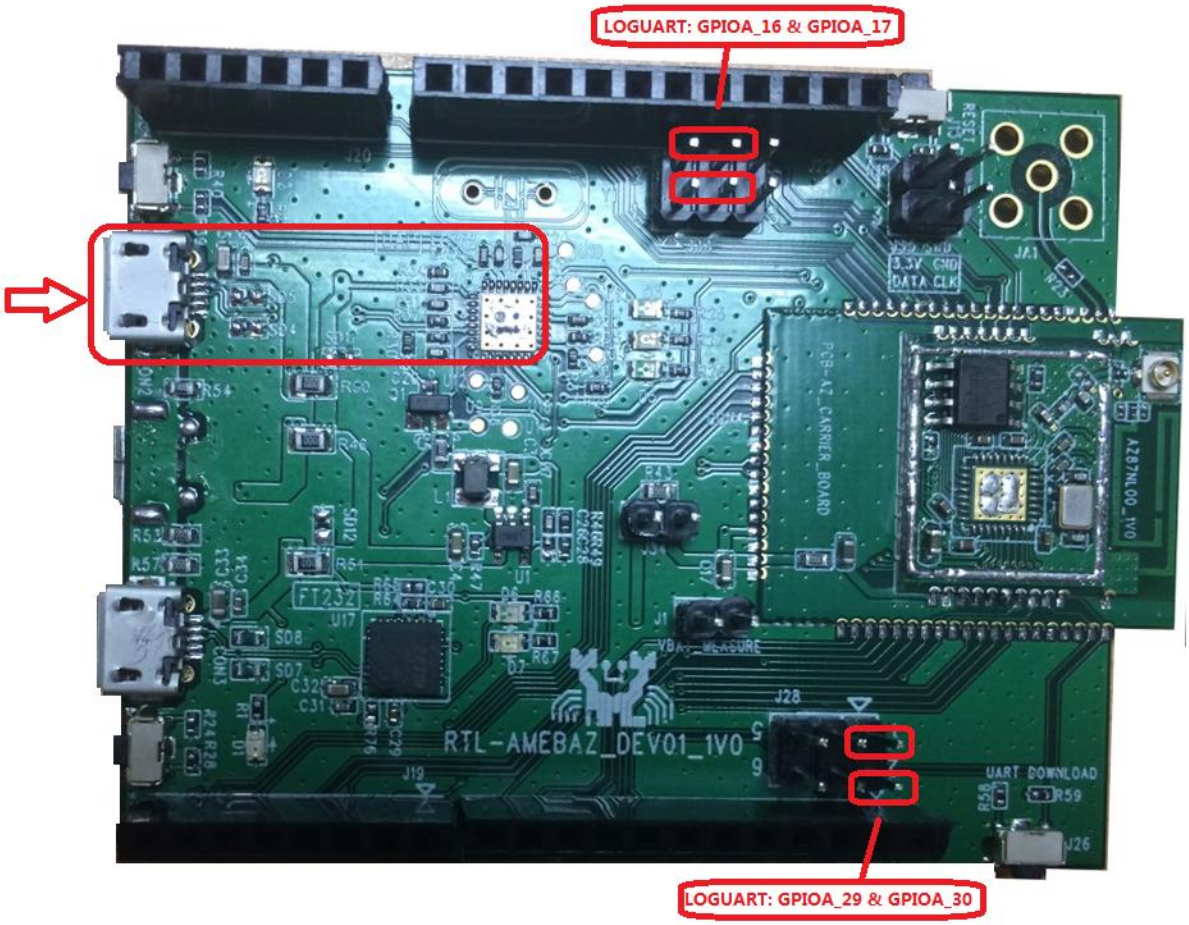


Figure 3 Ameba-Z CMSIS-DAP

6. DAP Firmware update

In DAP mode, the DAP firmware can be updated. Holding TGT_NRESET button (J24, red-circled) then press nRESET button (J17, blur-circled). Then the DAP mode window will show up.

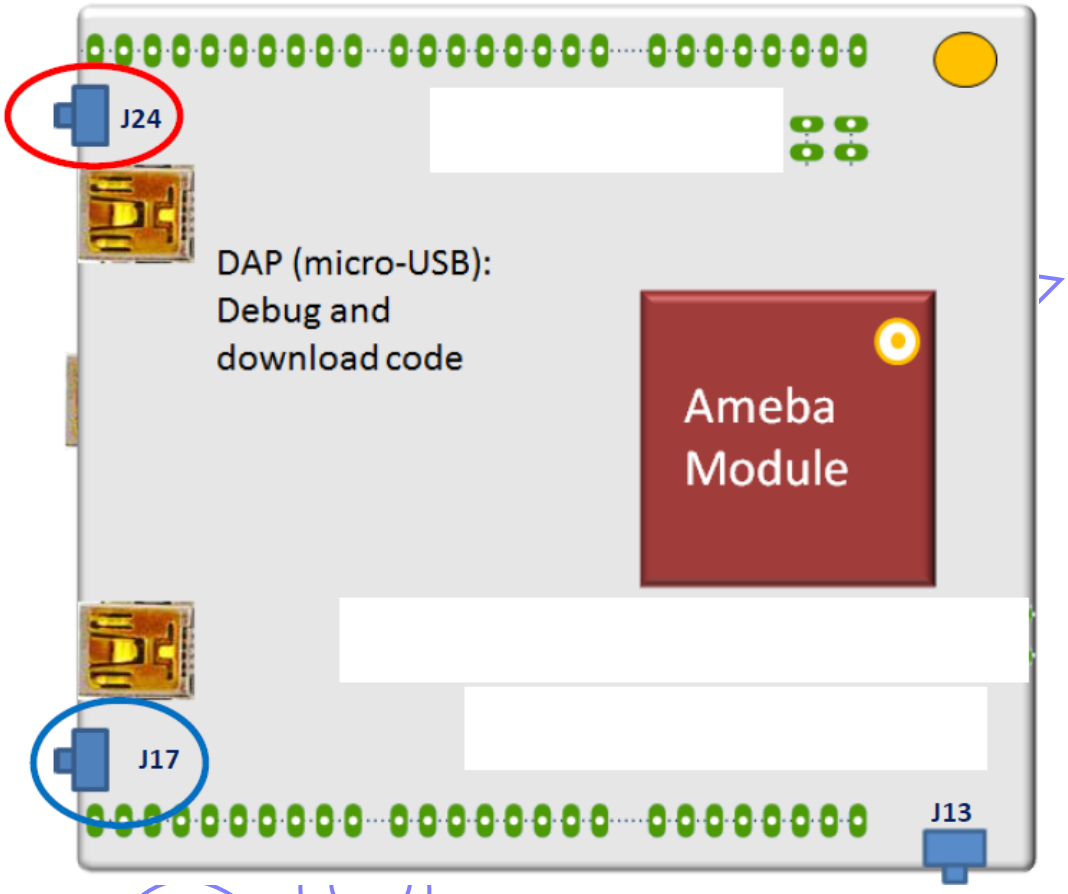


Figure 4 Ameba-Z CMSIS-DAP Firmware update

DAP window will show up when entering DAP mode.

7. Reference electrical schematics

7.1. DC power

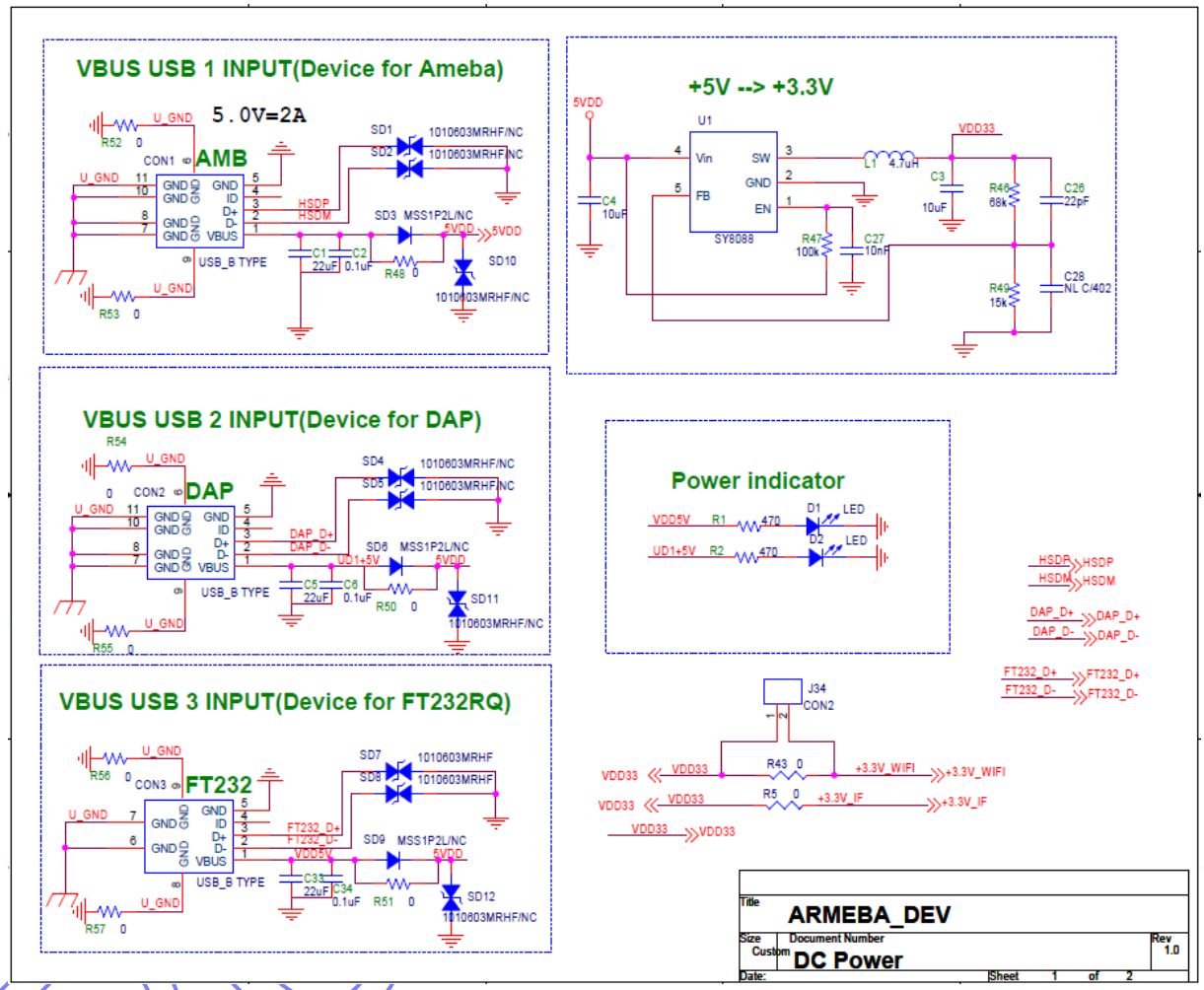


Figure 5 Ameba-Z Schematics DC-Power

7.2. DAP

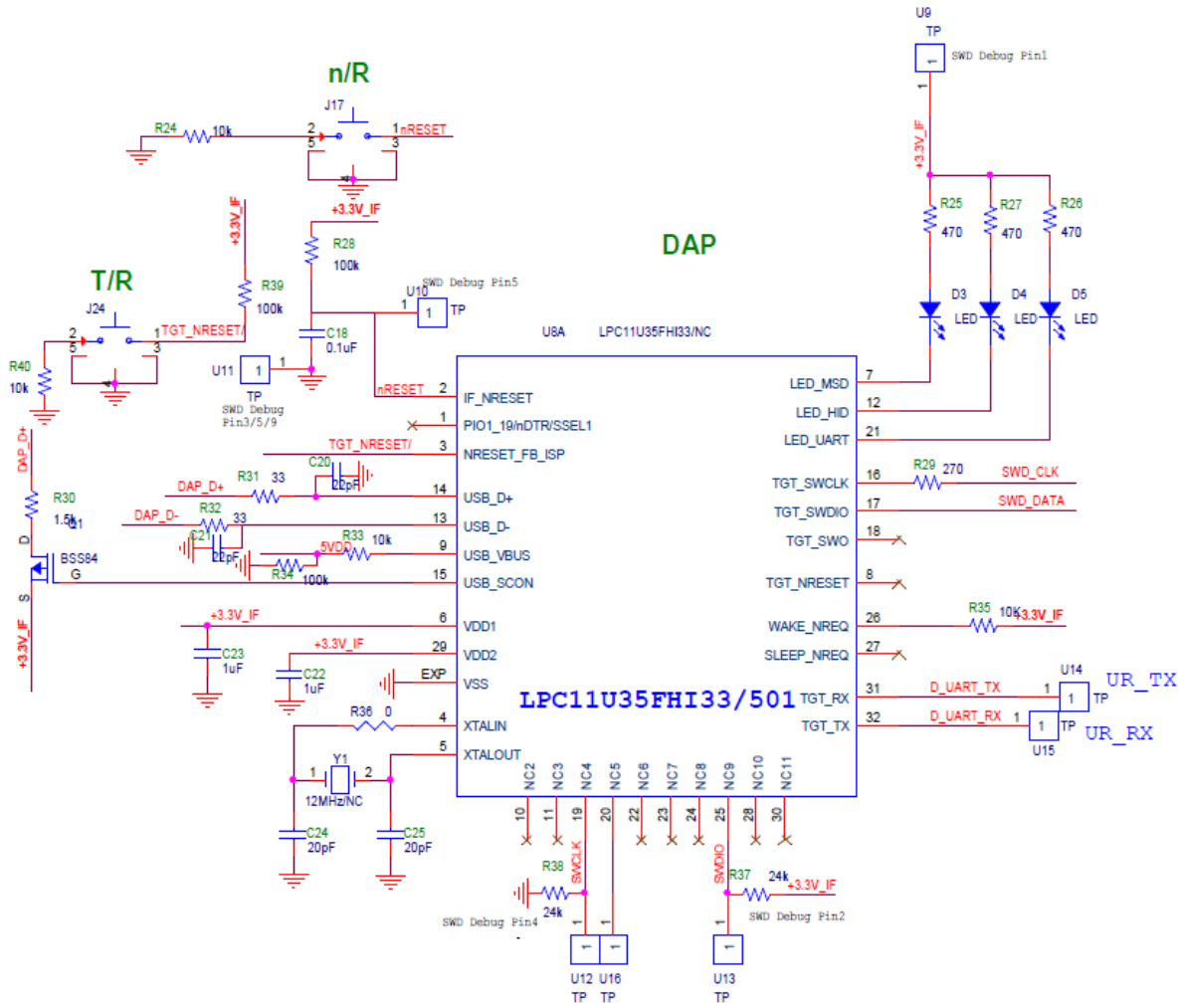


Figure 6 Ameba-Z Schematics DAP

7.3. FT232

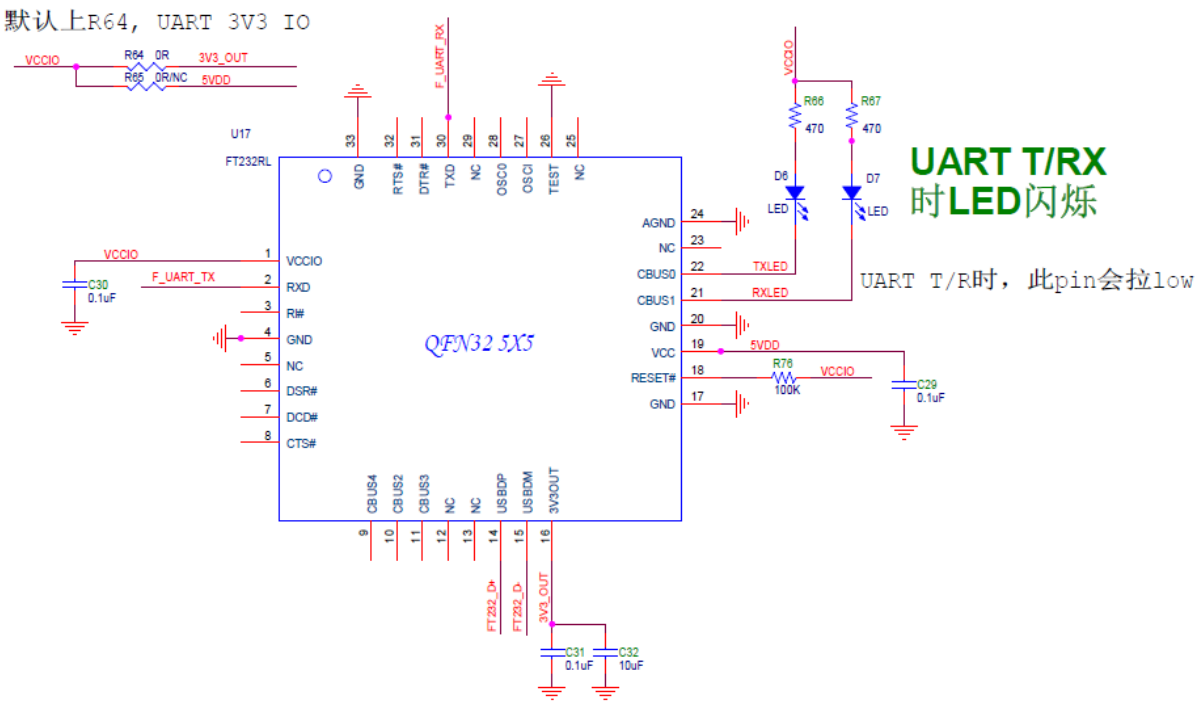


Figure 7 Ameba-Z Schematics FT-232

7.4. GPIO GROUP and Function-Mux

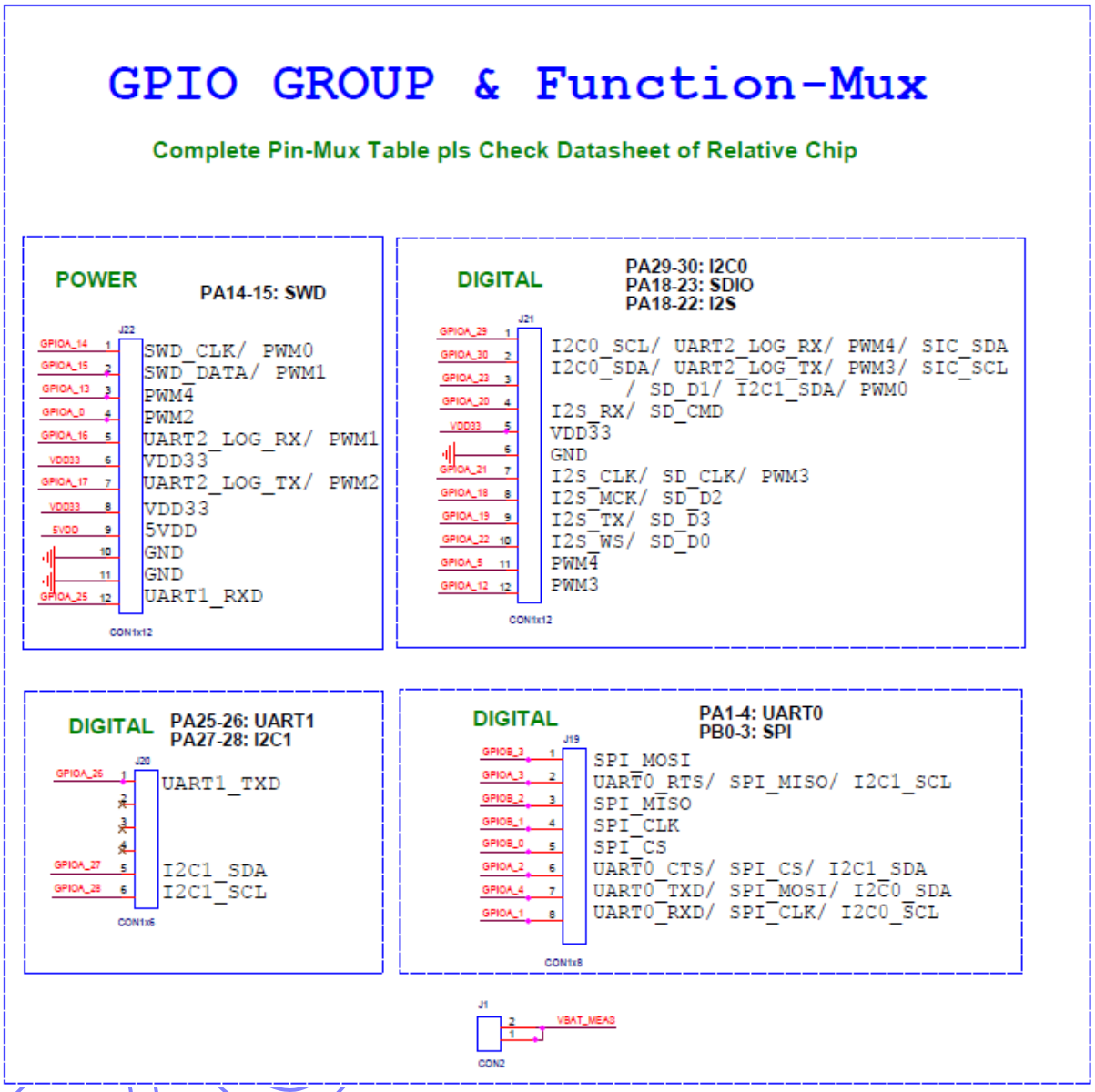


Figure 8 Ameba-Z Schematics GPIO Group & Function-Mux

7.5. SWD

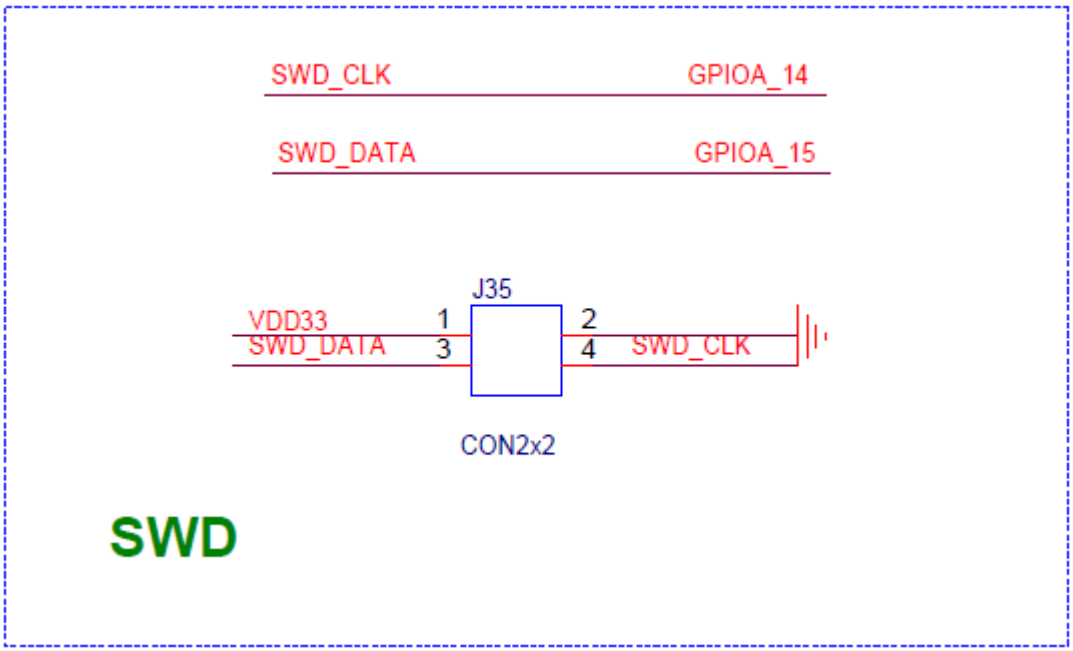


Figure 9 Ameba-Z Schematics SWD

7.6. UART LOG Selection

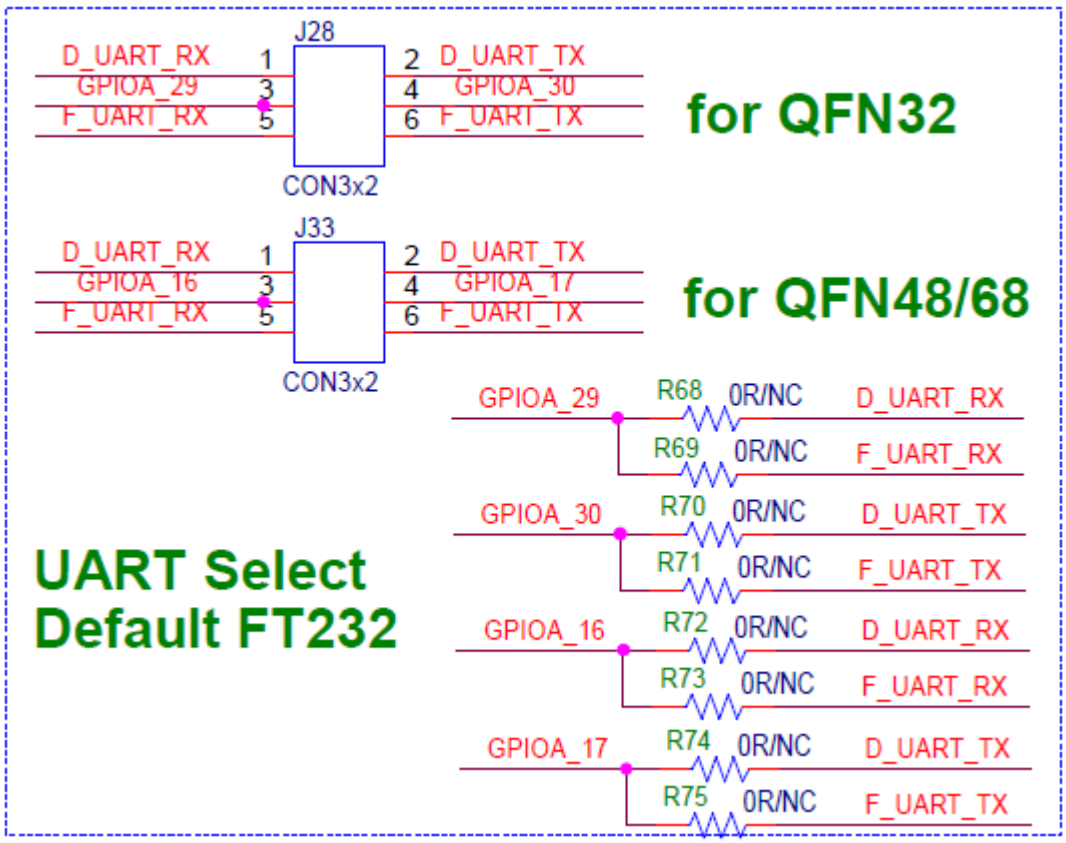


Figure 10 Ameba-Z Schematics UART-LOG Selection

7.7. 8710BN module

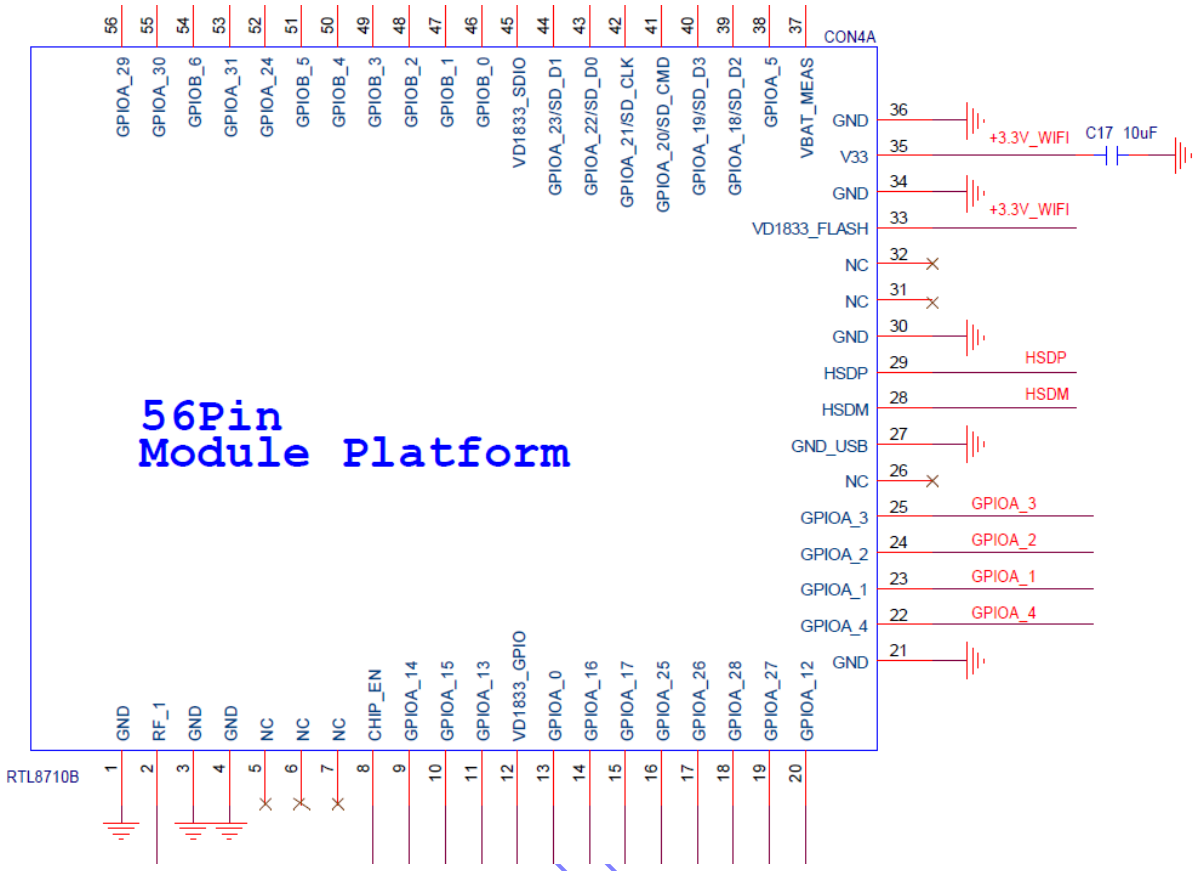


Figure 11 Ameba-Z Schematics 8710BN module