



UNIVERSIDAD POLITÉCNICA
DE LA ZONA METROPOLITANA DE GUADALAJARA

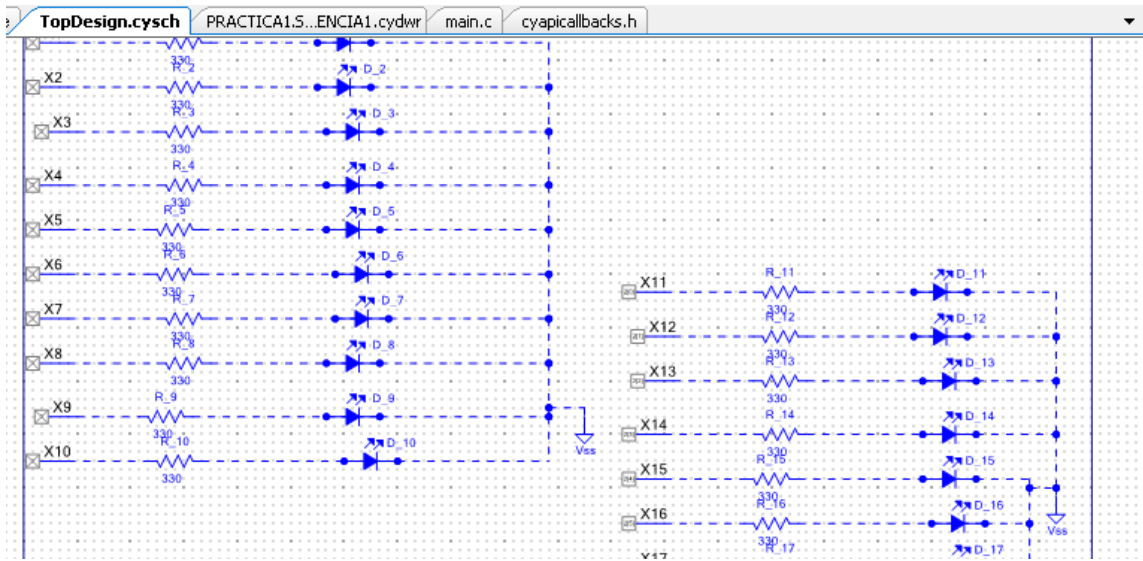
Práctica 1

Moisés Emanuel Martínez Noyola

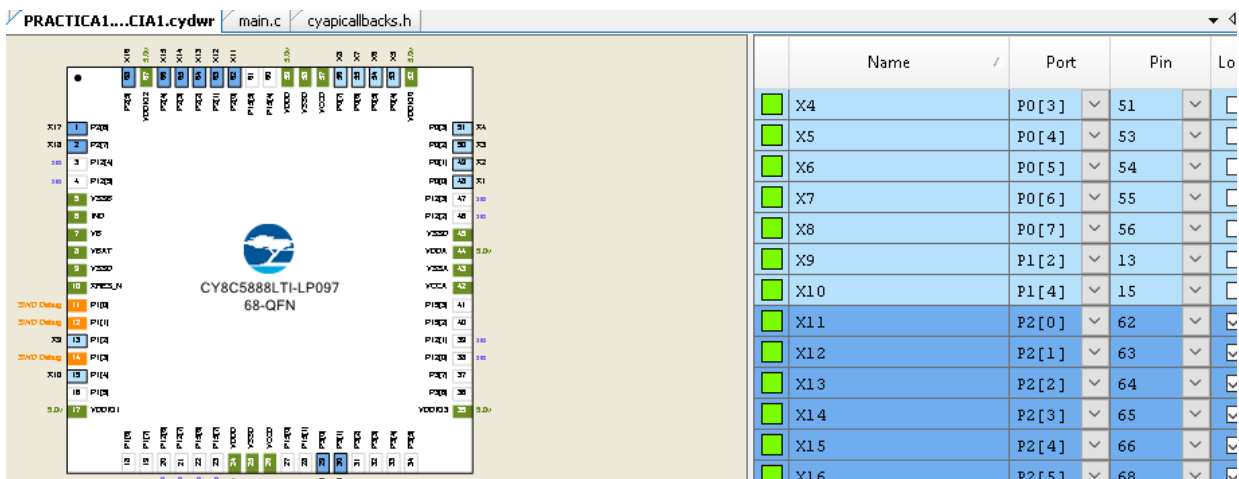
8°A Mecatrónica

Sistemas de embebidos

Primero armamos el circuito en forma de simulación.



En esta parte ajustamos nuestro pines para nuestra comodidad.



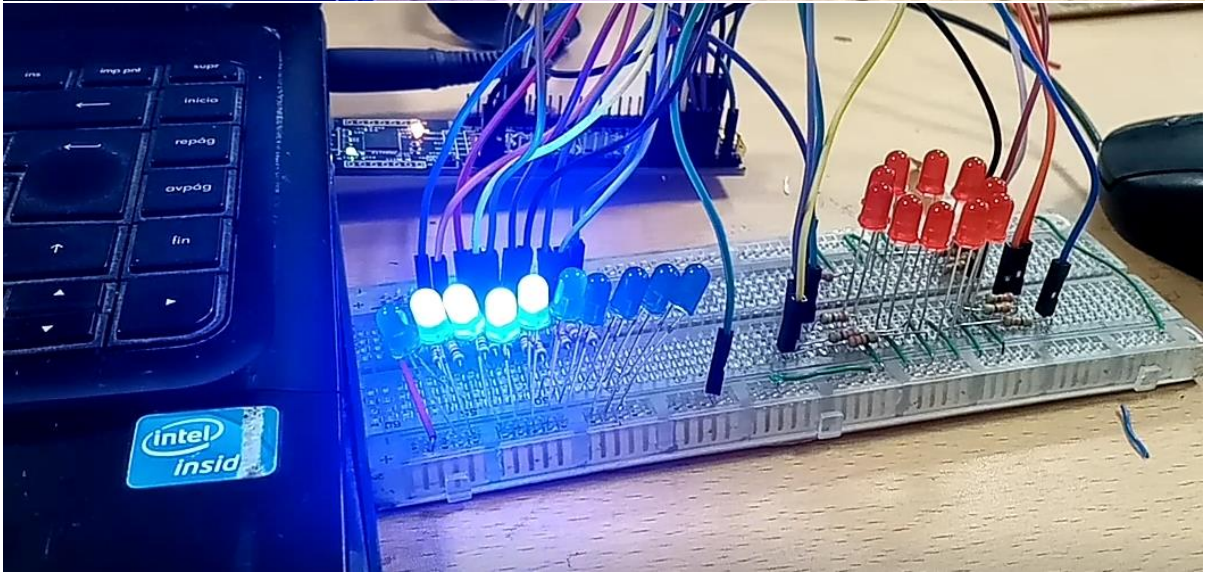
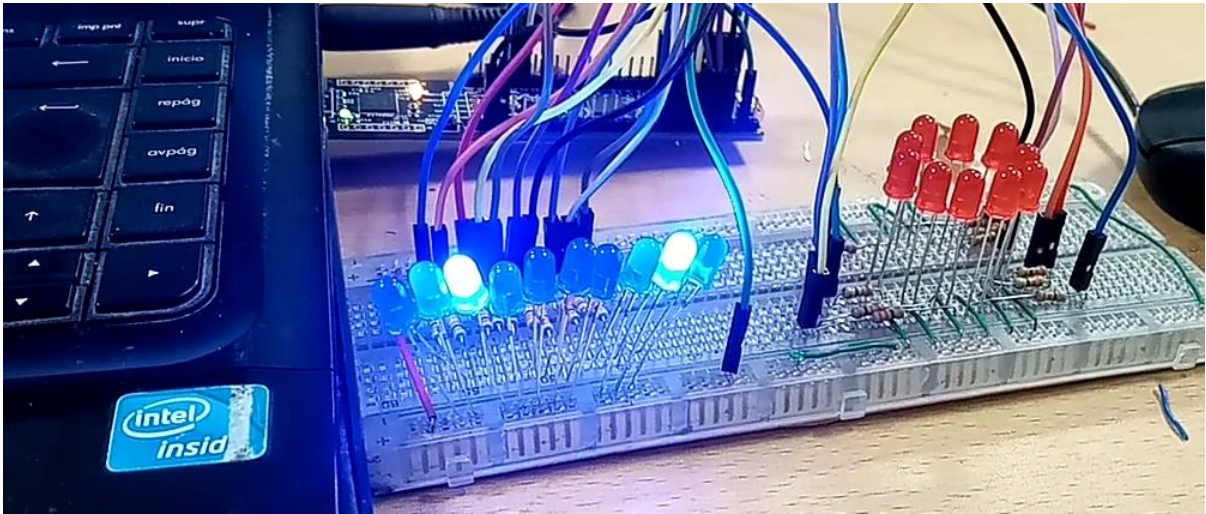
Aquí programamos las secuencias en lenguaje "c"

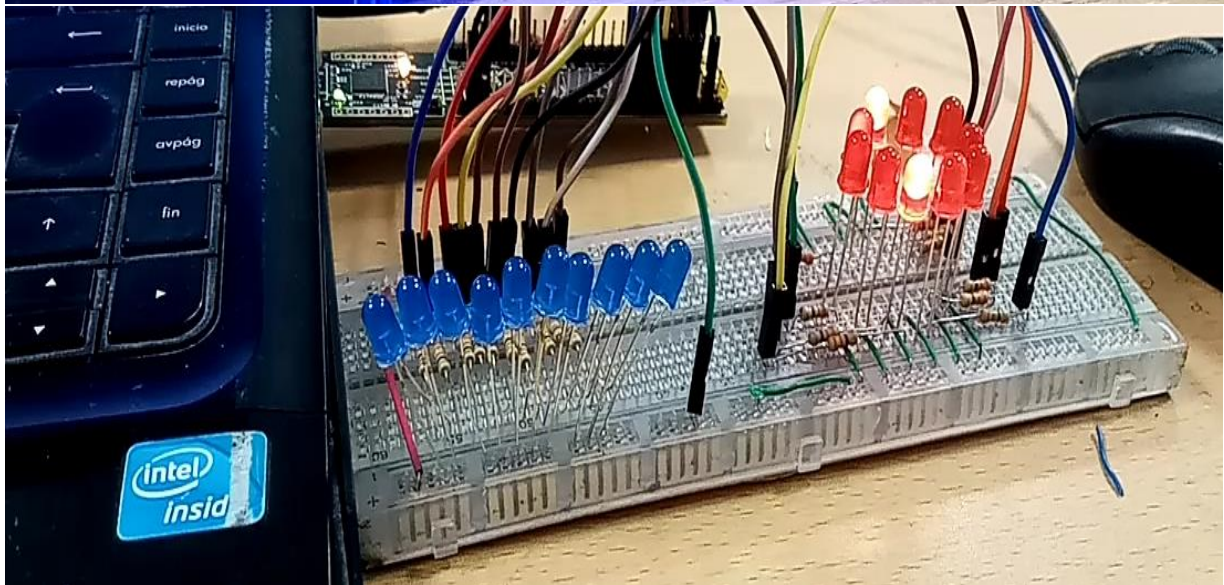
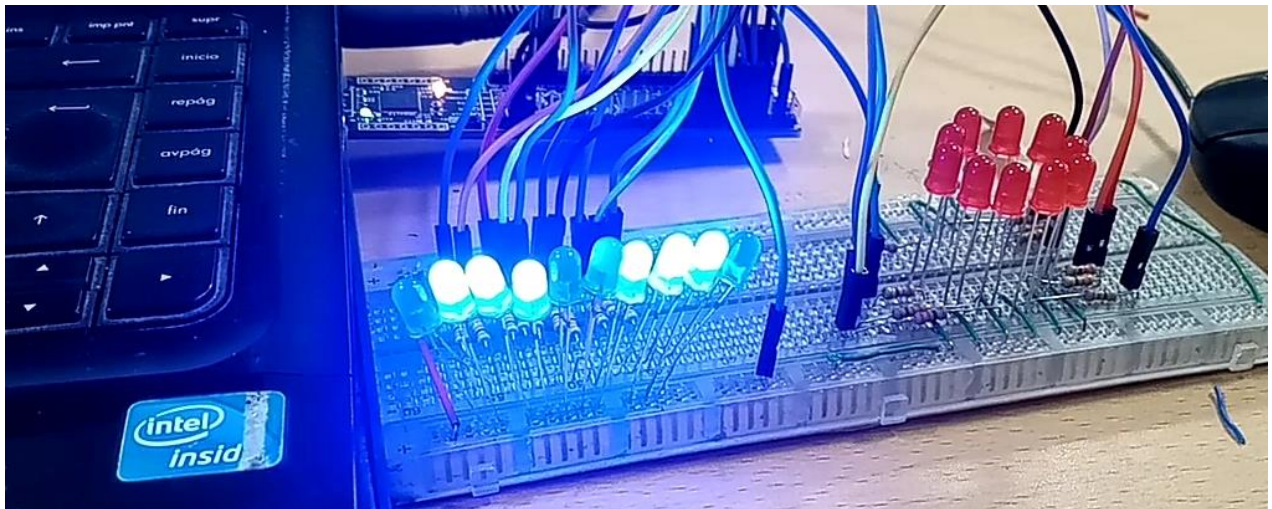
```
Start Page | TopDesign.cysch | PRACTICA1.5...ENCIA1.cydwr | main.c | cyapicalbacks.h
13  /* Place your initialization/startup code here (e.g. MyInst_Start())*/
14
15  int main(void) {
16      CyGlobalIntEnable;
17      //ledParpadea(); //Funcion que hace parpadear el LED integrado (loop infinito)
18      for(;;) {
19
20
21
22          //Serie 1//
23
24          X11_Write(1);
25          CyDelay(300);
26          X11_Write(0);
27          X12_Write(1);
28          X20_Write(1);
29          CyDelay(300);
30          X20_Write(0);
31          X12_Write(0);
32          X13_Write(1);
33          X19_Write(1);
34          CyDelay(300);
35          X13_Write(0);
36          X19_Write(0);
37          X14_Write(1);
38          X18_Write(1);
39          CyDelay(300);
40
41          //Termina serie 1//
42
43          //Serie 2//
44
45          X1_Write(1);
46          CyDelay(300);
47          X10_Write(1);
48          CyDelay(300);
49          X1_Write(0);
50          CyDelay(300);
51          X2_Write(1);
52          CyDelay(300);
53          X10_Write(0);
54          CyDelay(300);
55          X9_Write(1);
56          CyDelay(300);
57          X2_Write(0);
58          CyDelay(300);
59          X3_Write(1);
60          CyDelay(500);
61          X9_Write(0);
62          CyDelay(300);
63          X8_Write(1);
64          CyDelay(300);
65          X3_Write(0);
66          CyDelay(300);
67          X7_Write(1);
68          CyDelay(300);
69          X4_Write(1);
70          CyDelay(300);
71          X5_Write(1);
72          CyDelay(300);
73          X6_Write(1);
74          CyDelay(300);
75          X7_Write(0);
76          CyDelay(300);
77          X4_Write(0);
78          CyDelay(300);
79          X5_Write(0);
80          CyDelay(300);
81          X6_Write(0);
82          CyDelay(300);
83          X7_Write(1);
84          CyDelay(300);
85          X4_Write(1);
86          CyDelay(300);
87          X5_Write(1);
88          CyDelay(300);
89          X6_Write(1);
90          CyDelay(300);
91          X7_Write(0);
92          CyDelay(300);
93          X4_Write(0);
94          CyDelay(300);
95          X5_Write(0);
96          CyDelay(300);
97          X6_Write(0);
98          CyDelay(300);
99          X7_Write(1);
100         CyDelay(300);
101         X4_Write(1);
102         CyDelay(300);
103         X5_Write(1);
104         CyDelay(300);
105         X6_Write(1);
106         CyDelay(300);
107         X7_Write(0);
108         CyDelay(300);
109         X4_Write(0);
110         CyDelay(300);
111         X5_Write(0);
112         CyDelay(300);
113         X6_Write(0);
114         CyDelay(300);
115         X7_Write(1);
116         CyDelay(300);
117         X4_Write(1);
118         CyDelay(300);
119         X5_Write(1);
120         CyDelay(300);
121         X6_Write(1);
122         CyDelay(300);
123         X7_Write(0);
124         CyDelay(300);
125         X4_Write(0);
126         CyDelay(300);
127         X5_Write(0);
128         CyDelay(300);
129         X6_Write(0);
130         CyDelay(300);
131         X7_Write(1);
132         CyDelay(300);
133         X4_Write(1);
134         CyDelay(300);
135         X5_Write(1);
136         CyDelay(300);
137         X6_Write(1);
138         CyDelay(300);
139         X7_Write(0);
140         CyDelay(300);
141         X4_Write(0);
142         CyDelay(300);
143         X5_Write(0);
144         CyDelay(300);
145         X6_Write(0);
146         CyDelay(300);
147         X7_Write(1);
148         CyDelay(300);
149         X4_Write(1);
150         CyDelay(300);
151         X5_Write(1);
152         CyDelay(300);
153         X6_Write(1);
154         CyDelay(300);
155         X7_Write(0);
156         CyDelay(300);
157         X4_Write(0);
158         CyDelay(300);
159         X5_Write(0);
160         CyDelay(300);
161         X6_Write(0);
162         CyDelay(300);
163         X7_Write(1);
164         CyDelay(300);
165         X4_Write(1);
166         CyDelay(300);
167         X5_Write(1);
168         CyDelay(300);
169         X6_Write(1);
170         CyDelay(300);
171         X7_Write(0);
172         CyDelay(300);
173         X4_Write(0);
174         CyDelay(300);
175         X5_Write(0);
176         CyDelay(300);
177         X6_Write(0);
178         CyDelay(300);
179         X7_Write(1);
180         CyDelay(300);
181         X4_Write(1);
182         CyDelay(300);
183         X5_Write(1);
184         CyDelay(300);
185         X6_Write(1);
186         CyDelay(300);
187         X7_Write(0);
188         CyDelay(300);
189         X4_Write(0);
190         CyDelay(300);
191         X5_Write(0);
192         CyDelay(300);
193         X6_Write(0);
194         CyDelay(300);
195         X7_Write(1);
196         CyDelay(300);
197         X4_Write(1);
198         CyDelay(300);
199         X5_Write(1);
200         CyDelay(300);
201         X6_Write(1);
202         CyDelay(300);
203         X7_Write(0);
204         CyDelay(300);
205         X4_Write(0);
206         CyDelay(300);
207         X5_Write(0);
208         CyDelay(300);
209         X6_Write(0);
210         CyDelay(300);
211         X7_Write(1);
212         CyDelay(300);
213         X4_Write(1);
214         CyDelay(300);
215         X5_Write(1);
216         CyDelay(300);
217         X6_Write(1);
218         CyDelay(300);
219         X7_Write(0);
220         CyDelay(300);
221         X4_Write(0);
222         CyDelay(300);
223         X5_Write(0);
224         CyDelay(300);
225         X6_Write(0);
226         CyDelay(300);
227         X7_Write(1);
228         CyDelay(300);
229         X4_Write(1);
230         CyDelay(300);
231         X5_Write(1);
232         CyDelay(300);
233         X6_Write(1);
234         CyDelay(300);
235         X7_Write(0);
236         CyDelay(300);
237         X4_Write(0);
238         CyDelay(300);
239         X5_Write(0);
240         CyDelay(300);
241         X6_Write(0);
242         CyDelay(300);
243         X7_Write(1);
244         CyDelay(300);
245         X4_Write(1);
246         CyDelay(300);
247         X5_Write(1);
248         CyDelay(300);
249         X6_Write(1);
250         CyDelay(300);
251         X7_Write(0);
252         CyDelay(300);
253         X4_Write(0);
254         CyDelay(300);
255         X5_Write(0);
256         CyDelay(300);
257         X6_Write(0);
258         CyDelay(300);
259         X7_Write(1);
260         CyDelay(300);
261         X4_Write(1);
262         CyDelay(300);
263         X5_Write(1);
264         CyDelay(300);
265         X6_Write(1);
266         CyDelay(300);
267         X7_Write(0);
268         CyDelay(300);
269         X4_Write(0);
270         CyDelay(300);
271         X5_Write(0);
272         CyDelay(300);
273         X6_Write(0);
274         CyDelay(300);
275         X7_Write(1);
276         CyDelay(300);
277         X4_Write(1);
278         CyDelay(300);
279         X5_Write(1);
280         CyDelay(300);
281         X6_Write(1);
282         CyDelay(300);
283         X7_Write(0);
284         CyDelay(300);
285         X4_Write(0);
286         CyDelay(300);
287         X5_Write(0);
288         CyDelay(300);
289         X6_Write(0);
290         CyDelay(300);
291         X7_Write(1);
292         CyDelay(300);
293         X4_Write(1);
294         CyDelay(300);
295         X5_Write(1);
296         CyDelay(300);
297         X6_Write(1);
298         CyDelay(300);
299         X7_Write(0);
300         CyDelay(300);
301         X4_Write(0);
302         CyDelay(300);
303         X5_Write(0);
304         CyDelay(300);
305         X6_Write(0);
306         CyDelay(300);
307         X7_Write(1);
308         CyDelay(300);
309         X4_Write(1);
310         CyDelay(300);
311         X5_Write(1);
312         CyDelay(300);
313         X6_Write(1);
314         CyDelay(300);
315         X7_Write(0);
316         CyDelay(300);
317         X4_Write(0);
318         CyDelay(300);
319         X5_Write(0);
320         CyDelay(300);
321         X6_Write(0);
322         CyDelay(300);
323         X7_Write(1);
324         CyDelay(300);
325         X4_Write(1);
326         CyDelay(300);
327         X5_Write(1);
328         CyDelay(300);
329         X6_Write(1);
330         CyDelay(300);
331         X7_Write(0);
332         CyDelay(300);
333         X4_Write(0);
334         CyDelay(300);
335         X5_Write(0);
336         CyDelay(300);
337         X6_Write(0);
338         CyDelay(300);
339         X7_Write(1);
340         CyDelay(300);
341         X4_Write(1);
342         CyDelay(300);
343         X5_Write(1);
344         CyDelay(300);
345         X6_Write(1);
346         CyDelay(300);
347         X7_Write(0);
348         CyDelay(300);
349         X4_Write(0);
350         CyDelay(300);
351         X5_Write(0);
352         CyDelay(300);
353         X6_Write(0);
354         CyDelay(300);
355         X7_Write(1);
356         CyDelay(300);
357         X4_Write(1);
358         CyDelay(300);
359         X5_Write(1);
360         CyDelay(300);
361         X6_Write(1);
362         CyDelay(300);
363         X7_Write(0);
364         CyDelay(300);
365         X4_Write(0);
366         CyDelay(300);
367         X5_Write(0);
368         CyDelay(300);
369         X6_Write(0);
370         CyDelay(300);
371         X7_Write(1);
372         CyDelay(300);
373         X4_Write(1);
3
```

```
121
122 //Serie 3//
123
124 X1_Write(1);
125 X2_Write(1);
126 X3_Write(1);
127 CyDelay(300);
128 X4_Write(1);
129 X1_Write(0);
130 CyDelay(300);
131 X5_Write(1);
132 X2_Write(0);
133 CyDelay(300);
134 X6_Write(1);
135 X3_Write(0);
136 CyDelay(300);
137 X7_Write(1);
138 X4_Write(0);
139 CyDelay(300);
140 X8_Write(1);
141 X5_Write(0);
142 CyDelay(300);
143 X9_Write(1);
144 X6_Write(0);
145 CyDelay(500);
146 X10_Write(1);
147 X7_Write(0);
```

```
154 CyDelay(300);
155
156 //Termina serie 3//
157
158 //Serie 4//
159
160 X1_Write(1);
161 X10_Write(1);
162 CyDelay(300);
163 X2_Write(1);
164 X9_Write(1);
165 CyDelay(300);
166 X3_Write(1);
167 X8_Write(1);
168 CyDelay(300);
169 X1_Write(0);
170 X10_Write(0);
171 X4_Write(1);
172 X7_Write(1);
173 CyDelay(300);
174 X9_Write(0);
175 X2_Write(0);
176 X5_Write(1);
177 X6_Write(1);
178 CyDelay(300);
179 X3_Write(0);
180 X7_Write(0);
```

```
190 //Termina serie 4//
191
192 //Serie 5//
193
194 X11_Write(1);
195 CyDelay(300);
196 X11_Write(0);
197 X13_Write(1);
198 X19_Write(1);
199 CyDelay(300);
200 X13_Write(0);
201 X19_Write(0);
202 X20_Write(1);
203 X12_Write(1);
204 CyDelay(300);
205 X20_Write(0);
206 X12_Write(0);
207 X18_Write(1);
208 X14_Write(1);
209 CyDelay(300);
210 X18_Write(0);
211 X14_Write(0);
212 X13_Write(1);
213 X19_Write(1);
214 CyDelay(300);
215 X19_Write(0);
216 X13_Write(0);
```





Conclusión.

Trabajar con esta tarjeta, en mi opinión, es más sencillo que trabajar con la raspberry e igualmente funcional. Aparte de la comodidad y facilidad, es más económica.