1.2 a. 采用流水线提高性能
b. 通过冗余提高可靠性
c. 采用预测提高性能
d. 加速大概率事件
e. 存储器层次
f. 采用并行提高性能
g. 顾问摩尔定律的设计
h. 使用抽象简化设计

1.4 a. 1280 × 1024 像素 = 1310720 像素

故 1310720 × 3 × 1 = 3932160 bytes/frame

b. $time = \frac{3932160\ bytes \times 8\ bits/byte}{10^8\ bits/second} = 0.31$ 秒

1.7 a. $CPI_A = \frac{1.1 \times 10^9}{1.0 \times 10^9} = 1.1$

$CPI_B = \frac{1.5 \times 10^9}{1.2 \times 10^9} = 1.25$

b. 由 时钟频率 $= \frac{CPI \times 执行数}{执行时间}$

故设执行时间 = t 则 $f_A = \frac{1.0 \times 10^9 \cdot 1.1}{t}$

$f_B = \frac{1.2 \times 10^9 \cdot 1.25}{t}$

故 $\frac{f_A}{f_B} = \frac{1.1 \times 10^9}{1.2 \times 1.25 \times 10^9} \approx 0.73$

c. 执行时间 $t_A = 1.1s$, $t_B = 1.5s$

$t_{new} = \frac{1.1 \times 6 \times 10^8}{10^9} = 0.66s$

故 $\frac{t_A}{t_{new}} = \frac{1.1}{0.66} = 1.67$ $\frac{t_B}{t_{new}} = \frac{1.5}{0.66} = 2.27$

1.9. (1) 单核执行时间 $t_1 = \frac{2.56\times10^9 + 1.28\times10^9\times12 + 5\times2.56\times10^8}{2\times10^9} = 9.6s$

多核: $t_p = \frac{2.56\times10^9\times\frac{1}{0.7p} + 12\times1.28\times10^9\times\frac{1}{0.7p} + 5\times2.56\times10^8}{2\times10^9} = (0.64 + \frac{12.8}{p})s$

分别代入 $p=2, 4, 8$ 得 $t_2 = 7.04s$ $t_4 = 3.84s$ $t_8 = 2.24s$

加速比 $S_2 = \frac{9.6}{7.04} = 1.36$ $S_8 = \frac{9.6}{2.24} = 4.29$

$S_4 = \frac{9.6}{3.84} = 2.5$

(2) 单核: $t_1' = \frac{2\times2.56\times10^9 + 1.28\times12\times10^9 + 5\times2.56\times10^8}{2\times10^9} = 10.88s$

多核: $t_p' = \frac{2.56\times2\times10^9\times\frac{1}{0.7p} + 12\times1.28\times10^9\times\frac{1}{0.7p} + 5\times2.56\times10^8}{2\times10^9}$

$= (0.64 + \frac{14.6}{p})s$ 加速 $p=2, 4, 8$ 的

$t_2' = 7.94s$ $t_8' = 2.465s$

$t_4' = 4.29s$

(3) 设降低为原来的 m 倍 则

$t_1'' = \frac{2.56\times10^9 + 1.28\times10^9\times12m + 5\times2.56\times10^8}{2\times10^9} = t_4$

又 $t_4 = \frac{(2.56\times10^9 + 1.28\times10^9\times12)\times\frac{1}{2.8} + 5\times2.56\times10^8}{2\times10^9}$

分 $m = 0.25$ 故新 CPI 降低到 $\frac{1}{4}\times12 = 3$

1.11. (1) $CPI = \frac{750}{0.333\times10^{-9}\times2.38\times10^{12}} = 0.95$

(2) 功值 $= \frac{9650}{750} = 12.86$

(3) CPU时间 $= \frac{CPI\times指令数}{时钟频率}$, 故增长10%

(4) $\frac{t'}{t} = 1.1\times1.05 = 1.155$ 故增加 15.5%

(5) 由于 $score = \frac{t_{ref}}{t}$

故 $\frac{score'}{score} = \frac{t}{t'} = \frac{1}{1.155} = 0.86$ 即分数下降了 14%

(6) $CPI_{new} = \frac{700 \times 4 \times 10^9}{0.85 \times 2.38 \times 10^{12}} = 1.38$

(7) $\frac{f_{new}}{f} = \frac{4}{3} = 1.33$, $\frac{CPI_{new}}{CPI} = \frac{1.38}{0.95} = 1.45$

故不相同。其原因是虽然指令下降了15%，但CPU时间只下降了7%.

(8) $\frac{700}{750} \approx 93.3\%$ 故减少了 6.7%

(9) 设指令数为 n ，由于 $指令数 = \frac{执行时间 \times 主频}{CPI}$

故 $n = \frac{960 \times 0.9 \times 4 \times 10^9 \times 10^9}{1.61} = 2146$

(10) 由于 $t = \frac{CPI \times 指令数}{主频}$

故 $f_1 = \frac{f}{0.9} = 3.33GHz$

(11) 由上式有 $\frac{f_1}{f} = \frac{0.85}{0.8}$ 故 $f_1 = 3.19\ GHz$

1.12. (1) $t(P1) = \frac{0.9 \times 5 \times 10^9}{4 \times 10^9} = 1.125\ s$

$t(P2) = \frac{0.75 \times 1 \times 10^9}{3 \times 10^9} = 0.25\ s$

故 $t(P1) > t(P2) \Rightarrow$ 性能$(P1) <$ 性能$(P2)$

又 $CR(P1) > CR(P2)$ 故说法错误

(2) $t_{P1} = \frac{0.9 \times 1 \times 10^9}{4 \times 10^9} = 0.225\ s$

故 $IN(P2) = \frac{0.225 \times 3 \times 10^9}{0.75} = 9 \times 10^8$

(3) $MIPS = \frac{CR}{CPI \times 10^6}$

故 $MIPS(P1) = \frac{4 \times 10^9}{0.9 \times 10^6} = 4.44 \times 10^3$

$MIPS(P2) = \frac{3 \times 10^9}{0.75 \times 10^6} = 4 \times 10^3$

故 $MIPS(P1) > MIPS(P2)$，而P2的性能更好

故说法错误

(4) $MFLOPS(P1) = \frac{4 \times 5 \times 10^9 \times 0.4}{0.9 \times 10^6} = 1.78 \times 10^3$

$MFLOPS(P2) = \frac{3 \times 1 \times 10^9 \times 0.4}{0.75 \times 10^6} = 1.6 \times 10^3$

15.

核心数	执行时间	总时间	加速比	实际加速比/理想加速比
1	100			
2	50	54	$\frac{100}{54}=1.85$	$\frac{1.85}{2}=0.93$
4	25	29	$\frac{100}{29}=3.45$	$\frac{3.45}{4}=0.86$
8	12.5	16.5	$\frac{100}{16.5}=6.06$	$\frac{6.06}{8}=0.76$
16	6.25	10.25	$\frac{100}{10.25}=9.76$	$\frac{9.76}{16}=0.61$
32	3.125	7.125	$\frac{100}{7.125}=14.04$	$\frac{14.04}{32}=0.44$
64	1.5625	5.5625	$\frac{100}{5.5625}=17.98$	$\frac{17.98}{64}=0.28$
128	0.78125	4.78125	$\frac{100}{4.78125}=20.92$	$\frac{20.92}{128}=0.16$