4.17 41)

Instruction 1: Invalid target address (EX)

Instruction 2: Invalid data address (MEM)

- (1) 日流水岛的EX和MEM阶级添加异常检测器。当异常生时,我们得将流水战中导致异常的指金之后更改为100ps 之后,我们将相位导致理程序的地址发送到 pc ,可用一个多路变用器单元实现
- (3) II处于ID阶档、故与刘被正常提取。然后II进入EX 阶段,II进入ID阶段。由于JR被军名,故口被转换为nop。 然后执行并常处理程序
- (4) 新们可以没计一个针指了 异常被用的发明, ID/以注册 指定 将称取异常处理纸序的地址 金峰环/10信号=0, 对产生nops 到达 ID/欧哥存器多路多用器的信号是1
- (s)均与(4)拘同,降了我们使用cause register 辛汁年内存他儿

4.18 (1) Li \$rs, 0

LOOP: beg \$rs, \$rb, DONE

SLL \$110, \$15.2

add \$ r 11 , \$ r 1 , \$ r 10

lw \$ r12, 0 (\$ r(1)

lw \$110, 4(\$111)

sub \$ r12, \$ r12, \$ r10

sll \$ 10, \$15, 2

add \$ 111, \$ 12, \$ 110

sw \$r12,0(\$r11)

addi \$ 15, \$ 15 - 2

i 400P

DONE :

12)

I	Instructions			Pipeline																					
ADD BEQ ADD LW LW SUB ADD SW ADDI BEW BEQ ADD LW	R5,R0,R0 R5,R0,End R10,R5,R1 R11,0(R10) R10,1(R10) R10,1(R10) R10,R11,R10 R11,R5,R2 R10,0(R11) R5,R5,2 R0,R0,Again R5,R6,End R10,R5,R1 R11,0(R10)		ID IF		ID ID IF	ME EX **	ME EX ID ID IF	EX	ME **	EX ID ID IF	EX **	ID ID IF	WB ME EX **	WB ME EX ID	WB ME EX	ME EX	ME	WB ME	WB						
LW SUB ADD SW ADDI BEW BEQ	R10,1(R10) R10,R11,R10 R11,R5,R2 R10,0(R11) R5,R5,2 R0,R0,Again R5,R6,End													IF	**		**	ID ID IF	**	EX **	EX ID ID IF	ME EX EX ID	ME ME EX	WB ME	WB

(ን)

ADD R5.R0.R0
Again: ADD R10.R5.R1
BEQ R5.R6.End
LW R11.0(R10)
ADD R12.R5.R2
LW R10.1(R10)
ADDI R5.R5.2
SUB R10.R11.R10
SW R10.0(R12)
BEQ R0.R0.Again

End:

Note that we are now computing a+i before we check whether we should continue the loop. This is OK because we are allowed to "trash" R10. If we exit the loop one extra instruction is executed, but if we stay in the loop we allow both of the memory instructions to execute in parallel with other instructions

14)

I	nstructions												Pip	elir	ie								
ADD	R5,R0,R0	IF	ID	EX	ME	WB																	
ADD	R10,R5,R1	IF	ID	**	EX	ME	WB																
BEQ	R5,R6,End		IF	**	ID	ΕX	ME	WB															
LW	R11,0(R10)		ΙF	**	ID	ΕX	ME	WB															
ADD	R12, R5, R2				IF	ID	EX	ME	WB														
LW	R10,1(R10)				IF	ID	EX	ME	WB														
ADDI	R5, R5, 2					IF	ID	EX	ME	WB													
SUB	R10,R11,R10					IF	ID	**	ΕX	ME	WB												
SW	R10,0(R12)						IF	**	ID	EX	ME	WB											
BEQ	RO, RO, Again						ΙF	**	ID	EX	ME	WB											
ADD	R10, R5, R1								IF	**	ID	EX	ME	WB									
BEQ	R5, R6, End								IF	**	ID	* *	EX	ME	WB								
LW	R11,0(R10)										IF	**	ID	EX	ME	WB							
ADD	R12, R5, R2										IF	**	ID	EX	ME	WB							
LW	R10,1(R10)												IF	ID	EX	ME	WB						
ADDI	R5, R5, 2												ΙF	ID	ΕX	ME	WB						
SUB	R10,R11,R10													IF	ID	**	EX	ME	WB				
	R10,0(R12)													IF	ID	**	EX	ME	WB				
	RO, RO, Again														ΙF	**	ID	EX	ME	WB			
ADD	R10, R5, R1														IF	**	ID	* *	EX	ME	WB		
BEQ	R5, R6, End																IF	**	ID	EX	ME	WB	

(5)

CPI for 1- issue	(PI for 2- issue	Speedup
1.11 (10 cycles per 9 instructions).	1.06 (19 cycles per 18 instructions). Neither	1.05
There is 1 stall cycle in each	of the two LW instructions can execute in	
iteration due to a data hazard	parallel with another instruction, and SUB	
between the second LW and the	stalls because it depends on the second LW.	
next instruction (SUB).	The SW instruction executes in parallel with	
	ADD I in even-numbered iterations.	

(6)

CPI for 1- issue

CPI for 2- issue

Speedup

1.11

0.83 (15 cycles per 18 instructions). In all iterations, SUB is stalled because it depends on the second LW. The only instructions that execute in odd-numbered iterations as a pair are ADD I and BEQ. In even-numbered iterations, only the two LW instruction cannot execute as a pair.

(2)
$$[40 + 2 \times 70 + 60 + 140 = 480 \text{ pJ}]$$

$$(3) 140 + 70 + 60 + 140 = 410pT$$

$$\frac{410}{480} = 0.854$$

(4) before: 250 ps after: 无效变 [由于150 ps + 90ps < 250 ps)

(S) 这个改变不会引起任何问题。根据流水成设计的 接原则, 时钟周期 时间,今你等于最慢 的处迟时间。因此,这种变化不会争致对钟周期的变化(仍为 250 ps)

(b) I- Mem active energy: 140 pJ I- Mem Latency: 200 ps

Clock cycle time: 250 ps

Total I-Mem energy: 140 pJ + 50ps. 0.1.140 pJ / 200ps = 143.5 pJ

Idle energy % : 3.5 p] / [43.5 p] = 2.44%