TRUE-RMS-TO-DC CONVERTER
Mini-Project Report

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ACKNOWLEDGEMENT OF INTEGRITY

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Contribution Table

Student Name	Responsible for …
Jiayi Gu	Designing and testing rectification circuit, integration of all sub-circuits and debugging.
Hanlin Xu	Designing and building the multiplier/divider network
Gengxuan Shang	Designing and building of low pass filter circuit
Yuehua Guo	Designing and building the multiplier/divider network

1. Introduction

The project entails the design and creation of a functioning true RMS-to-DC converter. The role of such a device is to measure the effective voltage/current of an AC signal input (RMS) and produce an output DC signal matching this value. This type of device has applications to any field which requires the accurate measurement of AC signals, including power monitoring, instrumentation, audio equipment and industrial control systems. It is an indispensable part of modern day electrical and electronic systems for its precise and reliable measurements and real-time system monitoring. Compared to digital RMS calculations, analogue computation provides faster computation, delivering results with low latency, which may be critical in real-time systems. and lower cost as no microprocessors are needed and the power consumption is generally lower than what is used for software computation.

This report will include the design processes and stages in this project. To begin the design process, a survey of existing RMS-to-DC converter topologies will be conducted and an architecture will be selected to best serve the project requirements. A requirements analysis will follow to determine the final topology design (including the design of all circuit sub-blocks). To verify the viability of the design, LTspice will be used to simulate results, and the design will be iterated upon and refined as required. The final design will subsequently be prototyped and tested to ensure the desired functionality is achieved.

2. Literature Survey

2.1. Definition of Root Mean Square

The root mean square (RMS)[1] of a signal is defined practically as the level of DC required to produce an equivalent amount of power as an AC signal. To achieve this mathematically with a voltage, the signal must first be squared, the average taken and finally a square root must be applied to the result. The mathematical operation is notated as follows:

$$VRMS = \sqrt{\int_0^T Vin(t)^2 dt/T} \tag{2.1}$$

As seen above, a squaring operation is needed, followed by a time-based averaging circuit and finding the square root of the output. [2]

2.2. Squaring Voltage

To square a voltage, the input voltage can be multiplied by itself. This can be done via analogue multipliers, which accept 2 different signals, and outputs the result of multiplying the signals. Typically analogue multiplier circuitries include:

1. Gilbert Cell, which makes use of differential pairs of BJTs. This method is temperature sensitive, and is complex to implement. [3]
2. Log Antilog Amplifiers which use the logarithmic properties of diodes and transistors. Diodes and transistors are temperature dependent, and component values cause large differences in output. [4]
3. Variable Transconductance Multipliers that use a regular operational amplifier with the amplification controlled by a varistor typically implemented as with FETs. This method requires maintaining the FET inside the linear operating range, which limits the total operating range of the circuit. [5]

Based on different implementations, the multiplier may or may not be able to compute the multiplication for both positive and negative voltages. Consequently, rectification of the input voltage may be necessary to ensure circuit stability.

2.3. Rectification

Full wave rectification is possible with 4 diodes.[6] However, this requires the input amplitude to be more than 0.7V and the output voltage to have 0.7V subtracted, making it only suitable for large input amplitudes in the hundreds of volts. For input signals with lower amplitudes, precision rectifiers implemented with diodes and operational amplifiers is possible, which can output rectified voltage for signals with very small amplitude.

2.4. Finding Square Root

2.4.1. Explicit Computation

The explicit method is the most intuitive, as it involves straightforwardly replicating the computation process for the square root.[7] This involves creating individual circuitry that computes the square root of an input voltage, takes the average and takes the square root of the average. This method can achieve high bandwidth and accuracy [1], but has the drawback of having to deal with signals that vary wildly in amplitude, as squaring any input signal will enormously increase its amplitude. As a consequence, this topology is only viable across a very limited input range.

2.4.2. Implicit Computation

This method uses feedback to perform the square root function implicitly[8], typically via a multiplier and divider network by which it bypasses the need to deal with the full range of the squared input signal amplitude and to implement an explicit square root circuit. This topology generally requires fewer components to build than the explicit computation topology, and thus a lower cost. However, its bandwidth is relatively small compared to that of the explicit method.

2.5. Time Based Averaging

Time based averaging of voltage is analogous to integrating the voltage over a long period of time. This can be done utilizing capacitor properties.

2.5.1. Active Low Pass Filter

Active low pass filters, or integrators, can achieve this desired integration while also amplifying the signal. They provide a cleaner frequency response than passive filters[9]. They are more costly due to the need for operational amplifiers, but are very flexible in design such that more functionalities and transfer functions can be implemented.

2.5.2. Passive Low Pass Filter

Passive low pass filters typically require only resistors and capacitors, making it very simple to implement. It provides a reliable way for integration with no external power supplied.

3. Design Specifications

The primary objective is to design a circuit that accurately converts an AC signal to its RMS (Root Mean Square) value while meeting the following specifications:

Table 1: Design Requirements [x]

Criteria	Expectations
Power Supply Characteristics	● Range: ±5V ● Circuit Current < 200mA
Input Signal Characteristics	● Waveform type (sine, square, triangle, etc) ● Peak-to-peak voltage: 100mV to 200mV ● Frequency range: DC to 10kHz ● Voltage crest factors: 1 to 3 ● Input Impedance: ≥ 1MΩ ● Input Capacitance: ≤ 50pF ● Device to maintain peak operability at 25℃
Output Characteristics	● Margin of error: 5% - 10% ● 1MΩ < Output impedance ≤ 10MΩ ● Settling time ≤ 10s ● Converter must be accurately measure the RMS value of different waveform types and produce the corresponding DC output ● Commercial (Fluke / Keysight / Tektronix) True RMS Multimeter and AD2 to be used for the output DC measurement and validating design operation

3.1. Requirements Analysis

The input signal has a relative low amplitude, and needs to accommodate a wide range of frequencies. When designing, the converter stages need to be tested under a variety of conditions to ensure peak operability in all cases. Since 4 quadrant multipliers typically have low frequency ranges and Gilbert Cell may be difficult to implement, single quadrant multipliers will likely be used. As seen from [3], IC that utilizes this will require rectification. The low amplitude necessitates a precision full wave rectification instead of regular rectification via only diodes.

In this project, an implicit computational topology for the square root has been utilized. This is done to reduce the number of components, and thus reduce development time. The aim being to develop a functional prototype and verify if limitations are present and if it can reach the desired accuracy in output. If the prototype does not operate in all of the desired frequency range, the explicit method can then be used, as all parts of the implicit method can be reused in the explicit method.

3.2. Design Goals

The primary objective is to design a circuit that accurately converts an AC signal to its RMS, using only elementary circuit components and general ICs such as operational amplifiers. The design should measure RMS on frequency ranges from DC signals to 10kHz AC signals accurately working with a range of waveforms, including but not limited to sine waves, triangle waves, square waves and PWM waves. The design should cater towards small signal operations as the input signal amplitude is between 100 to 200 millivolts peak to peak. Additionally, offsets between -1 to 1 Volt need to be handled, where RMS value is computed including the voltage offset to the small signal input. The project aims to deliver output RMS voltages within 3% of the mathematically correct RMS of the input signal, within a planning and development time of 5 weeks. The expected sub circuits include a module that performs the absolute value of the input voltage, a multiplier divider module and a time based averaging module.

4. Design Description

4.1. Theoretical Design

4.1.1. Rectifier

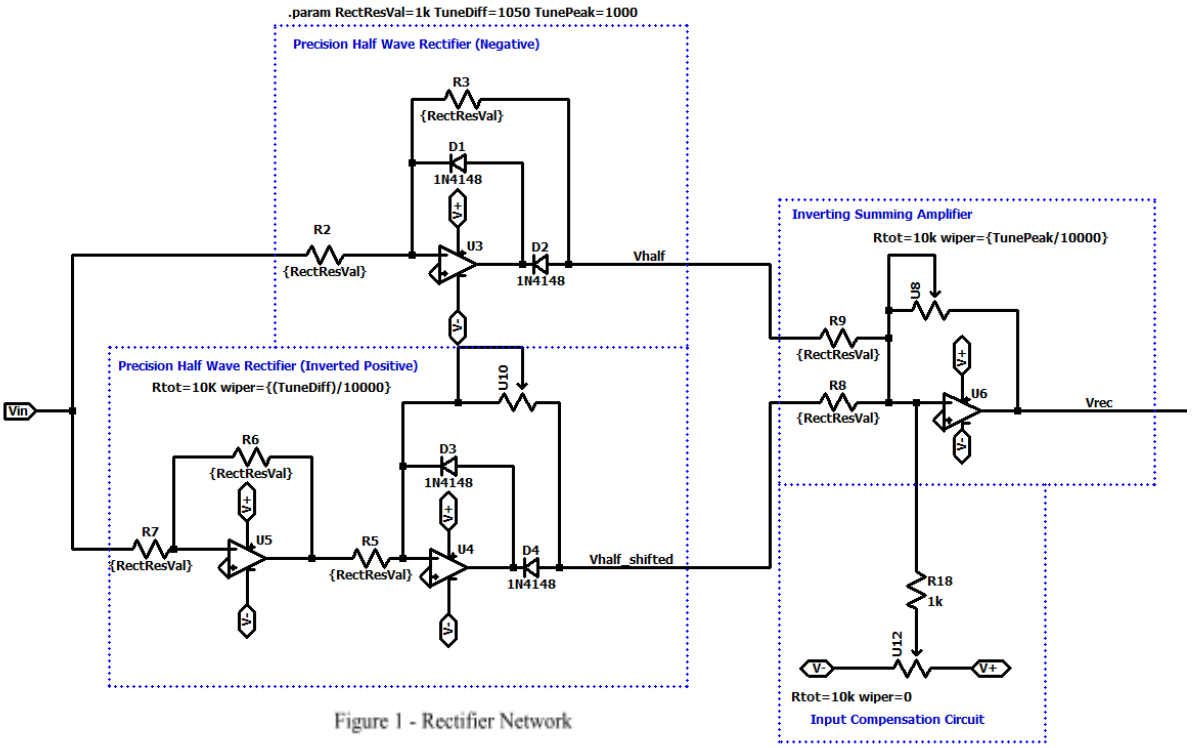


Figure 1 - Rectifier Network

Since the input signal amplitude is low, a regular full wave rectifier is not used. Instead, the approach uses a precision full wave rectification circuit, consisting of an inverting amplifier, two half wave rectifiers and a summing amplifier.

For each of the half wave rectifier, the mathematical analysis is as follows:

For Vin > 0: Diode D3 is open, and D4 conducts. The configuration becomes identical to an inverting amplifier, such that $V_{rec} = V_{in} *- (R9/R8) =- V_{in}$, as R8 = R9.

For Vin < 0: D3 conducts, and D4 is open. Vin is shorted to the output terminal of the operational amplifier. Vrec = 0 in this case.

An inverting amplifier is added in front of one of the half wave rectifiers to shift the input phase by 180 degrees, and the inverting summing sums each half of the half wave rectifiers to get a full wave rectified output. Effectively, this captures the negates and captures the positive half of the wave, captures the negative half of the wave, and negates the sum of these 2 half-rectified waves, giving a fully rectified wave, such that $V_{rec} =- ((- V_{in} for V_{in} > 0) + (V_{in} for V_{in} < 0))$

It is worth noting that precision full wave rectification with 2 less op amps is possible, by summing Vin with two times the negative half wave rectified output, i.e. $V_{rec} = V_{in} - 2 * (V_{in} for V_{in} < 0)$

However, that design is forgone due to the presence of negative peaks that it produces as the input transitions from negative to positive, especially at higher frequencies, observed in the physical circuit implementation. It is suspected that slew rate limitation caused this phenomena.

4.1.2. Multiplier/Divider

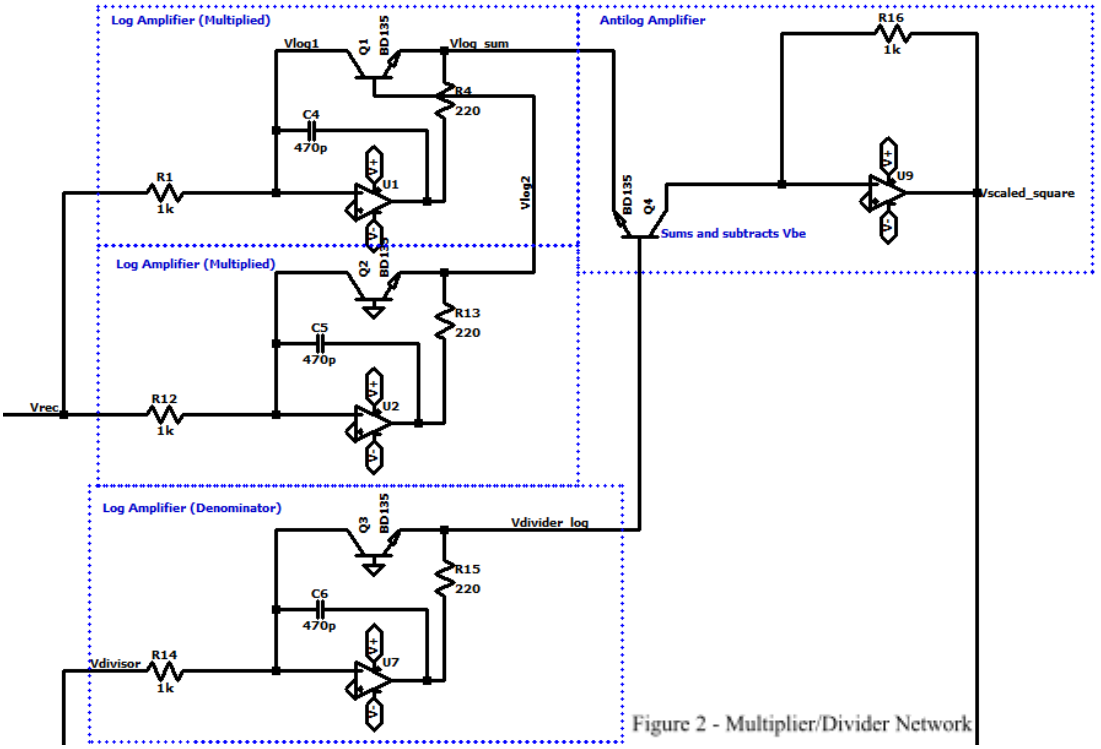


Figure 2 - Multiplier/Divider Network

The log and antilog amp equation with transistor is given as:

$$V_{out} = -V_T ln[\frac{I_c}{I_s}] = -V_{be}, \quad V_T = (kT/q), \quad I_c = \frac{V_{in}}{R_1}$$

$$where\ I_s\ is\ the\ saturation\ current, k = Boltzmann's\ constant, T = temperature\ (in\ K) \tag{4.1}$$

The multiplier/divider circuit operates with the logarithmic relationship between transistors' base-emitter voltage and the collector current.

$$V_{be\,Q1} + V_{be\,Q2} = V_{be\,Q3} + V_{be\,Q4} \quad as\ each\ pair\ of\ transistors\ base\ emitter\ terminals\ are\ connected \tag{4.2}$$

$$As\ V_{be} = V_T ln(\frac{I_c}{I_s}),\ we\ have\ V_T ln(I_{c1}) + V_T ln(I_{c2}) = V_T ln(I_{c3}) + V_T ln(I_{c4}) \tag{4.3}$$

$$such\ that\ I_{c1} * I_{c2} = I_{c3} * I_{c4}$$

$$By\ I_{c1} = I_{c2} = \frac{V_{rec}}{1k},\ I_{c3} = \frac{V_{divisor}}{1k},\ I_{c4} = \frac{V_{scaled\ square}}{1k},\ V_{rec} * V_{rec} = V_{divisor} * V_{scale\ square} \tag{4.4}$$

$$Rearranging\ gives\ the\ multiplier/divider\ transfer\ function: \frac{V_{rec}^{\ 2}}{V_{divisor}} = V_{scale\ square}$$

4.1.3. Low Pass Filter

The design of the low pass filter aims to incorporate the largest capacitance possible in order to maximise the averaging time constant to yield more accurate results. However, it is worth noting that the settling time is also a limiting factor.

The time constant is calculated as follows:

(4.5)

$$\tau\ (seconds)\ = \frac{0.025\ seconds}{\mu F} \times\ C\ (F)$$

With increasing the averaging time, the full settling time will also increase. In the theoretical design, a combination of 1.5kΩ and 100nF is used. However, this is expected to change with experiments inside the physical circuit.

4.1.4. Implicit Square Root Calculation via Feedback

By feeding the average value of the squared voltage as the divisor for the multiplier/divider circuit, we are able to obtain the RMS voltage implicitly.

$$Here,\ the\ output\ of\ low\ pass\ filter\ gives\ Avg(V_{scaled\ square}) = Avg(\frac{V_{rec}^{\ 2}}{Avg(V_{scaled\ square})}). \quad (4.6)$$

$$Rearranging\ the\ equation\ gives\colon \sqrt{Avg(V_{rec}^{\ 2})} = Avg(V_{scaled\ square}) = V_{RMS} \quad (4.7)$$

4.2. Practical Considerations

4.2.1. Rectifier

10k Potentiometers are used for scaling in the summing amplifier and in one of the half wave rectifiers, such that each rectified half wave can be individually scaled to compensate for component value differences. Additionally, an input compensation network is added to compensate for possible offsets of the operational amplifier and improve accuracy.

4.2.2. Multiplier/Divider

The division operation removes the I_s constant from the transfer function, such that the effects of the temperature on the circuit output is compensated for. Additional scaling factors will be considered at the end of the entire circuit, minimizing the number of potentiometers that need to be individually tuned.

4.2.3. Low Pass Filter

Since an active low pass filter is employed in the circuit, additional amplification may be present. Similar to the effects of the multiplier, scalings will be applied together at the end to mitigate the effects. Capacitance value will also be adjusted such that a longer averaging time can be achieved for better accuracy while remaining below 10 seconds.

Table 2: Circuit Component Mapping.

Design Component	**Physical Component**
1.5kΩ resistor	470Ω resistor in series with 1kΩ resistor
NPN BJT	BD135
Diode	1N4148
Operational Amplifier	TL084

4.3. Practical Design and Simulation

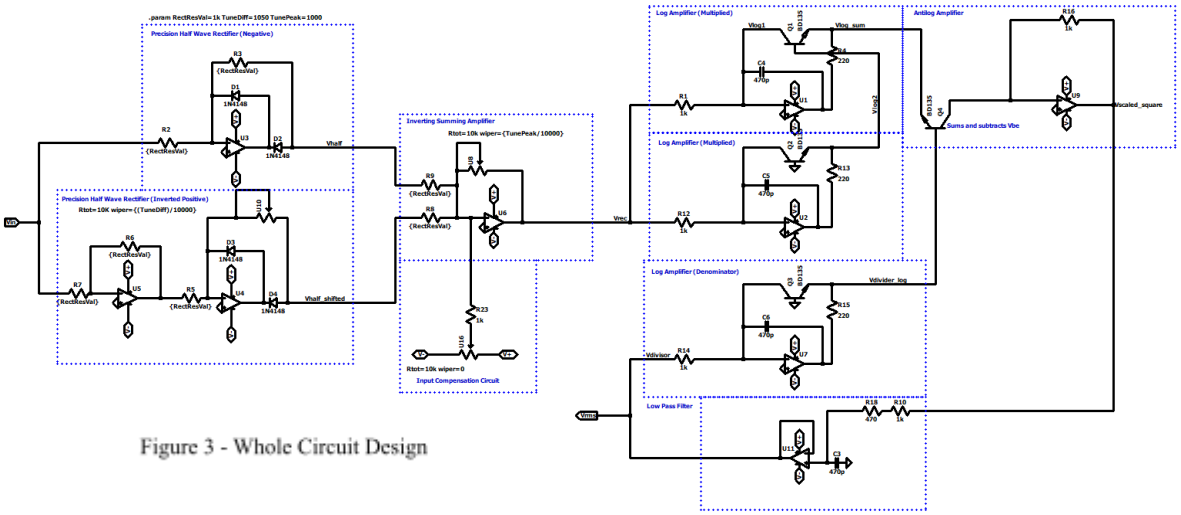


Figure 3 - Whole Circuit Design

4.3.1. Rectifier

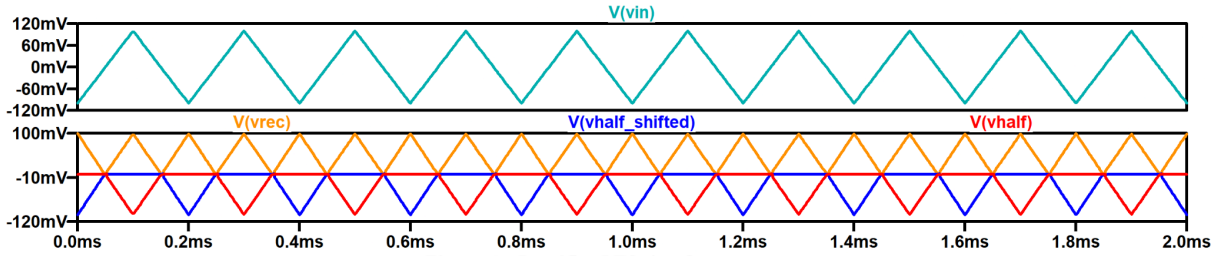


Figure 4 - Rectifier LTSpice Output

The rectifier is capable of outputting clean rectified waves. It is noted that the peaks of the rectified negative half and the positive half are not matching in amplitude. In building practical circuits, this can be remediated by adding potentiometers in order to compensate for these differences.

4.3.2. Multiplier/Divider

A DC Sweep is performed on this sub-circuit, with the divider set as 1 Volt. The output gives a clean quadratic shape when the input voltage is positive, vindicating the operability of the circuit in the designated operating range. However, the circuit transfer function breaks down below 0 volt, and above 1.18V. This indicates that the circuit cannot operate with negative voltage demonstrating the expected need for a rectification stage before the multiplier/divider. Additionally, since the input voltage can reach at most 1.2V due to the offset, this design can give less accurate results if waves such as PWM with a peak to peak voltage of 200mV and 1 Volt offset is given as input. In the physical implementation, the output voltage from the rectifier can be attenuated to ensure that the input to the squarer stays within its operating range.

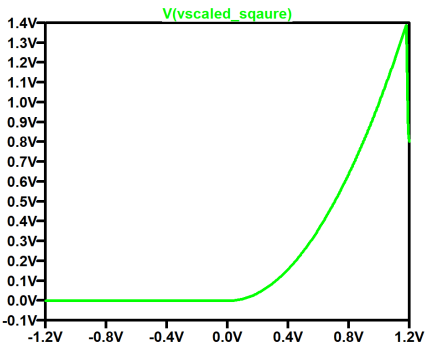


Figure 5 - Multiplier Squaring Config DC Sweep

4.3.3. Low Pass Filter

The graph indicates that the settling time for this integrator circuit lies between 3 to 4s. This is within the design specification of 10s. While there may be amplification as this is an active low pass filter, it is expected that in physical implementation, additional output buffering and scaling will be required. This scaling will be adjusted to compensate for errors caused by

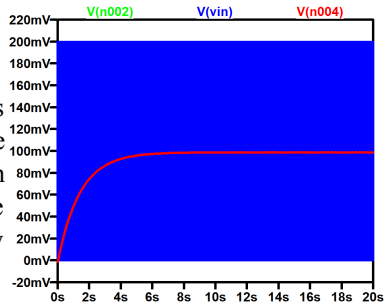


Figure 6 - Low Pass Filter Settling in Triangle Wave Input

all component value differences throughout the circuit. This will be done manually via a potentiometer, and is hence not simulated here.

5. Physical Implementation

Due to mismanagement of resources, the team was not able to obtain Waveform captures. Instead, output will be described.

5.1. Rectifier

Two 10kΩ potentiometers are used for tuning the output gain and the differences between the rectified negative and positive cycles. Voltage losses and small offsets in this section of the circuit can be compensated via turning these potentiometers.

Additionally, during physical testing, we noticed that the output voltage can be offsetted from 0 by approximately 2 mV. We suspected that this is due to some offset voltage inherent in the TL974 we are using. To compensate for this, an input compensation network is used, which involves a 1k potentiometer connected in conjunction with a 100k resistor between +5 and -5 volts. We use this potentiometer to add voltage into the negative terminal of the summing amplifier, compensating for the offset voltage. Via adding this network, rectified waveform for signals with smaller amplitudes intersecting zero can be adjusted to start from 0 volts.

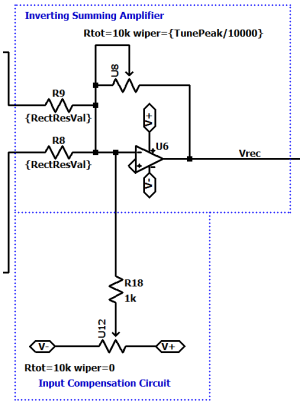


Figure 7 - Summing Amplifier in Rectifier with Offset Compensation

5.2. Multiplier/Divider

Small decoupling capacitors are added to the circuit, and high pass capacitors are added to the connections between the rectifier and the multiplier/divider network, with the intention of grounding high frequency noises.

5.3. Low Pass Filter

We noticed that at low frequencies, the output RMS voltage is no longer a DC value, possibly due to the high cutoff frequency when using a small capacitor. While the initial design incorporated a smaller 100n capacitance to account for the limit on settling time, it was found through practical testing that a 470u capacitor could still achieve a sufficiently short settling time. The 100n Capacitor has thus been replaced with the 470u capacitor. This decreases the cutoff frequency for this low pass filter. In other words, the integration is done over a longer period of time, allowing for more accurate time based averaging, and a more precise output of the RMS voltage.

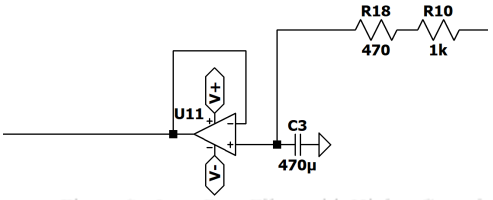


Figure 8 - Low Pass Filter with Higher Capacitance

5.4. Output Scaling and Buffering

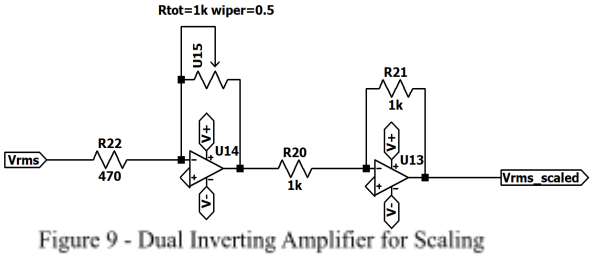
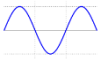
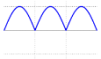
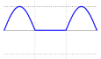
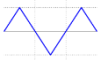
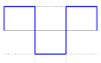
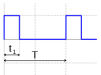


Figure 9 - Dual Inverting Amplifier for Scaling

In the physical implementation of the circuit, the output RMS is higher than the expected simulation value from LTSpice. Consequently, a final scaling stage is added at the end to be able to manually adjust the gain and compensate for any differences between the simulation and reality from different component values and wire resistances. To enable both amplification and attenuation, 2 inverting amplifiers are used, where the first one scales the signal, and second one inverts the signal back to positive. A 1k Potentiometer is used in conjunction with a 470Ω resistor. This enables scaling factors for 0 to 2.13.

6. Results and Discussion

Table 3: RMS Measurement Results

Wave Type	Function	Plot	Crest Factor (CF)	Ideal RMS Value (V_{rms})	Measured RMS Value ($V_{rms-meas}$)	Measured Error (%)
DC	1		1	1	990mv	-1
Sine Wave	$sin\,(t)$		$\sqrt{2}$	$\frac{1}{\sqrt{2}}$	70.2mV	-0.7
Full Wave Rectified Sine Wave	$\lvert sin(t)\rvert$		$\sqrt{2}$	$\frac{1}{\sqrt{2}}$	70.4mV	-0.4
Half Wave Rectified Sine Wave	$\sum_{n=-\infty}^{\infty} HS(t + 2\pi n)$ *where* $HS(t) = \{ sin(t)\ if\ 0 \leq t \leq \pi$ $\{0\ otherwise$		2	$\frac{1}{2}$	49.4mV	-1.2
Triangle Wave	$\sum_{n=-\infty}^{\infty} \Lambda(t + n)$		$\sqrt{3}$	$\frac{1}{\sqrt{3}}$	56.9mV	-1.4
Square Wave	$\sum_{n=-\infty}^{\infty} \Pi(t + n)$		1	1	98.7	-2.2
PWM Signal	$\sum_{n=-\infty}^{\infty} PWM(t + nT)$ *where* $PWM(t) = \{1\ if\ 0 \leq t \leq t_r$ $\{0\ otherwise$		$\sqrt{\frac{T}{t_1}}$	$\sqrt{\frac{t_1}{T}}$	81.7mV at 70% duty cycle	-2.4
Sine Wave with Offset	$sin\,(t) + k$		$\sqrt{2}$ +k	$\sqrt{1/4 + k^2}$	k = 1 1.021	1.8

6.1. Result Analysis

On average, the error from the true value is approximately -0.7857%. It is noticed that the amplitude generally decreases with lower frequencies at <100Hz, but the increase is very minimal and not impactful to the said result. This is well within the project's initial goals of designing a circuit that archives 3 to 5 % error rate. However, this accuracy stems from being able to fine tune the circuit. It is worth noting that any changes to component placing, or simply unplugging and plugging the measurement probes can have a noticeable effect on the output amplitude, mandating a new fine tune.

6.2. Challenges

6.2.1. Rectifier Design

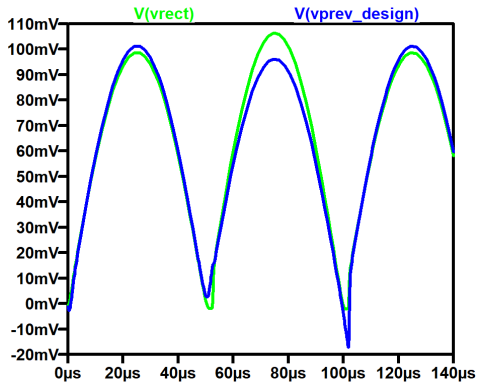


Figure 10 - Rectifier Design Output Comparison

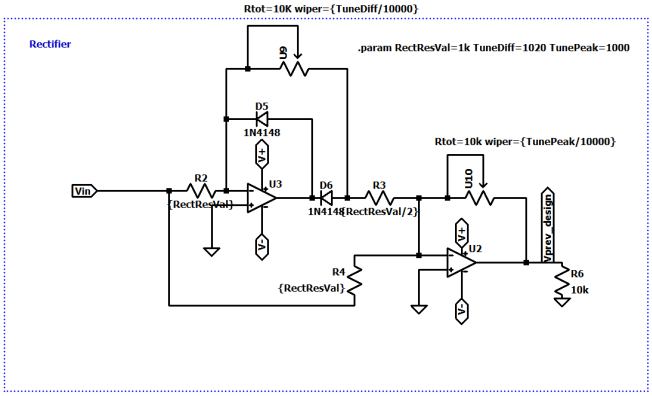


Figure 11 - Failed Rectifier Design

Multiple designs of the rectifier are trialed in this project. After determining functionality in LTSpice, they are individually built and tested. Specifically, we tried a simpler design using only 2 operational amplifiers. This design archives the correct waveform. However, in experimentation, it was noticed that it produces large negative peaks which may affect the functionality of future blocks in the design. In the physical circuit, this negative peak is more significant than the simulation, such that up to -30mV peaks are seen on inputs with 100mV peak to peak amplitude.

6.2.2. Square Root Circuit - Explicit to Implicit

We faced significant challenges when transitioning from explicit to implicit methods for building a square root circuit. Initially, we used log and antilog amplifiers but encountered instability due to the saturation current (Is). To address these issues, we decided to implement a feedback loop based on the idea in [8].

6.2.3. Squaring Circuit

Our initial design employed a log and antilog amplifier for the multiplier as described in [4]. However, this design is highly temperature-dependent due to the saturation current (Is), which, while not significantly affecting results in LTspice simulations, then proved extremely unstable in practical circuits. To minimise this issue, we implemented a square/divide circuit as outlined in section 4.3.2.

6.2.4. Noise - Gain in Low Pass

At input signal amplitude of 100mV peak to peak at 0V offset, the squared voltage can be very low. If the peak is 50mV after rectification, the squared voltage would be only 2.5mV at its peak. Here, the noise had tangible impacts to the output RMS value. To mitigate the effect, high pass filters in the form of small capacitors to ground are added between the stages of the circuit, such that noise at higher frequencies can be sunken into ground. Decoupling capacitors are added between the rails, and at the connections between the power supply and the operational amplifiers, such that power supply noise is lowered, and clean rails are provided to the amplifiers. In the process, the team attempted amplifying the rectification result. However, it was noticed that the squaring circuit implemented does not operate correctly beyond input voltages of over 1.4V. Hence, to ensure peak operability even with 1V offset, no extra signal amplification is used.

7. Conclusion

This project examined the implementation of a true RMS to DC converter using analog electronic devices. A literature survey was conducted which examined the different methods of RMS calculation and the various circuit topologies used to implement the conversion. The decision was made to implement the circuit using the implicit calculation topology to reduce the number of components used. Ultimately all design objectives were achieved, and the final build performed as intended. A potential future expansion on the project could be to implement the explicit computation method as well and compare its behavior with the implicit model.

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APPENDIX

Include supplementary information here for assessment.

Bill of Materials

Material	**Amount Used (Part Number: Quantity)**
Breadboard	400 Holes: 3
Polarised Capacitor	470uF: 1, 10uF: 4
Unpolarised Capacitor	100nF: 7, 470pF: 3, 22pF: 1
Resistor	1kΩ: 14, 470Ω: 1, 220Ω: 3
BJT	BD135: 4
Operational Amplifiers	TL084: 3
Potentiometers	10k: 2, 1k: 2
Diodes	1N4148: 4

End of Report

Delete the following before submitting your design:

Report Guidelines

- Submit your report on Moodle in **PDF** file format only. Your report should be no longer than **8-10 pages**. Include page numbers except front page.
- Include a properly formatted Table of Contents before the Introduction and after the title page.
- No changes to be made to the title page, expect where you need to fill in information within the provided fields. Use 12/13 pt Times New Roman font on Title page.
- Level 1 and Level 2 headings provided in the template above must remain without change. Edit the text under them as required.
- You may add additional Level 2 headings where appropriate. You are encouraged to provide your own Level 3 and Level 4 headings where appropriate to describe your implementation. Heading names must be succinct and appropriate to the task.
- Structure the report using appropriate headings, include clear explanations, accurate calculations, relevant measurements, and supporting visuals in the form Waveform, LTspice and design drawings. Similar format as the workshop manual shall be implemented.
- Figure captions below each figure – include figure number and appropriate text explaining the figure. Figures should be numbered based on section numbers.
- Equations should have an equation number and be referenced in text. Ensure it is presented professionally with proper formatting, grammar, and referencing. Equations should be numbered based on section numbers. Use the equation editor to present your equation. Not pasted as image.
- Each table should have a caption placed above it. Tables should be numbered according to section numbers.
- Font size recommendations;
    - Report font = Times New Roman
    - Regular text = 10 pt (Justified formatting)
    - Section
        - Level 1 Headings = 16 pt (bold)
        - Level 2 Headings = 14 pt (bold)
        - Level 3 Headings = 12 pt (bold)
        - Level 4 Headings = 10 pt (bold)
    - Figure Captions, Equations and References = 10 pt
- LTspice schematics must be displayed and reported with White backgrounds, black wires and traces and black components shapes and text, set appropriate wire thickness and font sizes in the Control Panel/Settings. Turn OFF grid on the Schematic
- LTspice waveforms must be displayed with White background, Black/Red/Dark Green/Dark Blue/Orange trace colours only. Set trace thickness, axis font sizes and grid settings appropriately.
- When undertaking captures from WAVEFORMS set your background to be “WHITE” i.e. Light Mode and Plot Widths to be **4**. Disable Channel Acquisition Noise and Edge Histogram. Increase font sizes to appropriate values for your reports.
- Marks will be deducted where reports do not conform to the above recommendations.