Chapter 1

Transistor Biasing

The basic function of transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as **faithful amplification**. In order to achieve this, means are provided to ensure that input circuit (i.e. base-emitter junction) of the transistor remains forward biased and output circuit (i.e. collector-base junction) always remains reverse biased during all parts of the signal. This is known as transistor biasing. In this chapter, we shall discuss how transistor biasing helps in achieving faithful amplification.

The theory of transistor reveals that it will function properly if its input circuit (i.e. base-emitter junction) remains forward biased and output circuit (i.e. collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied:

(i) Proper zero signal collector current

(ii) Minimum proper base-emitter voltage (V_{BE}) at any instant

(iii) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (i) and (ii) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (iii) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics i.e. between saturation to cut off.

(i) Proper zero signal collector current. Consider an NPN transistor circuit shown in Fig. 1.1 (i). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.

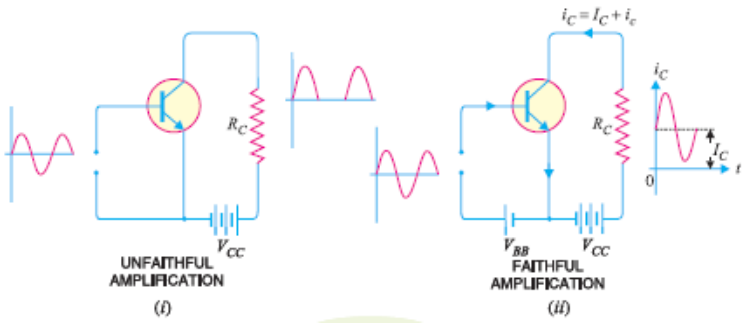


Fig. 1.1

Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. 1.1 (ii). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as zero signal collector current I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases.

However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. The value of zero signal collector current should be at least equal to the maximum collector current due to signal alone i.e.

Zero signal collector current ≥ Max. collector current due to signal alone

Illustration: Suppose a signal applied to the base of a transistor gives a peak collector current of 1mA. Then zero signal collector current must be at least equal to 1mA so that even during the peak of negative half-cycle of the signal, there is no cut off as shown in Fig. 1.2 (i). If zero signal collector current is less, say 0.5 mA as shown in Fig. 1.2 (ii), then some part (shaded portion) of the negative half-cycle of signal will be cut off in the output.

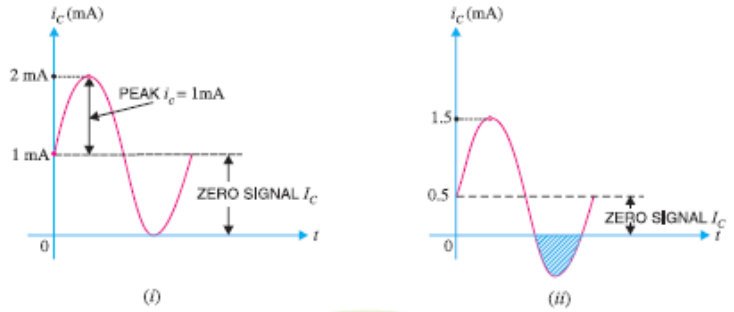


Fig. 1.2

(ii) Proper minimum base-emitter voltage. In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for Si transistors at any instant.

Fig. 1.3

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for Si transistors as shown in Fig. 1.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

(iii) Proper minimum V_{CE} at any instant. For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called knee voltage (See Fig. 1.4).

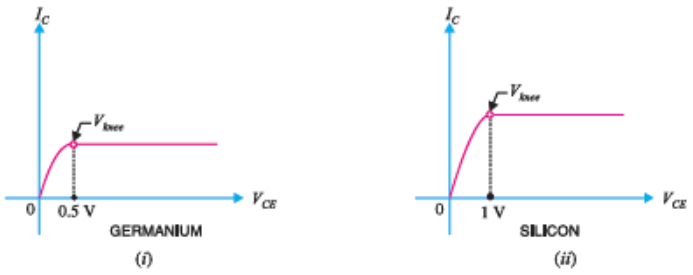


Fig. 1.4

When V_{CE} is too low (less than 0.5V for Ge transistors and 1V for Si transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely: (i) proper zero signal collector current, (ii) proper base-emitter voltage at any instant and (iii) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as transistor biasing. The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as biasing circuit. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Example 1.1

An npn silicon transistor has V_{CC} = 6 V and the collector load R_C = 2.5 kΩ.

Find:

(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.

(ii) The minimum zero signal collector current required.

Solution

Collector supply voltage, V_{CC} = 6 V

Collector load, R_C = 2.5 kΩ

(i) We know that for faithful amplification, VCE should not be less than 1V for silicon transistor.

∴ Max. Voltage allowed across R_C = 6 − 1 = 5 V

∴ Max. allowed collector current = 5 V/R_C = 5 V/2.5 kΩ = 2 mA

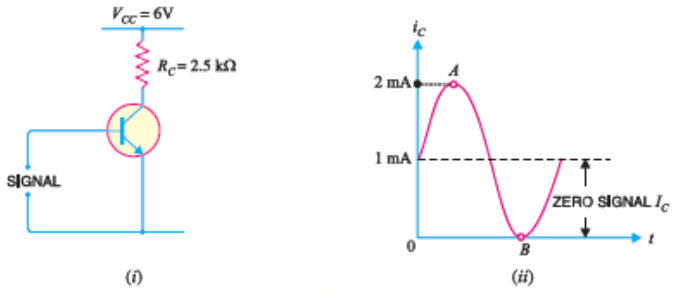


Fig. 1.5

Thus, the maximum collector current allowed during any part of the signal is 2 mA. If the collector current is allowed to rise above this value, V_{CE} will fall below 1 V. Consequently, value of β will fall, resulting in unfaithful amplification.

(ii) During the negative peak of the signal, collector current can at the most be allowed to become zero. As the negative and positive half cycles of the signal are equal, therefore, the change in collector current due to these will also be equal but in opposite direction.

∴ Minimum zero signal collector current required = 2 mA/2 = 1 mA

During the positive peak of the signal [point A in Fig. 1.5 (ii)], i_C = 1 + 1 = 2mA and during the negative peak (point B),

i_C = 1 − 1 = 0 mA

Example 1.2

A transistor employs a 4 kΩ load and V_{CC} = 13V. What is the maximum input signal if β = 100 ? Given V_{knee} = 1V and a change of 1V in V_{BE} causes a change of 5mA in collector current

Solution

Collector supply voltage, V_{CC} = 13 V

Knee voltage, V_{knee} = 1 V

Collector load, R_C = 4 kΩ

∴ Max. allowed voltage across R_C = 13 − 1 = 12 V

∴ Max. allowed collector current, $i_C = \frac{12V}{R_c} = \frac{12V}{4k\Omega}$ = 3mA

Maximum base current, $i_B = \frac{i_c}{\beta} = \frac{3mA}{100}$ = 30 μA

Now $\frac{\text{Collector current}}{\text{Base voltage (signal voltage)}}$ = 5 mA/V

∴ Base voltage (signal voltage) = $\frac{\text{Collector current}}{5\ \text{mA/V}}$ = 600mA

Inherent Variations of Transistor Parameters

In practice, the transistor parameters such as β, V_{BE} are not the same for every transistor even of the same type. To give an example, BC147 is a silicon npn transistor with β varying from 100 to 600 i.e. β for one transistor may be 100 and for the other it may be 600, although both of them are BC147. This large variation in parameters is a characteristic of transistors. The major reason for these

variations is that transistor is a new device and manufacturing techniques have not too much advanced. For instance, it has not been possible to control the base width and it may vary, although slightly, from one transistor to the other even of the same type. Such small variations result in large change in transistor parameters such as β, V_{BE} etc.

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. It is, therefore, very important that biasing network be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. In other words, the operating point should be independent of transistor parameters variations.

Stabilisation

The collector current in a transistor changes rapidly when

(i) the temperature changes,

(ii) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (i.e. zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates making the operating point independent of these variations. This is known as stabilisation. The process of making operating point independent of temperature changes or variations in transistor parameters is known as stabilisation.

Once stabilisation is done, the zero-signal I_C and V_{CE} become independent of temperature variations or replacement of transistor i.e. the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons:

(i) Temperature dependence of I_C

(ii) Individual variations

(iii) Thermal runaway

(i) Temperature dependence of I_C. The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point i.e. to hold I_C constant inspite of temperature variations.

(ii) Individual variations. The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates stabilising the operating point i.e. to hold I_C constant irrespective of individual variations in transistor parameters.

(iii) Thermal runaway. The collector current for a CE configuration is given by:

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \quad ...(i)$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (i) that if I_{CBO} increases, the collector current I_C increases by $(\beta + 1)\ I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as thermal runaway. In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised i.e. I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in $\beta\ I_B$ will compensate for the increase in $(\beta + 1)\ I_{CBO}$, keeping I_C nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification.

The biasing network associated with the transistor should meet the following requirements:

(i) It should ensure proper zero signal collector current.

(ii) It should ensure that V_{CE} does not fall below 0.5 V for Ge transistors and 1 V for silicon transistors at any instant.

(iii) It should ensure the stabilisation of operating point

Stability Factor

It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor S. It is defined as under:

The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} at constant β and I_B is called stability factor i.e.

Stability factor, $S = \frac{dI_c}{dI_{co}}$ at constant I_B and β

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus a stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of S is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

The general expression of stability factor for a C.E. configuration can be obtained as under:

$I_C = \beta\ I_B + (\beta + 1)\ I_{CO}$

** Differentiating above expression w.r.t. I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{co}}{dI_c}$$

$$\text{Or } 1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{co}}{dI_c} = \frac{1}{S}\right]$$

$$\text{Or } S = \frac{(\beta + 1)}{1 - \beta \frac{dI_B}{dI_C}}$$

Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from the battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (i.e. V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply (i.e. V_{CC}):

(i) Base resistor method

(ii) Emitter bias method

(iii) Biasing with collector-feedback resistor

(iv) Voltage-divider bias

In all these methods, the same basic principle is employed i.e. required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is selected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1 V for silicon transistors. For example, if $\beta = 100$ and the zero signal collector current I_C is to be set at 1mA, then I_B is made equal to IC /β = 1/100 = 10 μA. Thus, the biasing network should be so designed that a base current of 10 μA flows in the zero signal conditions.

Base Resistor Method

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for npn transistor (See Fig. 1.6) and between base and negative end of supply for pnp transistor. Here, the required zero signal base current is provided by VCC and it flows through R_B. It is because now base is positive w.r.t. emitter i.e. base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

Circuit analysis

It is required to find the value of R_B so that required collector current flows in the zero signal conditions.

Let I_C be the required zero signal collector current.

$\therefore I_B = \frac{I_c}{\beta}$

Considering the closed circuit ABENA and applying Kirchhoff 's voltage law, we get,

$V_{CC} = I_B R_B + V_{BE}$

or $I_B R_B = V_{CC} - V_{BE}$

$\therefore R_B = \frac{V_{CC} - V_{BE}}{I_B}$ ... (i)

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (i).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from exp. (i) that:

$R_B = \frac{V_{CC}}{I_B}$

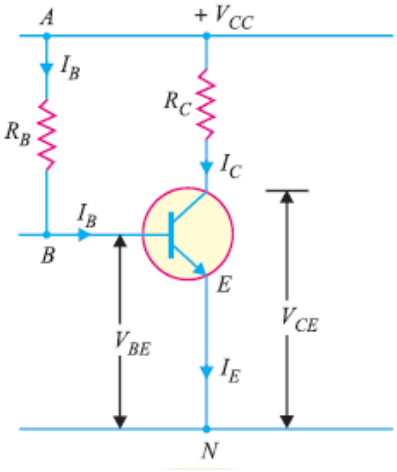


Fig. 1.6

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence,

R_B can always be found directly, and for this reason, this method is sometimes called fixed-bias method.

Stability factor

Stability factor, $S = \frac{(\beta + 1)}{1 - \beta \frac{dI_B}{dI_C}}$

In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$. Putting the value of

$dI_B/dI_C = 0$ in the above expression, we have,

Stability factor, $S = \beta + 1$

Thus the stability factor in a fixed bias is $(\beta + 1)$. This means that I_C changes $(\beta + 1)$ times as much as any change in I_{CO}. For instance, if $\beta = 100$, then $S = 101$ which means that I_C increases 101 times faster than I_{CO}. Due to the large value of S in a fixed bias, it has poor thermal stability.

Advantages

(i) This biasing circuit is very simple as only one resistance R_B is required.

(ii) Biasing conditions can easily be set and the calculations are simple.

(iii) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages

(i) This method provides poor stabilisation. It is because there is no means to stop a self increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

(ii) The stability factor is very high. Therefore, there are strong chances of thermal runaway. Due to these disadvantages, this method of biasing is rarely employed.

Example 1.3

Fig. 1.7 (i) shows biasing with base resistor method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE}. Neglect small base-emitter voltage. Given that $\beta = 50$.

(ii) If R_B in this circuit is changed to 50 kΩ, find the new operating point.

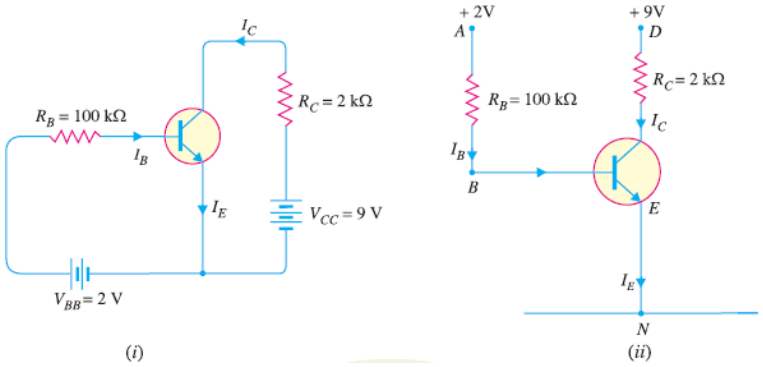


Fig. 1.7

In the circuit shown in Fig. 1.7 (*i*), biasing is provided by a battery V_{BB} (= 2V) in the base circuit which is separate from the battery V_{CC} (= 9V) used in the output circuit. The same circuit is shown in a simplified way in Fig. 1.7 (*ii*). Here, we need show only the supply voltages, + 2V and + 9V. It may be noted that negative terminals of the power supplies are grounded to get a complete path of current.

(*i*) Referring to Fig.1.7 (*ii*) and applying Kirchhoff 's voltage law to the circuit *ABEN*, we get,

$I_B R_B + V_{BE} = 2V$

As V_{BE} is negligible,

$\therefore I_B = \frac{2V}{R_B} = \frac{2V}{100k\Omega} = 20\ \mu$ A

Collector current, $I_C = \beta I_B = 50 \times 20\ \mu$ A = 1000 μA = **1 mA**

Applying Kirchhoff 's voltage law to the circuit *DEN*, we get,

$I_C R_C + V_{CE} = 9$

or 1 mA × 2 kΩ + $V_{CE} = 9$

or $V_{CE} = 9 - 2 =$ **7 V**

(*ii*) When R_B is made equal to 50 kΩ, then it is easy to see that base current is doubled *i.e.* $I_B = 40$ μA.

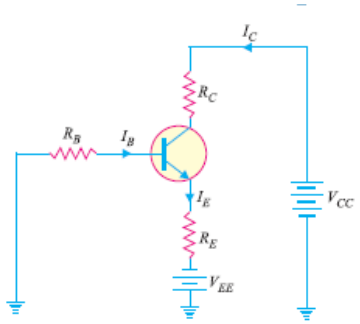
∴ Collector current, $I_C = \beta I_B = 50 \times 40 = 2000\ \mu$ A = 2 mA

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 9 - 2$ mA × 2 kΩ = 5 V

∴ New operating point is **5 V, 2 mA.**

Emitter Bias Circuit

Fig. 1.8 shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources; one positive (+ V_{CC}) and the other negative (– V_{EE}). Normally, the two supply voltages will be equal. For example, if V_{CC} = + 20V (d.c.), then VEE = – 20V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.



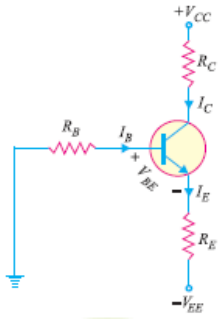


Fig. 1.8 Fig. 1.9

We shall first redraw the circuit in Fig. 1.8 as it usually appears on schematic diagrams. This means deleting the battery symbols as shown in Fig. 1.9. All the information is still (See Fig. 1.9) on the diagram except that it is in condensed form. That is a negative supply voltage – VEE is applied to the bottom of R_E and a positive voltage of + V_{CC} to the top of R_C.

Circuit Analysis of Emitter Bias

Fig. 1.9 shows the emitter bias circuit. We shall find the Q-point values (i.e. d.c. I_C and d.c. V_{CE}) for this circuit.

(i) Collector current (I_C). Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 1.9, we have,

$$– I_BR_B – V_{BE} – I_ER_E + V_{EE} = 0$$

$$\therefore V_{EE} = I_BR_B + V_{BE} + I_ER_E$$

Now $I_C \cong I_E$ and $I_C = \beta I_B \therefore I_B \cong \frac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $V_{EE} – V_{BE} = I_E (R_B/\beta + R_E)$

$$\therefore I_E = \frac{V_{EE} - V_{BE}}{R_E + {}^{R_B}/_{\beta}}$$

Since $I_C \cong I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + {}^{R_B}/_{\beta}}$$

(ii) Collector-emitter voltage (V_{CE}). Fig. 1.10 shows the various voltages of the emitter bias circuit w.r.t. ground

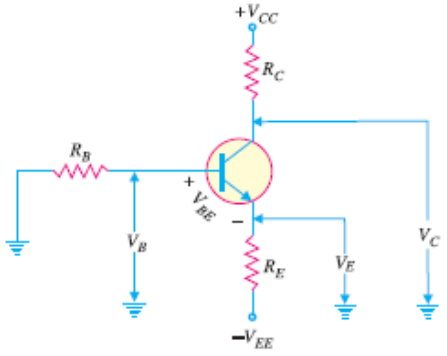


Fig. 1.10

Emitter voltage w.r.t. ground is

$V_E = – V_{EE} + I_E R_E$

Base voltage w.r.t. ground is

$V_B = V_E + V_{BE}$

Collector voltage w.r.t. ground is

$V_C = V_{CC} – I_C R_C$

Subtracting V_E from V_C and using the approximation $I_C \cong IE$, we have,

$V_C – V_E = (V_{CC} – I_C R_C) – (– V_{EE} + I_C R_E)$ ($\because I_E \cong I_C$)

or $V_{CE} = V_{CC} + V_{EE} – I_C (R_C + R_E)$

Alternatively, Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. 1.9 (Refer back), we have,

$V_{CC} – I_C R_C – V_{CE} – I_C* R_E + V_{EE} = 0$

or $V_{CE} = V_{CC} + VEE – I_C (R_C + R_E)$

Stability of Emitter bias: The expression for collector current I_C for the emitter bias circuit is given by;

$I_C \cong I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes:

$I_C = \frac{V_{EE} - V_{BE}}{R_E}$

This condition makes I_C ($\cong I_E$) independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes:

$I_C (\cong I_E) = \frac{V_{EE}}{R_E}$

This condition makes I_C ($\cong I_E$) independent of V_{BE}.

If I_C ($\cong I_E$) is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

Example 1.4

For the emitter bias circuit shown in Fig. 1.11, find I_E, I_C,V_C and V_{CE} for β = 85 and V_{BE} = 0.7V.

Solution

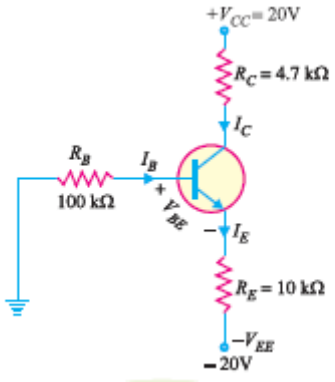


Fig. 1.11

$I_C \cong I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.7V}{10k\Omega + 100k\Omega/85}$ = 1.73 mA

$V_C = V_{CC} - I_C R_C$ = 20V – (1.73 mA) (4.7 kΩ) = 11.9V

$V_E = -V_{EE} + I_E R_E$ = – 20V + (1.73 mA) (10 kΩ) = – 2.7V

∴ $V_{CE} = V_C - V_E$ = 11.9 – (– 2.7V) = 14.6V

Example 1.5

Determine how much the Q-point in Fig. 1.11 (above) will change over a temperature range where β increases from 85 to 100 and VBE decreases from 0.7V to 0.6V.

Solution

For β = 85 and V_{BE} = 0.7V

As calculated in the above example, I_C = 1.73 mA and V_{CE} = 14.6V.

For β = 100 and V_{BE} = 0.6V

$I_C \cong I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.6V}{10k\Omega + 100k\Omega/100}$1.76 mA

$V_C = V_{CC} - I_C R_C$ = 20V – (1.76 mA) (4.7 kΩ) = 11.7V

$V_E = -V_{EE} + I_E R_E$ = – 20V + (1.76 mA) (10 kΩ) = – 2.4V

∴ $V_{CE} = V_C - V_E$ = 11.7 – (– 2.4) = 14.1V

% age change in I_C = $\frac{1.76\text{ mA} - 1.73\text{ mA}}{1.73\text{ mA}} \times 100$ = 1.7% (increase)

% age change in V_{CE} = $\frac{14.1V - 14.6V}{14.1V} \times 100$ = – 3.5% (decrease)

Biasing with Collector Feedback Resistor

In this method, one end of R_B is connected to the base and the other end to the collector as shown in Fig. 1.12. Here, the required zero signal base current is determined not by V_{CC} but by the collector base voltage V_{CB}. It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

Circuit analysis:

The required value of R_B needed to give the zero signal current I_C can be determined as follows. Referring to Fig. 1.12,

$V_{CC} = *I_C R_C + I_B R_B + V_{BE}$

or $R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$ ($I_C = \beta I_B$)

Alternatively, $V_{CE} = V_{BE} + V_{CB}$

or $V_{CB} = V_{CE} - V_{BE}$

$\therefore R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}$; where $I_B = \frac{I_C}{\beta}$

It can be shown mathematically that stability factor S for this method of biasing is less than

$(\beta + 1)$ i.e. Stability factor, $S < (\beta + 1)$

Therefore, this method provides better thermal stability than the fixed bias.

Note. It can be easily proved (See **Example 1.17) that Q-point values (I_C and V_{CE}) for the circuit shown in Fig. 1.12 are given by ;

$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}$

and $V_{CE} = V_{CC} - I_C R_C$

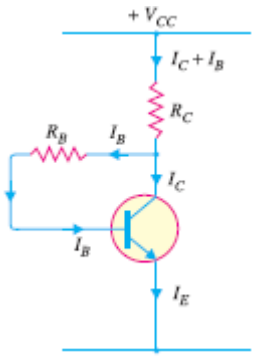


Fig. 1.12

Advantages

(i) It is a simple method as it requires only one resistance R_B.

(ii) This circuit provides some stabilisation of the operating point as discussed below:

$V_{CE} = V_{BE} + V_{CB}$

Suppose the temperature increases. This will increase collector leakage current and hence the total collector current. But as soon as collector current increases, V_{CE} decreases due to greater drop across R_C. The result is that V_{CB} decreases i.e. lesser voltage is available across R_B. Hence the base current I_B decreases. The smaller I_B tends to decrease the collector current to original value.

Disadvantages

(i) The circuit does not provide good stabilisation because stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and other effects.

(ii) This circuit provides a negative feedback which reduces the gain of the amplifier as explained hereafter. During the positive half-cycle of the signal, the collector current increases. The increased collector current would result in greater voltage drop across RC. This will reduce the base current and hence collector current.

Example 1.6

Fig. 1.13 shows a silicon transistor biased by collector feedback resistor method.

Determine the operating point. Given that $\beta = 100$.

Solution

$V_{CC} = 20V$, $R_B = 100\ k\Omega$, $R_C = 1k\Omega$

Since it is a silicon transistor, $V_{BE} = 0.7$ V.

Assuming I_B to be in mA and using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - \beta I_C R_C}{I_B}$$

or $100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1$

or $200\ I_B = 19.3$

or $I_B = \frac{19.3}{200} = 0.096$ mA

∴ Collector current, $I_C = \beta\ I_B = 100 \times 0.096 = 9.6$ mA

Collector-emitter voltage is

$V_{CE} = V_{CC} - I_C\ R_C$

$= 20 - 9.6\ mA \times 1\ k\Omega$

$= 10.4$ V

∴ Operating point is 10.4 V, 9.6 mA.

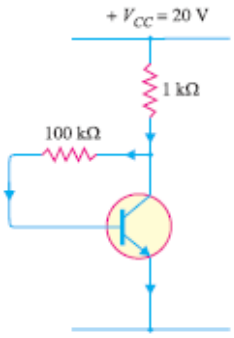


Fig. 1.13

Alternatively

$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{20V - 0.7V}{100\ k\Omega/100 + 1\ k\Omega} = \frac{19.3V}{2k\Omega}$

$V_{CE} = V_{CC} - I_C R_C = 20V - 9.65\ mA \times 1\ k\Omega = 10.35V$

A very slight difference in the values is due to manipulation of calculations.

Voltage Divider Bias Method

This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} (See Fig. 1.24) and provide biasing. The emitter resistance RE provides stabilisation. The name ‘‘voltage divider’’ comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero-signal condition.

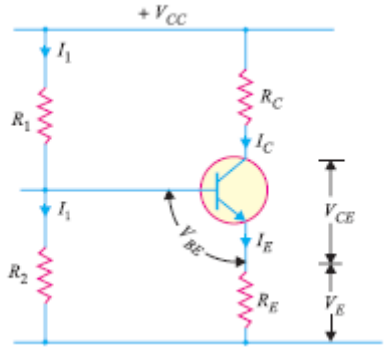


Fig. 1.14

Circuit analysis

Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

(i) Collector current I_C:

$I_1 = \frac{V_{CC}}{R_1 + R_2}$

∴ Voltage across resistance R_2 is

$V_2 = (\frac{V_{CC}}{R_1 + R_2})\ R_2$

Applying Kirchhoff 's voltage law to the base circuit of Fig. 1.24,

$V_2 = V_{BE} + V_E$

or $V_2 = V_{BE} + I_E\ R_E$

or $I_E = \frac{V_2 - V_{BE}}{R_E}$

Since $I_E \cong I_C$

$\therefore I_C = \frac{V_2 - V_{BE}}{R_E}$ ...(i)

It is clear from exp. (i) above that I_C does not at all depend upon β. Though I_C depends upon V_{BE} but in practice $V_2 >> V_{BE}$ so that I_C is practically independent of V_{BE}. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured. It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

(ii) Collector-emitter voltage V_{CE}. Applying Kirchhoff 's voltage law to the collector side,

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$= I_C R_C + V_{CE} + I_C R_E$ ($I_E \cong I_C$)

$= I_C\ (R_C + R_E) + V_{CE}$

$\therefore V_{CE} = V_{CC} - I_C\ (R_C + R_E)$

Stabilisation: In this circuit, excellent stabilisation is provided by R_E. Consideration of eq. (i) reveals this fact.

$V_2 = V_{BE} + I_C\ R_E$

Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across emitter resistance R_E to increase. As voltage drop across R_2 (i.e. V_2) is *independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor: It can be shown mathematically that stability factor of the circuit is given by :

Stability factor, $S = \frac{(\beta+1)(R_0 - R_E)}{R_0 + R_E + \beta R_E}$

$= (\beta + 1) \times \frac{1 + \frac{R_0}{R_E}}{\beta + 1 + \frac{R_0}{R_E}}$

Where $R_0 = \frac{R_1 R_2}{R_1 + R_2}$

If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 and the stability factor becomes:

Stability factor = $(\beta + 1) \times \frac{1}{\beta + 1} = 1$

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, R_0/R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Chapter 2

Single Stage Transistor Amplifiers

When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as single stage transistor amplifier.

A single stage transistor amplifier has one transistor, bias circuit and other auxiliary components. Although a practical amplifier consists of a number of stages, yet such a complex circuit can be conveniently split up into separate single stages. By analysing carefully only a single stage and using this single stage analysis repeatedly, we can effectively analyse the complex circuit. It follows, therefore, that single stage amplifier analysis is of great value in understanding the practical amplifier circuits.

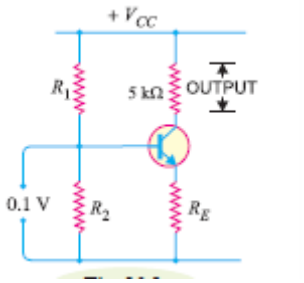


Fig. 2.1

How Transistor Amplifies?

Fig. 2.1 shows a single stage transistor amplifier. When a weak a.c. signal is given to the base of transistor, a small base current (which is a.c.) starts flowing. Due to transistor action, a much larger (β times the base current) a.c. current flows through the collector load R_C. As the value of R_C is quite high (usually 4-10 kΩ), therefore, a large voltage appears across R_C. Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

The action of transistor amplifier can be beautifully explained by referring to Fig. 2.1. Suppose a change of 0.1V in signal voltage produces a change of 2 mA in the collector current. Obviously, a signal of only 0.1V applied to the base will give an output voltage = 2 mA × 5 kΩ = 10V. Thus, the transistor has been able to raise the voltage level of the signal from 0.1V to 10V i.e. voltage amplification or stage gain is 100.

Graphical Demonstration of Transistor Amplifier

The function of transistor as an amplifier can also be explained graphically. Fig. 2.2 shows the output characteristics of a transistor in CE configuration. Suppose the zero signal base current is 10 μA i.e. this is the base current for which the transistor is biased by the biasing network. When an a.c. signal is applied to the base, it makes the base, say positive in the first half-cycle and negative in the second half cycle.

Therefore, the base and collector currents will increase in the first half-cycle when base-emitter junction is more forward-biased. However, they will decrease in the second half-cycle when the base-emitter junction is less forward biased.

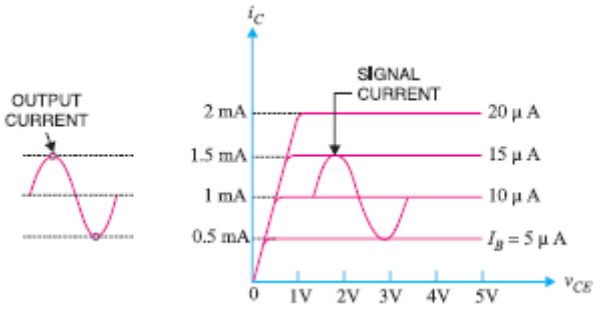


Fig. 2.2

For example, consider a sinusoidal signal which increases or decreases the base current by 5 μA in the two half-cycles of the signal. Referring to Fig. 2.2, it is clear that in the absence of signal, the base current is 10μA and the collector current is 1 mA. However, when the signal is applied in the base circuit, the base current and hence collector current change continuously. In the first half-cycle peak of the signal, the base current increases to 15 μA and the corresponding collector current is 1.5 mA. In the second half-cycle peak, the base current is reduced to 5 μA and the corresponding collector current is 0.5 mA. For other values of the signal, the collector current is inbetween these values i.e. 1.5 mA and 0.5 mA.

It is clear from Fig. 2.2 that 10 μA base current variation results in 1mA (1,000 μA) collector current variation i.e. by a factor of 100. This large change in collector current flows through collector resistance R_C. The result is that output signal is much larger than the input signal. Thus, the transistor has done amplification.

Practical Circuit of Transistor Amplifier

It is important to note that a transistor can accomplish faithful amplification only if proper associated circuitry is used with it. Fig. 2.3 shows a practical single stage transistor amplifier. The various circuit elements and their functions are described below:

(i) Biasing circuit. The resistances R_1, R_2 and R_E form the biasing and stabilisation circuit. The biasing circuit must establish a proper operating point otherwise a part of the negative half-cycle of the signal may be cut off in the output.

(ii) Input capacitor C_{in}. An electrolytic capacitor C_{in} (≅ 10 μF) is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance will come across R_2 and thus change the bias. The capacitor C_{in} allows only a.c. signal to flow but isolates the signal source from

R_2.*

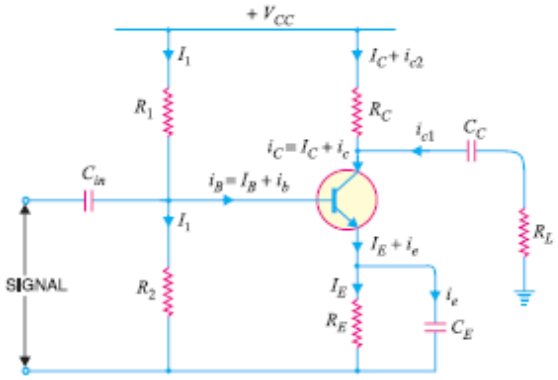


Fig. 2.3

(iii) Emitter bypass capacitor C_E. An emitter bypass capacitor C_E ($\cong 100\mu F$) is used in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby reducing the output voltage.

(iv) Coupling capacitor C_C. The coupling capacitor C_C ($\cong 10\mu F$) couples one stage of amplification to the next stage. If it is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C. This is because R_C will come in parallel with the upper resistance R_1 of the biasing network of the next stage, thereby altering the biasing conditions of the latter. In short, the coupling capacitor C_C isolates the d.c. of one stage from the next stage, but allows the passage of a.c. signal.

Various circuit currents: It is useful to mention the various currents in the complete amplifier circuit. These are shown in the circuit of Fig. 2.3.

(i) Base current. When no signal is applied in the base circuit, d.c. base current I_B flows due to biasing circuit. When a.c. signal is applied, a.c. base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by:

$$i_B = I_B + i_b$$

(ii) Collector current. When no signal is applied, a d.c. collector current I_C flows due to biasing circuit. When a.c. signal is applied, a.c. collector current i_c also flows. Therefore, the total collector current i_C is given by:

$$i_C = I_C + i_c$$

where $I_C = \beta I_B$ = zero signal collector current

$i_c = \beta i_b$ = collector current due to signal.

(iii) Emitter current. When no signal is applied, a d.c. emitter current I_E flows. With the application of signal, total emitter current i_E is given by:

$$i_E = I_E + i_e$$

It is useful to keep in mind that:

$$I_E = I_B + I_C$$

$$i_e = i_b + i_c$$

Now base current is usually very small, therefore, as a reasonable approximation,

$I_E \cong I_C$ and $i_e \cong i_c$

Example 2.1

What is the role of emitter bypass capacitor C_E in C_E amplifier circuit shown in Fig. 2.3? Illustrate with a numerical example.

Solution

The emitter bypass capacitor C_E (See Fig. 2.3) connected in parallel with R_E plays an important role in the circuit. If it is not used, the amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby reducing the a.c. output voltage and hence the voltage gain of the amplifier.

Let us illustrate the effect of C_E with a numerical example. Suppose R_E = 1000Ω and capacitive reactance of C_E at the signal frequency is 100Ω (i.e. X_{C_E} = 100Ω). Then 10/11 of a.c emitter current will flow through CE and only 1/11 through RE. The signal voltage developed across R_E is, therefore, only 1/11 of the voltage which would have been developed if C_E were not present. In practical circuits, the value of C_E is so selected that it almost entirely bypasses the a.c. signal (the name for C_E is obvious). For all practical purposes, we consider C_E to be a short for a.c. signals.

Example 2.2

Select a suitable value for the emitter bypass capacitor in Fig. 2.4 if the amplifier is to operate over a frequency range from 2 kHz to 10 kHz.

Solution

An amplifier usually handles more than one frequency. Therefore, the value of C_E is so selected that it provides adequate bypassing for the lowest of all the frequencies. Then it will also be a good bypass ($X_C \propto 1/f$) for all the higher frequencies. Suppose the minimum frequency to be handled by C_E is f_{min}. Then C_E is considered a good bypass if at f_{min}

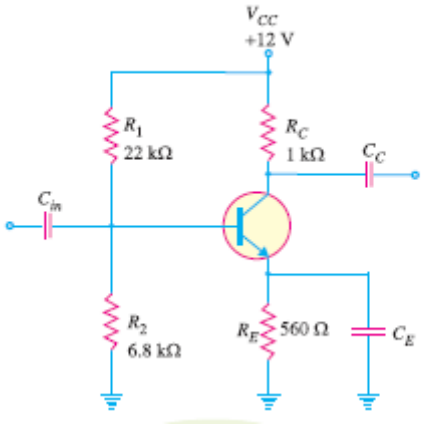


Fig. 2.4

$X = \frac{R_E}{10}$

In the given problem, f_{min} = 2kHz ; R_E = 560Ω.

∴ 10 X_{C_E} = 560

or X_{C_E} = 560/10 = 56Ω

or $\frac{1}{2\pi f_{min}\, C_E}$

∴ $C_E = \frac{1}{2\pi f_{min}\, 56} = \frac{1}{2\pi \times (2 \times 10^3) \times 56} = 1.42 \times 10^{-6} = 1.42\ \mu F$

Note. While discussing CE amplifier, the reader should be very particular about the role of CE.

Phase Reversal

In common emitter connection, when the input signal voltage increases in the positive sense, the output voltage increases in the negative direction and vice-versa. In other words, there is a phase difference of 180° between the input and output voltage in CE connection. This is called phase reversal.*

The phase difference of 180° between the signal voltage and output voltage in a common emitter amplifier is known as phase reversal.

Consider a common emitter amplifier circuit shown in Fig. 2.5. The signal is fed at the input terminals (i.e. between base and emitter) and output is taken from collector and emitter end of supply. The total instantaneous output voltage v_{CE} is given by:

$$**v_{CE} = V_{CC} - i_C R_C \quad ...(i)$$

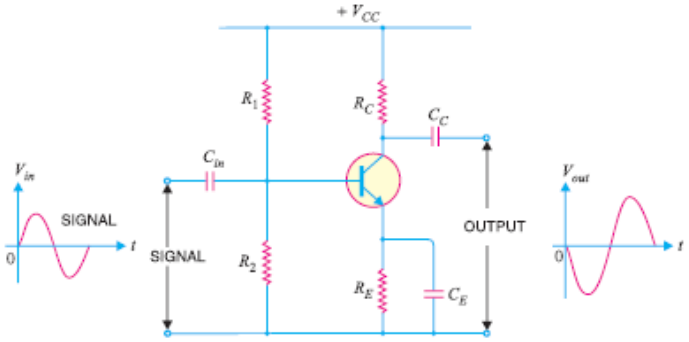


Fig. 2.5

When the signal voltage increases in the positive half-cycle, the base current also increases. The result is that collector current and hence voltage drop $i_C R_C$ increases. As V_{CC} is constant, therefore, output voltage v_{CE} decreases. In other words, as the signal voltage is increasing in the positive half-cycle, the output voltage is increasing in the negative sense i.e. output is 180° out of phase with the input. It follows, therefore, that in a common emitter amplifier, the positive half-cycle of the signal appears as amplified negative half-cycle in the output and vice-versa. It may be noted that amplification is not affected by this phase reversal.

The fact of phase reversal can be readily proved mathematically. Thus differentiating exp. (i), we get,

$$dv_{CE} = 0 - di_c R_C$$

or $$dv_{CE} = - di_c R_C$$

The negative sign shows that output voltage is 180° out of phase with the input signal voltage.

Graphical demonstration: The fact of phase reversal in CE connection can be shown graphically with the help of output characteristics and load line (See Fig. 2.6).

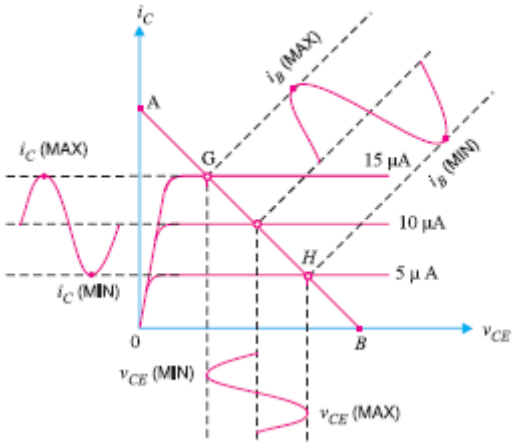


Fig. 2.6

In Fig. 2.6, AB is the load line. The base current fluctuates between, say ± 5 μA with 10μA as the zero signal base current. From the figure, it is clear that when the base current is maximum in the positive direction, v_{CE} becomes maximum in the negative direction (point G in Fig. 2.6). On the other hand, when the base current is maximum in the negative direction, v_{CE} is maximum in the positive sense (point H in Fig. 2.6). Thus, the input and output voltages are in phase opposition or equivalently, the transistor is said to produce a 180º phase reversal of output voltage w.r.t. signal voltage.

Note. No phase reversal of voltage occurs in common base and common collector amplifier. The a.c. output voltage is in phase with the a.c. input signal. For all three amplifier configurations; input and output currents are in phase.

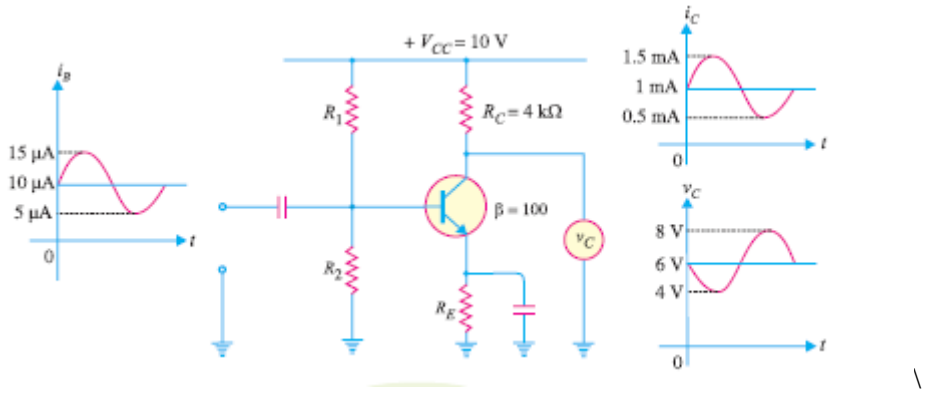


Fig. 2.7

The output voltage, $v_C = V_{CC} - i_C R_C$

(i) When signal current is zero (i.e., in the absence of signal), $i_C = 1$ mA.

$\therefore v_C = V_{CC} - i_C R_C = 10 \text{ V} - 1 \text{ mA} \times 4 \text{ k}\Omega = 6\text{V}$

(ii) When signal reaches positive peak value, iC = 1.5 mA.

$\therefore v_C = V_{CC} - i_C R_C = 10 \text{ V} - 1.5 \text{ mA} \times 4 \text{ k}\Omega = 4 \text{ V}$

Note that as i_C increases from 1mA to 1.5 mA, v_C decreases from 6V to 4V. Clearly, output voltage is 180° out of phase from the input voltage as shown in Fig. 2.7.

(iii) When signal reaches negative peak, iC = 0.5 mA.

$\therefore v_C = V_{CC} - i_C R_C = 10 \text{ V} - 0.5 \text{ mA} \times 4 \text{ k}\Omega = 8 \text{ V}$

Note that as i_C decreases from 1.5 mA to 0.5 mA, v_C increases from 4 V to 8 V. Clearly, output voltage is 180° out of phase from the input voltage. The following points may be noted carefully about CE amplifier:

(a) The input voltage and input current are in phase.

(b) Since the input current and output current are in phase, input voltage and output current are in phase.

(c) Output current is 180° out of phase with the output voltage (v_C). Therefore, input voltage and output voltage are 180° out of phase.

Input/Output Phase Relationships

The following points regarding the input / output phase relationships between currents and voltages for the various transistor configurations may be noted:

(i) For every amplifier type (CE, CB and CC), the input and output currents are in phase. When the input current decreases, the output current also decreases and vice-versa

(ii) Remember that common emitter (CE) circuit is the only configuration that has input and output voltages 180° out of phase.

(iii) For both common base (CB) and common collector (CC) circuits, the input and output voltages are in phase. If the input voltage decreases, the output voltage also decreases and vice-versa.

D.C. And A.C. Equivalent Circuits

In a transistor amplifier, both d.c. and a.c. conditions prevail. The d.c. sources set up d.c. currents and voltages whereas the a.c. source (i.e. signal) produces fluctuations in the transistor currents and voltages.

Therefore, a simple way to analyse the action of a transistor is to split the analysis into two parts viz. a d.c. analysis and an a.c. analysis. In the d.c. analysis, we consider all the d.c. sources at the same time and work out the d.c. currents and voltages in the circuit. On the other hand, for a.c. analysis, we consider all the a.c. sources at the same time and work out the a.c. currents and voltages. By adding the d.c. and a.c. currents and voltages, we get the total currents and voltages in the circuit. For example, consider the amplifier circuit shown in Fig. 2.8. This circuit can be easily analysed by splitting it into d.c. equivalent circuit and a.c equivalent circuit.

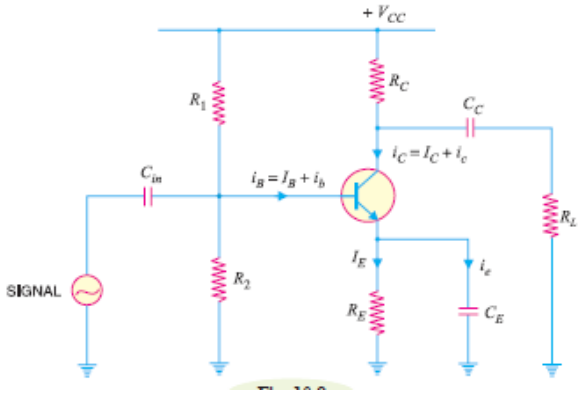


Fig. 2.8

(i) D. C. equivalent circuit. In the d.c. equivalent circuit of a transistor amplifier, only d.c. conditions are to be considered i.e. it is presumed that no signal is applied. As direct current cannot flow through a capacitor, therefore, all the capacitors look like open circuits in the d.c. equivalent circuit. It follows, therefore, that in order to draw the equivalent d.c. circuit, the following two steps are applied to the transistor circuit:

(a) Reduce all a.c. sources to zero.

(b) Open all the capacitors.

Applying these two steps to the circuit shown in Fig. 2.8, we get the d.c. equivalent circuit shown in Fig. 2.9. We can easily calculate the d.c. currents and voltages from this circuit.

(ii) A.C. equivalent circuit. In the a.c. equivalent circuit of a transistor amplifier, only a.c. conditions are to be considered. Obviously, the d.c. voltage is not important for such a circuit and may be considered zero. The capacitors are generally used to couple or bypass the a.c. signal. The designer intentionally selects capacitors that are large enough to appear as short circuits to the a.c. signal. It follows, therefore, that in order to draw the a.c. equivalent circuit, the following two steps are applied to the transistor circuit:

(a) Reduce all d.c. sources to zero (i.e. $V_{CC} = 0$).

(b) Short all the capacitors.

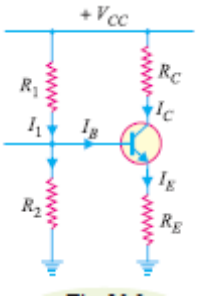


Fig. 2.9

Applying these two steps to the circuit shown in Fig. 2.8, we get the a.c. *equivalent circuit shown in Fig. 2.10. We can easily calculate the a.c. currents and voltages from this circuit.

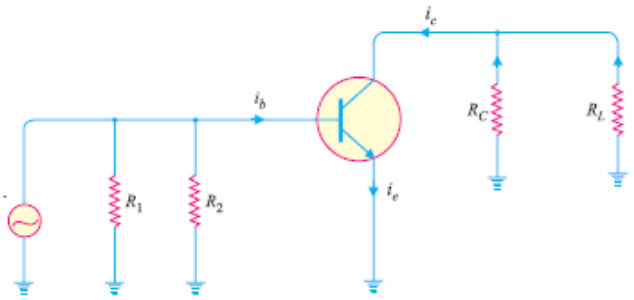


Fig. 2.10

It may be seen that total current in any branch is the sum of d.c. and a.c. currents through that branch. Similarly, the total voltage across any branch is the sum of d.c. and a.c. voltages across that branch.

Example 2.3

For the transistor amplifier circuit shown in Fig. 2.8, determine:

(i) d.c. load and a.c. load

(ii) maximum collector-emitter voltage and collector current under d.c. conditions

(iii) maximum collector-emitter voltage and collector current when a.c. signal is applied

Solution

Refer back to the transistor amplifier circuit shown in Fig. 2.8.

(i) The d.c. load for the transistor is Thevenin's equivalent resistance as seen by the collector and emitter terminals. Thus referring to the d.c. equivalent circuit shown in Fig. 2.9, Thevenin's equivalent resistance can be found by shorting the voltage source (i.e. V_{CC}) as shown in Fig. 2.11. Because a voltage source looks like a short, it will bypass all other resistances except R_C and R_E which will appear in series. Consequently, transistor amplifier will see a d.c. load of $R_C + R_E$ i.e d.c. load = $R_C + R_E$

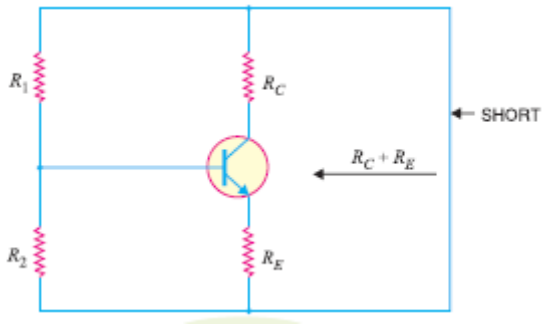


Fig. 2.11

Referring to the a.c. equivalent circuit shown in Fig. 2.10, it is clear that as far as a.c. signal is concerned, resistance R_C appears in parallel with R_L. In other words, transistor amplifier sees an a.c. load equal to $R_C \parallel R_L$

i.e. a.c. load, $R_{AC} = R_C \parallel R_L$

$= \frac{R_C R_L}{R_C + R_L}$

(ii) Referring to d.c. equivalent circuit of Fig. 2.9,

$V_{CC} = V_{CE} + I_C (R_C + R_E)$

The maximum value of V_{CE} will occur when there is no collector current i.e. $I_C = 0$.

∴ Maximum $V_{CE} = V_{CC}$

The maximum collector current will flow when $V_{CE} = 0$.

∴ Maximum $I_C = \frac{V_{CC}}{R_C + R_E}$

(iii) When no signal is applied, V_{CE} and I_C are the collector-emitter voltage and collector current respectively. When a.c. signal is applied, it causes changes to take place above and below the operating point Q (i.e. V_{CE} and I_C).

Maximum collector current due to a.c. signal = $*I_C$

∴ Maximum positive swing of a.c. collector-emitter voltage

$= I_C \times R_{AC}$

Total maximum collector-emitter voltage

$= V_{CE} + I_C R_{AC}$

Maximum positive swing of a.c. collector current

$= V_{CE}/R_{AC}$

∴ Total maximum collector current

$= I_C + V_{CE}/R_{AC}$

Load Line Analysis

The output characteristics are determined experimentally and indicate the relation between V_{CE} and I_C. However, the same information can be obtained in a much simpler way by representing the mathematical relation between I_C and V_{CE} graphically. As discussed before, the relationship between V_{CE} and I_C is linear so that it can be represented by a straight line on the output characteristics. This is known as a load line. The points lying on the load line give the possible values of V_{CE} and I_C in the output circuit. As in a transistor circuit both d.c. and a.c. conditions exist, therefore, there are two types of load lines, namely; d.c. load line and a.c. load line. The former determines the locus of I_C and V_{CE} in the zero signal conditions and the latter shows these values when the signal is applied.

(i) d.c. load line. It is the line on the output characteristics of a transistor circuit which gives the values of I_C and V_{CE} corresponding to zero signal or d.c. conditions. Consider the transistor amplifier shown in Fig. 2.12. In the absence of signal, d.c. conditions prevail in the circuit as shown in Fig. 2.13 (i). Referring to this circuit and applying Kirchhoff's voltage law,

$V_{CE} = V_{CC} - I_C R_C - I_E R_E$

or $V_{CE} = V_{CC} - I_C (R_C + R_E)$ ...(i)

($I_E \cong I_C$)

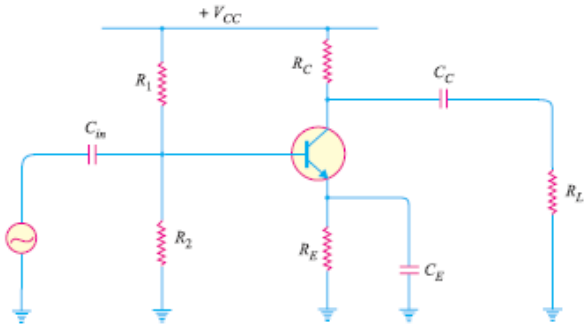


Fig. 2.12

As for a given circuit, V_{CC} and $(R_C + R_E)$ are constant, therefore, it is a first degree *equation and can be represented by a straight line on the output characteristics. This is known as d.c. load line and determines the loci of V_{CE} and I_C points in the zero signal conditions. The d.c. load line can be readily plotted by locating two end points of the straight line.

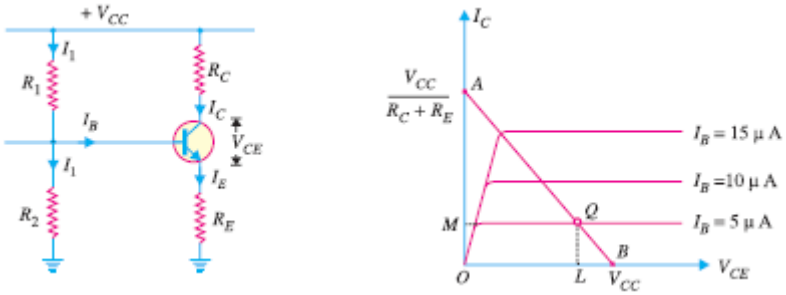


Fig. 2.13

The value of V_{CE} will be maximum when $I_C = 0$. Therefore, by putting $I_C = 0$ in exp. (i), we get,

Max. $V_{CE} = V_{CC}$

This locates the first point B ($OB = V_{CC}$) of the d.c. load line.

The value of I_C will be maximum when $V_{CE} = 0$.

$\therefore$ Max. $I_C = \frac{V_{CC}}{R_C + R_E}$

This locates the second point A ($OA = V_{CC}/R_C + R_E$) of the d.c. load line. By joining points A and B, d.c. load line AB is constructed [See Fig. 2.13 (ii)].

Alternatively. The two end points of the d.c. load line can also be determined in another way.

$V_{CE} + I_C (R_C + R_E) = V_{CC}$

Dividing throughout by V_{CC}, we have,

$$\frac{V_{CE}}{V_{CC}} + \frac{I_C}{V_{CC}/R_C + R_E} = 1 \quad ...(i)$$

The equation of a line having intercepts a and b on x-axis and y-axis respectively is given by;

$$\frac{x}{a} + \frac{y}{b} = 1 \quad ...(ii)$$

Comparing eqs. (i) and (ii), we have,

Intercept on x-axis = V_{CC}

Intercept on y-axis = $\frac{V_{CC}}{R_C + R_E}$

With the construction of d.c. load line on the output characteristics, we get the complete information about the output circuit of transistor amplifier in the zero signal conditions. All the points showing zero signal I_C and V_{CE} will obviously lie on the d.c. load line. At the same time I_C and V_{CE} conditions in the circuit are also represented by the output characteristics. Therefore, actual operating conditions in the circuit will be represented by the point where d.c. load line intersects the base current curve under study. Thus, referring to Fig. 2.13 (ii), if $I_B = 5\mu A$ is set by the biasing circuit, then Q (i.e. intersection of 5μA curve and load line) is the operating point.

(ii) a.c. load line. This is the line on the output characteristics of a transistor circuit which gives the values of i_C and v_{CE} when signal is applied.

Referring back to the transistor amplifier shown in Fig. 2.12, its a.c. equivalent circuit as far as output circuit is concerned is as shown in Fig. 2.14 (i). To add a.c. load line to the output characteristics, we again require two end points–one maximum collector-emitter voltage point and the other maximum collector current point. Under the application of a.c. signal, these values are (refer to Example 2.3) :

Max. collector-emitter voltage = $V_{CE} + I_C R_{AC}$. This locates the point C of the a.c. load line on the collector-emitter voltage axis.

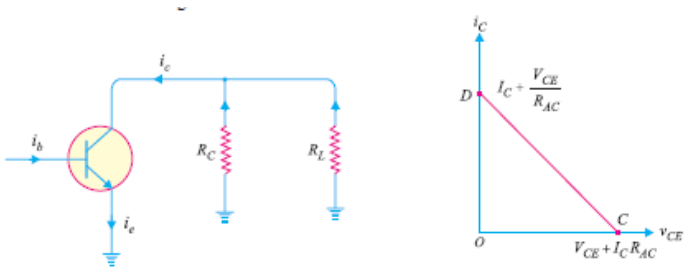


Fig. 2.14

Maximum collector current = $I_C + \frac{V_{CE}}{R_{AC}}$

where $R_{AC} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L}$

This locates the point D of a.c. load line on the collector-current axis. By joining points C and D, the a.c.load line CD is constructed [See Fig. 2.14 (ii)].

Example 2.4

For the transistor amplifier shown in Fig. 2.15, R_1 = 10 kΩ, R_2 = 5 kΩ, R_C = 1 kΩ, RE = 2 kΩ and R_L = 1 kΩ.

(i) Draw d.c. load line (ii) Determine the operating point (iii) Draw a.c. load line.

Assume V_{BE} = 0.7 V.

Solution

(i) d.c. load line: To draw d.c. load line, we require two end points viz maximum V_{CE} point and maximum I_C point.

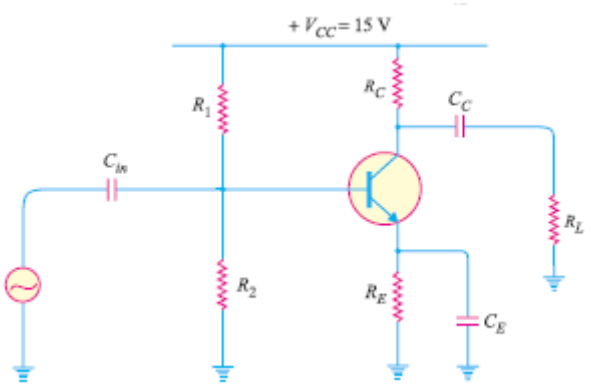


Fig. 2.15

Maximum $V_{CE} = V_{CC}$ = 15 V

This locates the point B (OB=15 V) of the d.c. load line.

Maximum $I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15V}{(1+2)k\Omega}$ = 5 mA

This locates the point A (OA = 5 mA) of the d.c. load line. Fig. 2.16 (i) shows the d.c. load line AB.

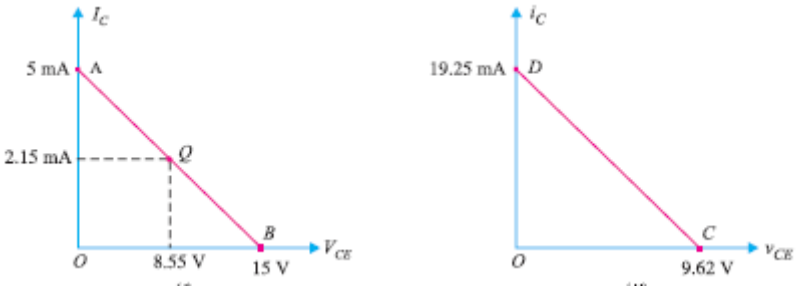


Fig. 2.16

(ii) Operating point Q. The voltage across R2 (= 5 kΩ) is *5 V i.e. V_2 = 5 V.

Now $V_2 = V_{BE} + I_E R_E$

$\therefore I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{(5-0.7)V}{2k\Omega} = 2.15$ mA

$\therefore I_C = I_E = 2.15$ mA

Now $V_{CE} = V_{CC} - I_C (R_C + R_E) = 15 - 2.15$ mA $\times$ 3 kΩ = 8.55 V

∴ Operating point Q is 8.55 V, 2.15 mA. This is shown on the d.c. load line.

(iii) a.c. load line. To draw a.c. load line, we require two end points viz. maximum collector-emitter voltage point and maximum collector current point when signal is applied.

a.c. load, $R_{AC} = R_C \parallel R_L = \frac{1 \times 1}{1+1} = 0.5$ kΩ

∴ Maximum collector-emitter voltage

$= V_{CE} + I_C R_{AC}$ [See Example 2.3]

= 8.55 + 2.15 mA × 0.5 kΩ = 9.62 volts

This locates the point C (OC = 9.62 V) on the v_{CE} axis.

Maximum collector current = $I_C + V_{CE}/R_{AC}$

= 2.15 + (8.55 V/0.5 kΩ) = 19.25 mA

This locates the point D (OD = 19.25mA) on the i_C axis. By joining points C and D, a.c. load line CD is constructed [See Fig. 2.16 (ii)].

Example 2.5

In a transistor amplifier, the operating point Q is fixed at 8V, 1mA. When a.c. signal is applied, the collector current and collector-emitter voltage change about this point. During the positive peak of signal, i_C = 1.5 mA and v_{CE} = 7 V and during negative peak, i_C = 0.5mA and v_{CE} = 9V. Show this phenomenon with the help of a.c. load line.

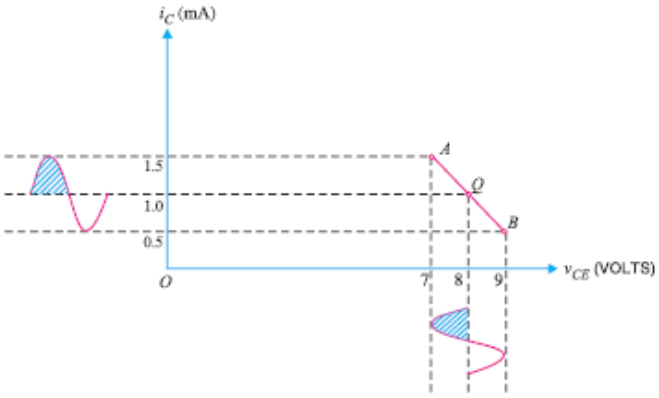


Fig. 2.17

Solution

Fig. 2.17 shows the whole process. When no signal is applied, v_{CE} = 8 V and i_C = 1mA. This is represented by the operating point Q on the a.c. load line. During the positive half cycle of a.c. signal, i_C swings from 1 mA to 1.5 mA and v_{CE} swings from 8 V to 7 V. This is represented by point A on the a.c. load line. During the negative half-cycle of the signal, i_C swings from 1 mA to 0.5 mA and v_{CE} swings from 8 V to 9 V. This is represented by the point B on the a.c. load line.

The following points may be noted:

(i) When a.c. signal is applied, the collector current and collector-emitter voltage variations take place about the operating point Q.

(ii) When a.c. signal is applied, operating point moves along the a.c. load line. In other words, at any instant of a.c. signal, the co-ordinates of collector current and collector-emitter voltage are on the a.c. load line.

Voltage Gain

The basic function of an amplifier is to raise the strength of an a.c. input signal. The voltage gain of the amplifier is the ratio of a.c. output voltage to the a.c. input signal voltage. Therefore, in order to find the voltage gain, we should consider only the a.c. currents and voltages in the circuit. For this purpose, we should look at the a.c. equivalent circuit of transistor amplifier. For facility of reference, the a.c. equivalent circuit of transistor amplifier is redrawn in Fig. 2.18.

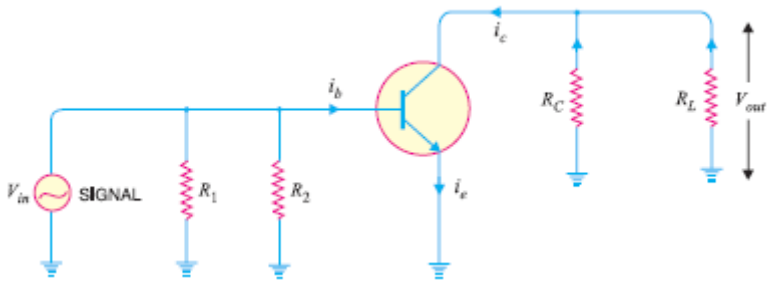


Fig. 2.18

It is clear that as far as a.c. signal is concerned, load R_C appears in parallel with R_L. Therefore, effective load for a.c. is given by:

a.c. load, $R_{AC} = R_C \parallel R_L = C_L = \frac{R_C \times R_L}{R_C + R_L}$

Output voltage, $V_{out} = i_c R_{AC}$

Input voltage, $V_{in} = i_b R_{in}$

∴ Voltage gain, $A_v = V_{out}/V_{in}$

$= \frac{i_c R_{AC}}{i_b R_{in}} = \beta \times \frac{R_{AC}}{R_{in}}$ $\quad [\frac{i_c}{i_b} = \beta]$

Incidentally, power gain is given by;

$A_p = \frac{i_c^2 R_{AC}}{i_b^2 R_{in}} = \beta^2 \times \frac{R_{AC}}{R_{in}}$

Example 2.6

In the circuit shown in Fig. 2.19, find the voltage gain. Given that β = 60 and input resistance Rin = 1 kΩ.

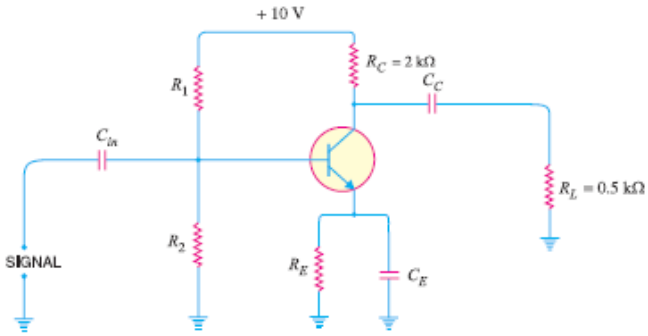


Fig. 2.19

Solution

So far as voltage gain of the circuit is concerned, we need only R_{AC}, β and R_{in}.

Effective load, $R_{AC} = R_C \parallel R_L$

$= \frac{R_C \times R_L}{R_C + R_L} = \frac{2 \times 0.5}{2 + 0.5} = 0.4\ k\Omega$

∴ Voltage gain = $\beta \times \frac{R_{AC}}{R_{in}} = \frac{60 \times 0.4k\Omega}{1k\Omega} = 24$

Example 2.7

In a transistor amplifier, when the signal changes by 0.02V, the base current changes by 10 μA and collector current by 1mA. If collector load RC = 5 kΩ and RL = 10 kΩ, find: (i) current gain (ii) input impedance (iii) a.c. load (iv) voltage gain (v) power gain

Solution

$\Delta I_B = 10\ \mu A$, $\Delta I_C = 1mA$, $\Delta V_{BE} = 0.02\ V$, $R_C = 5\ k\Omega$, $R_L = 10\ k\Omega$

(i) Current gain, $\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{1mA}{10\mu A} = 100$

(ii) Input impedance, $R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.02V}{10\mu A} = 2\ k\Omega$

(iii) a.c. load, $R_{AC} = \frac{R_C \times R_L}{R_C + R_L} = \frac{5 \times 10}{5 + 10} = 3.3\ k\Omega$

(iv) Voltage gain, $A_v = \beta \times \frac{R_{AC}}{R_{in}} = 100 \times \frac{3.3}{2} = 165$

(v) Power gain, A_p = current gain × voltage gain = 100 × 165 = 16500

Chapter 3

Power Amplifiers

A practical amplifier always consists of a number of stages that amplify a weak signal until sufficient power is available to operate a loudspeaker or other output device. The first few stages in this multistage amplifier have the function of only voltage amplification. However, the last stage is designed to provide maximum power. This final stage is known as power stage.

The term audio means the range of frequencies which our ears can hear. The range of human hearing extends from 20 Hz to 20 kHz. Therefore, audio amplifiers amplify electrical signals that have a frequency range corresponding to the range of human hearing i.e. 20 Hz to 20 kHz. Fig. 3.1 shows the block diagram of an audio amplifier. The early stages build up the voltage level of the signal while the last stage builds up power to a level sufficient to operate the loudspeaker.

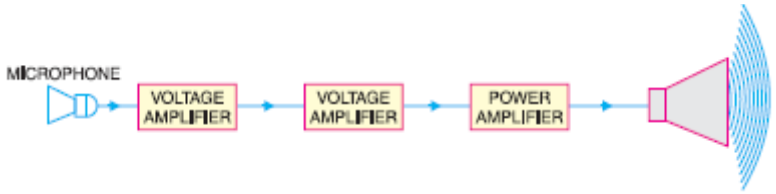


Fig. 3.1

In this chapter, we shall talk about the final stage in a multistage amplifier—the power amplifier.

Transistor Audio Power Amplifier

Signals that have audio frequency range is known as transistor audio power amplifier.

In general, the last stage of a multistage amplifier is the power stage. The power amplifier differs from all the previous stages in that here a concentrated effort is made to obtain maximum output power. A transistor that is suitable for power amplification is generally called a power transistor. It differs from other transistors mostly in size; it is considerably larger to provide for handling the great amount of power. Audio power amplifiers are used to deliver a large amount of power to a low resistance load. Typical load values range from 300Ω (for transmission antennas) to 8Ω (for loudspeakers). Although these load values do not cover every possibility, they do illustrate the fact that audio power amplifiers usually drive low-resistance loads. The typical power output rating of a power amplifier is 1W or more.

Small-Signal and Large-Signal Amplifiers

The input signal to a multistage amplifier is generally small (a few mV from a cassette or CD or a few μV from an antenna). Therefore, the first few stages of a multistage amplifier handle small signals and have the function of only voltage amplification. However, the last stage handles a large signal and its job is to produce a large amount of power in order to operate the output device (e.g. speaker).

(i) Small-signal amplifiers. Those amplifiers which handle small input a.c. signals (a few μV or a few mV) are called small-signal amplifiers. Voltage amplifiers generally fall in this class. The small-signal amplifiers are designed to operate over the linear portion of the output characteristics. Therefore, the transistor parameters such as current gain, input impedance, output impedance etc. do not change as the amplitude of the signal changes. Such amplifiers amplify the signal with little or no distortion.

(ii) Large-signal amplifiers. Those amplifiers which handle large input a.c. signals (a few volts) are called large-signal amplifiers. Power amplifiers fall in this class. The large-signal amplifiers are designed to provide a large amount of a.c. power output so that they can operate the output device e.g. a speaker. The main features of a large-signal amplifier or power amplifier are the circuit's power

efficiency, the maximum amount of power that the circuit is capable of handling and the impedance matching to the output device. It may be noted that all large-signal amplifiers are not necessarily power amplifiers but it is safe to say that most are. In general, where amount of power involved is 1W or more, the amplifier is termed as power amplifier.

Output Power of Amplifier

An amplifier converts d.c. power drawn from d.c. supply V_{CC} into a.c. output power. The output power is always less than the input power because losses occur in the various resistors present in the circuit. For example, consider the R-C coupled amplifier circuit shown in Fig. 3.2. The currents are flowing through various resistors causing I^2R loss. Thus power loss in R_1 is $I_1^2R_1$, power loss in R_C is $I_C^2R_C$, power loss in R_E is $I_E^2R_E$ and so on. All these losses appear as heat. Therefore, losses occurring in an amplifier not only decrease the efficiency but they also increase the temperature of the circuit.

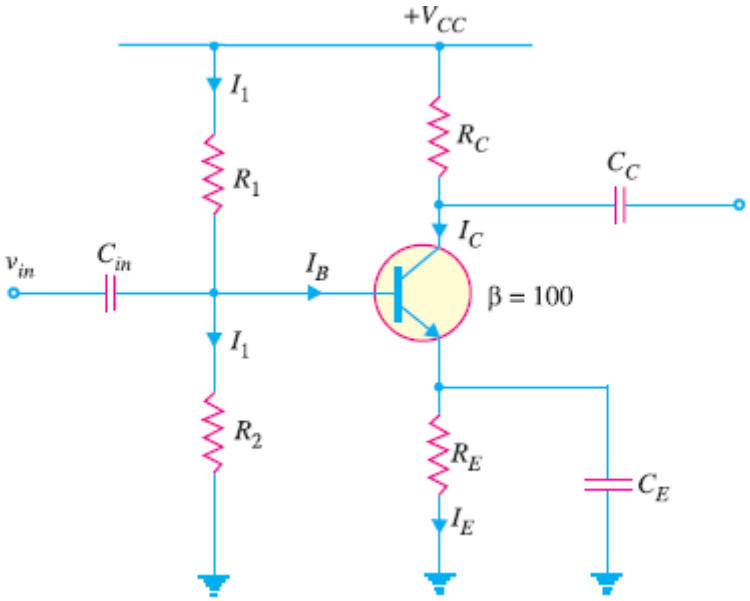


Fig. 3.2

When load R_L is connected to the amplifier, A.C. output power, $P_O = V_L^2/R_L$

Where V_L = r.m.s. value of load voltage

Example 3.1

If in Fig. 3.2; R_1 = 10 kΩ ; R_2 = 2.2 kΩ ; R_C = 3.6 kΩ ; R_E = 1.1. kΩ and V_{CC} = + 10 V, find the d.c. power drawn from the supply by the amplifier.

Solution

The current I_1 flowing through R_1 also flows through R_2 (a reasonable assumption because I_B is small).

$$I_1 = \frac{V_{CC}}{R_1 + R_2} = \frac{10V}{10k\Omega + 2.2k\Omega} = \frac{10V}{12.2k\Omega} = 0.82 \text{ mA}$$

D.C. voltage across R_2, $V_2 = I_1R_2 = 0.82 \text{ mA} \times 2.2 \text{ k}\Omega = 1.8V$

D.C. voltage across R_E, $V_E = V_2 - V_{BE} = 1.8V - 0.7V = 1.1V$

D.C. emitter current, $I_E = V_E/R_E = 1.1V/1.1\ k\Omega = 1\ mA$

$\therefore I_C \cong I_E = 1\ mA$

Total d.c current I_T drawn from the supply is

$I_T = I_C + I_1 = 1\ mA + 0.\ 82\ mA = 1.82\ mA$

$\therefore$ D.C. power drawn from the supply is

$P_{dc} = V_{CC}\ I_T = 10V \times 1.82\ mA = 18.2\ mW$

Difference between Voltage and Power Amplifiers

The distinction between voltage and power amplifiers is somewhat artificial since useful power (i.e. product of voltage and current) is always developed in the load resistance through which current flows. The difference between the two types is really one of degree; it is a question of how much voltage and how much power. A voltage amplifier is designed to achieve maximum voltage amplification.

It is, however, not important to raise the power level. On the other hand, a power amplifier is designed to obtain maximum output power.

1. Voltage amplifier. The voltage gain of an amplifier is given by:

$A_v = \beta \times \frac{R_C}{R_{in}}$

In order to achieve high voltage amplification, the following features are incorporated in such amplifiers:

(i) The transistor with high β (>100) is used in the circuit. In other words, those transistors are employed which have thin base.

(ii) The input resistance Rin of the transistor is sought to be quite low as compared to the collector load RC.

(iii) A relatively high load RC is used in the collector. To permit this condition, voltage amplifiers are always operated at low collector currents (≅1 mA). If the collector current is small, we can use large R_C in the collector circuit.

2. Power amplifier. A power amplifier is required to deliver a large amount of power and as such it has to handle large current. In order to achieve high power amplification, the following features are incorporated in such amplifiers:

(i) The size of power transistor is made considerably larger in order to dissipate the heat produced in the transistor during operation.

(ii) The base is made thicker to handle large currents. In other words, transistors with comparatively smaller β are used.

(iii) Transformer coupling is used for impedance matching.

Example 3.2

A power amplifier operated from 12V battery gives an output of 2W. Find the maximum collector current in the circuit.

Solution

Let I_C be the maximum collector current.

Power = battery voltage × collector current

or $2 = 12 \times I_C$

$\therefore I_C = \frac{2}{12} = \frac{1}{6}$ A = 166.7 mA

Chapter 4

Amplifiers with Negative Feedback

A practical amplifier has a gain of nearly one million i.e. its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce hum due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible.

The noise level in amplifiers can be reduced considerably by the use of negative feedback i.e. by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

Feedback

The process of injecting a fraction of output energy of some device back to the input is known as feedback.

The principle of feedback is probably as old as the invention of first machine but it is only some 50 years ago that feedback has come into use in connection with electronic circuits. It has been found very useful in reducing noise in amplifiers and making amplifier operation stable. Depending upon whether the feedback energy aids or opposes the input signal, there are two basic types of feedback in amplifiers viz positive feedback and negative feedback.

(i) Positive feedback. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called positive feedback. This is illustrated in Fig. 4.1. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage V_f to be in phase with the input signal V_{in}.

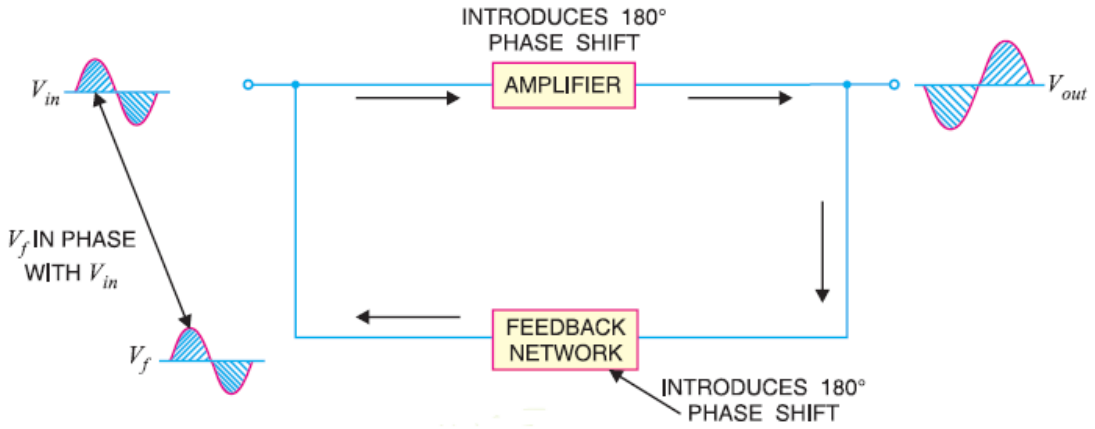


Fig. 4.1

The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers.

One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(ii) Negative feedback. When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called negative feedback. This is illustrated in Fig. 4.2. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so

designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage V_f is 180° out of phase with the input signal V_{in}.

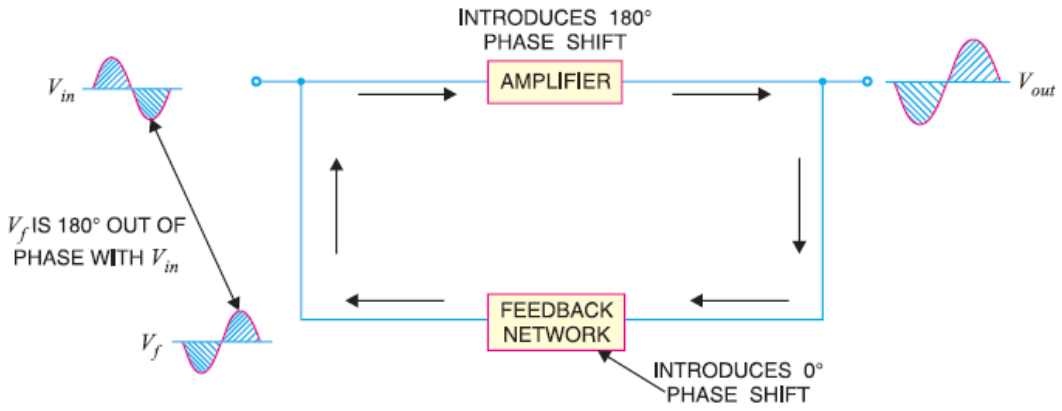


Fig. 4.2

Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

Principles of Negative Voltage Feedback In Amplifiers

A feedback amplifier has two parts viz an amplifier and a feedback circuit. The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input. Fig. 4.3 *shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative. The output of the amplifier is 10 V. The fraction mv of this output i.e. 100 mV is fedback to the input where it is applied in series with the input signal of 101 mV. As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier.

Referring to Fig. 4.3, we have,

Gain of amplifier without feedback, $A_v = \frac{10\ V}{1\ mV} = 10{,}000$

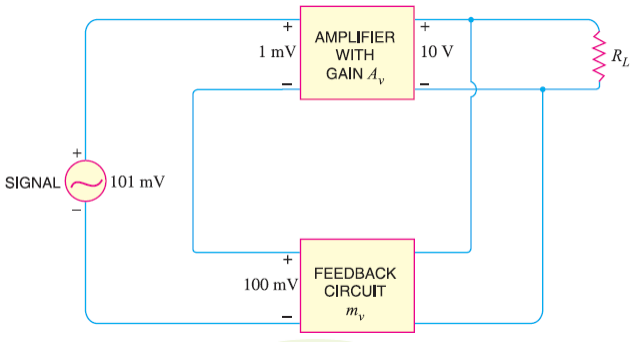


Fig. 4.3

Fraction of output voltage fedback, $m_v = \frac{100\ mV}{10\ mV} = 0.01$

Gain of amplifier with negative feedback, $A_{vf} = \frac{10\ V}{101\ mV} = 100$

The following points are worth noting:

(i) When negative voltage feedback is applied, the gain of the amplifier is **reduced. Thus, the gain of above amplifier without feedback is 10,000 whereas with negative feedback, it is only 100.

(ii) When negative voltage feedback is employed, the voltage actually applied to the amplifier is extremely small. In this case, the signal voltage is 101 mV and the negative feedback is 100 mV so that voltage applied at the input of the amplifier is only 1 mV.

(iii) In a negative voltage feedback circuit, the feedback fraction mv is always between 0 and 1.

(iv) The gain with feedback is sometimes called closed-loop gain while the gain without feedback is called open-loop gain. These terms come from the fact that amplifier and feedback circuits form a "loop". When the loop is "opened" by disconnecting the feedback circuit from the input, the amplifier's gain is A_v, the "open-loop" gain. When the loop is "closed" by connecting the feedback circuit, the gain decreases to A_{vf} , the "closed-loop" gain.

Gain of Negative Voltage Feedback Amplifier

Consider the negative voltage feedback amplifier shown in Fig. 4.4. The gain of the amplifier without feedback is A_v. Negative feedback is then applied by feeding a fraction m_v of the output voltage e0 back to amplifier input. Therefore, the actual input to the amplifier is the signal voltage eg minus feedback voltage $m_v e_0$ i.e.,

Actual input to amplifier = $e_g - m_v e_0$

The output e_0 must be equal to the input voltage $e_g - m_v e_0$ multiplied by gain A_v of the amplifier i.e., $(e_g - m_v e_0) A_v = e_0$

or $A_v e_g - A_v m_v e_0 = e_0$

or $e_0 (1 + A_v m_v) = A_v e_g$

or $\frac{e_0}{e_g} = \frac{A_v}{1+ A_v m_v}$

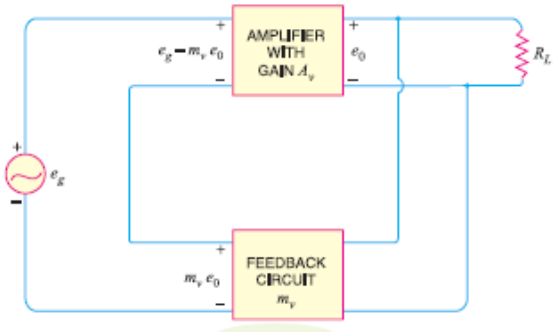


Fig. 4.4

But e_0/e_g is the voltage gain of the amplifier with feedback.

∴ Voltage gain with negative feedback is

$A_{vf} = \frac{A_v}{1+ A_v m_v}$

It may be seen that the gain of the amplifier without feedback is A_v. However, when negative voltage feedback is applied, the gain is reduced by a factor $1 + A_v m_v$. It may be noted that negative voltage feedback does not affect the current gain of the circuit.

Example 4.1

The voltage gain of an amplifier without feedback is 3000. Calculate the voltage gain of the amplifier if negative voltage feedback is introduced in the circuit. Given that feedback fraction $m_v = 0.01$.

Solution

$A_v = 3000$, $m_v = 0.01$

∴ Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v} = \frac{3000}{1 + 3000 \times 0.01} = \frac{3000}{31} = 97$$

Example 4.2

Fig. 4.3 shows the negative voltage feedback amplifier. If the gain of the amplifier without feedback is 10,000, find: (i) feedback fraction (ii) overall voltage gain (iii) output voltage if input voltage is 1 mV.

Solution

$A_v = 10{,}000$, $R_1 = 2\ k\Omega$, $R_2 = 18\ k\Omega$

(i) Feedback fraction, $m_v = \frac{R_1}{R_1 + R_2} = \frac{2}{2 + 18} = 0.1$

(ii) Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v} = \frac{10{,}000}{1 + 10{,}000 \times 0.1} = 10$$

(iii) Output voltage = A_{vf} × input voltage = 10 × 1 mV = 10 mV

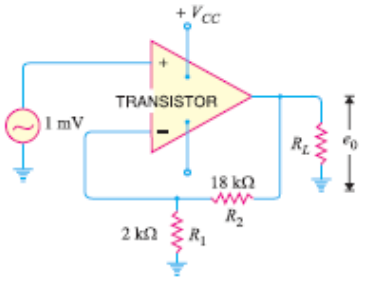


Fig. 4.3

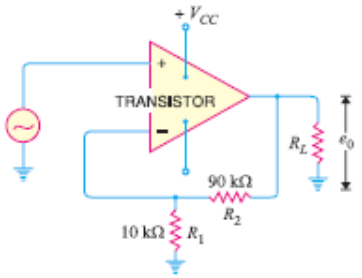


Fig. 4.4