If the output is smaller than the input, this is called the **attenuation**. *GdB* is positive for the
gain and negative for the attenuation. For example, a gain of 60 dB indicates that the output is the input multiplied by 1000 while a gain of –20 dB shows that the input is reduced (attenuated) by 10 times by the system.

THE DIGITAL VOLTMETER (DVM)

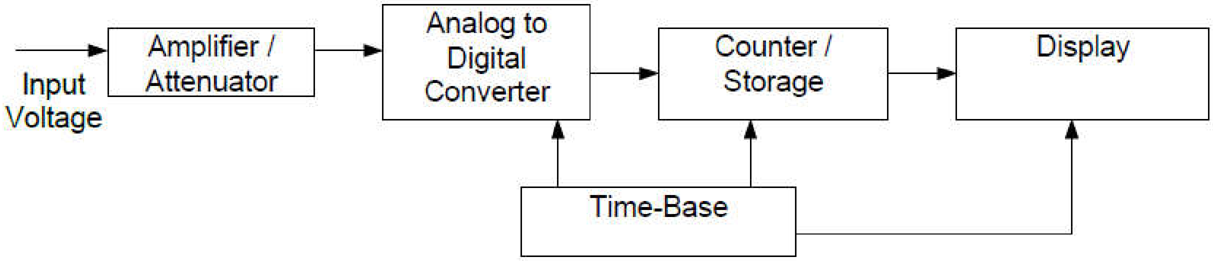
Use, Advantages and Operation

It is a device used for measuring the magnitude of DC voltages. AC voltages can be measured after
rectification and conversion to DC forms. DC/AC currents can be measured by passing them through
a known resistance (internally or externally connected) and determining the voltage developed
across the resistance (*V=IxR*).

The result of the measurement is displayed on a digital readout in numeric form as in the case of the counters. Most DVMs use the principle of time period measurement. Hence, the voltage is converted into a time interval "*t*" first. No frequency division is involved. Input range selection automatically changes the position of the decimal point on the display. The unit of measure is also highlighted in most devices to simplify the reading and annotation. The DVM has several advantages over the analog type voltmeters as:

 Input range: from 1.000 000 V to 1,000.000 V with automatic range selection.
 Absolute accuracy: as high as 0.005% of the reading.
 Stability
 Resolution: 1 part in 106 (1 V can be read in 1 V range).
 Input impedance: *Ri* 10 M ; *Ci* 40 pF
 Calibration: internal standard derived from a stabilized reference voltage source.
 Output signals: measured voltage is available as a BCD (binary coded decimal) code and can
be send to computers or printers.

It is composed of an amplifier/attenuator, an analog to digital converter, storage, display and timing circuits. There is also a power supply to provide the electrical power to run electronic components. The circuit components except the analog to digital converter circuits are similar to the ones used in electronic counters. The input range selection can be manually switched between ranges to get most accurate reading or it can be auto ranging that switches between ranges automatically for best reading.



A simplified diagram for a digital voltmeter

The Analog to Digital Converter (ADC) – Sample and Hold

The analog to digital converter contains a sample and hold circuit, and conversion circuits. The
sample and hold is composed of an electronic switch and a capacitor. The switch turns on and off at regular intervals. The capacitor charges and assumes the level of the input voltage as the switch is on. It holds the charge (hence the level of the input voltage) as the switch is off. The unity-gain buffer eliminates the loading of the capacitor by proceeding analog to digital converter circuitry.shows a simplified diagram with the input and output waveforms of the circuit.

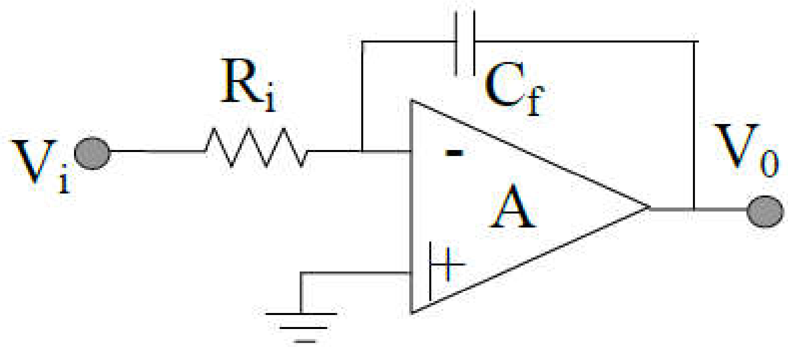
Digitization of Analog Signals

The input of the sample and hold circuit is a continuous time analog signal that can take any value any time. The output is a discrete time signal that can take any value but only at certain times. This signal can't be processed by a digital circuit unless it is converted into a digital code.
The analog input signal is continuous in time and it can take any value at any time. This is converted to a discrete-time signal that can accept any value but at certain times. The next stage is to divide the amplitude range into discrete steps as well by a process called the quantization. The figure exemplifies the principles for a 4-bit converter in which the dynamic range (the maximum peak to peak amplitude that the input signal can attain) is divided into 24 – 1 = 15 steps. A binary code (or binary coded decimal – BCD) is assigned for each level from 0000 to 1111 (1001 for BCD).

Integrating Type Analog to Digital Converters

The Basic Integrator

This type of converters generates a time interval

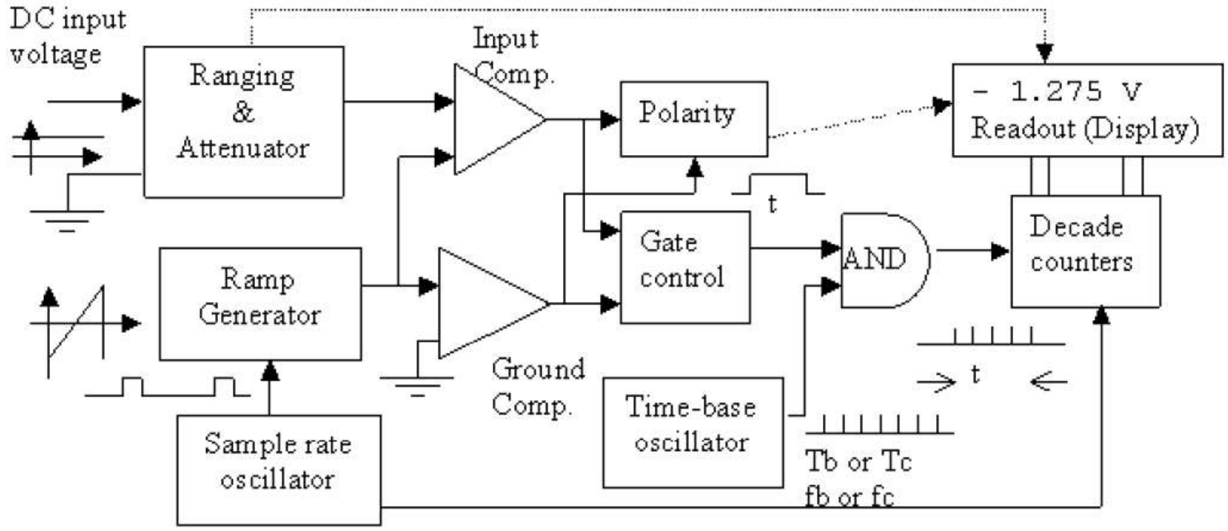


proportional to the input voltage. Then, this interval is measured and displayed using methods that were discussed in the counters section previously. The key circuit element is the integrator that generates an output that is related to the integral of the input. The basic integrator circuit is shown in Figure 4.45. It is similar to the inverting amplifier with the feedback resistor replaced by a capacitor. The input voltage V_i causes a current $I_i = {V_i}/{R_i}$ to flow through the capacitor C_f that generates an output voltage $V_0 = -\frac{1}{C_f}\int_0^t I_i dt - V_{co}$ since the inverting terminal of the op-amp is at virtual ground provided that the op-amp is not saturated. Hence, the output can be expressed as $V_0 = -\frac{1}{C_f R_i}\int_0^t V_i dt - V_{co}$. V_0 will decrease (or increase if V_i is negative) at a rate of $\frac{V_i}{R_i C_f}$

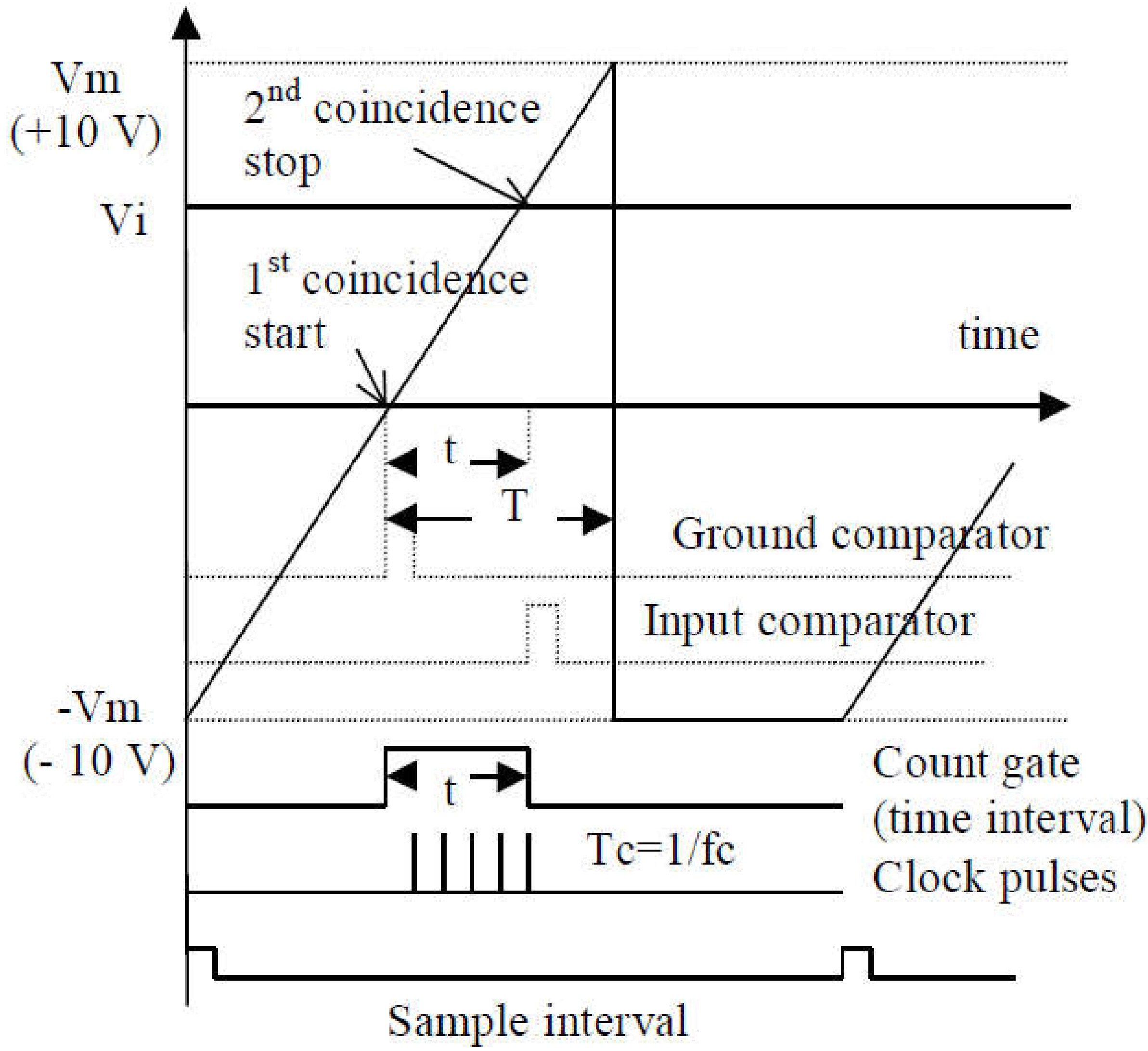
Functional Block Diagram of Ramp Type (Single Slope) DVM

Functional block diagram of a positive ramp type DVM is shown in Figure 4.46 The timing diagram is given in Fig. It has two major sections as the voltage to time conversion unit and time measurement unit. The conversion unit has a ramp generator that operates under the control of the sample rate oscillator, two comparators and a gate control circuitry. The internally generated ramp voltage is applied to two comparators. The first comparator compares the ramp voltage into the input signal and produces a pulse output as the coincidence is achieved (as the ramp voltage becomes larger than the input voltage). The second comparator compares the ramp to the ground voltage (0 volt) and produces an output pulse at the coincidence.

The input voltage to the first comparator must be between □ *Vm*. The ranging and attenuation section scales the DC input voltage so that it will be within the dynamic range. The decimal point in the output display automatically positioned by the ranging circuits.



Simplified block diagram of a single-ramp type digital voltmeter



Timing diagram for a single-ramp digital voltmeter

The outputs of the two comparators derive the gate control circuit that generates and output
pulse that starts with the first coincidence pulse and ends with the second.
Thus, the duration of the pulse "*t*" can be computed from the triangles as

$$\frac{V_i}{V_m} = \frac{t}{T} \Rightarrow t = \frac{T}{V_m} V_i$$

Hence, the voltage to time conversion is done yielding "t" to V_i with T and V_m constant.

Number of time intervals (clock pulses) counted during this interval become:

$$N = t * f_c = V_i \frac{T * f_c}{V_m}$$

For the ramp voltage with fixed slope and time base that runs at fixed rate (*fc*) *N* is directly proportional to *Vi*. The multiplier *T.fc/Vm* is set to a constant factor of 10. The polarity of the voltage is indicated if it is "-". With no indication, it is understood that the polarity is "+". The polarity is detected by the polarity circuit with the help of comparator pulses. For positive slope ramp type voltmeter, the first coincidence of the ramp is with the ground voltage if the input is positive. With a negative input voltage however, the first coincidence will be with the input voltage. The display stays for sometimes (around three seconds) and then it is refreshed by the sample rate oscillator. A trigger pulse is applied to the ramp generator to initiate a new ramp. Meanwhile a reset (initialize) pulse is applied to the decade counters to clear the previously stored code.

The display indicates the polarity as well as the numbers in decimal and a decimal point. The first digit contains the polarity sign and the number displayed can be only "1" or "0" for most voltmeters. Therefore, this is called "half" digit. Hence, a three and a half digit display can have up to 1999 and a four and a half digit one can go up to 19999.

Q meter:

A **Q meter** is a piece of equipment used in the testing of radio frequency circuits. A Q meter measures Q, the quality factor of a circuit, which expresses how much energy is dissipated per cycle in a non-ideal reactive circuit:

$$Q = 2\pi \times \frac{\text{Peak Energy Stored}}{\text{Energy dissipated per cycle}}.$$

This expression applies to an RF and microwave filter, bandpass LC filter, or any resonator. It also can be applied to an inductor or capacitor at a chosen frequency. For inductors

$$Q = \frac{X_L}{R} = \frac{\omega L}{R}$$

Where XLis the reactance of the inductor, L is the inductance,W is the angular frequency and R is the resistance of the inductor. The resistance represents the loss in the inductor, mainly due to the resistance of the wire.Q meter works on the principle of series resonance. For LC band pass circuits and filters:

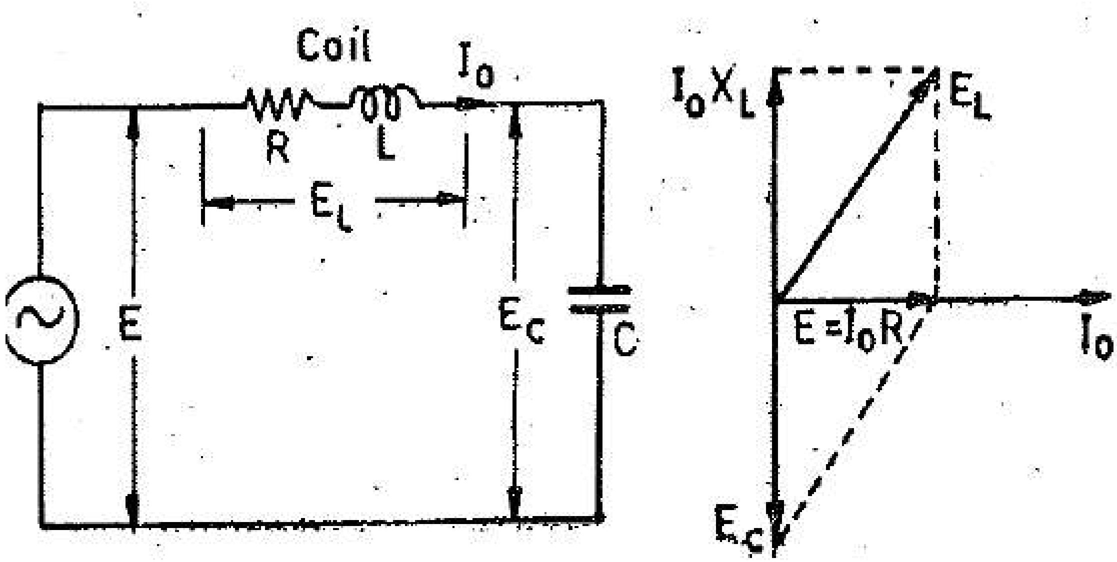
$$Q = \frac{F}{BW}$$

Where F is the resonant frequency (center frequency) and BW is the filter bandwidth. In a band pass filter using an LC resonant circuit, when the loss (resistance) of the inductor increases, its Q is reduced, and so the bandwidth of the filter is increased. In a coaxial cavity filter, there are no inductors and capacitors, but the cavity has an equivalent LC model with losses (resistance) and the Q factor can be applied as well.

OPERATION:

Internally, a minimal Q meter consists of a tuneable RF generator with a very low impedance output and a detector with a very high impedance input. There is usually provision to add a calibrated amount of high Q capacitance across the component under test to allow inductors to be measured in isolation. The generator is effectively placed in series with the tuned circuit formed by the components under test, and having negligible output resistance, does not materially affect the Q factor, while the detector measures the voltage developed across one element (usually the capacitor) and being high impedance in shunt does not affect the Q factor significantly either. The ratio of the developed RF voltage to the applied RF current, coupled with knowledge of the reactive impedance from the resonant frequency, and the source impedance, allows the Q factor to be directly read by scaling the detected voltage.

WORKING PRINCIPLE:



Principle of Working. The working of this useful laboratory i based upon the well-known chara a resonant series R, L, C circuit. F shows a coil of resistance R and i in series with a capacitor C.

At resonant frequency f_0 w

$$X_C = X_L$$

resonant frequency $f_0 = \frac{1}{2\pi\sqrt{LC}}$ and current $I_0 = \frac{E}{R}$.

The phasor diagram is shown in Fig. 23·11 (b).

Voltage across capacitor, $E_C = I_0 X_C = I_0 X_L = I_0 \omega_0 L$

Input voltage $E = I_0 R$ $\therefore \frac{E_C}{E} = \frac{I_0 \omega_0 L}{I_0 R} = \frac{\omega_0 L}{R} = Q$

or $$E_C = QE$$ ...

Thus the input voltage E is magnified Q times.

If the input voltage E is kept constant, the voltage appearing across the capacitor is E and a voltmeter connected across the capacitor can be calibrated to read the value of Q direc