



# L3G4200D

## MEMS motion sensor: ultra-stable three-axis digital output gyroscope

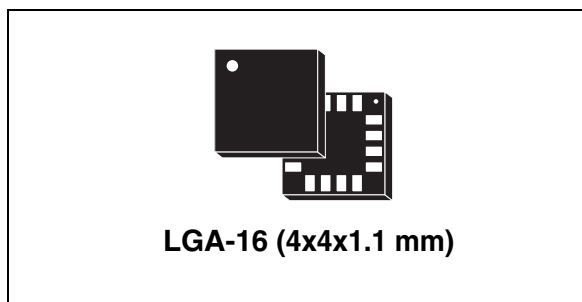
Preliminary data

### Features

- Three selectable full scales (250/500/2000 dps)
- I<sup>2</sup>C/SPI digital output interface
- 16 bit-rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low- and high-pass filters with user-selectable bandwidth
- Ultra-stable over temperature and time
- Wide supply voltage: 2.4 V to 3.6 V
- Low voltage-compatible IOs (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- Embedded FIFO
- High shock survivability
- Extended operating temperature range (-40 °C to +85 °C)
- ECOPACK<sup>®</sup> RoHS and "Green" compliant

### Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics



### Description

The L3G4200D is a low-power three-axis angular rate sensor able to provide unprecedented stability of zero rate level and sensitivity over temperature and time. It includes a sensing element and an IC interface capable of providing the measured angular rate to the external world through a digital interface (I<sup>2</sup>C/SPI).

The sensing element is manufactured using a dedicated micro-machining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3G4200D has a full scale of  $\pm 250/\pm 500/\pm 2000$  dps and is capable of measuring rates with a user-selectable bandwidth.

The L3G4200D is available in a plastic land grid array (LGA) package and can operate within a temperature range of -40 °C to +85 °C.

Table 1. Device summary

| Order code | Temperature range (°C) | Package             | Packing       |
|------------|------------------------|---------------------|---------------|
| L3G4200D   | -40 to +85             | LGA-16 (4x4x1.1 mm) | Tray          |
| L3G4200DTR | -40 to +85             | LGA-16 (4x4x1.1 mm) | Tape and reel |

# Contents

|          |  |           |
|----------|--|-----------|
| <b>1</b> | <b>Block diagram and pin description</b>         | <b>7</b>  |
| 1.1      | Pin description                                  | 7         |
| <b>2</b> | <b>Mechanical and electrical characteristics</b> | <b>10</b> |
| 2.1      | Mechanical characteristics                       | 10        |
| 2.2      | Electrical characteristics                       | 11        |
| 2.3      | Temperature sensor characteristics               | 11        |
| 2.4      | Communication interface characteristics          | 12        |
| 2.4.1    | SPI - serial peripheral interface                | 12        |
| 2.4.2    | I2C - inter IC control interface                 | 13        |
| 2.5      | Absolute maximum ratings                         | 14        |
| 2.6      | Terminology                                      | 15        |
| 2.6.1    | Sensitivity                                      | 15        |
| 2.6.2    | Zero-rate level                                  | 15        |
| 2.6.3    | Self-test  | 15        |
| 2.7      | Soldering information                            | 15        |
| <b>3</b> | <b>Main digital blocks</b>                       | <b>16</b> |
| 3.1      | Block diagram                                    | 16        |
| 3.2      | FIFO   | 16        |
| 3.2.1    | Bypass mode                                      | 16        |
| 3.2.2    | FIFO mode  | 17        |
| 3.2.3    | Stream mode                                      | 17        |
| 3.2.4    | Bypass-to-stream mode                            | 18        |
| 3.2.5    | Stream-to-FIFO mode                              | 19        |
| 3.2.6    | Retrieve data from FIFO                          | 19        |
| <b>4</b> | <b>Application hints</b>                         | <b>20</b> |
| <b>5</b> | <b>Digital interfaces</b>                        | <b>21</b> |
| 5.1      | I2C serial interface                             | 21        |
| 5.1.1    | I2C operation                                    | 22        |
| 5.2      | SPI bus interface                                | 23        |
| 5.2.1    | SPI read   | 24        |

|          |                                |           |
|----------|--------------------------------|-----------|
| 5.2.2    | SPI write                      | 25        |
| 5.2.3    | SPI read in 3-wire mode        | 26        |
| <b>6</b> | <b>Output register mapping</b> | <b>27</b> |
| <b>7</b> | <b>Register description</b>    | <b>29</b> |
| 7.1      | WHO_AM_I (0Fh)                 | 29        |
| 7.2      | CTRL_REG1 (20h)                | 29        |
| 7.3      | CTRL_REG2 (21h)                | 30        |
| 7.4      | CTRL_REG3 (22h)                | 31        |
| 7.5      | CTRL_REG4 (23h)                | 32        |
| 7.6      | CTRL_REG5 (24h)                | 32        |
| 7.7      | REFERENCE/DATACAPTURE (25h)    | 34        |
| 7.8      | OUT_TEMP (26h)                 | 34        |
| 7.9      | STATUS_REG (27h)               | 34        |
| 7.10     | OUT_X_L (28h), OUT_X_H (29h)   | 35        |
| 7.11     | OUT_Y_L (2Ah), OUT_Y_H (2Bh)   | 35        |
| 7.12     | OUT_Z_L (2Ch), OUT_Z_H (2Dh)   | 35        |
| 7.13     | FIFO_CTRL_REG (2Eh)            | 35        |
| 7.14     | FIFO_SRC_REG (2Fh)             | 35        |
| 7.15     | INT1_CFG (30h)                 | 36        |
| 7.16     | INT1_SRC (31h)                 | 36        |
| 7.17     | INT1_THS_XH (32h)              | 37        |
| 7.18     | INT1_THS_XL (33h)              | 37        |
| 7.19     | INT1_THS_YH (34h)              | 37        |
| 7.20     | INT1_THS_YL (35h)              | 38        |
| 7.21     | INT1_THS_ZH (36h)              | 38        |
| 7.22     | INT1_THS_ZL (37h)              | 38        |
| 7.23     | INT1_DURATION (38h)            | 38        |
| <b>8</b> | <b>Package information</b>     | <b>40</b> |
| <b>9</b> | <b>Revision history</b>        | <b>41</b> |

## List of tables

|           |   |    |
|-----------|---|----|
| Table 1.  | Device summary . . . . .  | 1  |
| Table 2.  | Pin description . . . . .   | 8  |
| Table 3.  | Filter values . . . . .   | 9  |
| Table 4.  | Mechanical characteristics @ Vdd = 3.0 V, T = 25 °C, unless otherwise noted . . . . .   | 10 |
| Table 5.  | Electrical characteristics @ Vdd =3.0 V, T=25 °C, unless otherwise noted . . . . .      | 11 |
| Table 6.  | Temp. sensor characteristics @ Vdd =3.0 V, T=25 °C, unless otherwise noted . . . . .    | 11 |
| Table 7.  | SPI slave timing values. . . . .  | 12 |
| Table 8.  | I2C slave timing values. . . . .  | 13 |
| Table 9.  | Absolute maximum ratings . . . . .  | 14 |
| Table 10. | PLL low-pass filter component values . . . . .  | 20 |
| Table 11. | Serial interface pin description . . . . .  | 21 |
| Table 12. | I2C terminology. . . . .  | 21 |
| Table 13. | SAD+read/write patterns. . . . .  | 22 |
| Table 14. | Transfer when master is writing one byte to slave . . . . .                             | 22 |
| Table 15. | Transfer when master is writing multiple bytes to slave . . . . .                       | 23 |
| Table 16. | Transfer when master is receiving (reading) one byte of data from slave . . . . .       | 23 |
| Table 17. | Transfer when master is receiving (reading) multiple bytes of data from slave . . . . . | 23 |
| Table 18. | Register address map. . . . .   | 27 |
| Table 19. | WHO_AM_I register . . . . .   | 29 |
| Table 20. | CTRL_REG1 register . . . . .  | 29 |
| Table 21. | CTRL_REG1 description . . . . .   | 29 |
| Table 22. | DR and BW configuration setting . . . . .   | 29 |
| Table 23. | Power mode selection configuration. . . . .   | 30 |
| Table 24. | CTRL_REG2 register . . . . .  | 30 |
| Table 25. | CTRL_REG2 description . . . . .   | 30 |
| Table 26. | High pass filter mode configuration . . . . .   | 31 |
| Table 27. | High pass filter cut off frequency configuration [Hz] . . . . .                         | 31 |
| Table 28. | CTRL_REG1 register . . . . .  | 31 |
| Table 29. | CTRL_REG3 description . . . . .   | 31 |
| Table 30. | CTRL_REG4 register . . . . .  | 32 |
| Table 31. | CTRL_REG4 description . . . . .   | 32 |
| Table 32. | Self test mode configuration . . . . .  | 32 |
| Table 33. | CTRL_REG5 register . . . . .  | 32 |
| Table 34. | CTRL_REG5 description . . . . .   | 32 |
| Table 35. | Out_Sel configuration setting . . . . .   | 33 |
| Table 36. | INT_SEL configuration setting . . . . .   | 33 |
| Table 37. | REFERENCE register. . . . .   | 34 |
| Table 38. | REFERENCE register description . . . . .  | 34 |
| Table 39. | OUT_TEMP register . . . . .   | 34 |
| Table 40. | OUT_TEMP register description. . . . .  | 34 |
| Table 41. | STATUS_REG register. . . . .  | 34 |
| Table 42. | STATUS_REG description . . . . .  | 34 |
| Table 43. | REFERENCE register. . . . .   | 35 |
| Table 44. | REFERENCE register description . . . . .  | 35 |
| Table 45. | FIFO mode configuration . . . . .   | 35 |
| Table 46. | FIFO_SRC register. . . . .  | 35 |
| Table 47. | FIFO_SRC register description. . . . .  | 35 |
| Table 48. | INT1_CFG register . . . . .   | 36 |

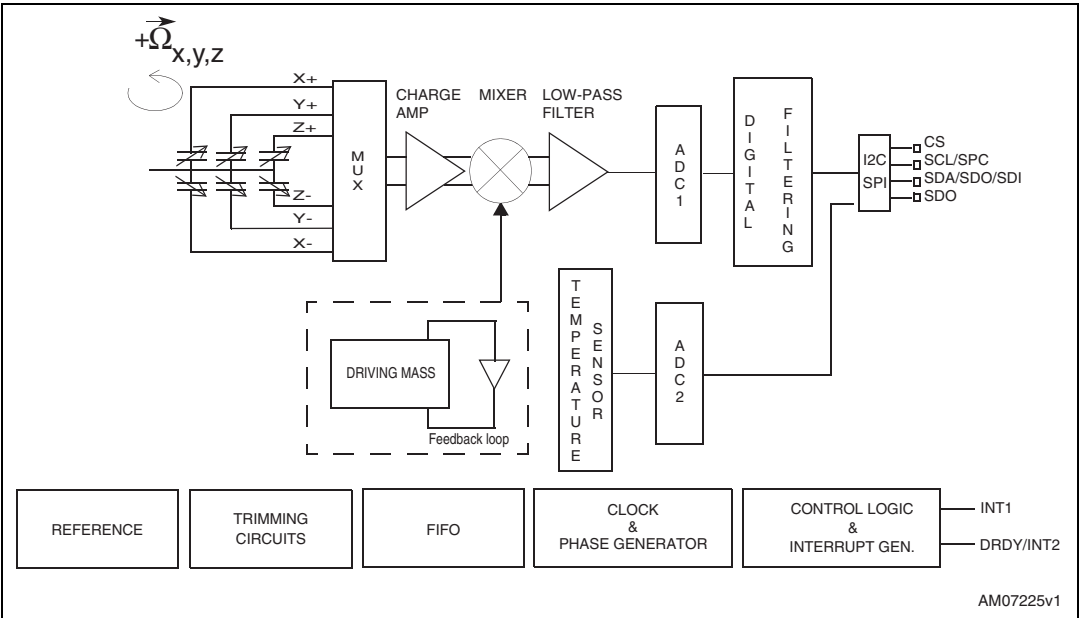
|           |                                 |    |
|-----------|---------------------------------|----|
| Table 49. | INT1_CFG description .....      | 36 |
| Table 50. | INT1_SRC register .....         | 36 |
| Table 51. | INT1_SRC description .....      | 37 |
| Table 52. | INT1_THS_XH register .....      | 37 |
| Table 53. | INT1_THS_XH description .....   | 37 |
| Table 54. | INT1_THS_XL register .....      | 37 |
| Table 55. | INT1_THS_XL description .....   | 37 |
| Table 56. | INT1_THS_YH register .....      | 37 |
| Table 57. | INT1_THS_YH description .....   | 37 |
| Table 58. | INT1_THS_YL register .....      | 38 |
| Table 59. | INT1_THS_YL description .....   | 38 |
| Table 60. | INT1_THS_ZH register .....      | 38 |
| Table 61. | INT1_THS_ZH description .....   | 38 |
| Table 62. | INT1_THS_ZL register .....      | 38 |
| Table 63. | INT1_THS_ZL description .....   | 38 |
| Table 64. | INT1_DURATION register .....    | 38 |
| Table 65. | INT1_DURATION description ..... | 38 |
| Table 66. | Document revision history ..... | 41 |

## List of figures

|            |   |    |
|------------|---|----|
| Figure 1.  | Block diagram . . . . .   | 7  |
| Figure 2.  | Pin connection . . . . .  | 7  |
| Figure 3.  | L3G4200D external low-pass filter values . . . . .                      | 8  |
| Figure 4.  | SPI slave timing diagram . . . . .                                      | 12 |
| Figure 5.  | I2C slave timing diagram . . . . .                                      | 13 |
| Figure 6.  | Block diagram . . . . .   | 16 |
| Figure 7.  | Bypass mode . . . . .   | 17 |
| Figure 8.  | FIFO mode . . . . .   | 17 |
| Figure 9.  | Stream mode . . . . .   | 18 |
| Figure 10. | Bypass-to-stream mode . . . . .   | 18 |
| Figure 11. | Trigger stream mode . . . . .   | 19 |
| Figure 12. | L3G4200D electrical connections and external component values . . . . . | 20 |
| Figure 13. | Read and write protocol . . . . .                                       | 24 |
| Figure 14. | SPI read protocol . . . . .   | 24 |
| Figure 15. | Multiple byte SPI read protocol (2-byte example). . . . .               | 25 |
| Figure 16. | SPI write protocol . . . . .  | 25 |
| Figure 17. | Multiple byte SPI write protocol (2-byte example). . . . .              | 26 |
| Figure 18. | SPI read protocol in 3-wire mode . . . . .                              | 26 |
| Figure 19. | INT1_Sel and Out_Sel configuration block diagram . . . . .              | 33 |
| Figure 20. | Wait disabled . . . . .   | 39 |
| Figure 21. | Wait enabled. . . . .   | 39 |
| Figure 22. | LGA-16: mechanical data and package dimensions . . . . .                | 40 |

# 1 Block diagram and pin description

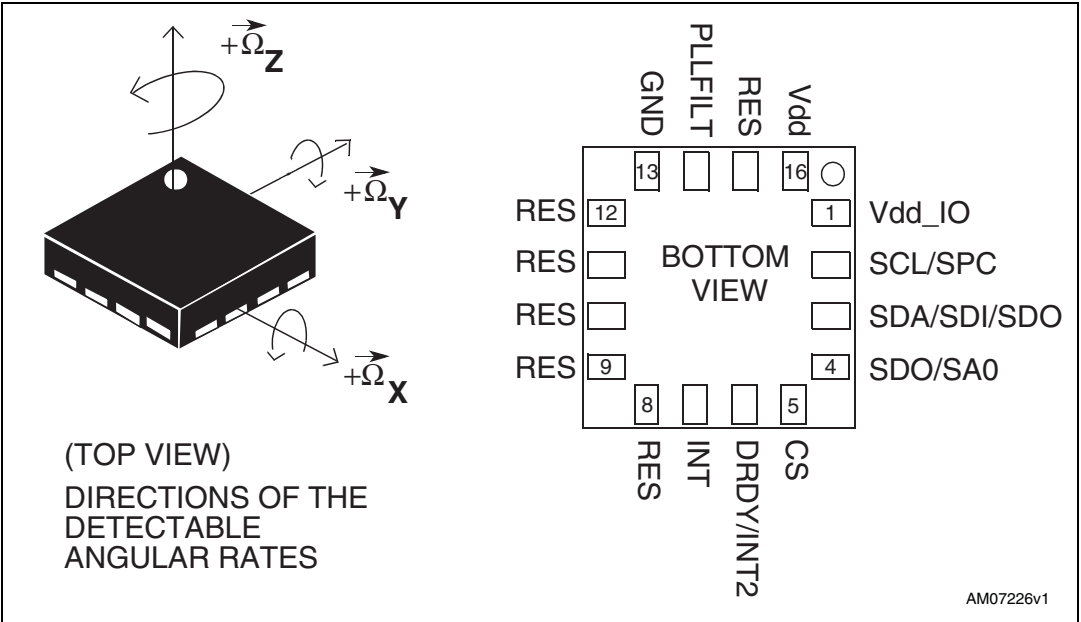
Figure 1. Block diagram



The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

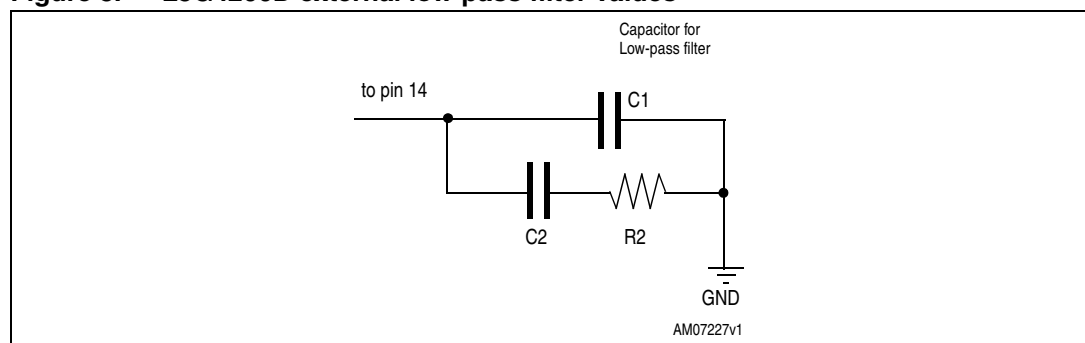
## 1.1 Pin description

Figure 2. Pin connection



**Table 2. Pin description**

| Pin# | Name              | Function  |
|------|-------------------|---|
| 1    | Vdd_IO            | Power supply for I/O pins   |
| 2    | SCL<br>SPC        | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)  |
| 3    | SDA<br>SDI<br>SDO | I <sup>2</sup> C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)  |
| 4    | SDO<br>SA0        | SPI serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address (SA0)  |
| 5    | CS                | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1:SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) |
| 6    | DRDY/INT2         | Data ready/FIFO interrupt   |
| 7    | INT1              | Programmable interrupt  |
| 8    | Reserved          | Connect to GND  |
| 9    | Reserved          | Connect to GND  |
| 10   | Reserved          | Connect to GND  |
| 11   | Reserved          | Connect to GND  |
| 12   | Reserved          | Connect to GND  |
| 13   | GND               | 0 V supply  |
| 14   | PLLFILT           | Phase-locked loop filter (see <a href="#">Figure 3</a> )  |
| 15   | Reserved          | Connect to Vdd  |
| 16   | Vdd               | Power supply  |

**Figure 3. L3G4200D external low-pass filter values (a)**

a. Pin 14 PLLFILT maximum voltage level is equal to Vdd.



**Table 3. Filter values**

| Parameter | Typical value |
|-----------|---------------|
| C1        | 10 nF         |
| C2        | 470 nF        |
| R2        | 10 k $\Omega$ |

## 2 Mechanical and electrical characteristics

### 2.1 Mechanical characteristics

**Table 4. Mechanical characteristics @ Vdd = 3.0 V, T = 25 °C, unless otherwise noted<sup>(1)</sup>**

| Symbol | Parameter   | Test condition         | Min. | Typ. <sup>(2)</sup> | Max. | Unit             |
|--------|---|------------------------|------|---------------------|------|------------------|
| FS     | Measurement range                                     | User-selectable        |      | ±250                |      | dps              |
|        |   |                        |      | ±500                |      |                  |
|        |   |                        |      | ±2000               |      |                  |
| So     | Sensitivity   | FS = 250 dps           |      | 8.75                |      | mdps/digit       |
|        |   | FS = 500 dps           |      | 17.50               |      |                  |
|        |   | FS = 2000 dps          |      | 70                  |      |                  |
| SoDr   | Sensitivity change vs. temperature                    | From -40 °C to +85 °C  |      | ±2                  |      | %                |
| DVoff  | Digital zero-rate level                               | FS = 250 dps           |      | ±10                 |      | dps              |
|        |   | FS = 500 dps           |      | ±15                 |      |                  |
|        |   | FS = 2000 dps          |      | ±75                 |      |                  |
| OffDr  | Zero-rate level change vs. temperature <sup>(3)</sup> | FS = 250 dps           |      | ±0.03               |      | dps/°C           |
|        |   | FS = 2000 dps          |      | ±0.04               |      | dps/°C           |
| NL     | Non linearity <sup>(4)</sup>                          | Best fit straight line |      | 0.2                 |      | % FS             |
| DST    | Self-test output change                               | FS = 250 dps           |      | 130                 |      | dps              |
|        |   | FS = 500 dps           |      | 200                 |      |                  |
|        |   | FS = 2000 dps          |      | 530                 |      |                  |
| Rn     | Rate noise density                                    | BW = 50 Hz             |      | 0.03                |      | dps/<br>sqrt(Hz) |
| ODR    | Digital output data rate                              |                        |      | 100/200/<br>400/800 |      | Hz               |
| Top    | Operating temperature range                           |                        | -40  |                     | +85  | °C               |

1. The product is factory calibrated at 3.0 V. The operational power supply range is specified in [Table 5](#).

2. Typical specifications are not guaranteed.

3. Min/max values have been estimated based on the measurements of the current gyros in production.

4. Guaranteed by design.

## 2.2 Electrical characteristics

**Table 5. Electrical characteristics @ Vdd =3.0 V, T=25 °C, unless otherwise noted<sup>(1)</sup>**

| Symbol | Parameter                                   | Test condition                  | Min. | Typ. <sup>(2)</sup> | Max.    | Unit |
|--------|---|---------------------------------|------|---------------------|---------|------|
| Vdd    | Supply voltage                              |                                 | 2.4  | 3.0                 | 3.6     | V    |
| Vdd_IO | I/O pins supply voltage <sup>(3)</sup>      |                                 | 1.71 |                     | Vdd+0.1 | V    |
| Idd    | Supply current                              |                                 |      | 6.1                 |         | mA   |
| IddSL  | Supply current in sleep mode <sup>(4)</sup> | Selectable by digital interface |      | 1.5                 |         | mA   |
| IddPdn | Supply current in power-down mode           | Selectable by digital interface |      | 5                   |         | μA   |
| Top    | Operating temperature range                 |                                 | -40  |                     | +85     | °C   |

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time compared to power-down mode.

## 2.3 Temperature sensor characteristics

**Table 6. Temp. sensor characteristics @ Vdd =3.0 V, T=25 °C, unless otherwise noted<sup>(1)</sup>**

| Symbol | Parameter  | Test condition | Min. | Typ. <sup>(2)</sup> | Max. | Unit     |
|--------|--|----------------|------|---------------------|------|----------|
| TSDr   | Temperature sensor output change vs. temperature |                |      | -1                  |      | °C/digit |
| TODR   | Temperature refresh rate                         |                |      | 1                   |      | Hz       |
| Top    | Operating temperature range                      |                | -40  |                     | +85  | °C       |

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

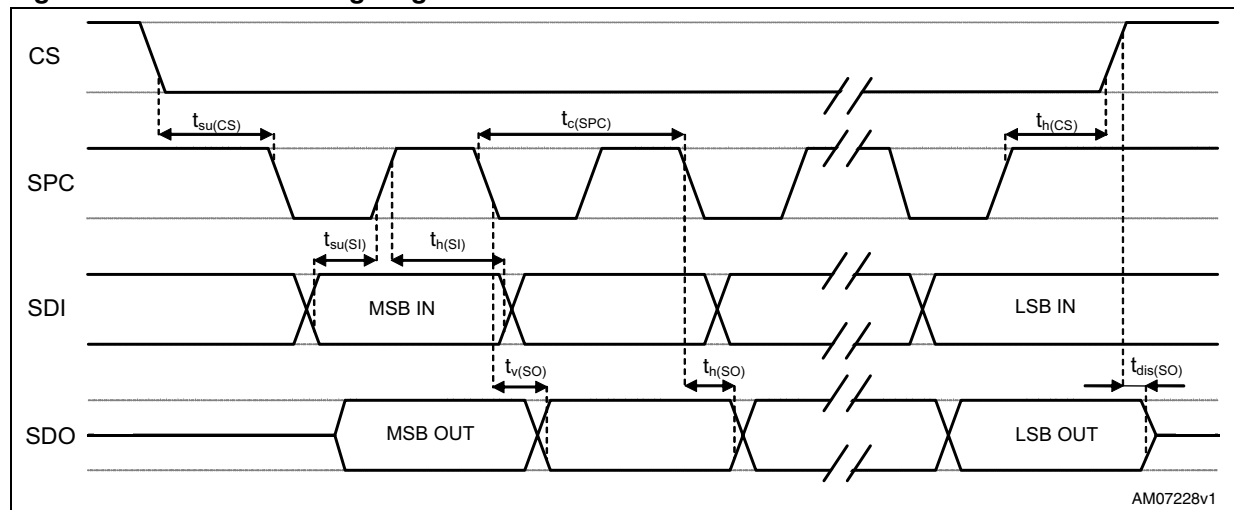
Subject to general operating conditions for Vdd and Top.

**Table 7. SPI slave timing values**

| Symbol   | Parameter               | Value <sup>(1)</sup> |      | Unit |
|----------|-------------------------|----------------------|------|------|
|          |                         | Min.                 | Max. |      |
| tc(SPC)  | SPI clock cycle         | 100                  |      | ns   |
| fc(SPC)  | SPI clock frequency     |                      | 10   | MHz  |
| tsu(CS)  | CS setup time           | 5                    |      | ns   |
| th(CS)   | CS hold time            | 8                    |      |      |
| tsu(SI)  | SDI input setup time    | 5                    |      |      |
| th(SI)   | SDI input hold time     | 15                   |      |      |
| tv(SO)   | SDO valid output time   |                      | 50   |      |
| th(SO)   | SDO output hold time    | 6                    |      |      |
| tdis(SO) | SDO output disable time |                      | 50   |      |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results; not tested in production.

**Figure 4. SPI slave timing diagram<sup>(b)</sup>**



b. Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both input and output ports.

## 2.4.2 I<sup>2</sup>C - inter IC control interface

Subject to general operating conditions for Vdd and Top.

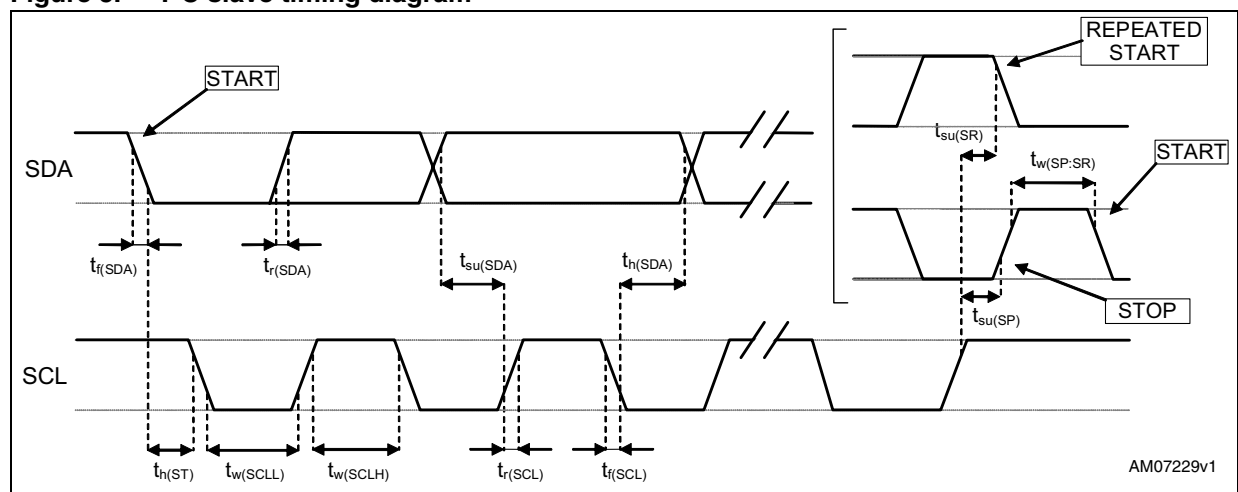
**Table 8. I<sup>2</sup>C slave timing values**

| Symbol                  | Parameter                                      | I <sup>2</sup> C standard mode <sup>(1)</sup> |      | I <sup>2</sup> C fast mode <sup>(1)</sup> |     | Unit    |
|-------------------------|--|---|------|---|-----|---------|
|                         |  | Min   | Max  | Min                                       | Max |         |
| $f_{(SCL)}$             | SCL clock frequency                            | 0   | 100  | 0   | 400 | kHz     |
| $t_{w(SCLL)}$           | SCL clock low time                             | 4.7   |      | 1.3                                       |     | $\mu$ s |
| $t_{w(SCLH)}$           | SCL clock high time                            | 4.0   |      | 0.6                                       |     |         |
| $t_{su(SDA)}$           | SDA setup time                                 | 250   |      | 100                                       |     | ns      |
| $t_{h(SDA)}$            | SDA data hold time                             | 0   | 3.45 | 0   | 0.9 | $\mu$ s |
| $t_{r(SDA)} t_{r(SCL)}$ | SDA and SCL rise time                          |   | 1000 | $20 + 0.1C_b^{(2)}$                       | 300 | ns      |
| $t_{f(SDA)} t_{f(SCL)}$ | SDA and SCL fall time                          |   | 300  | $20 + 0.1C_b^{(2)}$                       | 300 |         |
| $t_{h(ST)}$             | START condition hold time                      | 4   |      | 0.6                                       |     | $\mu$ s |
| $t_{su(SR)}$            | Repeated START condition setup time            | 4.7   |      | 0.6                                       |     |         |
| $t_{su(SP)}$            | STOP condition setup time                      | 4   |      | 0.6                                       |     |         |
| $t_{w(SP:SR)}$          | Bus free time between STOP and START condition | 4.7   |      | 1.3                                       |     |         |

1. Data based on standard I<sup>2</sup>C protocol requirement; not tested in production.

2.  $C_b$  = total capacitance of one bus line, in pF.

**Figure 5. I<sup>2</sup>C slave timing diagram <sup>(c)</sup>**



c. Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both ports.

## 2.5 Absolute maximum ratings

Any stress above that listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 9. Absolute maximum ratings**

| Symbol           | Ratings                            | Maximum value | Unit     |
|------------------|------------------------------------|---------------|----------|
| Vdd              | Supply voltage                     | -0.3 to 4.8   | V        |
| T <sub>STG</sub> | Storage temperature range          | -40 to +125   | °C       |
| Sg               | Acceleration <i>g</i> for 0.1 ms   | 10,000        | <i>g</i> |
| ESD              | Electrostatic discharge protection | 2 (HBM)       | kV       |



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part



This is an ESD sensitive device, improper handling can cause permanent damage to the part

## 2.6 Terminology

### 2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

### 2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and, therefore, the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

### 2.6.3 Stability over temperature and time

Thanks to the unique single driving mass approach and optimized design, ST gyroscopes are able to guarantee a perfect match of the MEMS mechanical mass and the ASIC interface, and deliver unprecedented levels of stability over temperature and time.

With Zero rate level and sensitivity performances, up to ten times better than equivalent products now available on the market, L3G4200D allows the user to avoid any further compensation and calibration during production for faster time to market, easy application implementation, higher performances and cost saving.

## 2.7 Soldering information

The LGA package is compliant with the ECOPACK<sup>®</sup>, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

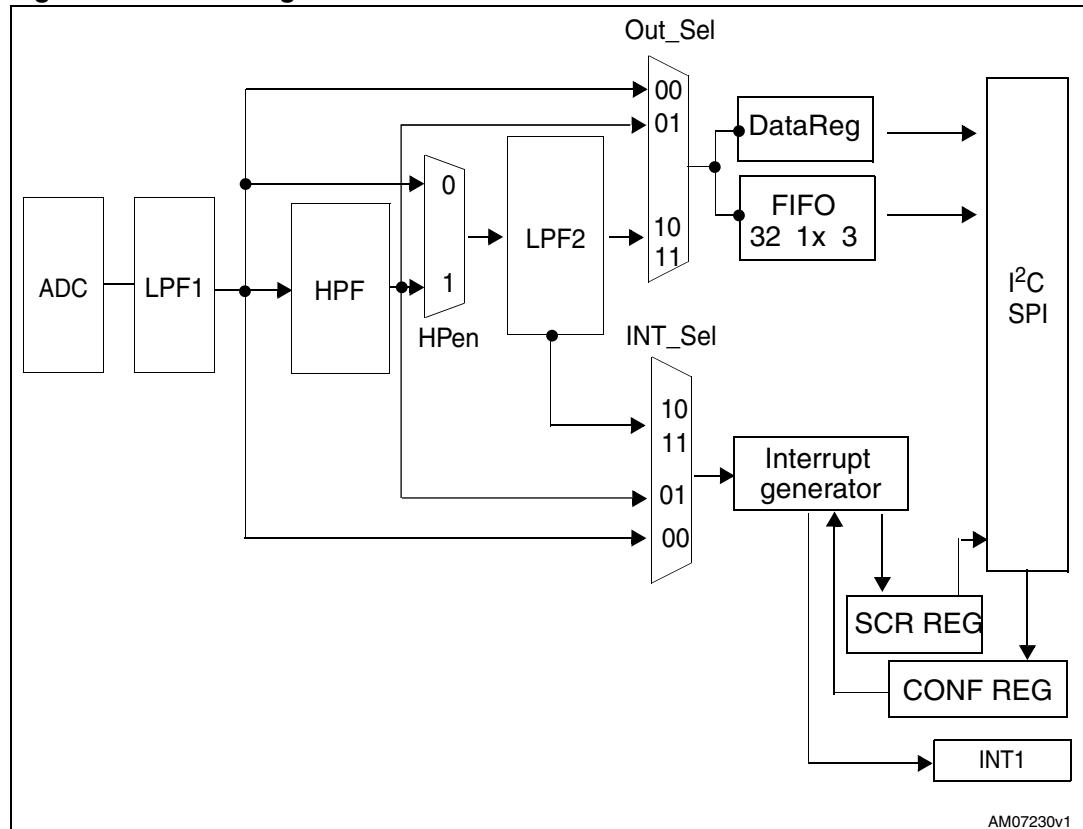
Leave “pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at [www.st.com/](http://www.st.com/).

## 3 Main digital blocks

### 3.1 Block diagram

Figure 6. Block diagram



### 3.2 FIFO

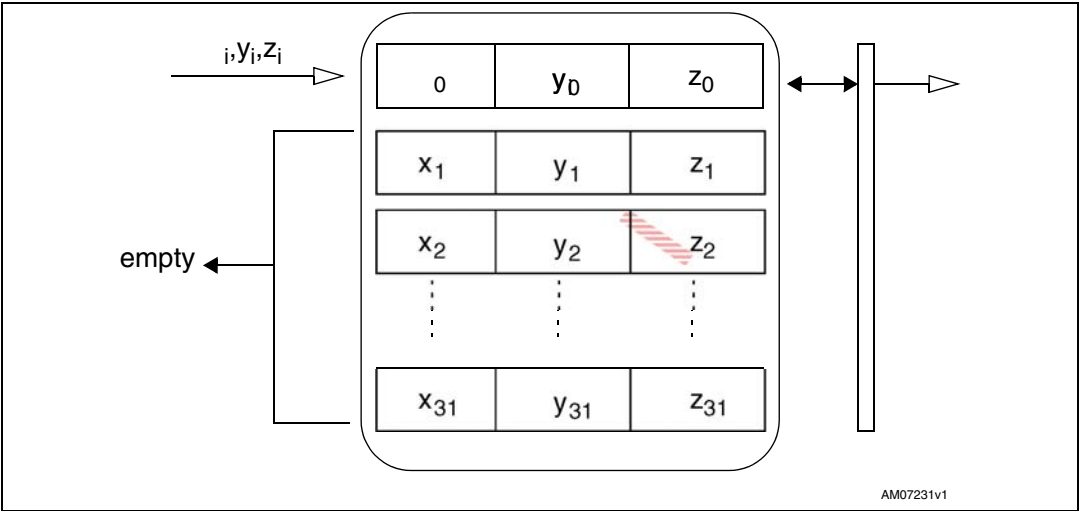
The L3G4200D embeds a 32-slot, 16-bit data FIFO for each of the three output channels: yaw, pitch, and roll. This allows consistent power saving for the system, as the host processor does not need to continuously poll data from the sensor. Instead, it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work in five different modes. Each mode is selected by the FIFO\_MODE bits in the FIFO\_CTRL\_REG. Programmable watermark level, FIFO\_empty or FIFO\_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL\_REG3), and event detection information is available in FIFO\_SRC\_REG. The watermark level can be configured to WTM4:0 in FIFO\_CTRL\_REG.

#### 3.2.1 Bypass mode

In bypass mode, the FIFO is not operational and for this reason it remains empty. As illustrated in [Figure 7](#), only the first address is used for each channel. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.



**Figure 7. Bypass mode**

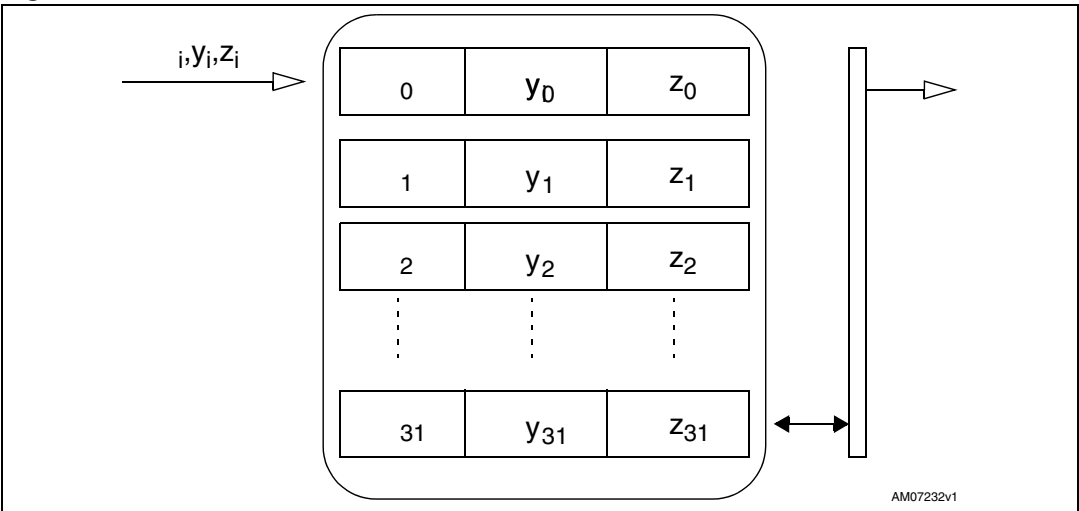


### 3.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch, and roll channels are stored in the FIFO. A watermark interrupt can be enabled (I2\_WMK bit in CTRL\_REG3), which is triggered when the FIFO is filled to the level specified in the WTM 4:0 bits of FIFO\_CTRL\_REG. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, it is necessary to write FIFO\_CTRL\_REG back to bypass mode.

FIFO mode is represented in [Figure 8](#).

**Figure 8. FIFO mode**



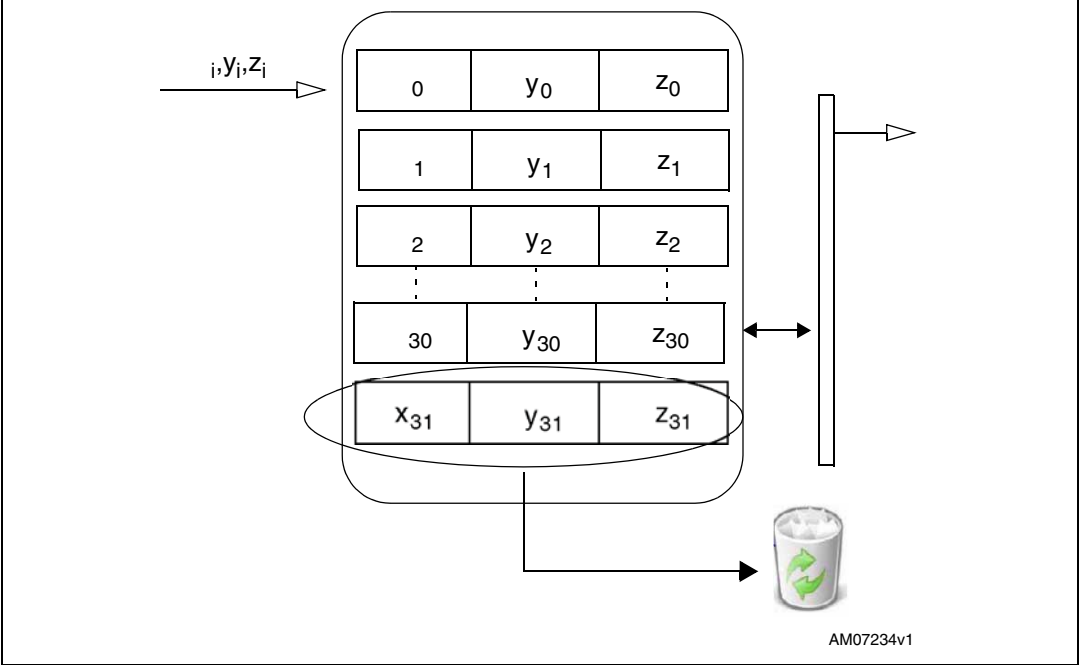
### 3.2.3 Stream mode

In stream mode, data from yaw, pitch, and roll measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO discards the

older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL\_REG3).

Stream mode is represented in [Figure 9](#).

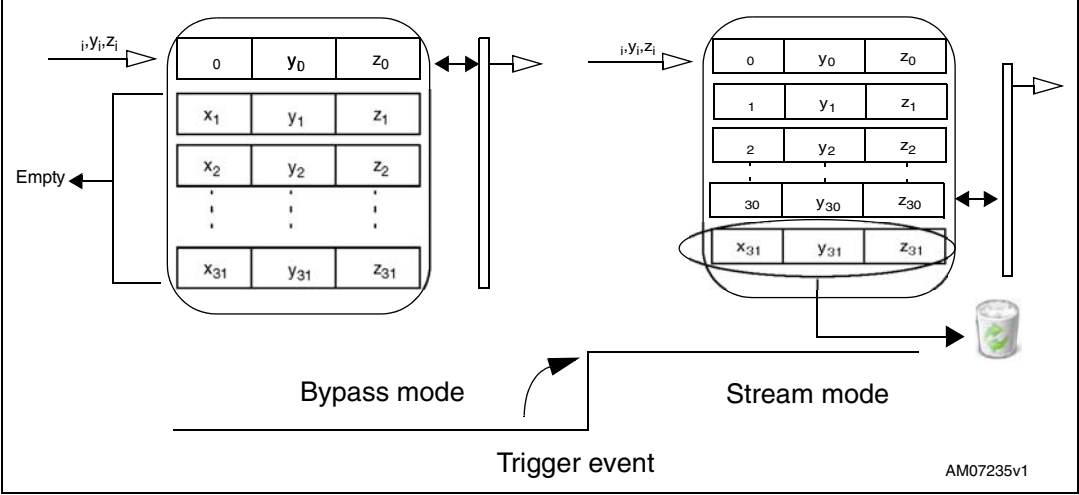
**Figure 9. Stream mode**



### 3.2.4 Bypass-to-stream mode

In bypass-to-stream mode, the FIFO starts operating in bypass mode, and once a trigger event occurs (related to INT1\_CFG register events), the FIFO starts operating in stream mode (see [Figure 10](#)).

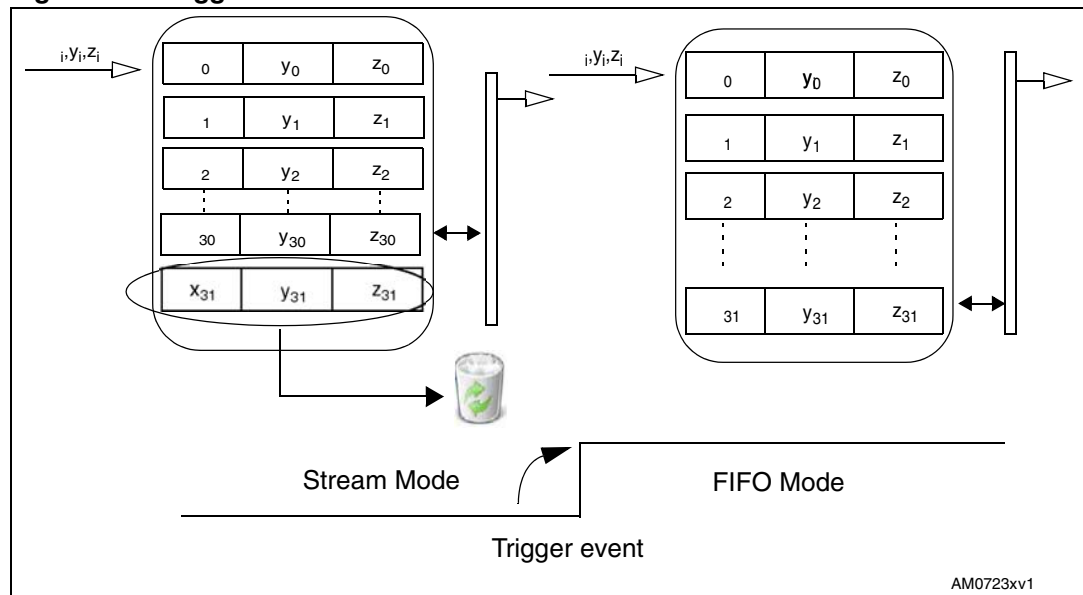
**Figure 10. Bypass-to-stream mode**



### 3.2.5 Stream-to-FIFO mode

In stream-to-FIFO mode, data from yaw, pitch, and roll measurements are stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2, setting the I2\_WTM bit in CTRL\_REG3, which is triggered when the FIFO is filled to the level specified in the WTM4:0 bits of FIFO\_CTRL\_REG. The FIFO continues filling until full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to INT1\_CFG register events), the FIFO starts operating in FIFO mode (see [Figure 11](#)).

**Figure 11. Trigger stream mode**

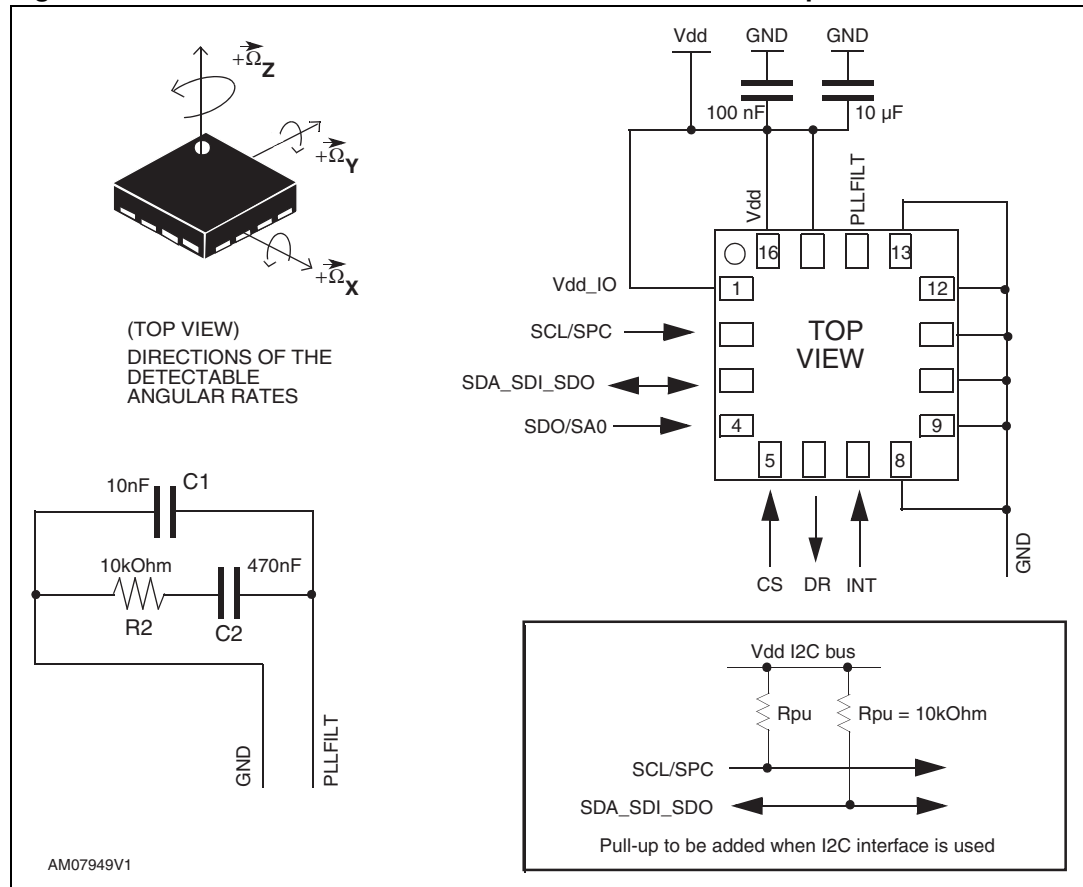


### 3.2.6 Retrieve data from FIFO

FIFO data is read through the OUT\_X, OUT\_Y and OUT\_Z registers. When the FIFO is in stream, trigger or FIFO mode, a read operation to the OUT\_X, OUT\_Y or OUT\_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll, and yaw data are placed in the OUT\_X, OUT\_Y and OUT\_Z registers and both single read and read\_burst (X, Y & Z with auto-incremental address) operations can be used. In read\_burst mode, when data included in OUT\_Z\_H is read, the system again starts to read information from addr OUT\_X\_L.

## 4 Application hints

Figure 12. L3G4200D electrical connections and external component values



Power supply decoupling capacitors (100 nF ceramic or polyester +10 μF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd\_IO are not connected together, power supply decoupling capacitors (100 nF and 10 μF between Vdd and common ground, 100 nF between Vdd\_IO and common ground) should be placed as near as possible to the device (common design practice).

The L3G4200D IC includes a PLL (phase locked loop) circuit to synchronize driving and sensing interfaces. Capacitors and resistors must be added at the **PLLFILT** pin (as shown in [Figure 12](#)) to implement a second-order low-pass filter. [Table 10](#) summarizes the PLL low-pass filter component values.

Table 10. PLL low-pass filter component values

| Component | Value         |
|-----------|---------------|
| C1        | 10 nF ± 10 %  |
| C2        | 470 nF ± 10 % |
| R2        | 10 kΩ ± 10 %  |

## 5 Digital interfaces

The registers embedded in the L3G4200D may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be software-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (i.e., connected to Vdd\_IO).

**Table 11. Serial interface pin description**

| Pin name    | Pin description   |
|-------------|---|
| CS          | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1:SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled) |
| SCL/SPC     | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)  |
| SDA/SDI/SDO | I <sup>2</sup> C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO)  |
| SDO         | SPI serial data output (SDO)<br>I <sup>2</sup> C least significant bit of the device address  |

### 5.1 I<sup>2</sup>C serial interface

The L3G4200D I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write data to registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in the table below.

**Table 12. I<sup>2</sup>C terminology**

| Term        | Description  |
|-------------|--|
| Transmitter | The device which sends data to the bus   |
| Receiver    | The device which receives data from the bus  |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master   |

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd\_IO through an external pull-up resistor. When the bus is free both the lines are high.

The I<sup>2</sup>C interface is compliant with fast mode (400 kHz) I<sup>2</sup>C standards as well as with normal mode.

### 5.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first 7 bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated with the L3G4200D is 110100xb. The SDO pin can be used to modify the least significant bit (LSb) of the device address. If the SDO pin is connected to the voltage supply, LSb is '1' (address 1101001b). Otherwise, if the SDO pin is connected to ground, the LSb value is '0' (address 1101000b). This solution permits the connection and addressing of two different gyroscopes to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded in the L3G4200D behaves like a slave device, and the following protocol must be adhered to. After the START (ST) condition, a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted. The 7 LSb represent the actual register address while the MSB enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is '1' (read), a REPEATED START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with the direction unchanged. [Table 13](#) describes how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 13. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SDO | R/W | SAD+R/W        |
|---------|----------|--------------|-----|----------------|
| Read    | 110100   | 0            | 1   | 11010001 (D1h) |
| Write   | 110100   | 0            | 0   | 11010000 (D0h) |
| Read    | 110100   | 1            | 1   | 11010011 (D3h) |
| Write   | 110100   | 1            | 0   | 11010010 (D2h) |

**Table 14. Transfer when master is writing one byte to slave**

|        |    |         |     |     |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |    |

**Table 15. Transfer when master is writing multiple bytes to slave**

|        |    |         |     |     |     |      |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |      | SAK |    |

**Table 16. Transfer when master is receiving (reading) one byte of data from slave**

|        |    |         |     |     |     |    |         |     |      |      |    |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | NMAK | SP |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |      |    |

**Table 17. Transfer when master is receiving (reading) multiple bytes of data from slave**

|        |    |       |     |     |     |    |       |     |      |     |      |     |      |      |    |
|--------|----|-------|-----|-----|-----|----|-------|-----|------|-----|------|-----|------|------|----|
| Master | ST | SAD+W |     | SUB |     | SR | SAD+R |     |      | MAK |      | MAK |      | NMAK | SP |
| Slave  |    |       | SAK |     | SAK |    |       | SAK | DATA |     | DATA |     | DATA |      |    |

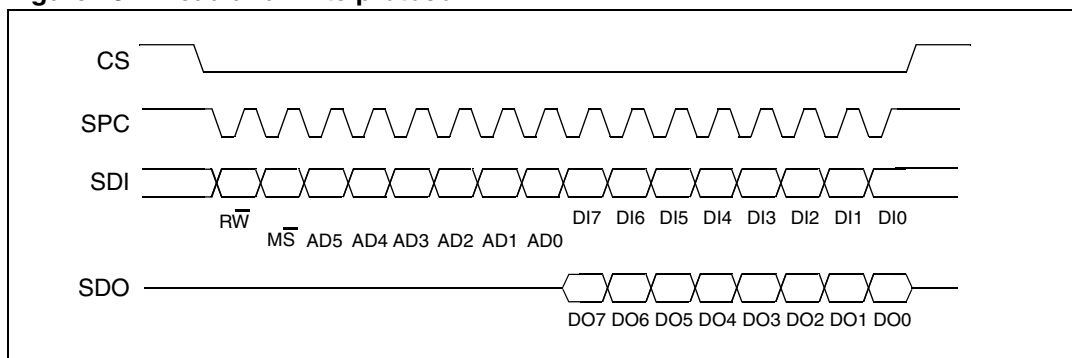
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e., it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1, while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is “master acknowledge” and NMAK is “no master acknowledge”.

## 5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading of the device registers. The serial interface interacts with the external world through 4 wires: **CS**, **SPC**, **SDI**, and **SDO**.

**Figure 13. Read and write protocol**

**CS** is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses, or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, etc.) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**Bit 0:**  $R\overline{W}$  bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

**Bit 1:**  $\overline{M\overline{S}}$  bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

**Bit 2-7:** address AD(5:0). This is the address field of the indexed register.

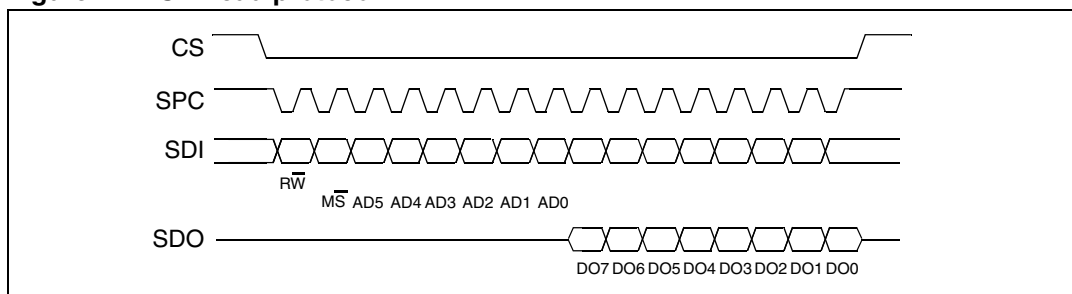
**Bit 8-15:** data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

**Bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the  $\overline{M\overline{S}}$  bit is 0, the address used to read/write data remains the same for every block. When the  $\overline{M\overline{S}}$  bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI read

**Figure 14. SPI read protocol**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

**Bit 0:** READ bit. The value is 1.

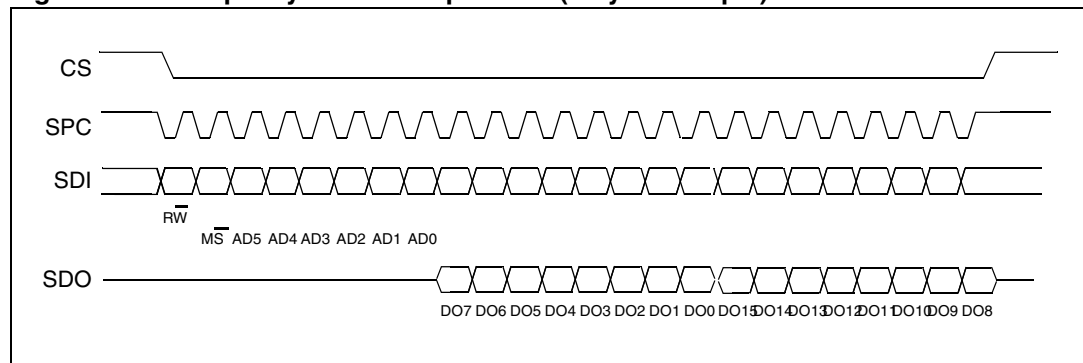
**Bit 1:**  $\overline{MS}$  bit. When 0, do not increment address; when 1, increment address in multiple reading.

**Bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**Bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

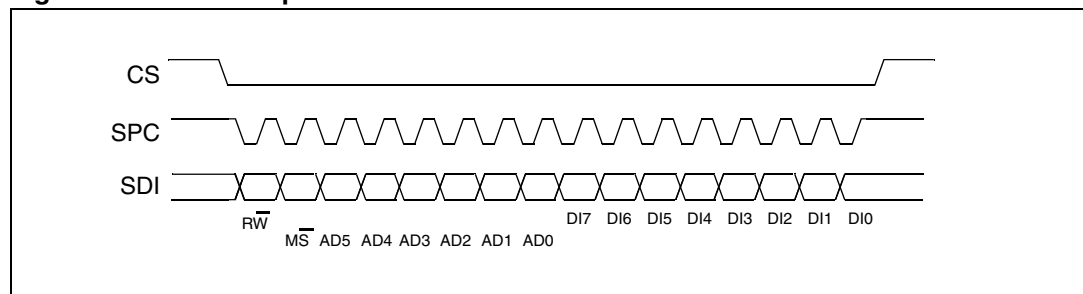
**Bit 16-...** : data DO(...-8). Further data in multiple byte reading.

**Figure 15. Multiple byte SPI read protocol (2-byte example)**



## 5.2.2 SPI write

**Figure 16. SPI write protocol**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

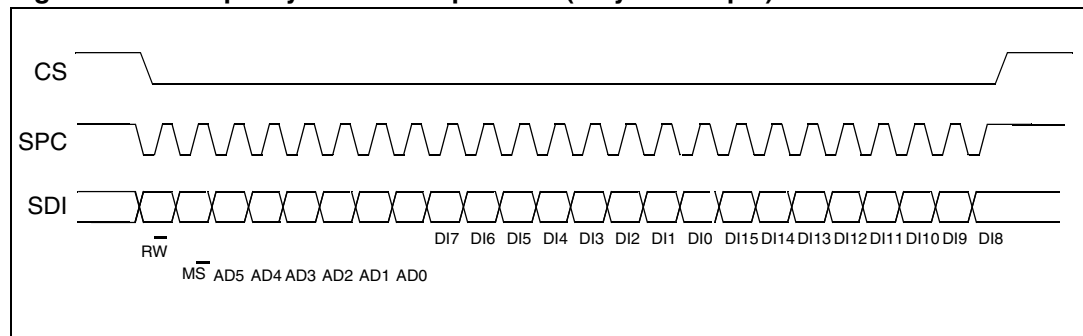
**Bit 0:** WRITE bit. The value is 0.

**Bit 1:**  $\overline{MS}$  bit. When 0, do not increment address; when 1, increment address in multiple writing.

**Bit 2-7:** address AD(5:0). This is the address field of the indexed register.

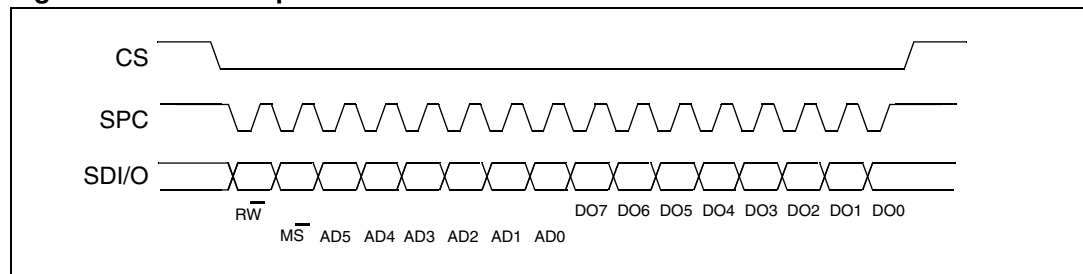
**Bit 8-15:** data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

**Bit 16-...** : data DI(...-8). Further data in multiple byte writing.

**Figure 17. Multiple byte SPI write protocol (2-byte example)**

### 5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM (SPI serial interface mode selection) bit to 1 in CTRL\_REG2.

**Figure 18. SPI read protocol in 3-wire mode**

The SPI read command is performed with 16 clock pulses:

**Bit 0:** READ bit. The value is 1.

**Bit 1:**  $\overline{MS}$  bit. When 0, do not increment address; when 1, increment address in multiple reading.

**Bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**Bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The multiple read command is also available in 3-wire mode.

## 6 Output register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

**Table 18. Register address map**

| Name          | Type | Register address |          | Default  | Comment |
|---------------|------|------------------|----------|----------|---------|
|               |      | Hex              | Binary   |          |         |
| Reserved      | -    | 00-0E            | -        | -        |         |
| WHO_AM_I      | r    | 0F               | 000 1111 | 11010011 |         |
| Reserved      | -    | 10-1F            | -        | -        |         |
| CTRL_REG1     | rw   | 20               | 010 0000 | 00000111 |         |
| CTRL_REG2     | rw   | 21               | 010 0001 | 00000000 |         |
| CTRL_REG3     | rw   | 22               | 010 0010 | 00000000 |         |
| CTRL_REG4     | rw   | 23               | 010 0011 | 00000000 |         |
| CTRL_REG5     | rw   | 24               | 010 0100 | 00000000 |         |
| REFERENCE     | rw   | 25               | 010 0101 | 00000000 |         |
| OUT_TEMP      | r    | 26               | 010 0110 | output   |         |
| STATUS_REG    | r    | 27               | 010 0111 | output   |         |
| OUT_X_L       | r    | 28               | 010 1000 | output   |         |
| OUT_X_H       | r    | 29               | 010 1001 | output   |         |
| OUT_Y_L       | r    | 2A               | 010 1010 | output   |         |
| OUT_Y_H       | r    | 2B               | 010 1011 | output   |         |
| OUT_Z_L       | r    | 2C               | 010 1100 | output   |         |
| OUT_Z_H       | r    | 2D               | 010 1101 | output   |         |
| FIFO_CTRL_REG | rw   | 2E               | 010 1110 | 00000000 |         |
| FIFO_SRC_REG  | r    | 2F               | 010 1111 | output   |         |
| INT1_CFG      | rw   | 30               | 011 0000 | 00000000 |         |
| INT1_SRC      | r    | 31               | 011 0001 | output   |         |
| INT1_TSH_XH   | rw   | 32               | 011 0010 | 00000000 |         |
| INT1_TSH_XL   | rw   | 33               | 011 0011 | 00000000 |         |
| INT1_TSH_YH   | rw   | 34               | 011 0100 | 00000000 |         |
| INT1_TSH_YL   | rw   | 35               | 011 0101 | 00000000 |         |
| INT1_TSH_ZH   | rw   | 36               | 011 0110 | 00000000 |         |
| INT1_TSH_ZL   | rw   | 37               | 011 0111 | 00000000 |         |
| INT1_DURATION | rw   | 38               | 011 1000 | 00000000 |         |

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

## 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

### 7.1 WHO\_AM\_I (0Fh)

**Table 19. WHO\_AM\_I register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
|---|---|---|---|---|---|---|---|

Device identification register.

### 7.2 CTRL\_REG1 (20h)

**Table 20. CTRL\_REG1 register**

|     |     |     |     |    |     |     |     |
|-----|-----|-----|-----|----|-----|-----|-----|
| DR1 | DR0 | BW1 | BW0 | PD | Zen | Yen | Xen |
|-----|-----|-----|-----|----|-----|-----|-----|

**Table 21. CTRL\_REG1 description**

|         |  |
|---------|--|
| DR1-DR0 | Output Data Rate selection. Refer to <a href="#">Table 22</a>                                  |
| BW1-BW0 | Bandwidth selection. Refer to <a href="#">Table 22</a>   |
| PD      | Power down mode enable. Default value: 0<br>(0: power down mode, 1: normal mode or sleep mode) |
| Zen     | Z axis enable. Default value: 1<br>(0: Z axis disabled; 1: Z axis enabled)                     |
| Yen     | Y axis enable. Default value: 1<br>(0: Y axis disabled; 1: Y axis enabled)                     |
| Xen     | X axis enable. Default value: 1<br>(0: X axis disabled; 1: X axis enabled)                     |

**DR<1:0>** is used to set ODR selection. **BW <1:0>** is used to set Bandwidth selection.

In the following table are reported all frequency resulting in combination of DR / BW bits.

**Table 22. DR and BW configuration setting**

| DR <1:0> | BW <1:0> | ODR [Hz] | Cut-Off |
|----------|----------|----------|---------|
| 00       | 00       | 100      | 12.5    |
| 00       | 01       | 100      | 25      |
| 00       | 10       | 100      | 25      |
| 00       | 11       | 100      | 25      |

**Table 22. DR and BW configuration setting (continued)**

| DR <1:0> | BW <1:0> | ODR [Hz] | Cut-Off |
|----------|----------|----------|---------|
| 01       | 00       | 200      | 12.5    |
| 01       | 01       | 200      | 25      |
| 01       | 10       | 200      | 50      |
| 01       | 11       | 200      | 70      |
| 10       | 00       | 400      | 20      |
| 10       | 01       | 400      | 25      |
| 10       | 10       | 400      | 50      |
| 10       | 11       | 400      | 110     |
| 11       | 00       | 800      | 30      |
| 11       | 01       | 800      | 35      |
| 11       | 10       | 800      | 50      |
| 11       | 11       | 800      | 110     |

Combination of **PD**, **Zen**, **Yen**, **Xen** are used to set device in different modes (power down / normal / sleep mode) according with the following table.

**Table 23. Power mode selection configuration**

| Mode       | PD | Zen | Yen | Xen |
|------------|----|-----|-----|-----|
| Power down | 0  | -   | -   | -   |
| Sleep      | 1  | 0   | 0   | 0   |
| Normal     | 1  | -   | -   | -   |

## 7.3 CTRL\_REG2 (21h)

**Table 24. CTRL\_REG2 register**

|                  |                  |      |      |       |       |       |       |
|------------------|------------------|------|------|-------|-------|-------|-------|
| 0 <sup>(1)</sup> | 0 <sup>(1)</sup> | HPM1 | HPM1 | HPCF3 | HPCF2 | HPCF1 | HPCF0 |
|------------------|------------------|------|------|-------|-------|-------|-------|

1. Value loaded at boot. This value must not be changed

**Table 25. CTRL\_REG2 description**

|                 |   |
|-----------------|---|
| HPM1-<br>HPM0   | High Pass filter Mode Selection. Default value: 00<br>Refer to <a href="#">Table 26</a> |
| HPCF3-<br>HPCF0 | High Pass filter Cut Off frequency selection<br>Refer to <a href="#">Table 28</a>       |

**Table 26. High pass filter mode configuration**

| HPM1 | HPM0 | High Pass filter Mode                       |
|------|------|---|
| 0    | 0    | Normal mode (reset reading HP_RESET_FILTER) |
| 0    | 1    | Reference signal for filtering              |
| 1    | 0    | Normal mode                                 |
| 1    | 1    | Autoreset on interrupt event                |

**Table 27. High pass filter cut off frequency configuration [Hz]**

| HPCF3 | ODR= 100 Hz | ODR= 200 Hz | ODR= 400 Hz | ODR= 800 Hz |
|-------|-------------|-------------|-------------|-------------|
| 0000  | 8           | 15          | 30          | 56          |
| 0001  | 4           | 8           | 15          | 30          |
| 0010  | 2           | 4           | 8           | 15          |
| 0011  | 1           | 2           | 4           | 8           |
| 0100  | 0.5         | 1           | 2           | 4           |
| 0101  | 0.2         | 0.5         | 1           | 2           |
| 0110  | 0.1         | 0.2         | 0.5         | 1           |
| 0111  | 0.05        | 0.1         | 0.2         | 0.5         |
| 1000  | 0.02        | 0.05        | 0.1         | 0.2         |
| 1001  | 0.01        | 0.02        | 0.05        | 0.1         |

## 7.4 CTRL\_REG3 (22h)

**Table 28. CTRL\_REG1 register**

|         |         |           |       |         |        |         |          |
|---------|---------|-----------|-------|---------|--------|---------|----------|
| I1_Int1 | I1_Boot | H_Lactive | PP_OD | I2_DRDY | I2_WTM | I2_ORun | I2_Empty |
|---------|---------|-----------|-------|---------|--------|---------|----------|

**Table 29. CTRL\_REG3 description**

|           |  |
|-----------|--|
| I1_Int1   | Interrupt enable on INT1 pin. Default value 0. (0: Disable; 1: Enable)           |
| I1_Boot   | Boot status available on INT1. Default value 0. (0: Disable; 1: Enable)          |
| H_Lactive | Interrupt active configuration on INT1. Default value 0. (0: High; 1:Low)        |
| PP_OD     | Push- Pull / Open drain. Default value: 0. (0: Push- Pull; 1: Open drain)        |
| I2_DRDY   | Date Ready on DRDY/INT2. Default value 0. (0: Disable; 1: Enable)                |
| I2_WTM    | FIFO Watermark interrupt on DRDY/INT2. Default value: 0. (0: Disable; 1: Enable) |
| I2_ORun   | FIFO Overrun interrupt on DRDY/INT2 Default value: 0. (0: Disable; 1: Enable)    |
| I2_Empty  | FIFO Empty interrupt on DRDY/INT2. Default value: 0. (0: Disable; 1: Enable)     |

## 7.5 CTRL\_REG4 (23h)

**Table 30. CTRL\_REG4 register**

|     |     |     |     |   |     |     |     |
|-----|-----|-----|-----|---|-----|-----|-----|
| BDU | BLE | FS1 | FS0 | - | ST1 | ST0 | SIM |
|-----|-----|-----|-----|---|-----|-----|-----|

**Table 31. CTRL\_REG4 description**

|         |  |
|---------|--|
| BDU     | Block Data Update. Default value: 0<br>(0: continuous update; 1: output registers not updated until MSB and LSB reading) |
| BLE     | Big/Little Endian Data Selection. Default value 0.<br>(0: Data LSB @ lower address; 1: Data MSB @ lower address)         |
| FS1-FS0 | Full Scale selection. Default value: 00<br>(00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)                        |
| ST1-ST0 | Self Test Enable. Default value: 00<br>(00: Self Test Disabled; Other: See <a href="#">Table</a> )                       |
| SIM     | SPI Serial Interface Mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface).                     |

**Table 32. Self test mode configuration**

| ST1 | ST0 | Self test mode                 |
|-----|-----|--------------------------------|
| 0   | 0   | Normal mode                    |
| 0   | 1   | Self test 0 (+) <sup>(1)</sup> |
| 1   | 0   | --                             |
| 1   | 1   | Self test 1 (-) <sup>(1)</sup> |

1. DST sign (absolute value in [Table 4](#))

## 7.6 CTRL\_REG5 (24h)

**Table 33. CTRL\_REG5 register**

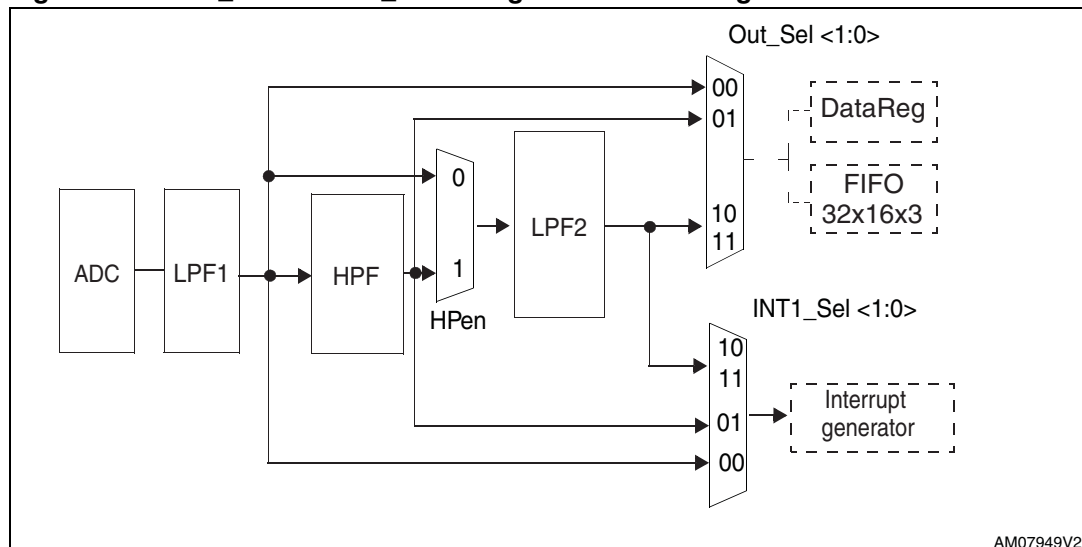
|      |         |    |      |           |           |          |          |
|------|---------|----|------|-----------|-----------|----------|----------|
| BOOT | FIFO_EN | -- | HPen | INT1_Sel1 | INT1_Sel0 | Out_Sel1 | Out_Sel0 |
|------|---------|----|------|-----------|-----------|----------|----------|

**Table 34. CTRL\_REG5 description**

|                         |  |
|-------------------------|--|
| BOOT                    | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content)                          |
| FIFO_EN                 | FIFO enable. Default value: 0<br>(0: FIFO disable; 1: FIFO Enable)   |
| HPen                    | High Pass filter Enable. Default value: 0<br>(0: HPF disabled; 1: HPF enabled. See <a href="#">Figure 20</a> ) |
| INT1_Sel1-<br>INT1_Sel0 | INT1 selection configuration. Default value: 0<br>(See <a href="#">Figure 20</a> )                             |
| Out_Sel1-<br>Out_Sel1   | Out selection configuration. Default value: 0<br>(See <a href="#">Figure 20</a> )                              |



Figure 19. INT1\_Sel and Out\_Sel configuration block diagram



AM07949V2

Table 35. Out\_Sel configuration setting

| Hpen | OUT_SEL1 | OUT_SEL0 | Description  |
|------|----------|----------|--|
| x    | 0        | 0        | Data in DataReg and FIFO are non-high-pass-filtered                  |
| x    | 0        | 1        | Data in DataReg and FIFO are high-pass-filtered                      |
| 0    | 1        | x        | Data in DataReg and FIFO are low-pass-filtered by LPF2               |
| 1    | 1        | x        | Data in DataReg and FIFO are high-pass and low-pass-filtered by LPF2 |

Table 36. INT\_SEL configuration setting

| Hpen | INT_SEL1 | INT_SEL2 | Description  |
|------|----------|----------|--|
| x    | 0        | 0        | Non-high-pass-filtered data are used for interrupt generation          |
| x    | 0        | 1        | High-pass-filtered data are used for interrupt generation              |
| 0    | 1        | x        | Low-pass-filtered data are used for interrupt generation               |
| 1    | 1        | x        | High-pass and low-pass-filtered data are used for interrupt generation |

## 7.7 REFERENCE/DATACAPTURE (25h)

**Table 37. REFERENCE register**

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |
|------|------|------|------|------|------|------|------|

**Table 38. REFERENCE register description**

|            |  |
|------------|--|
| Ref 7-Ref0 | Reference value for Interrupt generation. Default value: 0 |
|------------|--|

## 7.8 OUT\_TEMP (26h)

**Table 39. OUT\_TEMP register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 40. OUT\_TEMP register description**

|             |                   |
|-------------|-------------------|
| Temp7-Temp0 | Temperature data. |
|-------------|-------------------|

## 7.9 STATUS\_REG (27h)

**Table 41. STATUS\_REG register**

|       |     |     |     |       |     |     |     |
|-------|-----|-----|-----|-------|-----|-----|-----|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |
|-------|-----|-----|-----|-------|-----|-----|-----|

**Table 42. STATUS\_REG description**

|       |   |
|-------|---|
| ZYXOR | X, Y, Z -axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: new data has overwritten the previous one before it was read) |
| ZOR   | Z axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)          |
| YOR   | Y axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)          |
| XOR   | X axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)          |
| ZYXDA | X, Y, Z -axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)          |
| ZDA   | Z axis new data available. Default value: 0<br>(0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available) |
| YDA   | Y axis new data available. Default value: 0<br>(0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available) |
| XDA   | X axis new data available. Default value: 0<br>(0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available) |

## 7.10 OUT\_X\_L (28h), OUT\_X\_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

## 7.11 OUT\_Y\_L (2Ah), OUT\_Y\_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

## 7.12 OUT\_Z\_L (2Ch), OUT\_Z\_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

## 7.13 FIFO\_CTRL\_REG (2Eh)

**Table 43. REFERENCE register**

|     |     |     |      |      |      |      |      |
|-----|-----|-----|------|------|------|------|------|
| FM2 | FM1 | FM0 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |
|-----|-----|-----|------|------|------|------|------|

**Table 44. REFERENCE register description**

|           |   |
|-----------|---|
| FM2-FM0   | FIFO mode selection. Default value: 00 (see <a href="#">Table</a> ) |
| WTM4-WTM0 | FIFO threshold. Watermark level setting                             |

**Table 45. FIFO mode configuration**

| FM2 | FM1 | FM0 | FIFO mode             |
|-----|-----|-----|-----------------------|
| 0   | 0   | 0   | Bypass mode           |
| 0   | 0   | 1   | FIFO mode             |
| 0   | 1   | 0   | Stream mode           |
| 0   | 1   | 1   | Stream-to-FIFO mode   |
| 1   | 0   | 0   | Bypass-to-Stream mode |

## 7.14 FIFO\_SRC\_REG (2Fh)

**Table 46. FIFO\_SRC register**

|     |      |       |      |      |      |      |      |
|-----|------|-------|------|------|------|------|------|
| WTM | OVRN | EMPTY | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |
|-----|------|-------|------|------|------|------|------|

**Table 47. FIFO\_SRC register description**

|      |  |
|------|--|
| WTM  | Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level) |
| OVRN | Overflow bit status.<br>(0: FIFO is not completely filled; 1:FIFO is completely filled)                        |

**Table 47. FIFO\_SRC register description (continued)**

|           |  |
|-----------|--|
| EMPTY     | FIFO empty bit.<br>( 0: FIFO not empty; 1: FIFO empty) |
| FSS4-FSS1 | FIFO stored data level                                 |

## 7.15 INT1\_CFG (30h)

**Table 48. INT1\_CFG register**

|        |     |      |      |      |      |      |      |
|--------|-----|------|------|------|------|------|------|
| AND/OR | LIR | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |
|--------|-----|------|------|------|------|------|------|

**Table 49. INT1\_CFG description**

|        |  |
|--------|--|
| AND/OR | AND/OR combination of Interrupt events. Default value: 0<br>(0: OR combination of interrupt events 1: AND combination of interrupt events)   |
| LIR    | Latch Interrupt Request. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched)<br>Cleared by reading INT1_SRC reg.                                  |
| ZHIE   | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE   | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)   |
| YHIE   | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE   | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)   |
| XHIE   | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE   | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)   |

Configuration register for Interrupt source.

## 7.16 INT1\_SRC (31h)

**Table 50. INT1\_SRC register**

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |
|---|----|----|----|----|----|----|----|

**Table 51. INT1\_SRC description**

|    |   |
|----|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0 (0: no interrupt, 1: Z High event has occurred)  |
| ZL | Z low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)  |
| YH | Y high. Default value: 0 (0: no interrupt, 1: Y High event has occurred)  |
| YL | Y low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)  |
| XH | X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)  |
| XL | X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)  |

Interrupt source register. Read only register.

Reading at this address clears INT1\_SRC IA bit (and eventually the interrupt signal on INT1 pin) and allows the refreshment of data in the INT1\_SRC register if the latched option was chosen.

## 7.17 INT1\_THS\_XH (32h)

**Table 52. INT1\_THS\_XH register**

|   |        |        |        |        |        |       |       |
|---|--------|--------|--------|--------|--------|-------|-------|
| - | THSX14 | THSX13 | THSX12 | THSX11 | THSX10 | THSX9 | THSX8 |
|---|--------|--------|--------|--------|--------|-------|-------|

**Table 53. INT1\_THS\_XH description**

|                |   |
|----------------|---|
| THSX14 - THSX9 | Interrupt threshold. Default value: 0000 0000 |
|----------------|---|

## 7.18 INT1\_THS\_XL (33h)

**Table 54. INT1\_THS\_XL register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| THSX7 | THSX6 | THSX5 | THSX4 | THSX3 | THSX2 | THSX1 | THSX0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 55. INT1\_THS\_XL description**

|               |   |
|---------------|---|
| THSX7 - THSX0 | Interrupt threshold. Default value: 0000 0000 |
|---------------|---|

## 7.19 INT1\_THS\_YH (34h)

**Table 56. INT1\_THS\_YH register**

|   |        |        |        |        |        |       |       |
|---|--------|--------|--------|--------|--------|-------|-------|
| - | THSY14 | THSY13 | THSY12 | THSY11 | THSY10 | THSY9 | THSY8 |
|---|--------|--------|--------|--------|--------|-------|-------|

**Table 57. INT1\_THS\_YH description**

|                |   |
|----------------|---|
| THSY14 - THSY9 | Interrupt threshold. Default value: 0000 0000 |
|----------------|---|

## 7.20 INT1\_THS\_YL (35h)

**Table 58. INT1\_THS\_YL register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| THSR7 | THSY6 | THSY5 | THSY4 | THSY3 | THSY2 | THSY1 | THSY0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 59. INT1\_THS\_YL description**

|               |   |
|---------------|---|
| THSY7 - THSY0 | Interrupt threshold. Default value: 0000 0000 |
|---------------|---|

## 7.21 INT1\_THS\_ZH (36h)

**Table 60. INT1\_THS\_ZH register**

|   |        |        |        |        |        |       |       |
|---|--------|--------|--------|--------|--------|-------|-------|
| - | THSZ14 | THSZ13 | THSZ12 | THSZ11 | THSZ10 | THSZ9 | THSZ8 |
|---|--------|--------|--------|--------|--------|-------|-------|

**Table 61. INT1\_THS\_ZH description**

|                |   |
|----------------|---|
| THSZ14 - THSZ9 | Interrupt threshold. Default value: 0000 0000 |
|----------------|---|

## 7.22 INT1\_THS\_ZL (37h)

**Table 62. INT1\_THS\_ZL register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| THSZ7 | THSZ6 | THSZ5 | THSZ4 | THSZ3 | THSZ2 | THSZ1 | THSZ0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 63. INT1\_THS\_ZL description**

|               |   |
|---------------|---|
| THSZ7 - THSZ0 | Interrupt threshold. Default value: 0000 0000 |
|---------------|---|

## 7.23 INT1\_DURATION (38h)

**Table 64. INT1\_DURATION register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| WAIT | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----|----|----|

**Table 65. INT1\_DURATION description**

|         |   |
|---------|---|
| WAIT    | WAIT enable. Default value: 0 (0: disable; 1: enable) |
| D6 - D0 | Duration value. Default value: 000 0000               |

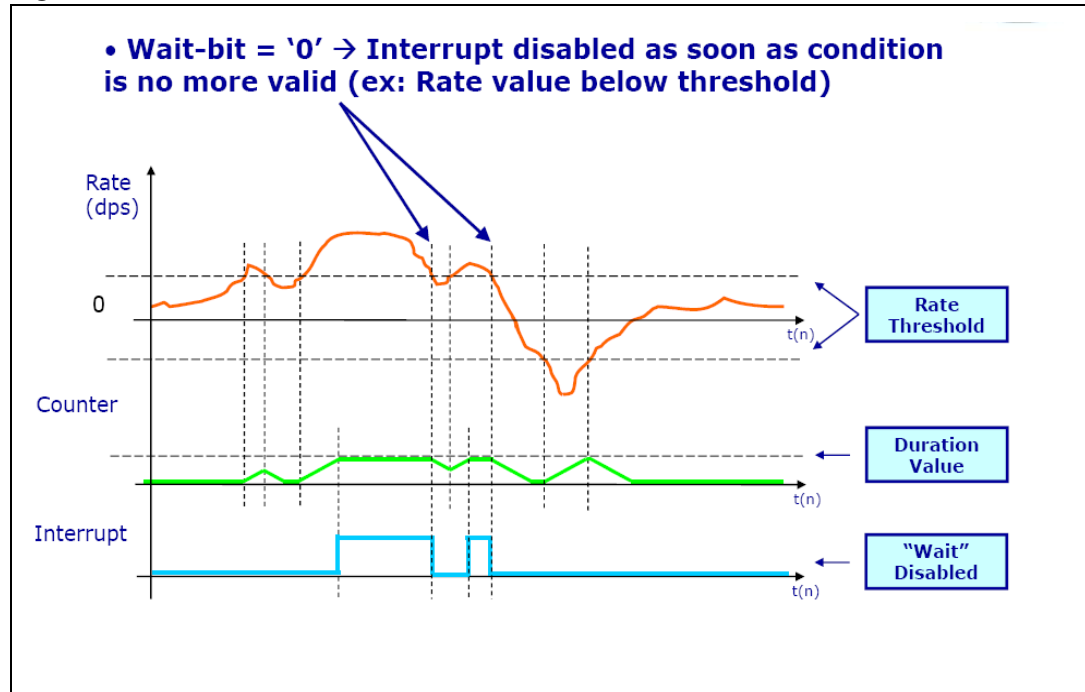
**D6 - D0** bits set the minimum duration of the Interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

**WAIT** bit has the following meaning:

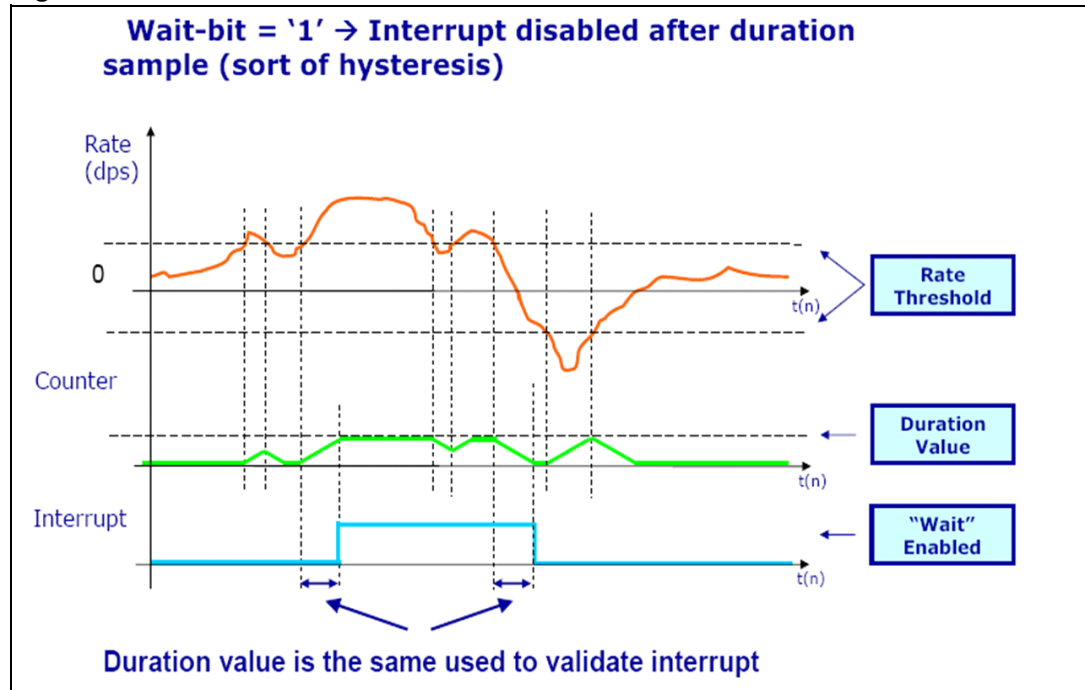
Wait = '0': the interrupt falls immediately if signal crosses the selected threshold

Wait = '1': if signal crosses the selected threshold, the interrupt falls only after the duration has counted number of samples at the selected data rate, written into the duration counter register.

**Figure 20. Wait disabled**



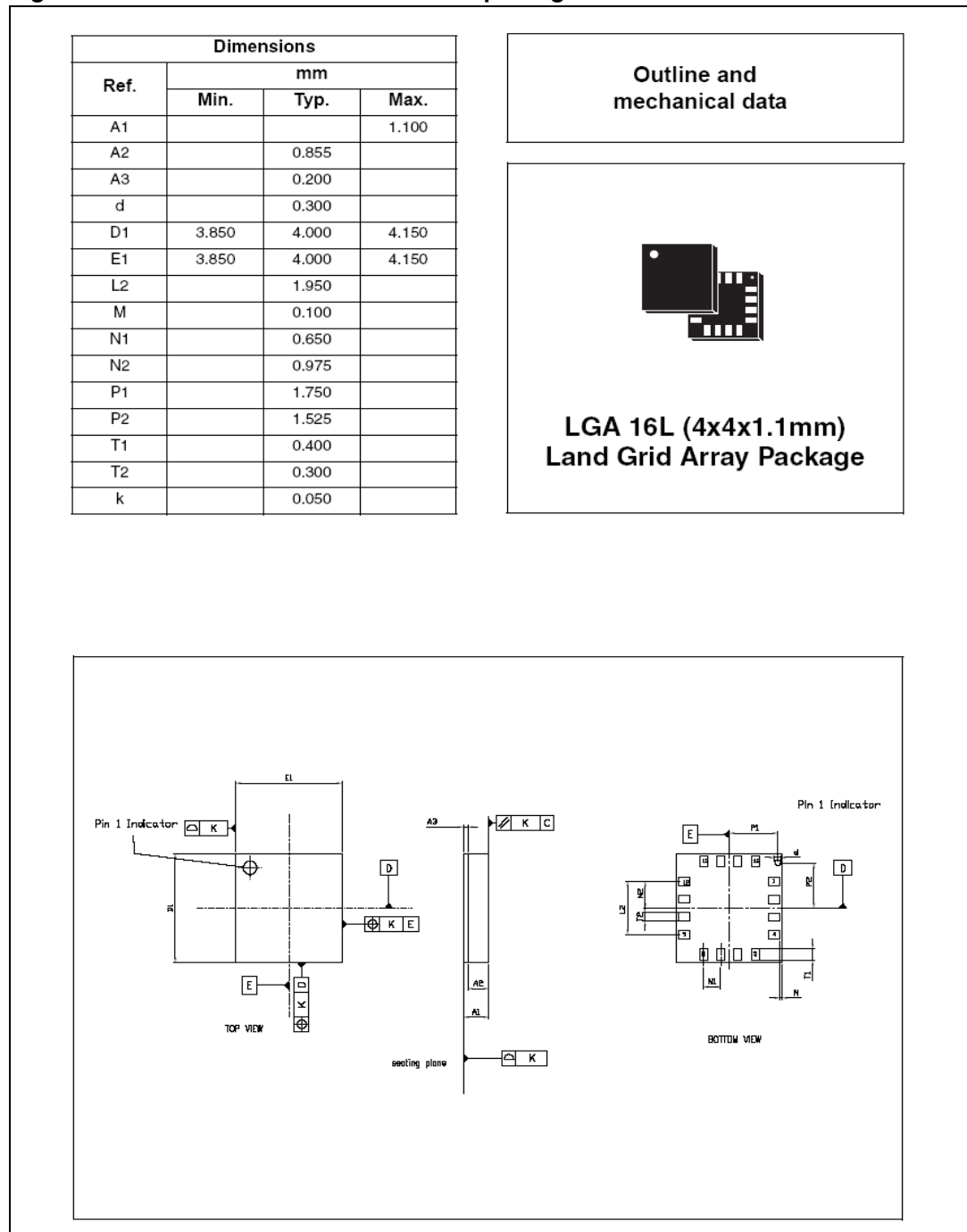
**Figure 21. Wait enabled**



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Figure 22. LGA-16: mechanical data and package dimensions**





## 9 Revision history

**Table 66. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 01-Apr-2010 | 1        | Initial release.  |
| 03-Sep-2010 | 2        | Complete datasheet review.  |
| 22-Dec-2010 | 3        | Inserted <a href="#">Section 6: Output register mapping</a> and <a href="#">Section 7: Register description</a> . |

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