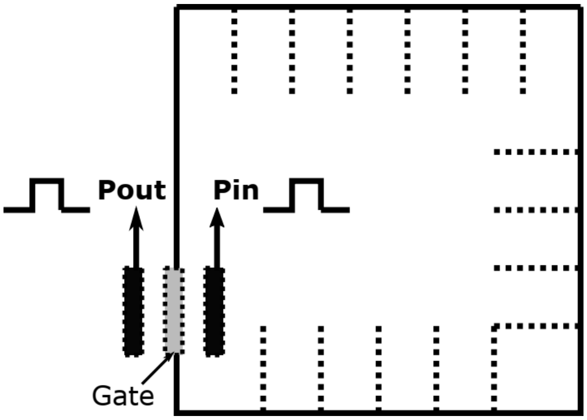
Car Park Count System Using FPGA

Design and implement a FPGA based system which counts the number of cars available in parking lot, which has a single entry and exit points. There are two inputs to this system one from pressure sensor (**Pout)** just outside the gate of the parking lot and the other from pressure sensor (**Pin**) just inside the gate of the parking lot. Assume that the pressure sensor generates a pulse (which is given as input to the system) when activated. The output of the system is a 4-bit signal "**CarCount**" which indicates the no of cars available in the parking lot. A representative figure of parking lot is shown below:



When a car enters the parking lot "**Pout"** gets activated first and then **"Pin"** gets activated (Car is moving from outside to inside). In this case the "**CarCount**" should be incremented by 1.
When the car exits the parking lot **"Pin"** gets activated first and then **"Pout"** gets activated (Car is moving from inside to outside). In this case the "**CarCount**" should be decremented by 1.
The "**CarCount**" does not change if none of the sensors are activated. The "**CarCount**" does not change if only one sensor is activated (i.e. if only **Pout** gets activated and **Pin** is not activated then it means that the car is at the gate but it has not entered the parking lot yet. Similarly, if only **Pin** gets activated and **Pout** is not then car is at the gate but it has not exited the parking lot yet)

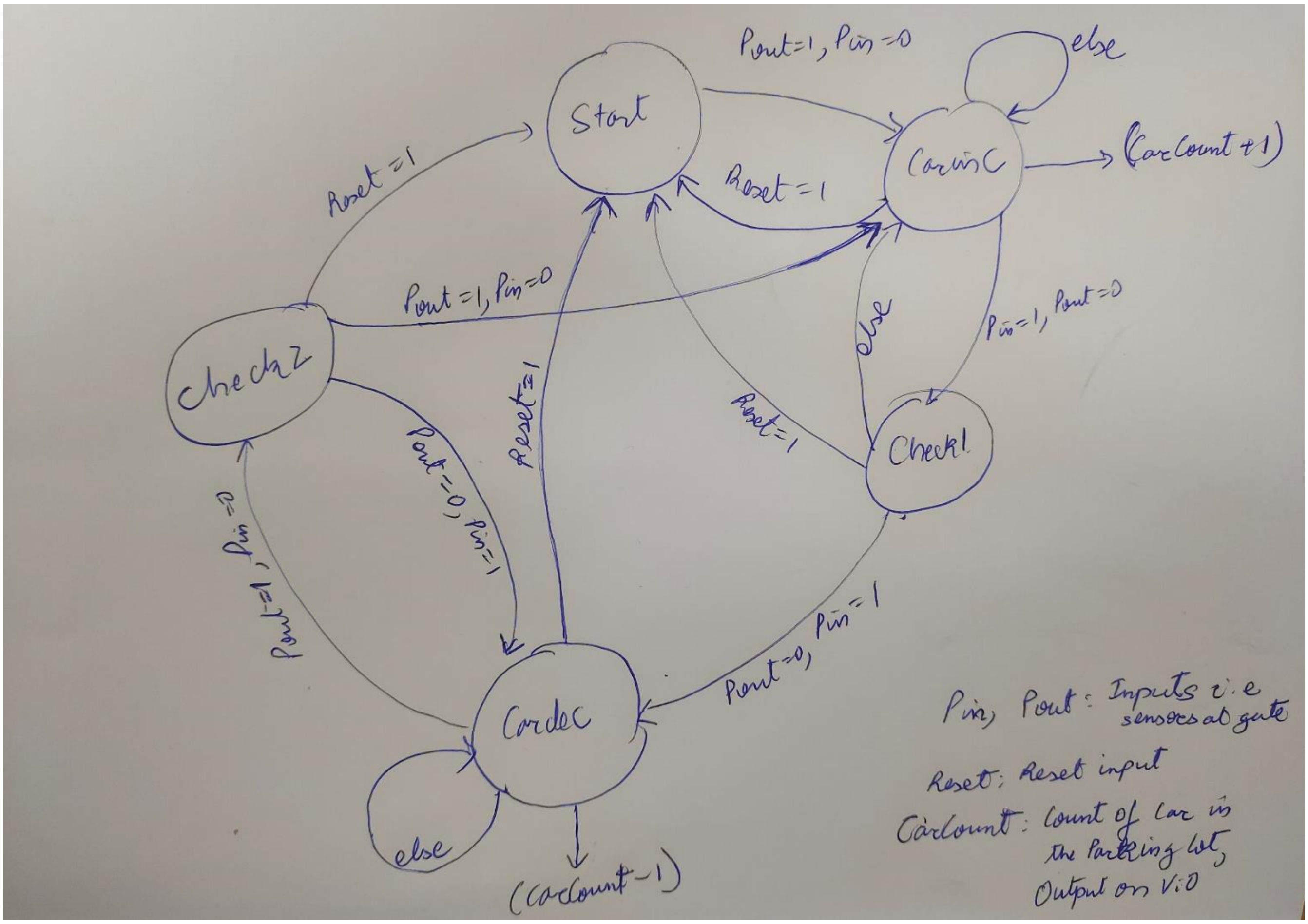
For implementation purpose, Assume the following

1. "**Pout**" is connected to push button switch: **T18**
2. "**Pin**" is connected to push button switch: **R16**
3. "**CarCoun**t" is connected to **VIO** (car count gets updated in VIO window)
4. "**Clk**" is connected to internal clock: **Y9**
5. "**Reset**" is connected to push button switch: **R18**

Answer the following questions which are related to the implementation of above design.

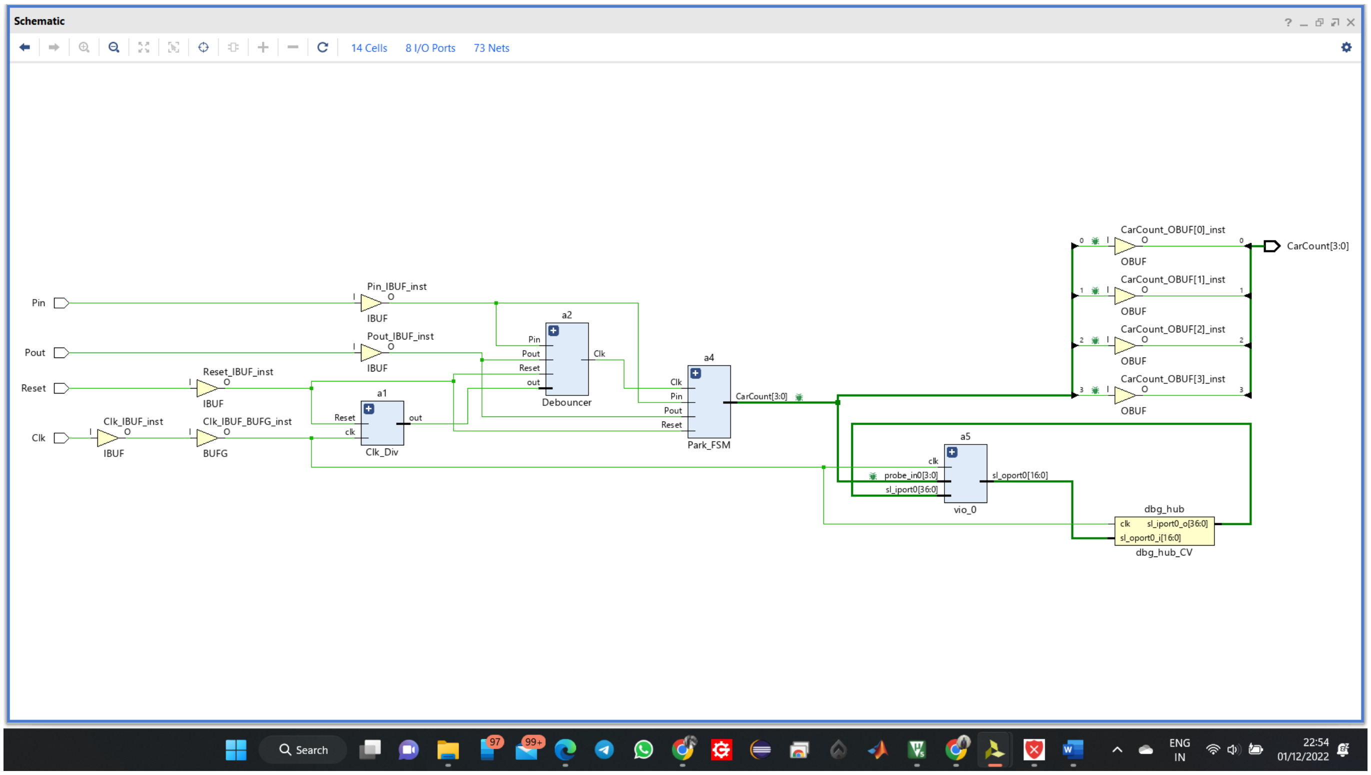
1. **<u>FSM of the Described System</u>**

   Answer:

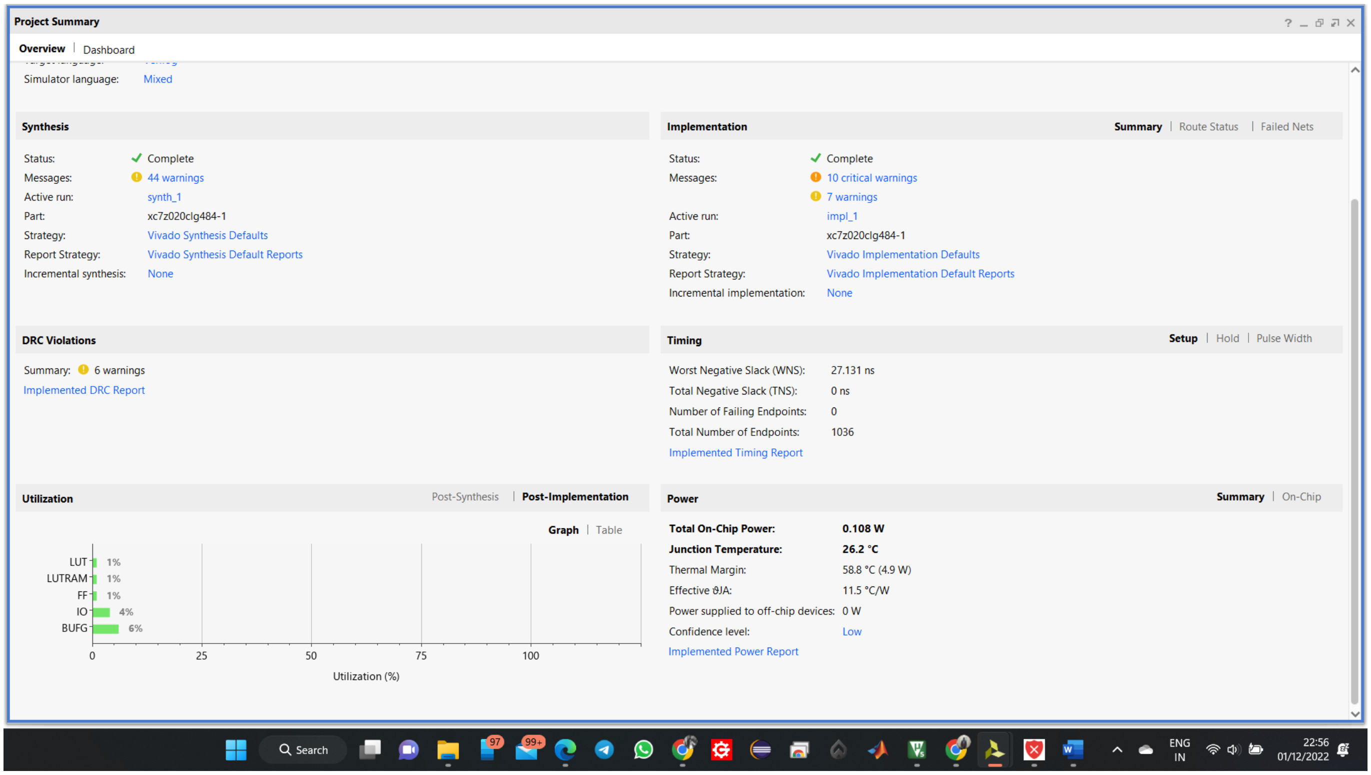


2. **Implement the design, test it and do IO Planning.**

3. Synthesize (**Run Synthesis**).



Hardware utilization.



Project Summary

Overview | Dashboard

Simulator language: Mixed

Synthesis

Status: ✓ Complete

Messages: 44 warnings

Active run: synth_1

Part: xc7z020clg484-1

Strategy: Vivado Synthesis Defaults

Report Strategy: Vivado Synthesis Default Reports

Incremental synthesis: None

Implementation — **Summary** | Route Status | Failed Nets

Status: ✓ Complete

Messages: 10 critical warnings
7 warnings

Active run: impl_1

Part: xc7z020clg484-1

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Implementation Default Reports

Incremental implementation: None

DRC Violations

Summary: 6 warnings

Implemented DRC Report

Timing — **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS): 27.131 ns

Total Negative Slack (TNS): 0 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 1036

Implemented Timing Report

Utilization — Post-Synthesis | **Post-Implementation**

Graph | Table

Power — **Summary** | On-Chip

Total On-Chip Power: **0.108 W**

Junction Temperature: **26.2 °C**

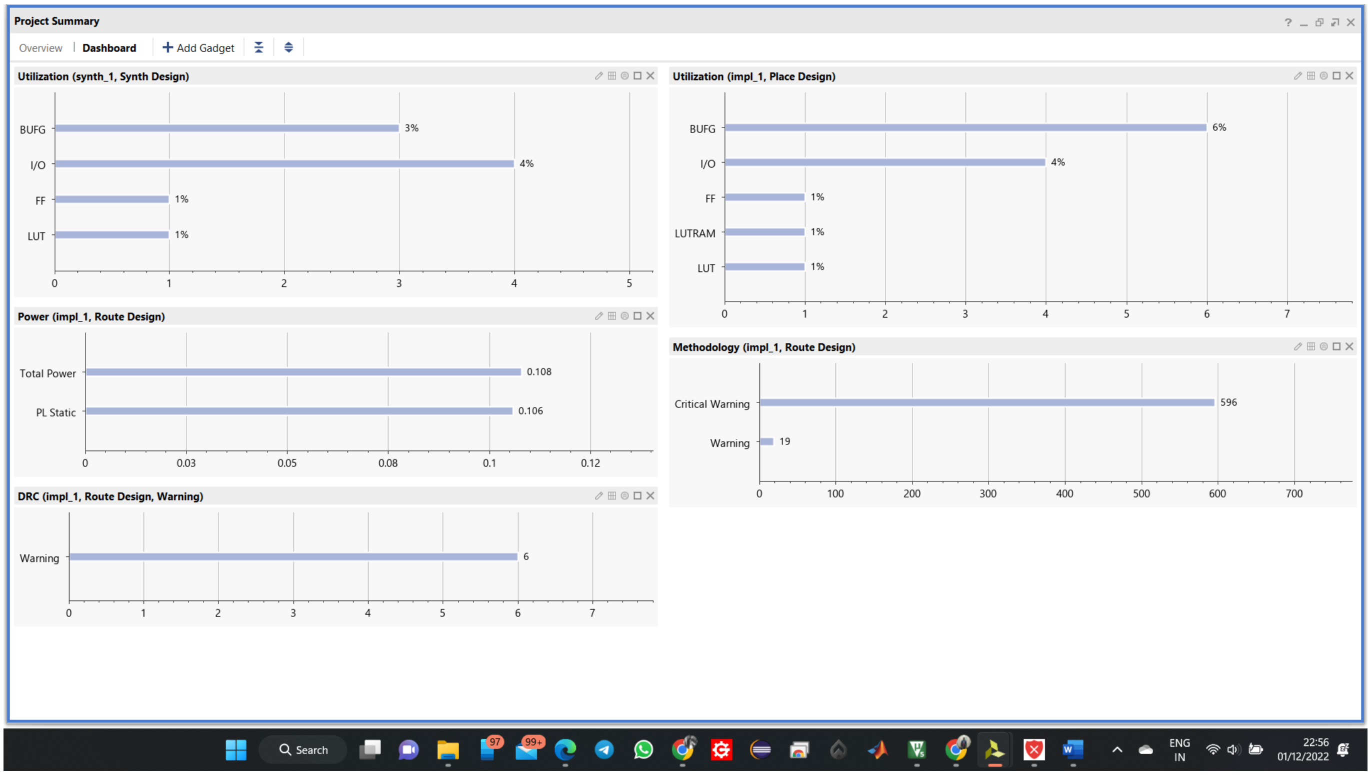
Thermal Margin: 58.8 °C (4.9 W)

Effective ϑJA: 11.5 °C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

Implemented Power Report


Project Summary
Overview
Dashboard
+ Add Gadget
Utilization (synth_1, Synth Design)
BUFG 3%
I/O 4%
FF 1%
LUT 1%
0 1 2 3 4 5
Utilization (impl_1, Place Design)
BUFG 6%
I/O 4%
FF 1%
LUTRAM 1%
LUT 1%
0 1 2 3 4 5 6 7
Power (impl_1, Route Design)
Total Power 0.108
PL Static 0.106
0 0.03 0.05 0.08 0.1 0.12
Methodology (impl_1, Route Design)
Critical Warning 596
Warning 19
0 100 200 300 400 500 600 700
DRC (impl_1, Route Design, Warning)
Warning 6
0 1 2 3 4 5 6 7
Search
97
99+
ENG
IN
22:56
01/12/2022