



PIC16F616/16HV616

Data Sheet

**14-Pin Flash-Based, 8-Bit
CMOS Microcontrollers**

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**MICROCHIP**

PIC16F616/16HV616

14-Pin Flash-Based, 8-Bit CMOS Microcontrollers

High-Performance RISC CPU:

- Only 35 instructions to learn:
 - All single-cycle instructions except branches
- Operating speed:
 - DC – 20 MHz oscillator/clock input
 - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$, typical
 - Software selectable frequency: 4 MHz or 8 MHz
- Power-Saving Sleep mode
- Voltage range:
 - PIC16F616: 2.0V to 5.5V
 - PIC16HV616: 2.0V to user defined maximum
- Industrial and Extended Temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT) with independent oscillator for reliable operation
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High Endurance Flash:
 - 100,000 write Flash endurance
 - Flash retention: > 40 years

Low-Power Features:

- Standby Current:
 - 50 nA @ 2.0V, typical
- Operating Current:
 - 20 μ A @ 32 kHz, 2.0V, typical
 - 220 μ A @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
 - 1 μ A @ 2.0V, typical

Peripheral Features:

- Shunt Voltage Regulator (PIC16HV616 only):
 - 5 volt regulation
 - 4 mA to 50 mA shunt range
- 11 I/O pins and 1 input only
- High current source/sink for direct LED drive
 - Interrupt-on-Change pin
 - Individually programmable weak pull ups
- Analog Comparator module with:
 - Two analog comparators
 - Programmable on-chip voltage reference (CVREF) module (% of VDD)
 - Comparator inputs and outputs externally accessible
 - SR Latch
 - Built-In Hysteresis (user selectable)
- A/D Converter:
 - 10-bit resolution and 8 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Timer1 Gate (count enable)
 - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
 - Option to use system clock as Timer1
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Enhanced Capture, Compare, PWM module:
 - 16-bit Capture, max resolution 12.5 ns
 - Compare, max resolution 200 ns
 - 10-bit PWM with 1, 2 or 4 output channels, programmable “dead time”, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins

PIC16F616/16HV616

Device	Program Memory	Data Memory	I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit	Voltage Range
	Flash (words)	SRAM (bytes)					
PIC16F616	2048	128	11	8	2	2/1	2.0-5.5V
PIC16HV616	2048	128	11	8	2	2/1	2.0-user defined

14-Pin Diagram (PDIP, SOIC, TSSOP)

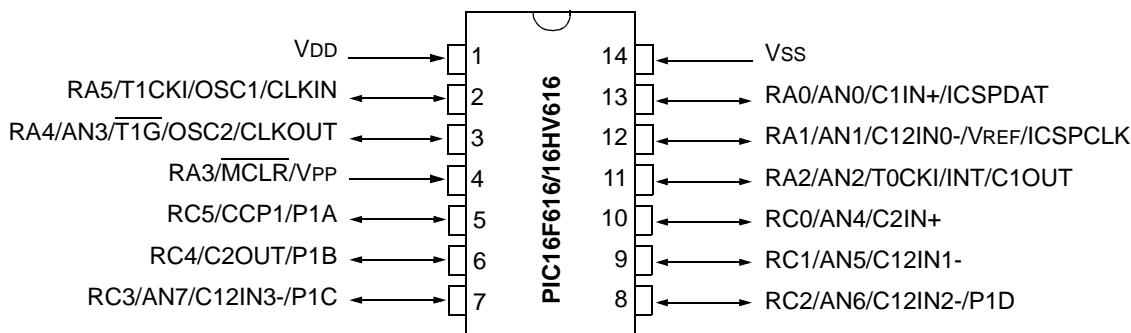


TABLE 1: DUAL IN-LINE PIN SUMMARY

I/O	Pin	Analog	Comparators	Timer	CCP	Interrupts	Pull-ups	Basic
RA0	13	AN0	C1IN+	—	—	IOC	Y	ICSPDAT
RA1	12	AN1/VREF	C12IN0-	—	—	IOC	Y	ICSPCLK
RA2	11	AN2	C1OUT	T0CKI	—	INT/IOC	Y	—
RA3 ⁽¹⁾	4	—	—	—	—	IOC	Y ⁽²⁾	MCLR/VPP
RA4	3	AN3	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	2	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RC0	10	AN4	C2IN+	—	—	—	—	—
RC1	9	AN5	C12IN1-	—	—	—	—	—
RC2	8	AN6	C12IN2-	—	P1D	—	—	—
RC3	7	AN7	C12IN3-	—	P1C	—	—	—
RC4	6	—	C2OUT	—	P1B	—	—	—
RC5	5	—	—	—	CCP1/P1A	—	—	—
—	1	—	—	—	—	—	—	VDD
—	14	—	—	—	—	—	—	Vss

Note 1: Input only.

2: Only when pin is configured for external MCLR.

16-Pin Diagram (QFN)

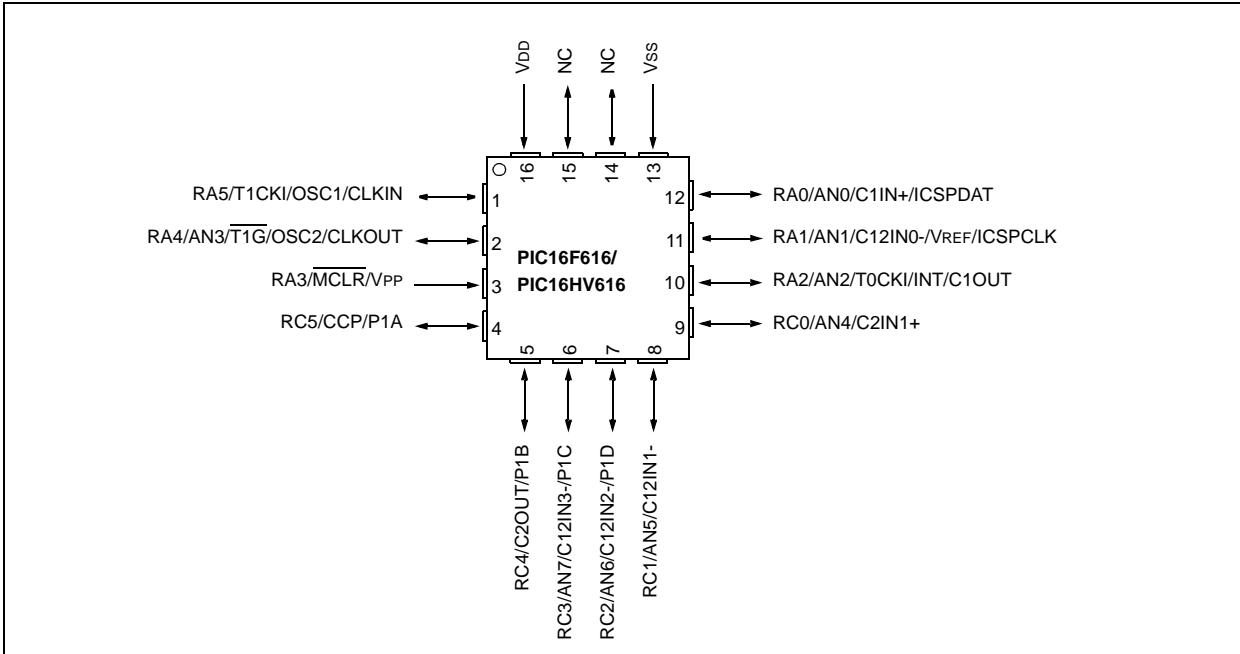


TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comparators	Timers	CCP	Interrupts	Pull-ups	Basic
RA0	12	AN0	C1IN+	—	—	IOC	Y	ICSPDAT
RA1	11	AN1/VREF	C12IN0-	—	—	IOC	Y	ICSPCLK
RA2	10	AN2	C1OUT	T0CKI	—	INT/IOC	Y	—
RA3 ⁽¹⁾	3	—	—	—	—	IOC	Y ⁽²⁾	MCLR/VPP
RA4	2	AN3	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	1	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RC0	9	AN4	C2IN+	—	—	—	—	—
RC1	8	AN5	C12IN1-	—	—	—	—	—
RC2	7	AN6	C12IN2-	—	P1D	—	—	—
RC3	6	AN7	C12IN3-	—	P1C	—	—	—
RC4	5	—	C2OUT	—	P1B	—	—	—
RC5	4	—	—	—	CCP1/P1A	—	—	—
—	16	—	—	—	—	—	—	VDD
—	13	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

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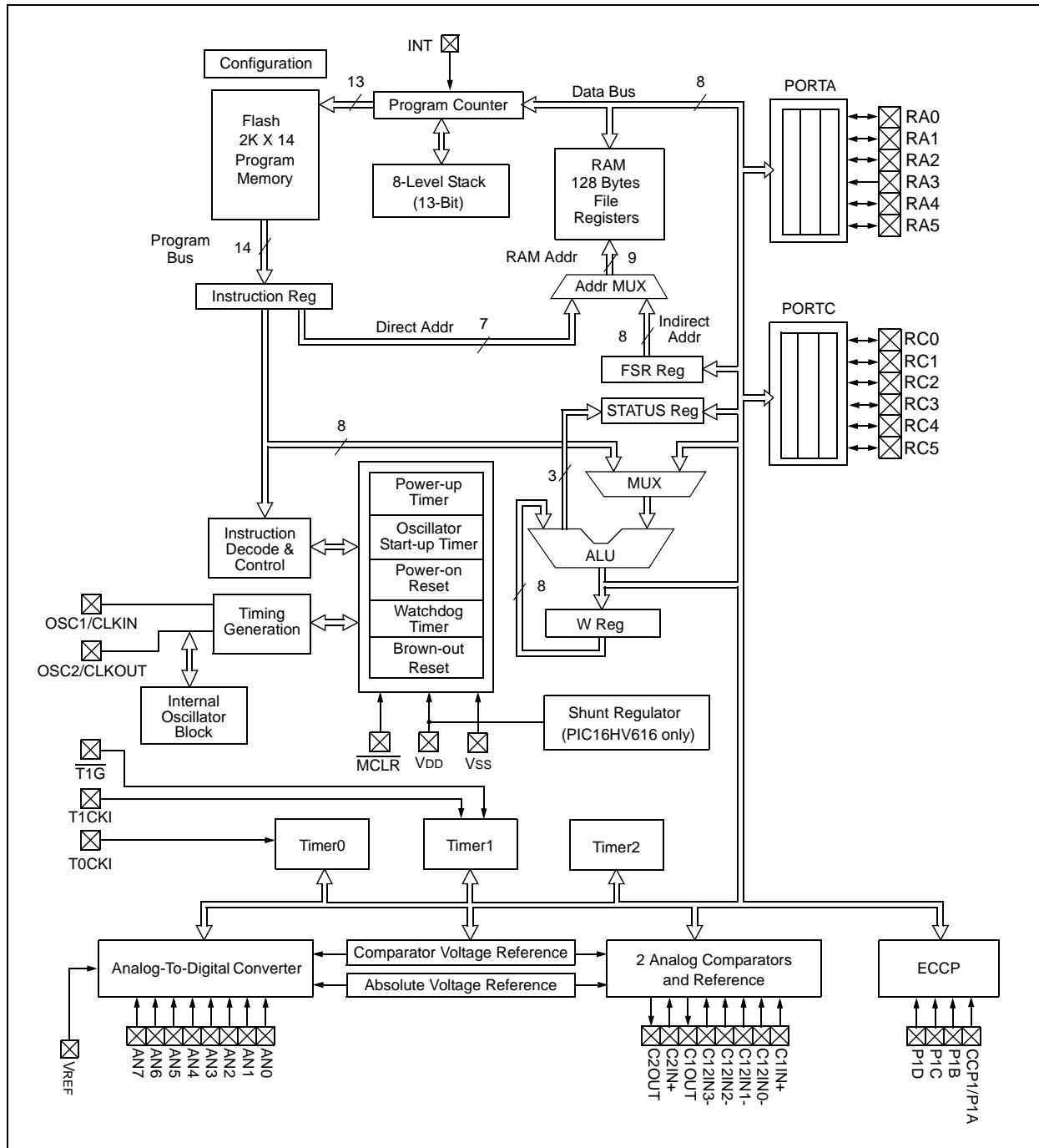
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1.0 DEVICE OVERVIEW

The PIC16F616/16HV616 is covered by this data sheet. It is available in 14-pin PDIP, SOIC, TSSOP and QFN packages. Figure 1-1 shows a block diagram of the PIC16F616/16HV616 device. Table 1-1 shows the pinout description.

FIGURE 1-1: PIC16F616/16HV616 BLOCK DIAGRAM



PIC16F616/16HV616

TABLE 1-1: PIC16F616/16HV616 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator C1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/AN1/C12IN0-/VREF/ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	C12IN0-	AN	—	Comparators C1 and C2 inverting input
	VREF	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator C1 output
RA3/ <u>MCLR</u> /VPP	RA3	TTL	—	PORTA input with interrupt-on-change
	<u>MCLR</u>	ST	—	Master Clear w/internal pull-up
	VPP	HV	—	Programming voltage
RA4/AN3/ <u>T1G</u> /OSC2/CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	<u>T1G</u>	ST	—	Timer1 gate (count enable)
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	Fosc/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
	AN4	AN	—	A/D Channel 4 input
	C2IN+	AN	—	Comparator C2 non-inverting input
RC1/AN5/C2IN-	RC1	TTL	CMOS	PORTC I/O
	AN5	AN	—	A/D Channel 5 input
	C12IN1-	AN	—	Comparators C1 and C2 inverting input
RC2/AN6/C12IN2-/P1D	RC2	TTL	CMOS	PORTC I/O
	AN6	AN	—	A/D Channel 6 input
	C12IN2-	AN	—	Comparators C1 and C2 inverting input
	P1D	—	CMOS	PWM output
RC3/AN7/P1C	RC3	TTL	CMOS	PORTC I/O
	AN7	AN	—	A/D Channel 7 input
	C12IN3-	AN	—	Comparators C1 and C2 inverting input
	P1C	—	CMOS	PWM output
RC4/C2OUT/P1B	RC4	TTL	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator C2 output
	P1B	—	CMOS	PWM output
RC5/CCP1/P1A	RC5	TTL	CMOS	PORTC I/O
	CCP1	ST	CMOS	Capture input/Compare output
	P1A	—	CMOS	PWM output
VDD	VDD	Power	—	Positive supply
VSS	VSS	Power	—	Ground reference

Legend: AN = Analog input or output

ST = Schmitt Trigger input with CMOS levels

CMOS = CMOS compatible input or output

TTL = TTL compatible input

HV = High Voltage

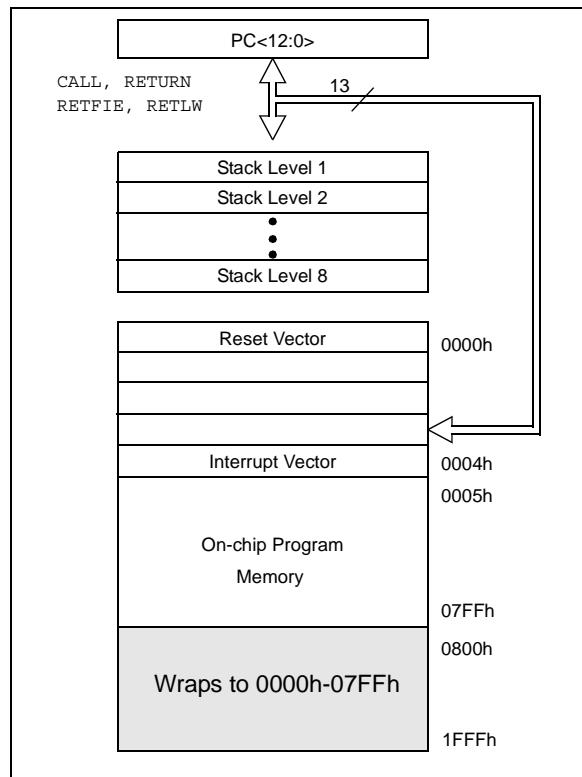
XTAL = Crystal

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F616/16HV616 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2K x 14 (0000h-07FFh) for the PIC16F616/16HV616 is physically implemented. Accessing a location above these boundaries will cause a wraparound within the first 2K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F616/16HV616



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. The RP0 bit of the STATUS register is the bank select bit.

RP0

- 0 → Bank 0 is selected
- 1 → Bank 1 is selected

Note: The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's.

PIC16F616/16HV616

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 in the PIC16F616/16HV616. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 “Indirect Addressing, INDF and FSR Registers”**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE PIC16F616/16HV616

	File Address	File Address
Indirect Addr.(1)	00h	Indirect Addr.(1)
TMR0	01h	OPTION_REG
PCL	02h	PCL
STATUS	03h	STATUS
FSR	04h	FSR
PORTA	05h	TRISA
	06h	
PORTC	07h	TRISC
	08h	
	09h	
PCLATH	0Ah	PCLATH
INTCON	0Bh	INTCON
PIR1	0Ch	PIE1
	0Dh	
TMR1L	0Eh	PCON
TMR1H	0Fh	
T1CON	10h	OSCTUNE
TMR2	11h	ANSEL
T2CON	12h	PR2
CCPR1L	13h	
CCPR1H	14h	
CCP1CON	15h	WPUA
PWM1CON	16h	IOCA
ECCPAS	17h	
	18h	
VRCON	19h	SRCON0
CM1CON0	1Ah	SRCON1
CM2CON0	1Bh	
CM2CON1	1Ch	
	1Dh	
ADRESH	1Eh	ADRESL
ADCON0	1Fh	ADCON1
	20h	General Purpose Registers 32 Bytes
General Purpose Registers 96 Bytes	6Fh	
	70h	Accesses 70h-7Fh
	7Fh	
Bank 0		Bank 1
		F0h
		FFh

PIC16F616/16HV616

TABLE 2-1: PIC16F616/16HV616 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	17, 104
01h	TMR0	Timer0 Module's Register								xxxx xxxx	37, 104
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17, 104
03h	STATUS	IRP ⁽¹⁾	RP1 ⁽¹⁾	RP0	TO	PD	Z	DC	C	0001 1xxx	11, 104
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	17, 104
05h	PORATA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	25, 104
06h	—	Unimplemented								—	—
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	33, 104
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter				---0 0000	17, 104	
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	13, 104
0Ch	PIR1	—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	15, 104
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	41, 104
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	41, 104
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	44, 104
11h	TMR2	Timer2 Module Register								0000 0000	47, 104
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	48, 104
13h	CCPR1L	Capture/Compare/PWM Register 1 Low Byte								XXXX XXXX	78, 104
14h	CCPR1H	Capture/Compare/PWM Register 1 High Byte								XXXX XXXX	78, 104
15h	CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	77, 104
16h	PWM1CON	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000	77, 104
17h	ECCPAS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000	92, 104
18h	—	Unimplemented								—	—
19h	VRCON	C1VREN	C2VREN	VR	VP6EN	VR3	VR2	VR1	VR0	0000 0000	62, 104
1Ah	CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	0000 -000	54, 104
1Bh	CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000	55, 104
1Ch	CM2CON1	MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	57, 104
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	72, 104
1Fh	ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	70, 104

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented
Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

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TABLE 2-2: PIC16F616/16HV616 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	—	—	Addressing this location uses contents of FSR to address data memory (not a physical register)	xxxx xxxx	17, 104					
81h	OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	12, 104
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17, 104
83h	STATUS	IRP ⁽¹⁾	RP1 ⁽¹⁾	RP0	TO	PD	Z	DC	C	0001 1xxx	11, 104
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	17, 104
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	25, 104
86h	—	Unimplemented								—	—
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISCO	--11 1111	33, 104
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter	---0 0000	17, 104				
8Bh	INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	13, 104
8Ch	PIE1	—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	14, 104
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	POR	BOR	---- --qq	16, 104
8Fh	—	Unimplemented								—	—
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	23, 104
91h	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	26, 104
92h	PR2	Timer2 Module Period Register								1111 1111	47, 105
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	WPUA ⁽²⁾	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	27, 105
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	27, 105
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	SRC0N0	SR1	SR0	C1SEN	C2REN	PULSS	PULSR	—	SRCLKEN	0000 00-0	59, 105
9Ah	SRC0N1	SRCS1	SRCS2	—	—	—	—	—	—	00-- ----	59, 105
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL	Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result								xxxx xxxx	72, 105
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	71, 105

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

Note 2: RA3 pull-up is enabled when MCLRE is '1' in the Configuration Word register.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uuu'

(where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 13.0 "Instruction Set Summary"**.

Note 1: Bits IRP and RP1 of the STATUS register are not used by the PIC16F616/16HV616 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	<u>TO</u>	<u>PD</u>	Z	DC	C
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	IRP: This bit is reserved and should be maintained as '0'
bit 6	RP1: This bit is reserved and should be maintained as '0'
bit 5	RP0: Register Bank Select bit (used for direct addressing) 1 = Bank 1 (80h – FFh) 0 = Bank 0 (00h – 7Fh)
bit 4	<u>TO</u> : Time-out bit 1 = After power-up, CLRWDAT instruction or SLEEP instruction 0 = A WDT time-out occurred
bit 3	<u>PD</u> : Power-down bit 1 = After power-up or by the CLRWDAT instruction 0 = By execution of the SLEEP instruction
bit 2	<u>Z</u> : Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	<u>DC</u> : Digit Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions), For Borrow, the polarity is reversed. 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result
bit 0	<u>C</u> : Carry/Borrow bit ⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions) 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

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2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External RA2/INT interrupt
- Timer0
- Weak pull-ups on PORTA

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit to '1' of the OPTION register. See **Section 5.1.3 "Software Programmable Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **RAPU:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual Port latch values
- bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/INT pin
0 = Interrupt on falling edge of RA2/INT pin
- bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on RA2/T0CKI pin
0 = Internal instruction cycle clock (Fosc/4)
- bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/T0CKI pin
0 = Increment on low-to-high transition on RA2/T0CKI pin
- bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| GIE | PEIE | TOIE | INTE | RAIE | TOIF | INTF | RAIF |
| bit 7 | bit 0 | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	TOIE: Timer0 Overflow Interrupt Enable bit 1 = Enables the Timer0 interrupt 0 = Disables the Timer0 interrupt
bit 4	INTE: RA2/INT External Interrupt Enable bit 1 = Enables the RA2/INT external interrupt 0 = Disables the RA2/INT external interrupt
bit 3	RAIE: PORTA Change Interrupt Enable bit ⁽¹⁾ 1 = Enables the PORTA change interrupt 0 = Disables the PORTA change interrupt
bit 2	TOIF: Timer0 Overflow Interrupt Flag bit ⁽²⁾ 1 = Timer0 register has overflowed (must be cleared in software) 0 = Timer0 register did not overflow
bit 1	INTF: RA2/INT External Interrupt Flag bit 1 = The RA2/INT external interrupt occurred (must be cleared in software) 0 = The RA2/INT external interrupt did not occur
bit 0	RAIF: PORTA Change Interrupt Flag bit 1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software) 0 = None of the PORTA <5:0> pins have changed state

Note 1: IOCA register must also be enabled.

2: TOIF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing TOIF bit.

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2.2.2.4 PIE1 Register

The PIE1 register contains the peripheral interrupt enable bits, as shown in Register 2-4.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit

1 = Enables the ADC interrupt

0 = Disables the ADC interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit

1 = Enables the CCP1 interrupt

0 = Disables the CCP1 interrupt

bit 4 **C2IE:** Comparator C2 Interrupt Enable bit

1 = Enables the Comparator C2 interrupt

0 = Disables the Comparator C2 interrupt

bit 3 **C1IE:** Comparator C1 Interrupt Enable bit

1 = Enables the Comparator C1 interrupt

0 = Disables the Comparator C1 interrupt

bit 2 **Unimplemented:** Read as '0'

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit

1 = Enables the Timer2 to PR2 match interrupt

0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit

1 = Enables the Timer1 overflow interrupt

0 = Disables the Timer1 overflow interrupt

2.2.2.5 PIR1 Register

The PIR1 register contains the peripheral interrupt flag bits, as shown in Register 2-5.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIF:** A/D Interrupt Flag bit

1 = A/D conversion complete

0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

bit 4 **C2IF:** Comparator C2 Interrupt Flag bit

1 = Comparator C2 output has changed (must be cleared in software)

0 = Comparator C2 output has not changed

bit 3 **C1IF:** Comparator C1 Interrupt Flag bit

1 = Comparator C1 output has changed (must be cleared in software)

0 = Comparator C1 output has not changed

bit 2 **Unimplemented:** Read as '0'

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit

1 = Timer2 to PR2 match occurred (must be cleared in software)

0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit

1 = Timer1 register overflowed (must be cleared in software)

0 = Timer1 has not overflowed

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2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 11-2) contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the software enable of the BOR.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0 ⁽¹⁾
—	—	—	—	—	—	<u>POR</u>	<u>BOR</u>
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **POR:** Power-on Reset Status bit

 1 = No Power-on Reset occurred

 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR:** Brown-out Reset Status bit

 1 = No Brown-out Reset occurred

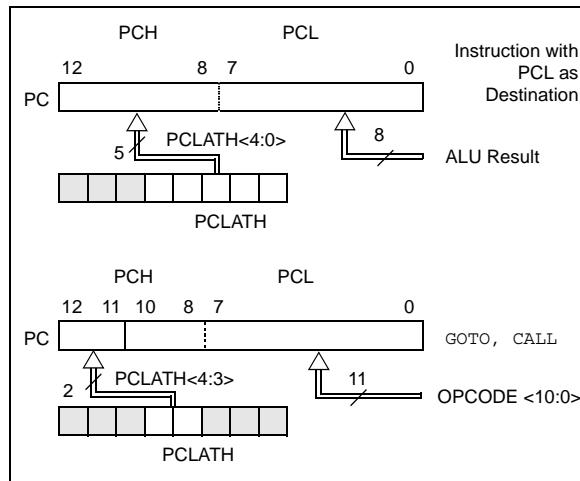
 0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: Reads as '0' if Brown-out Reset is disabled.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). Care should be exercised when jumping into a look-up table or program branch table (computed GOTO) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "Implementing a Table Read" (DS00556).

2.3.2 STACK

The PIC16F616/16HV616 Family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1:** There are no Status bits to indicate stack overflow or stack underflow conditions.
- 2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

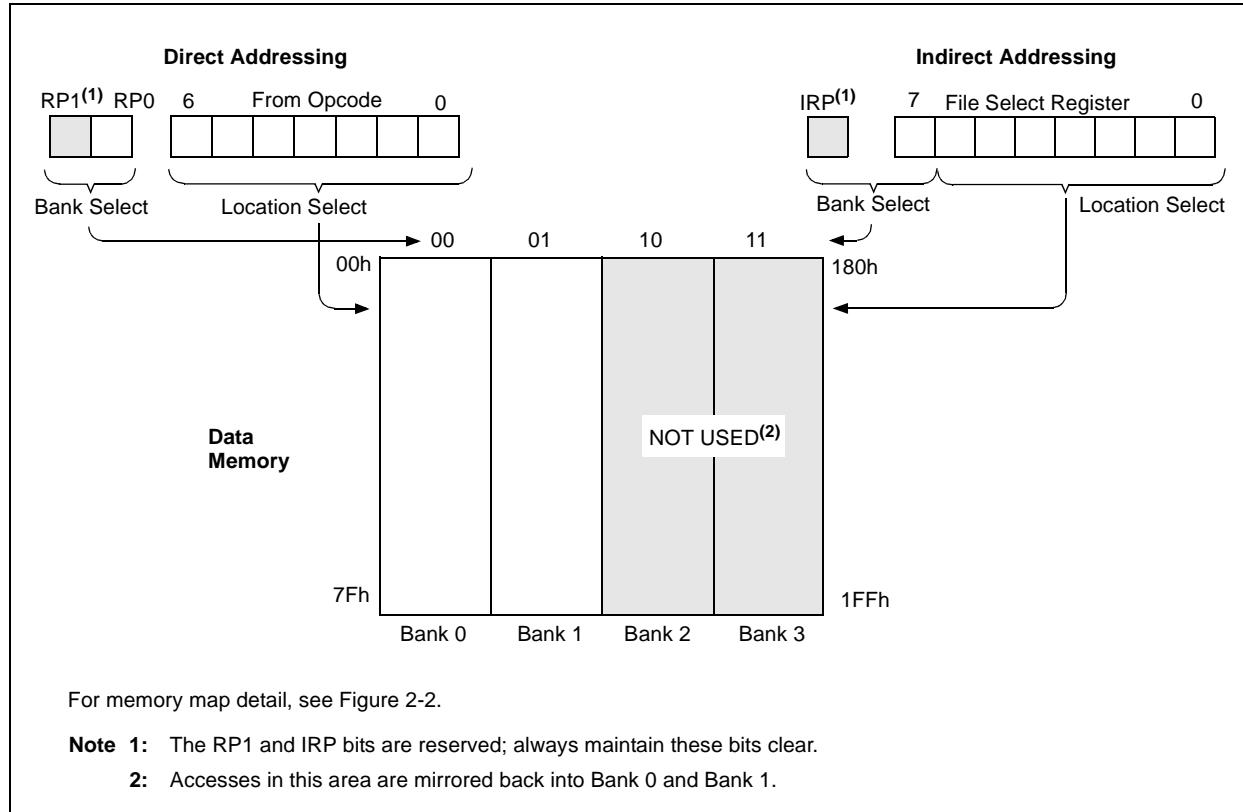
EXAMPLE 2-1: INDIRECT ADDRESSING

```

        MOVLW 0x20 ;initialize pointer
        MOVWF FSR ;to RAM
NEXT   CLRF INDF ;clear INDF register
        INCF FSR ;inc pointer
        BTFSS FSR,4 ;all done?
        GOTO NEXT ;no clear next
CONTINUE          ;yes continue
    
```

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FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F616/16HV616



3.0 OSCILLATOR MODULE

3.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the Oscillator module.

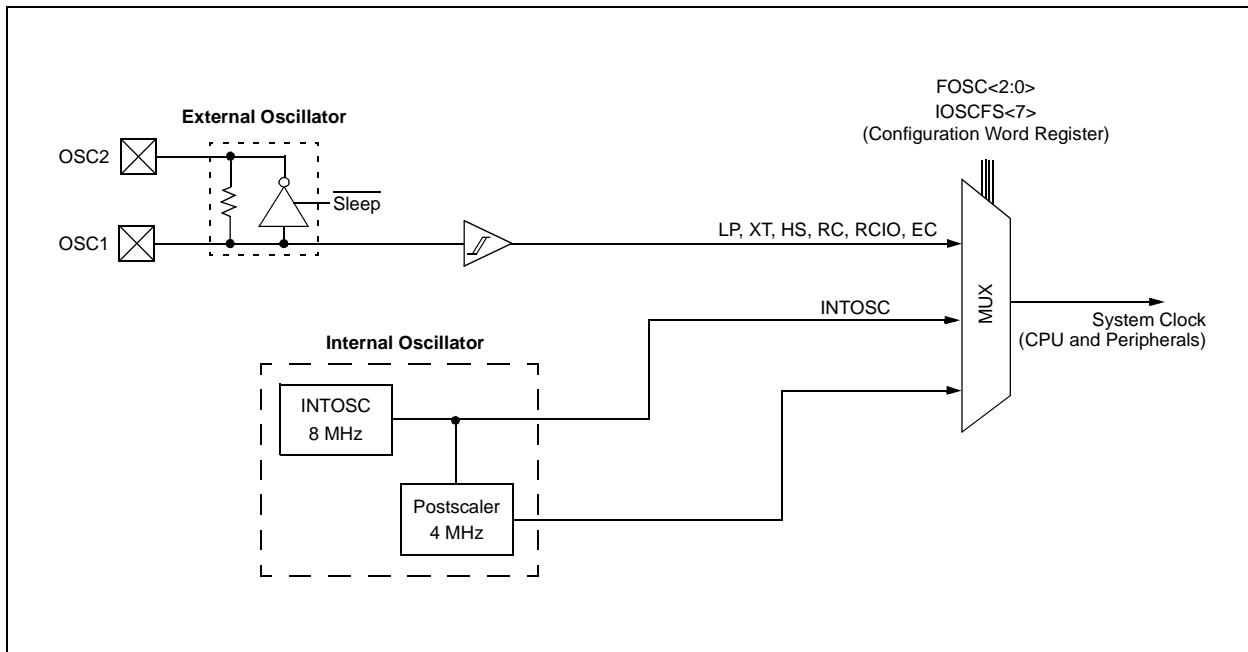
Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured with a choice of two selectable speeds: internal or external system clock source.

The Oscillator module can be configured in one of eight clock modes.

1. EC – External clock with I/O on OSC2/CLKOUT.
2. LP – 32 kHz Low-Power Crystal mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
6. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
7. INTOSC – Internal oscillator with Fosc/4 output on OSC1 and I/O on OSC1/CLKIN.
8. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The Internal Oscillator module provides a selectable system clock mode of either 4 MHz (Postscaler) or 8 MHz (INTOSC).

FIGURE 3-1: PICmicro® MCU CLOCK SOURCE BLOCK DIAGRAM



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3.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two selectable clock frequencies: 4 MHz and 8 MHz

The system clock can be selected between external or internal clock sources via the FOSC<2:0> bits of the Configuration Word register.

3.3 External Clock Modes

3.3.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

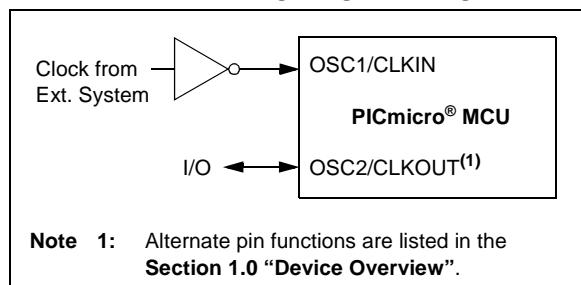
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	INTOSC	125 kHz to 8 MHz	Oscillator Warm-Up Delay (TWARM)
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)

3.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PICmicro® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION



3.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 3-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

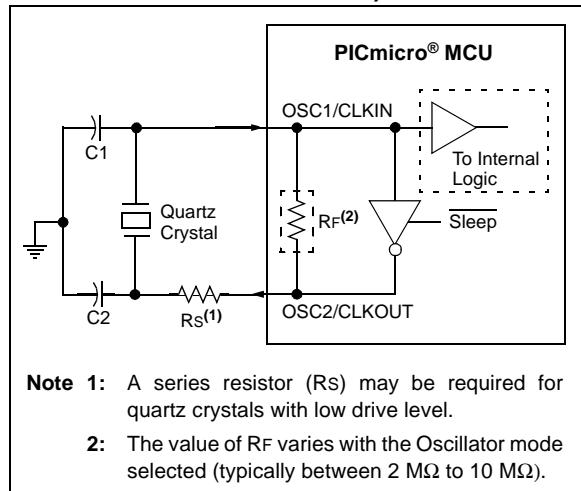
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

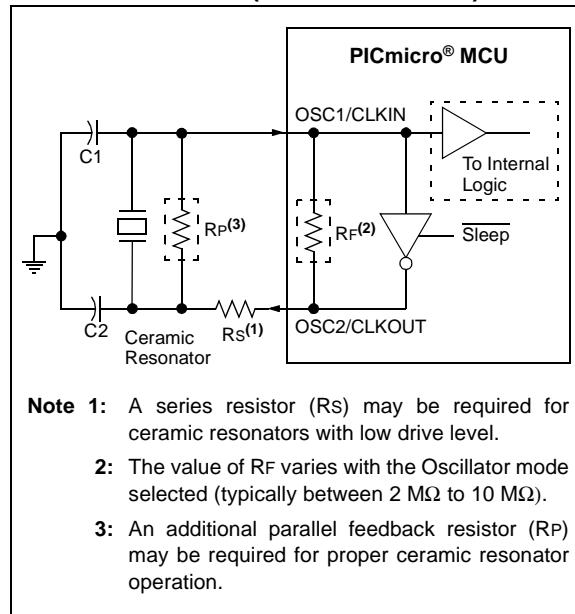
FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

- 2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.
- 3:** For oscillator design assistance, reference the following Microchip Applications Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC® and PICmicro® Devices" (DS00826)
 - AN849, "Basic PICmicro® Oscillator Design" (DS00849)
 - AN943, "Practical PICmicro® Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)

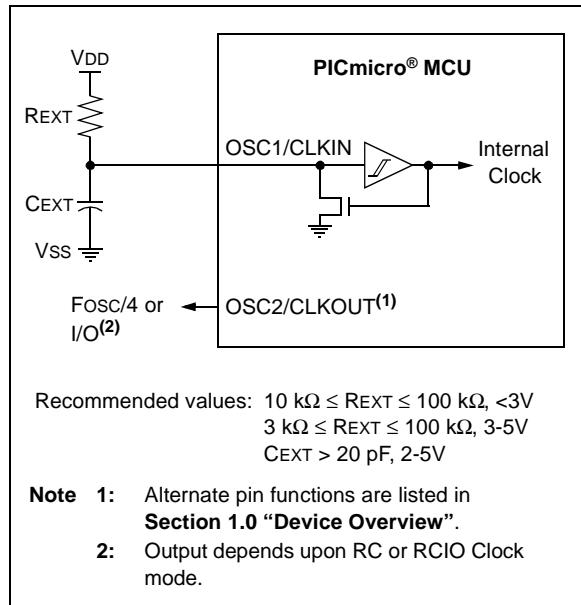


3.3.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.

FIGURE 3-5: EXTERNAL RC MODES



In RC mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.4 Internal Clock Modes

The Oscillator module provides a selectable system clock source of either 4 MHz or 8 MHz. The selectable frequency is configured through the IOSCFS bit of the Configuration Word.

The frequency of the internal oscillator can be trimmed with a calibration value in the OSCTUNE register.

3.4.1 INTOSC AND INTOSCIOS MODES

The INTOSC and INTOSCIOS modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 11.0 “Special Features of the CPU”** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIOS** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

3.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency

01110 =

•

•

•

00001 =

00000 = Oscillator module is running at the calibrated frequency.

11111 =

•

•

•

10000 = Minimum frequency

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	IOSCFS	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 11-1) for operation of all register bits.

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NOTES:

4.0 I/O PORTS

There are as many as twelve general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 PORTA and the TRISA Registers

PORTA is a 6-bit wide, bidirectional Port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '1'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the Port latch. All write operations are read-modify-write operations. Therefore, a write to a Port implies that the

REGISTER 4-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-0	R-x	R/W-0	R/W-0	R/W-0
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RA<5:0>:** PORTA I/O Pin bit

1 = PORTA pin is > VIH

0 = PORTA pin is < VIL

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit

1 = PORTA pin configured as an input (tri-stated)

0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.

2: TRISA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

Port pins are read, this value is modified and then written to the Port data latch. RA3 reads '0' when MCLRE = 1.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note: The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

EXAMPLE 4-1: INITIALIZING PORTA

```

BCF STATUS,RP0      ;Bank 0
CLRF PORTA          ;Init PORTA
BSF STATUS,RP0      ;Bank 1
CLRF ANSEL          ;digital I/O
MOVLW 0Ch           ;Set RA<3:2> as inputs
MOVWF TRISA         ;and set RA<5:4,1:0>
                     ;as outputs
BCF STATUS,RP0      ;Bank 0

```

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4.2 Additional Pin Functions

Every PORTA pin on the PIC16F616/16HV616 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

4.2.1 ANSEL REGISTER

The ANSEL register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected Port.

4.2.2 WEAK PULL-UPS

Each of the PORTA pins, except RA3, has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-4. Each weak pull-up is automatically turned off when the Port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the RAPU bit of the OPTION register). A weak pull-up is automatically enabled for RA3 when configured as MCLR and disabled when RA3 is an I/O. There is no software control of the MCLR pull-up.

4.2.3 INTERRUPT-ON-CHANGE

Each PORTA pin is individually configurable as an interrupt-on-change pin. Control bits IOC_{Ax} enable or disable the interrupt function for each pin. Refer to Register 4-5. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set the PORTA Change Interrupt Flag bit (RAIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

- Any read or write of PORTA. This will end the mismatch condition, then,
- Clear the flag bit RAIF.

A mismatch condition will continue to set flag bit RAIF. Reading PORTA will end the mismatch condition and allow flag bit RAIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOR Reset. After these resets, the RAIF flag will continue to be set if a mismatch is present.

Note: If a change on the I/O pin should occur when any PORTA operation is being executed, then the RAIF interrupt flag may not get set.

REGISTER 4-3: ANSEL: ANALOG SELECT REGISTER

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ANS7 | ANS6 | ANS5 | ANS4 | ANS3 | ANS2 | ANS1 | ANS0 |
| bit 7 | bit 0 | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

ANS<7:0>: Analog Select bits

Analog select between analog or digital function on pins AN<7:0>, respectively.

1 = Analog input. Pin is assigned as analog input⁽¹⁾.

0 = Digital I/O. Pin is assigned to Port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 4-4: WPUA: WEAK PULL-UP PORTA REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **WPUA<5:4>:** Weak Pull-up Control bits

 1 = Pull-up enabled

 0 = Pull-up disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **WPUA<2:0>:** Weak Pull-up Control bits

 1 = Pull-up enabled

 0 = Pull-up disabled

Note 1: Global RAPU must be enabled for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).

3: The RA3 pull-up is enabled when configured as MCLR and disabled as an I/O in the Configuration Word.

4: WPUA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

REGISTER 4-5: IOCA: INTERRUPT-ON-CHANGE PORTA REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCA<5:0>:** Interrupt-on-change PORTA Control bit

 1 = Interrupt-on-change enabled

 0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.

2: IOCA<5:4> always reads '1' in XT, HS and LP Oscillator modes.

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4.2.4 PIN DESCRIPTIONS AND DIAGRAMS

Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the Comparator or the ADC, refer to the appropriate section in this data sheet.

4.2.4.1 RA0/AN0/C1IN+/ICSPDAT

Figure 4-1 shows the diagram for this pin. The RA0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog non-inverting input to the comparator
- In-Circuit Serial Programming data

FIGURE 4-1: BLOCK DIAGRAM OF RA0

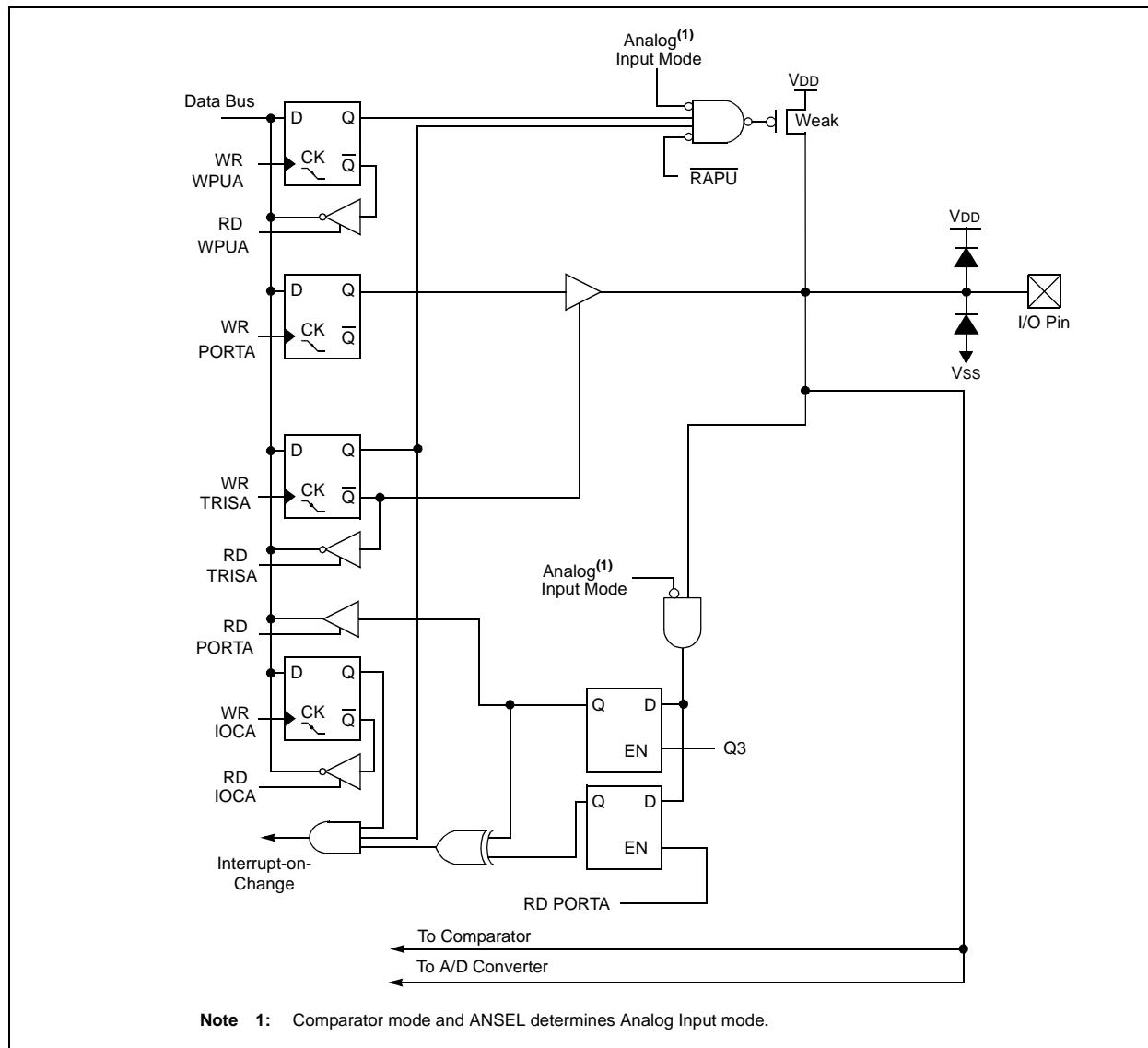
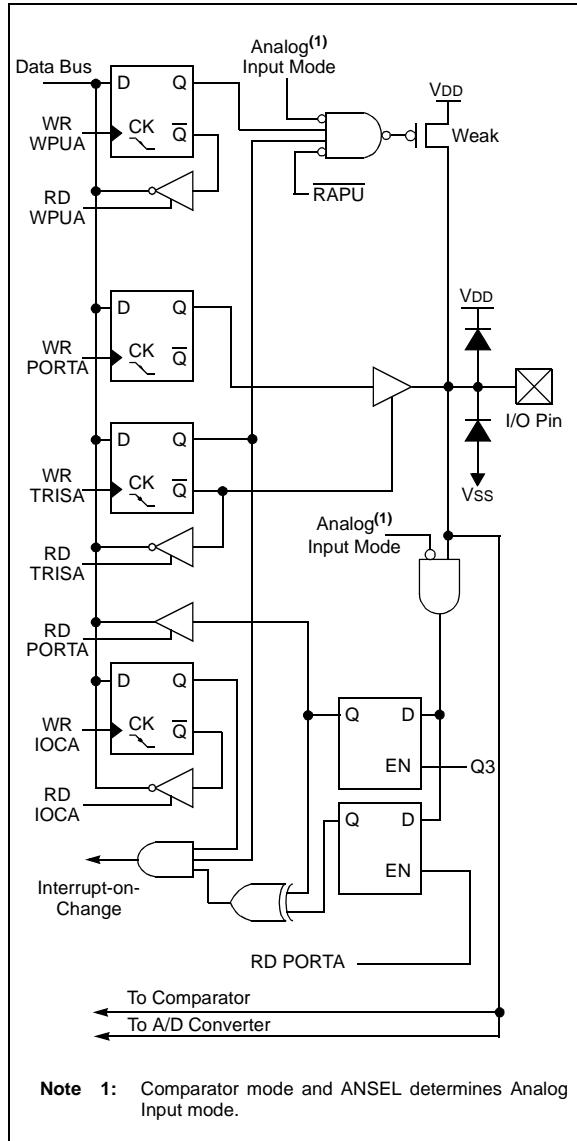


FIGURE 4-2: BLOCK DIAGRAM OF RA1



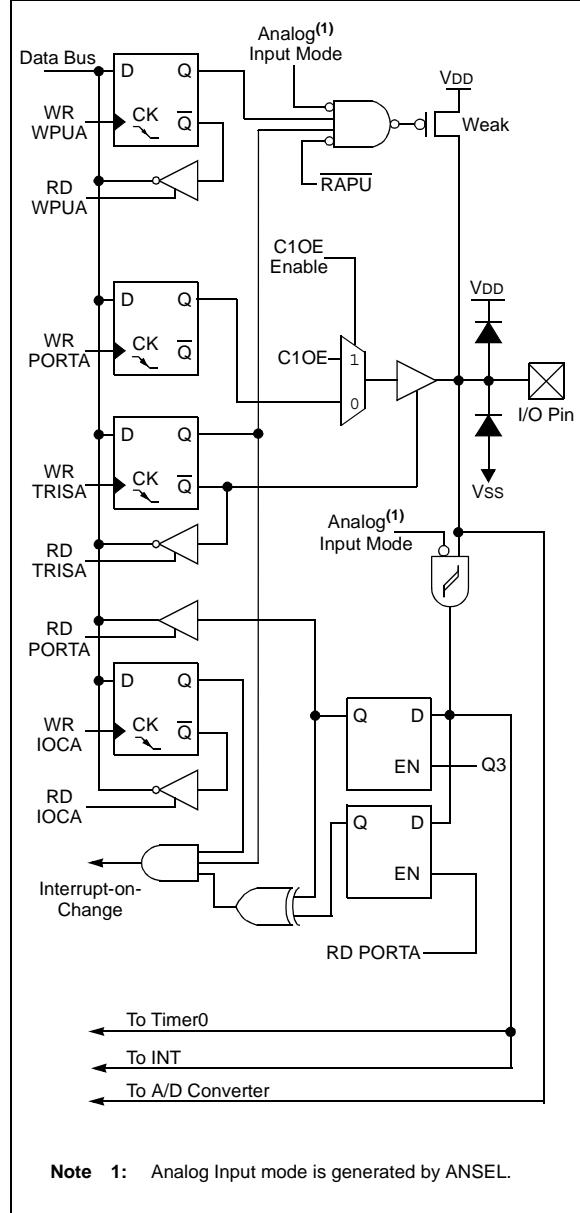
Note 1: Comparator mode and ANSEL determines Analog Input mode.

4.2.4.3 RA2/AN2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from Comparator C1

FIGURE 4-3: BLOCK DIAGRAM OF RA2



Note 1: Analog Input mode is generated by ANSEL.

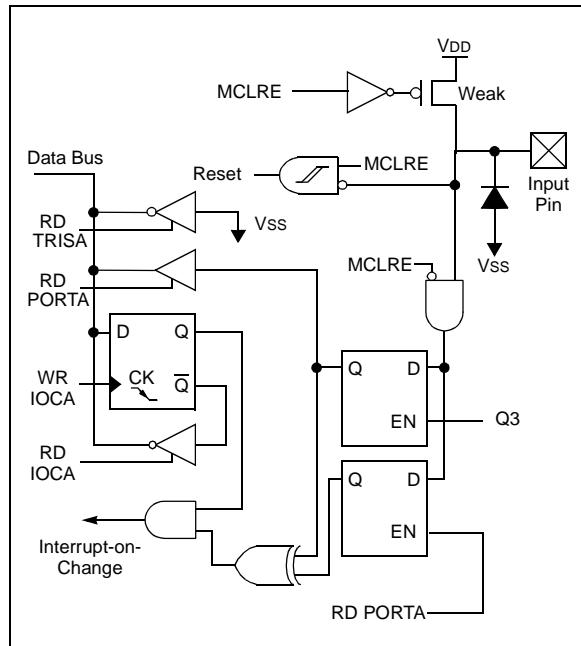
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4.2.4.4 RA3/MCLR/VPP

Figure 4-4 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up

FIGURE 4-4: BLOCK DIAGRAM OF RA3

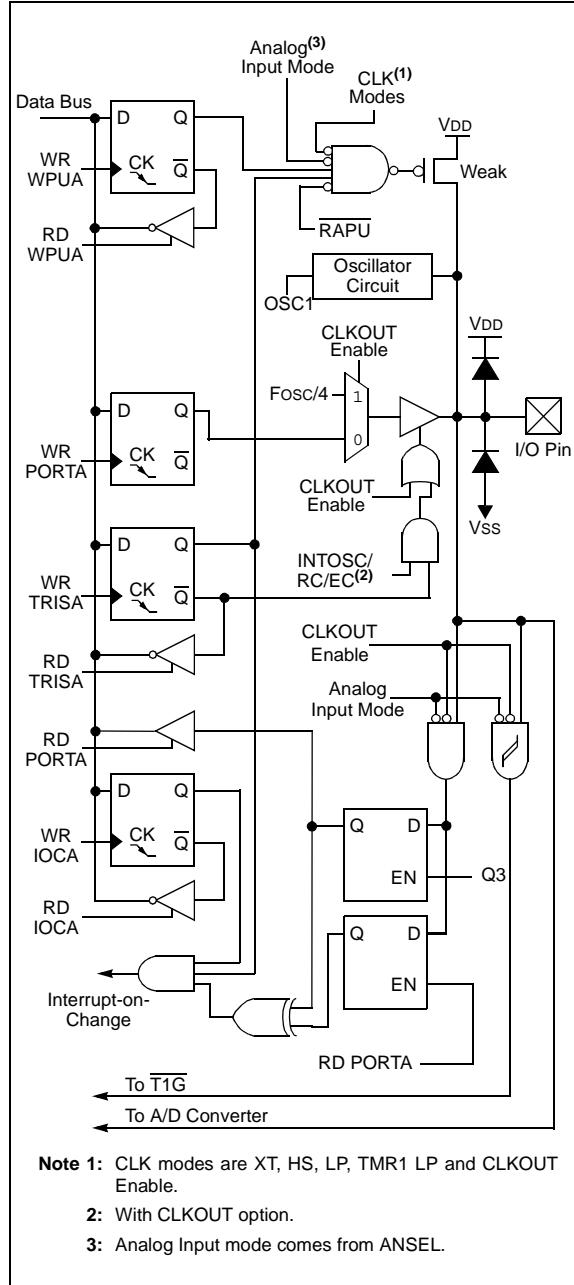


4.2.4.5 RA4/AN3/T1G/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a Timer1 gate (count enable)
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: CLK modes are XT, HS, LP, TMR1 LP and CLKOUT Enable.

2: With CLKOUT option.

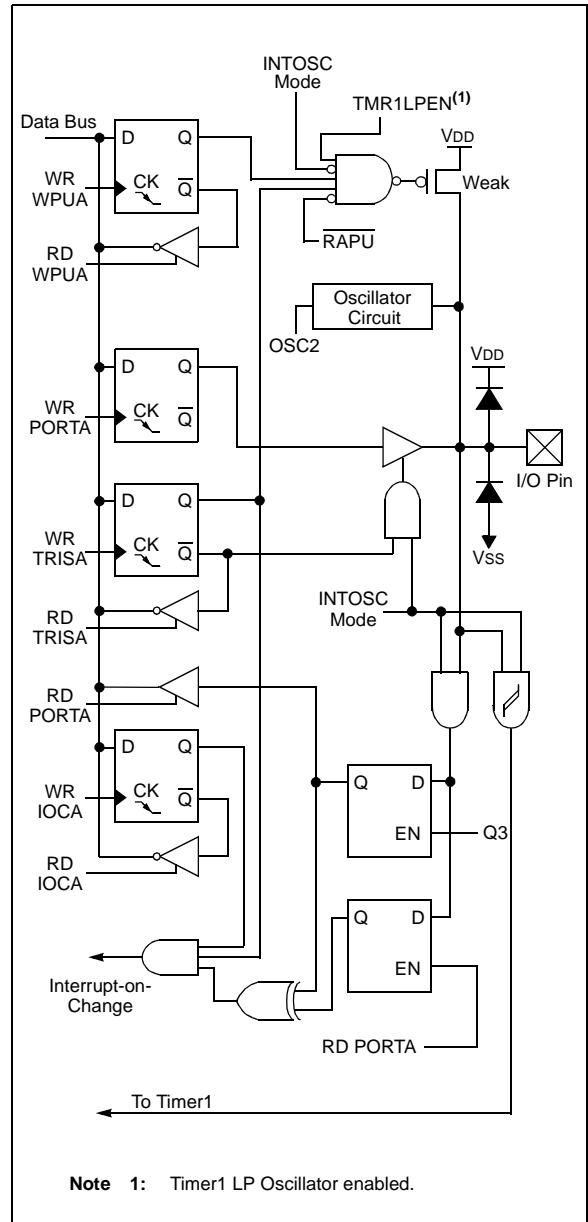
3: Analog Input mode comes from ANSEL.

4.2.4.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5



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TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1P	C1CH1	C1CH0	0000 -000	0000 -000
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--u0 u000
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
WPUA	—	—	WPUA5	WPUA4	—	WPUA2	WPUA1	WPUA0	--11 -111	--11 -111

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

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4.3.1 RC0/AN4/C2IN+

The RC0 is configurable to function as one of the following:

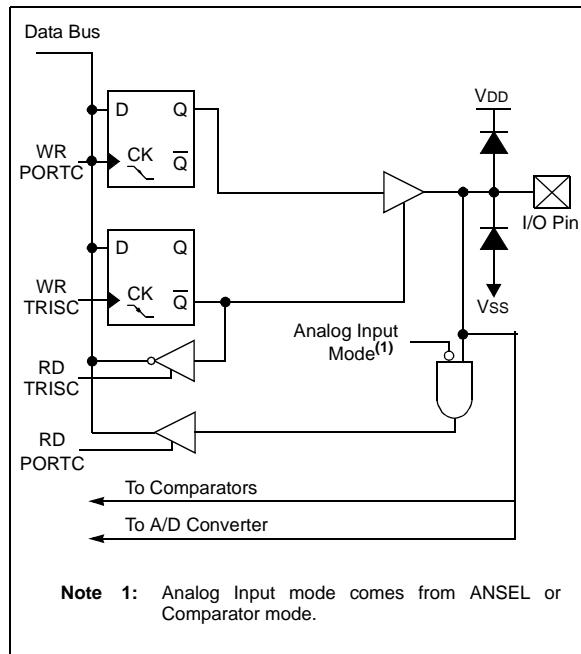
- a general purpose I/O
- an analog input for the ADC
- an analog non-inverting input to Comparator C2

4.3.2 RC1/AN5/C12IN1-

The RC1 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog inverting input to the comparator

FIGURE 4-7: BLOCK DIAGRAM OF RC0 AND RC1



4.3.3 RC2/AN6/C12IN2-/P1D

The RC2 is configurable to function as one of the following:

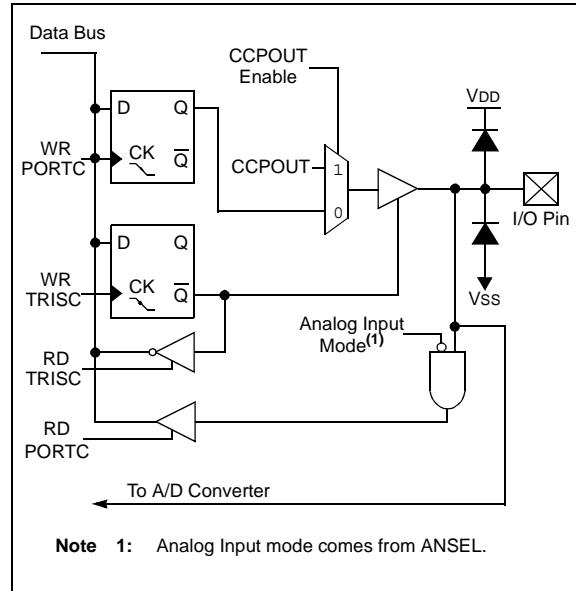
- a general purpose I/O
- an analog input for the ADC
- a digital output from the Enhanced CCP
- an analog input to Comparators C1 and C2

4.3.4 RC3/AN7/C12IN3-/P1C

The RC3 is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a digital output from the Enhanced CCP
- an analog inverting input to Comparators C1 and C2

FIGURE 4-8: BLOCK DIAGRAM OF RC2 AND RC3



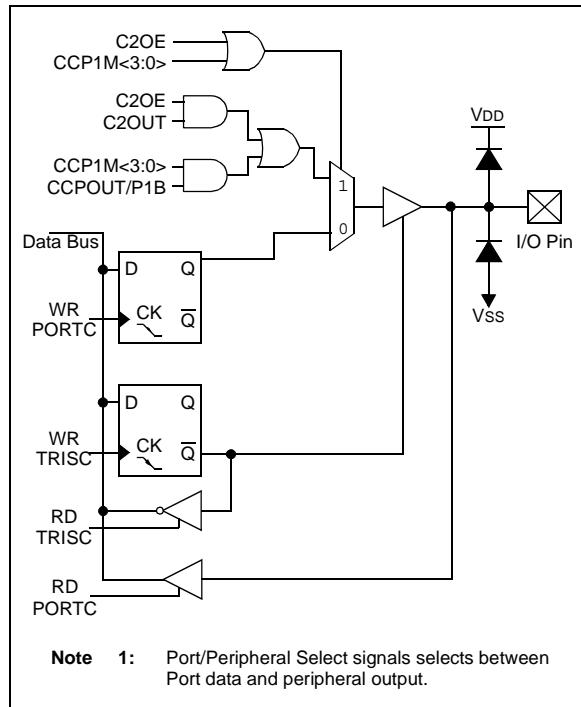
4.3.5 RC4/C2OUT/P1B

The RC4 is configurable to function as one of the following:

- a general purpose I/O
- a digital output from Comparator C2
- a digital output from the Enhanced CCP

Note: Enabling both C2OUT and P1B will cause a conflict on RC4 and create unpredictable results. Therefore, if C2OUT is enabled, the ECCP can not be used in Half-Bridge or Full-Bridge mode and vice-versa.

FIGURE 4-9: BLOCK DIAGRAM OF RC4



4.3.6 RC5/CCP1/P1A

The RC5 is configurable to function as one of the following:

- a general purpose I/O
- a digital input/output for the Enhanced CCP

FIGURE 4-10: BLOCK DIAGRAM OF RC5 PIN

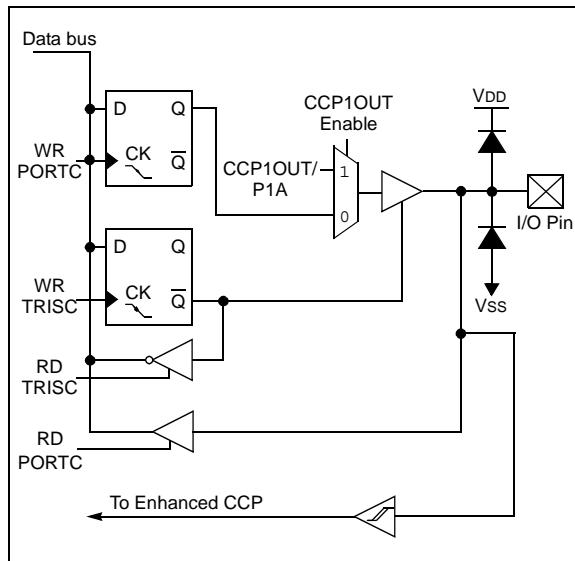


TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CCP1CON	P1M1	P1M0	DCB1	DCB0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	0000 -000	0000 -000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000	0000 -000
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	--uu 00uu
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

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NOTES:

5.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 5-1 is a block diagram of the Timer0 module.

5.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

5.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.

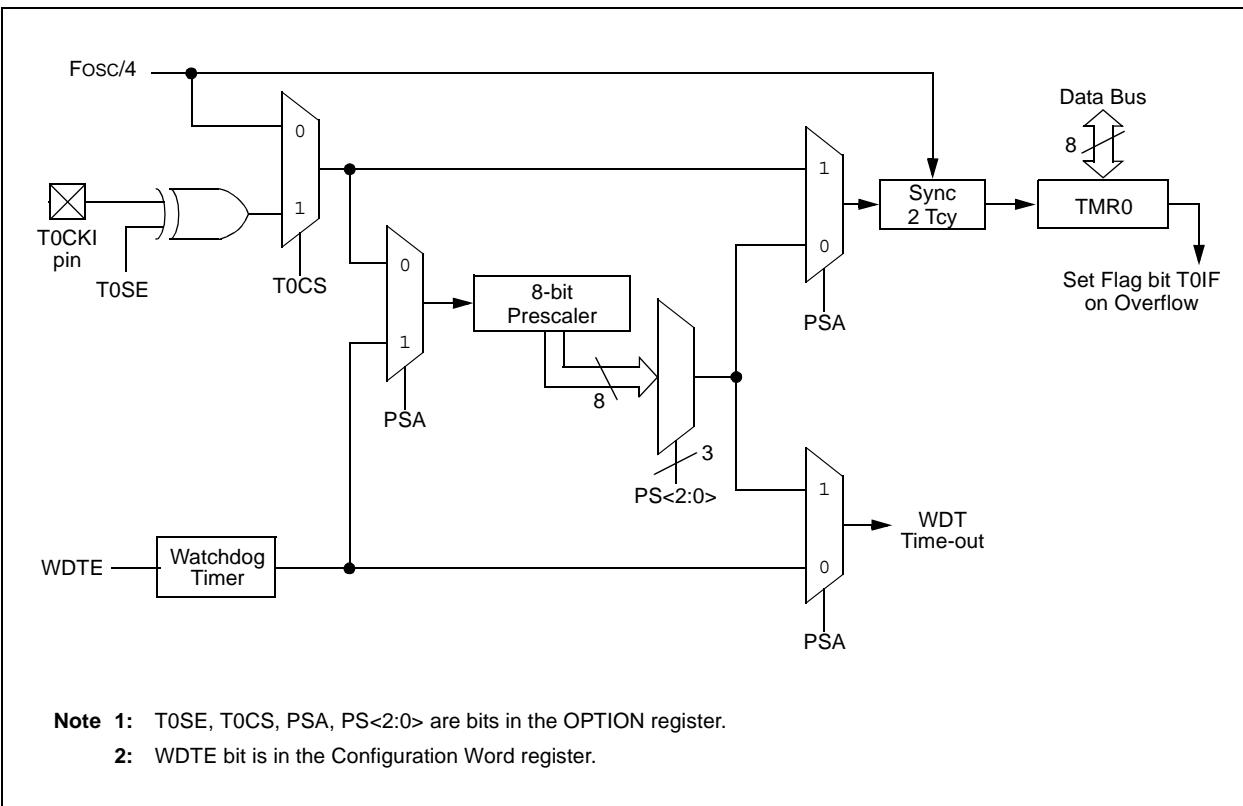
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

5.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



5.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

When the prescaler is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

5.1.3.1 Switching Prescaler Between Timer0 and WDT Modules

As a result of having the prescaler assigned to either Timer0 or the WDT, it is possible to generate an unintended device Reset when switching prescaler values. When changing the prescaler assignment from Timer0 to the WDT module, the instruction sequence shown in Example 5-1 must be executed.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0 → WDT)

```
BANKSEL TMRO      ;  
CLRWDT          ;Clear WDT  
CLRF  TMRO       ;Clear TMR0 and  
                 ;prescaler  
BANKSEL OPTION_REG ;  
BSF   OPTION_REG,PSA ;Select WDT  
CLRWDT          ;  
                 ;  
MOVLW b'11111000' ;Mask prescaler  
ANDWF OPTION_REG,W ;bits  
IORLW b'00000101' ;Set WDT prescaler  
MOVWF OPTION_REG  ;to 1:32
```

When changing the prescaler assignment from the WDT to the Timer0 module, the following instruction sequence must be executed (see Example 5-2).

EXAMPLE 5-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDT          ;Clear WDT and  
                 ;prescaler  
BANKSEL OPTION_REG ;  
MOVLW b'11110000' ;Mask TMR0 select and  
ANDWF OPTION_REG,W ;prescaler bits  
IORLW b'00000011' ;Set prescale to 1:16  
MOVWF OPTION_REG  ;
```

5.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The T0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The T0IF bit must be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

5.1.5 USING TIMER0 WITH AN EXTERNAL CLOCK

When Timer0 is in Counter mode, the synchronization of the T0CKI input and the Timer0 register is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, the high and low periods of the external clock source must meet the timing requirements as shown in **Section 15.0 “Electrical Specifications”**.

REGISTER 5-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	RAPU: PORTA Pull-up Enable bit 1 = PORTA pull-ups are disabled 0 = PORTA pull-ups are enabled by individual Port latch values																											
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of INT pin 0 = Interrupt on falling edge of INT pin																											
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on T0CKI pin 0 = Internal instruction cycle clock (Fosc/4)																											
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-high transition on T0CKI pin																											
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module																											
bit 2-0	PS<2:0>: Prescaler Rate Select bits																											
	<table border="1"> <thead> <tr> <th>BIT VALUE</th> <th>TMR0 RATE</th> <th>WDT RATE</th> </tr> </thead> <tbody> <tr><td>000</td><td>1 : 2</td><td>1 : 1</td></tr> <tr><td>001</td><td>1 : 4</td><td>1 : 2</td></tr> <tr><td>010</td><td>1 : 8</td><td>1 : 4</td></tr> <tr><td>011</td><td>1 : 16</td><td>1 : 8</td></tr> <tr><td>100</td><td>1 : 32</td><td>1 : 16</td></tr> <tr><td>101</td><td>1 : 64</td><td>1 : 32</td></tr> <tr><td>110</td><td>1 : 128</td><td>1 : 64</td></tr> <tr><td>111</td><td>1 : 256</td><td>1 : 128</td></tr> </tbody> </table>	BIT VALUE	TMR0 RATE	WDT RATE	000	1 : 2	1 : 1	001	1 : 4	1 : 2	010	1 : 8	1 : 4	011	1 : 16	1 : 8	100	1 : 32	1 : 16	101	1 : 64	1 : 32	110	1 : 128	1 : 64	111	1 : 256	1 : 128
BIT VALUE	TMR0 RATE	WDT RATE																										
000	1 : 2	1 : 1																										
001	1 : 4	1 : 2																										
010	1 : 8	1 : 4																										
011	1 : 16	1 : 8																										
100	1 : 32	1 : 16																										
101	1 : 64	1 : 32																										
110	1 : 128	1 : 64																										
111	1 : 256	1 : 128																										

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
TMR0	Timer0 Modules Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	TOIE	INTE	RAIE	TOIF	INTF	RAIF	0000 0000	0000 0000
OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISA	—	—	TRISAS5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

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NOTES:

6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or T1G pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with CCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

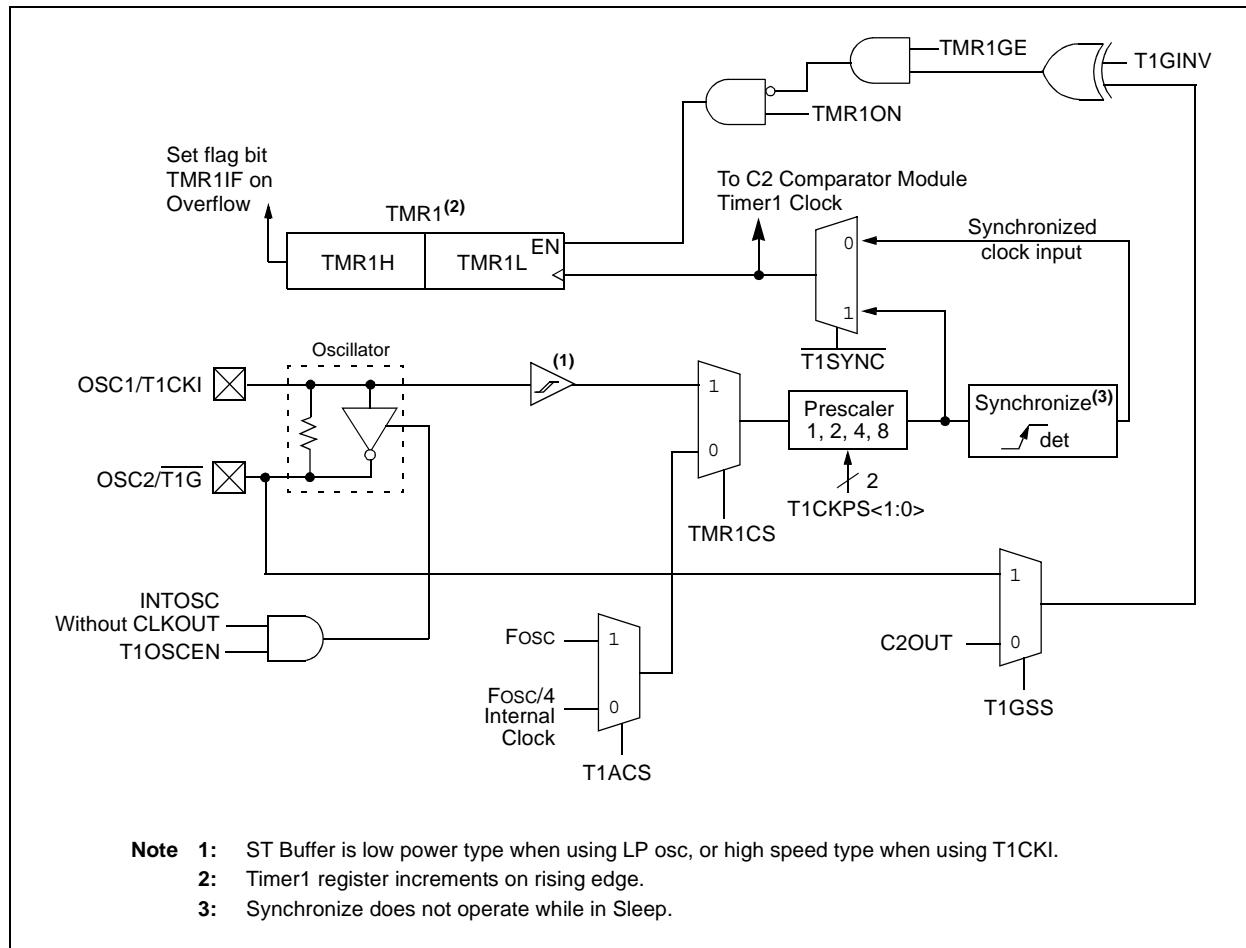
When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is Fosc/4. When TMR1CS = 1, the clock source is supplied externally.

Clock Source	TMR1CS	T1ACS
Fosc/4	0	0
Fosc	0	1
T1CKI pin	1	x

FIGURE 6-1: TIMER1 BLOCK DIAGRAM



6.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMR1H:TMR1L register pair will increment on multiples of FOSC as determined by the Timer1 prescaler.

6.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

6.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

6.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (amplifier output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when the oscillator is in the LP mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISA5 and TRISA4 bits are set when the Timer1 oscillator is enabled. RA5 and RA4 bits read as '0' and TRISA5 and TRISA4 bits read as '1'.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

6.6 Timer1 Gate

Timer1 gate source is software configurable to be the T1G pin or the output of Comparator C2. This allows the device to directly time external events using T1G or analog events using Comparator C2. See the CM2CON1 register (Register 8-3) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

Note: TMR1GE bit of the T1CON register must be set to use either T1G or C2OUT as the Timer1 gate source. See the CM2CON1 register (Register 8-3) for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the T1G pin or Comparator C2 output. This configures Timer1 to measure either the active-high or active-low time between events.

6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register
- T1SYNC bit of the T1CON register
- TMR1CS bit of the T1CON register
- T1OSCEN bit of the T1CON register (can be set)

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

6.9 ECCP Capture/Compare Time Base

The ECCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCP1H:CCP1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCP1H:CCP1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 10.0 “Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module”**.

6.10 ECCP Special Event Trigger

When the ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCP1H:CCP1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the Fosc to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 10.2.4 “Special Event Trigger”**.

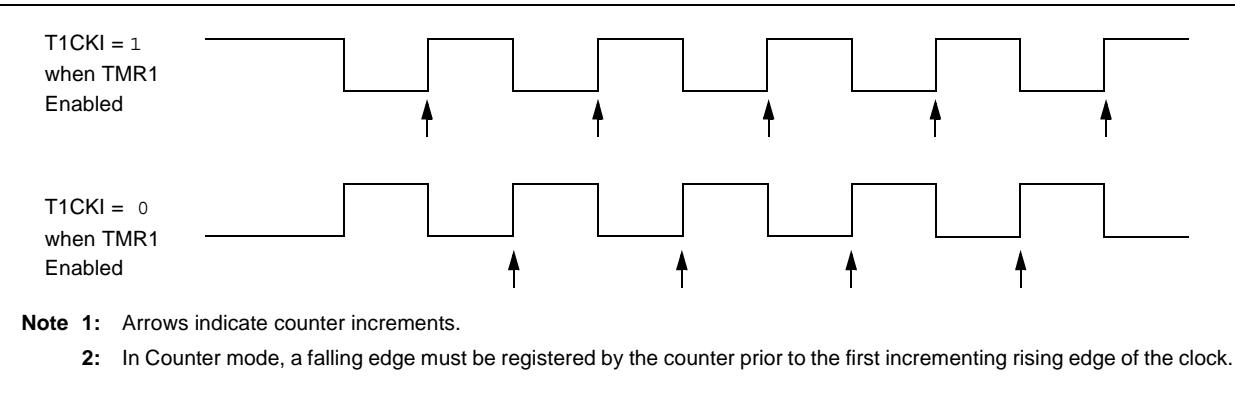
6.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 8.8.2 “Synchronizing Comparator C2 Output to Timer1”**.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



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6.12 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER 1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV ⁽¹⁾	TMR1GE ⁽²⁾	T1CKPS1	T1CKPS0	T1OSCEN	<u>T1SYNC</u>	TMR1CS	TMR1ON
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **T1GINV:** Timer1 Gate Invert bit⁽¹⁾

1 = Timer1 gate is active high (Timer1 counts when gate is high)

0 = Timer1 gate is active low (Timer1 counts when gate is low)

bit 6 **TMR1GE:** Timer1 Gate Enable bit⁽²⁾

If TMR1ON = 0:

This bit is ignored

If TMR1ON = 1:

1 = Timer1 is on if Timer1 gate is not active

0 = Timer1 is on

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale Value

10 = 1:4 Prescale Value

01 = 1:2 Prescale Value

00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit

If INTOSC without CLKOUT oscillator is active:

1 = LP oscillator is enabled for Timer1 clock

0 = LP oscillator is off

Else:

This bit is ignored

bit 2 **T1SYNC:** Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1:

1 = Do not synchronize external clock input

0 = Synchronize external clock input

TMR1CS = 0:

This bit is ignored. Timer1 uses the internal clock

bit 1 **TMR1CS:** Timer1 Clock Source Select bit

1 = External clock from T1CKI pin (on the rising edge)

0 = Internal clock (Fosc/4)

bit 0 **TMR1ON:** Timer1 On bit

1 = Enables Timer1

0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either T1G pin or C2OUT, as selected by the T1GSS bit of the CM2CON1 register, as a Timer1 gate source.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000	0000 -000
CM2CON1	MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	00-0 0010
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	-000 0-00
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register							xxxx xxxx	uuuu uuuu	
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register							xxxx xxxx	uuuu uuuu	
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

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NOTES:

7.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 7-1 for a block diagram of Timer2.

7.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock ($F_{osc}/4$). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

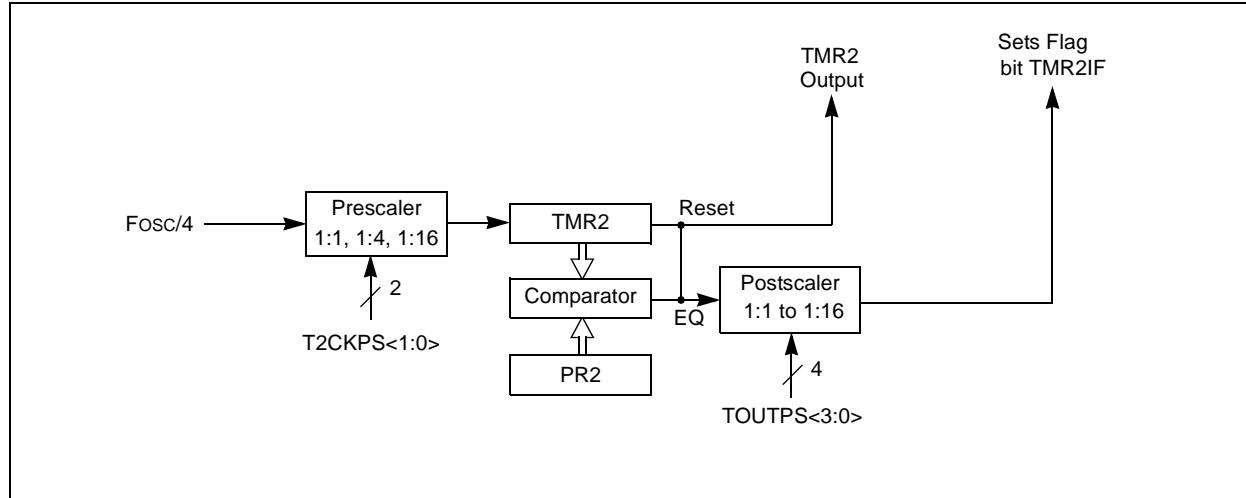
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by setting the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset).

Note: TMR2 is not cleared when T2CON is written.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



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REGISTER 7-1: T2CON: TIMER 2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits

0000 = 1:1 Postscaler

0001 = 1:2 Postscaler

0010 = 1:3 Postscaler

0011 = 1:4 Postscaler

0100 = 1:5 Postscaler

0101 = 1:6 Postscaler

0110 = 1:7 Postscaler

0111 = 1:8 Postscaler

1000 = 1:9 Postscaler

1001 = 1:10 Postscaler

1010 = 1:11 Postscaler

1011 = 1:12 Postscaler

1100 = 1:13 Postscaler

1101 = 1:14 Postscaler

1110 = 1:15 Postscaler

1111 = 1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

TABLE 7-1: SUMMARY OF ASSOCIATED TIMER2 REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	-000 0-00
PR2	Timer2 Module Period Register							1111 1111	1111 1111	
TMR2	Holding Register for the 8-bit TMR2 Register							0000 0000	0000 0000	
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for Timer2 module.

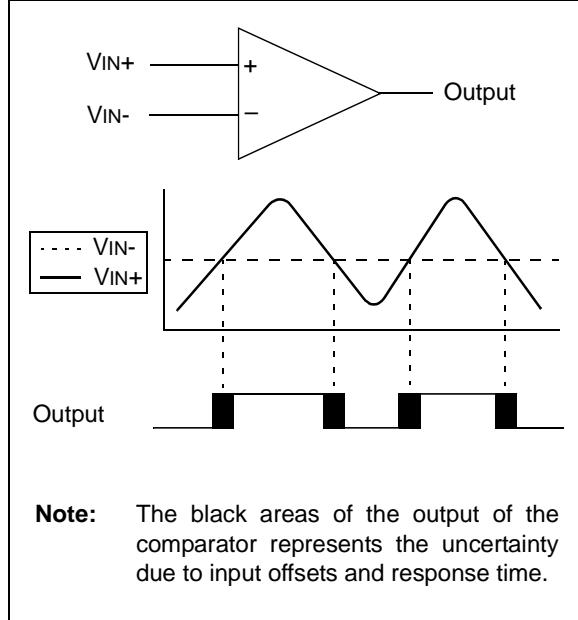
8.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the device. The Analog Comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- PWM shutdown
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- SR Latch
- Programmable and fixed voltage reference
- User-enable Comparator Hysteresis

Note: Only Comparator C2 can be linked to Timer1.

FIGURE 8-1: SINGLE COMPARATOR



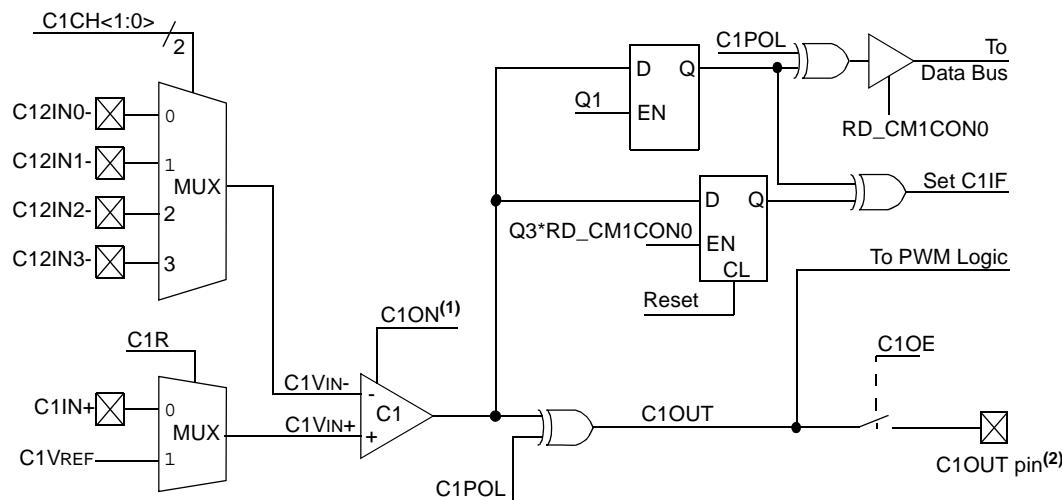
Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

8.1 Comparator Overview

A single comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at V_{IN+} is less than the analog voltage at V_{IN-} , the output of the comparator is a digital low level. When the analog voltage at V_{IN+} is greater than the analog voltage at V_{IN-} , the output of the comparator is a digital high level.

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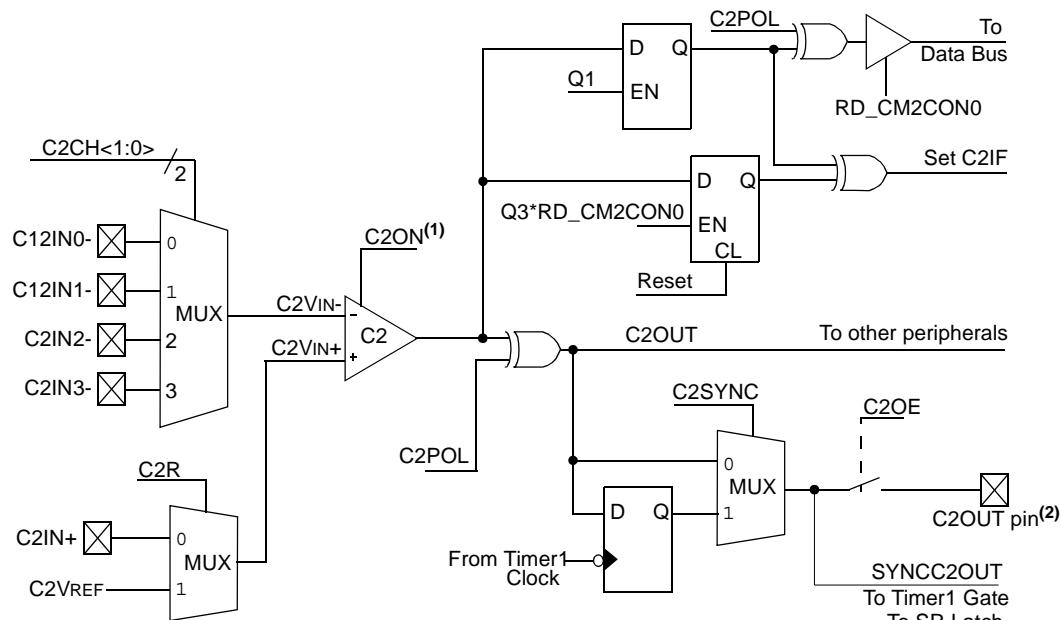
FIGURE 8-2: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C1ON = 0, the C1 comparator will produce a '0' output to the XOR Gate.

2: Output shown for reference only. See I/O port pin block diagram for more detail.

FIGURE 8-3: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.

2: Output shown for reference only. See I/O port pin block diagram for more detail.

8.2 Comparator Control

Each comparator has a separate control and Configuration register: CM1CON0 for Comparator C1 and CM2CON0 for Comparator C2. In addition, Comparator C2 has a second control register, CM2CON1, for controlling the interaction with Timer1 and simultaneous reading of both comparator outputs.

The CM1CON0 and CM2CON0 registers (see Registers 8-1 and 8-2, respectively) contain the control and Status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity

8.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator for minimum current consumption.

8.2.2 COMPARATOR INPUT SELECTION

The CxCH<1:0> bits of the CMxCON0 register direct one of four analog input pins to the comparator inverting input.

Note: To use CxIN+ and CxIN- pins as analog inputs, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

8.2.3 COMPARATOR REFERENCE SELECTION

Setting the CxR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 8.10 “Comparator Voltage Reference”** for more information on the internal voltage reference module.

8.2.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CM2CON1 register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CxON bit of the CMxCON0 register must be set.

Note 1: The CxOE bit overrides the Port data latch. Setting the CxON has no impact on the Port override.

2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

8.2.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 8-1 shows the output state versus input conditions, including polarity control.

TABLE 8-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVIN- > CxVIN+	0	0
CxVIN- < CxVIN+	0	1
CxVIN- > CxVIN+	1	1
CxVIN- < CxVIN+	1	0

8.3 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 15.0 “Electrical Specifications”** for more details.

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8.4 Comparator Interrupt Operation

The comparator interrupt flag can be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8-2 and Figure 8-3). One latch is updated with the comparator output level when the CMxCON0 register is read. This latch retains the value until the next read of the CMxCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. At this point the two mismatch latches have opposite output levels which is detected by the exclusive-or gate and fed to the interrupt circuitry. The mismatch condition persists until either the CMxCON0 register is read or the comparator output returns to the previous state.

- Note 1:** A write operation to the CMxCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.
- 2:** Comparator interrupts will operate correctly regardless of the state of CxOE.

The comparator interrupt is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMxCON0 register to clear the mismatch registers. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMxCON0 register, or CM2CON1 register, to determine the actual change that has occurred.

The CxIF bit of the PIR1 register is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

The CxEI bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR1 register will still be set if an interrupt condition occurs.

FIGURE 8-4: COMPARATOR INTERRUPT TIMING W/O CMxCON0 READ

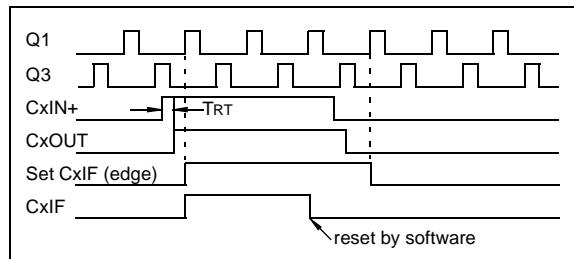
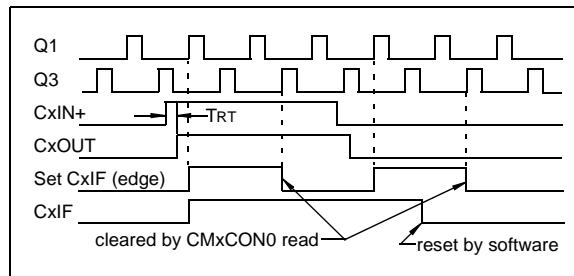


FIGURE 8-5: COMPARATOR INTERRUPT TIMING WITH CMxCON0 READ



- Note 1:** If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF of the PIR1 register interrupt flag may not get set.

- 2:** When either comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μ s for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

8.5 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in **Section 15.0 “Electrical Specifications”**. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. Each comparator is turned off by clearing the CxON bit of the CMxCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CxIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the Sleep instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the interrupt service routine.

8.6 Effects of a Reset

A device Reset forces the CMxCON0 and CM2CON1 registers to their Reset states. This forces both comparators and the voltage references to their OFF states.

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REGISTER 8-1: CM1CON0: COMPARATOR 1 CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **C1ON:** Comparator C1 Enable bit

- 1 = Comparator C1 is enabled
- 0 = Comparator C1 is disabled

bit 6 **C1OUT:** Comparator C1 Output bitIf C1POL = 1 (inverted polarity):

- C1OUT = 0 when C1VIN+ > C1VIN-
- C1OUT = 1 when C1VIN+ < C1VIN-

If C1POL = 0 (non-inverted polarity):

- C1OUT = 1 when C1VIN+ > C1VIN-
- C1OUT = 0 when C1VIN+ < C1VIN-

bit 5 **C1OE:** Comparator C1 Output Enable bit

- 1 = C1OUT is present on the C1OUT pin⁽¹⁾
- 0 = C1OUT is internal only

bit 4 **C1POL:** Comparator C1 Output Polarity Select bit

- 1 = C1OUT logic is inverted
- 0 = C1OUT logic is not inverted

bit 3 **Unimplemented:** Read as '0'bit 2 **C1R:** Comparator C1 Reference Select bit (non-inverting input)

- 1 = C1VIN+ connects to C1VREF output
- 0 = C1VIN+ connects to C1IN+ pin

bit 1-0 **C1CH<1:0>:** Comparator C1 Channel Select bit

- 00 = C12IN0- pin of C1 connects to C1VIN-
- 01 = C12IN1- pin of C1 connects to C1VIN-
- 10 = C12IN2- pin of C1 connects to C1VIN-
- 11 = C12IN3- pin of C1 connects to C1VIN-

Note 1: Comparator output requires the following three conditions: C1OE = 1, C1ON = 1 and corresponding port TRIS bit = 0.

REGISTER 8-2: CM2CON0: COMPARATOR 2 CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	C2ON: Comparator C2 Enable bit 1 = Comparator C2 is enabled 0 = Comparator C2 is disabled
bit 6	C2OUT: Comparator C2 Output bit <u>If C2POL = 1 (inverted polarity):</u> C2OUT = 0 when C2VIN+ > C2VIN- C2OUT = 1 when C2VIN+ < C2VIN- <u>If C2POL = 0 (non-inverted polarity):</u> C2OUT = 1 when C2VIN+ > C2VIN- C2OUT = 0 when C2VIN+ < C2VIN-
bit 5	C2OE: Comparator C2 Output Enable bit 1 = C2OUT is present on C2OUT pin ⁽¹⁾ 0 = C2OUT is internal only
bit 4	C2POL: Comparator C2 Output Polarity Select bit 1 = C2OUT logic is inverted 0 = C2OUT logic is not inverted
bit 3	Unimplemented: Read as '0'
bit 2	C2R: Comparator C2 Reference Select bits (non-inverting input) 1 = C2VIN+ connects to C2VREF 0 = C2VIN+ connects to C2IN+ pin
bit 1-0	C2CH<1:0>: Comparator C2 Channel Select bits 00 = C2VIN- pin of C2 connects to C12IN0- 01 = C2VIN- pin of C2 connects to C12IN1- 10 = C2VIN- pin of C2 connects to C12IN2- 11 = C2VIN- pin of C2 connects to C12IN3-

Note 1: Comparator output requires the following three conditions: C2OE = 1, C2ON = 1 and corresponding port TRIS bit = 0.

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8.7 Comparator Analog Input Connection Considerations

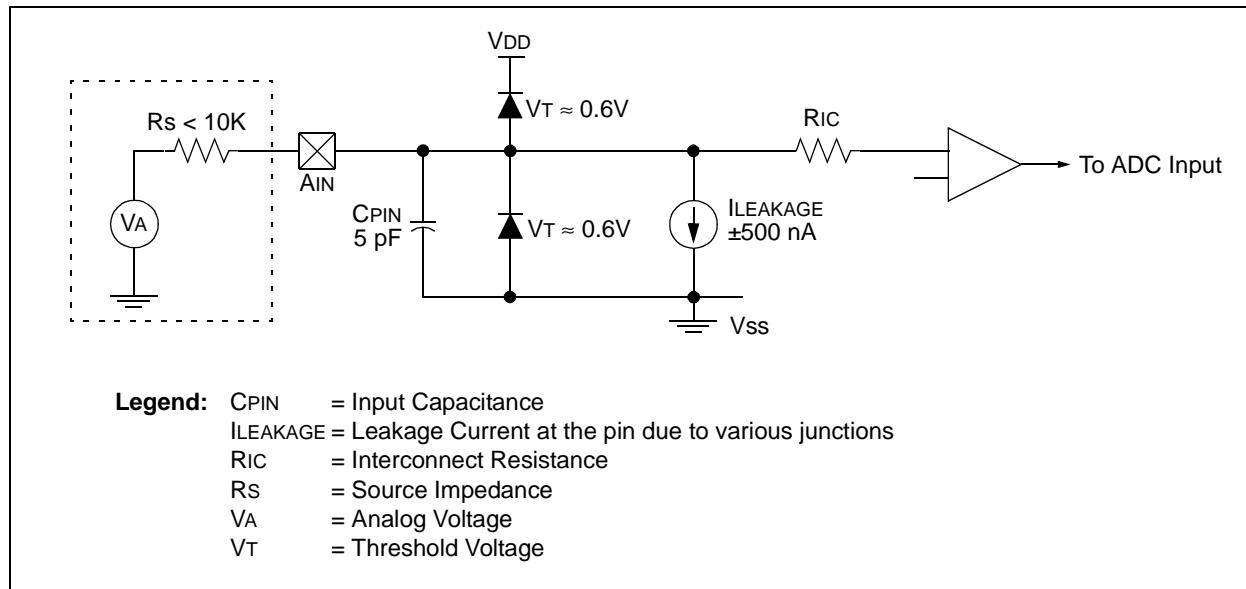
A simplified circuit for an analog input is shown in Figure 8-6. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10\text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 8-6: ANALOG INPUT MODEL



8.8 Additional Comparator Features

There are three additional comparator features:

- Timer1 count enable (gate)
- Synchronizing output with Timer1
- Simultaneous read of comparator outputs

8.8.1 COMPARATOR C2 GATING TIMER1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CM2CON1 register will enable Timer1 to increment based on the output of Comparator C2. This requires that Timer1 is on and gating is enabled. See **Section 6.0 “Timer1 Module with Gate Control”** for details.

It is recommended to synchronize the comparator with Timer1 by setting the C2SYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

8.8.2 SYNCHRONIZING COMPARATOR C2 OUTPUT TO TIMER1

The Comparator C2 output can be synchronized with Timer1 by setting the C2SYNC bit of the CM2CON1 register. When enabled, the C2 output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 8-3) and the Timer1 Block Diagram (Figure 6-1) for more information.

8.8.3 SIMULTANEOUS COMPARATOR OUTPUT READ

The MC1OUT and MC2OUT bits of the CM2CON1 register are mirror copies of both comparator outputs. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note 1: Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 8-3: CM2CON1: COMPARATOR 2 CONTROL REGISTER 1

R-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 7	MC1OUT: Mirror Copy of C1OUT bit
bit 6	MC2OUT: Mirror Copy of C2OUT bit
bit 5	Unimplemented: Read as ‘0’
bit 4	T1ACS: Timer1 Alternate Clock Select bit 1 = Timer1 clock source is the system clock (Fosc) 0 = Timer1 clock source is the internal clock Fosc/4)
bit 3	C1HYS: Comparator C1 Hysteresis Enable bit 1 = Comparator C1 Hysteresis enabled 0 = Comparator C1 Hysteresis disabled
bit 2	C2HYS: Comparator C2 Hysteresis Enable bit 1 = Comparator C2 Hysteresis enabled 0 = Comparator C2 Hysteresis disabled
bit 1	T1GSS: Timer1 Gate Source Select bit 1 = Timer1 gate source is $\overline{T1G}$ 0 = Timer1 gate source is SYNCC2OUT.
bit 0	C2SYNC: Comparator C2 Output Synchronization bit 1 = C2 Output is synchronous to falling edge of Timer1 clock 0 = C2 Output is asynchronous

8.9 Comparator SR Latch

The SR latch module provides additional control of the comparator outputs. The module consists of a single SR latch and output multiplexers. The SR latch can be set, reset or toggled by the comparator outputs. The SR latch may also be set or reset, independent of comparator output, by control bits in the SRCON0 control register. The SR latch output multiplexers select whether the latch outputs or the comparator outputs are directed to the I/O port logic for eventual output to a pin.

The SR latch also has a variable clock, which is connected to the set input of the latch. The SRCLKEN bit of SRCON0 enables the SR latch set clock. The clock will periodically pulse the set input of the latch. Control over the frequency of the SR latch set clock is provided by the SRCS<1:0> bits of SRCON1 register.

8.9.1 LATCH OPERATION

The latch is a Set-Reset latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. Each latch input is connected to a comparator output and a software controlled pulse generator. The latch can be set by C1OUT or the PULSS bit of the SRCON0 register. The latch can be reset by C2OUT or the PULSR bit of the SRCON0 register. The latch is reset-dominant, therefore, if both Set and Reset

inputs are high the latch will go to the Reset state. Both the PULSS and PULSR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

8.9.2 LATCH OUTPUT

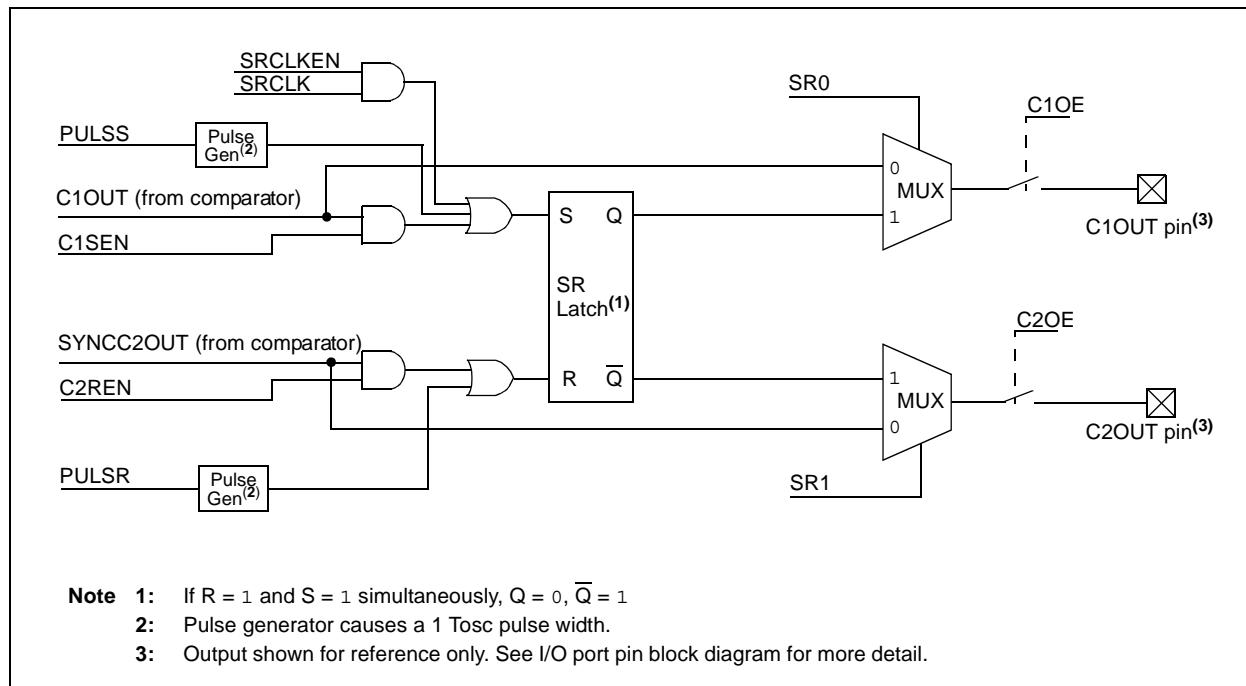
The SR<1:0> bits of the SRCON0 register control the latch output multiplexers and determine four possible output configurations. In these four configurations, the CxOUT I/O port logic is connected to:

- C1OUT and C2OUT
- C1OUT and SR latch \bar{Q}
- C2OUT and SR latch Q
- SR latch Q and \bar{Q}

After any Reset, the default output configuration is the unlatched C1OUT and C2OUT mode. This maintains compatibility with devices that do not have the SR latch feature.

The applicable TRIS bits of the corresponding ports must be cleared to enable the Port pin output drivers. Additionally, the CxOE comparator output enable bits of the CMxCON0 registers must be set in order to make the comparator or latch outputs available on the output pins. The latch configuration enable states are completely independent of the enable states for the comparators.

FIGURE 8-7: SR LATCH SIMPLIFIED BLOCK DIAGRAM



REGISTER 8-4: SRCON0: SR LATCH CONTROL 0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/S-0	R/S-0	U-0	R/W-0
SR1 ⁽²⁾	SR0 ⁽²⁾	C1SEN	C2REN	PULSS	PULSR	—	SRCLKEN
bit 7	bit 0						

Legend:

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

S = Bit is set only -

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 7	SR1: SR Latch Configuration bit ⁽²⁾ 1 = C2OUT pin is the latch Q output 0 = C2OUT pin is the C2 comparator output
bit 6	SR0: SR Latch Configuration bits ⁽²⁾ 1 = C1OUT pin is the latch Q output 0 = C1OUT pin is the C1 Comparator output
bit 5	C1SEN: C1 Set Enable bit 1 = C1 comparator output sets SR latch 0 = C1 comparator output has no effect on SR latch
bit 4	C2REN: C2 Reset Enable bit 1 = C2 comparator output resets SR latch 0 = C2 comparator output has no effect on SR latch
bit 3	PULSS: Pulse the SET Input of the SR Latch bit 1 = Triggers pulse generator to set SR latch. Bit is immediately reset by hardware. 0 = Does not trigger pulse generator
bit 2	PULSR: Pulse the Reset Input of the SR Latch bit 1 = Triggers pulse generator to reset SR latch. Bit is immediately reset by hardware. 0 = Does not trigger pulse generator
bit 1	Unimplemented: Read as '0'
bit 0	SRCLKEN: SR Latch Set Clock Enable bit 1 = Set input of SR latch is pulsed with SRCLK 0 = Set input of SR latch is not pulsed with the SRCLK

- Note 1:** The C1OUT and C2OUT bits in the CMxCON0 register will always reflect the actual comparator output (not the level on the pin), regardless of the SR latch operation.
- 2:** To enable an SR Latch output to the pin, the appropriate CxOE, and TRIS bits must be properly configured.

REGISTER 8-5: SRCON1: SR LATCH CONTROL 1 REGISTER

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
SRCS1	SRCS0	—	—	—	—	—	—
bit 7	bit 0						

Legend:

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

S = Bit is set only -

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 7-6	SRCS<1:0>: SR Latch Clock Prescale bits 00 = 1:4 Prescale value 01 = 1:8 Prescale value 10 = 1:16 Prescale value 11 = 1:32 Prescale value
bit 5-0	Unimplemented: Read as '0'

8.10 Comparator Voltage Reference

The comparator voltage reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to Vss
- Ratiometric with VDD
- Fixed Reference (0.6)

The VRCON register (Register 8-6) controls the voltage reference module shown in Figure 8-8.

8.10.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

8.10.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 8-1: CVREF OUTPUT VOLTAGE

$$VRR = 1 \text{ (low range):}$$

$$CVREF = (VR<3:0>/24) \times VDD$$

$$VRR = 0 \text{ (high range):}$$

$$CVREF = (VDD/4) + (VR<3:0> \times VDD/32)$$

The full range of Vss to VDD cannot be realized due to the construction of the module. See Figure 8-8.

8.10.3 OUTPUT CLAMPED TO Vss

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

8.10.4 OUTPUT RATIO METRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 15.0 “Electrical Specifications”**.

8.10.5 FIXED VOLTAGE REFERENCE

The fixed voltage reference is independent of VDD, with a nominal output voltage of 0.6V. This reference can be enabled by setting the VP6EN bit of the VRCON register to '1'.

8.10.6 FIXED VOLTAGE REFERENCE STABILIZATION PERIOD

When the fixed voltage reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See the electrical specifications section for the minimum delay requirement.

8.10.7 VOLTAGE REFERENCE SELECTION

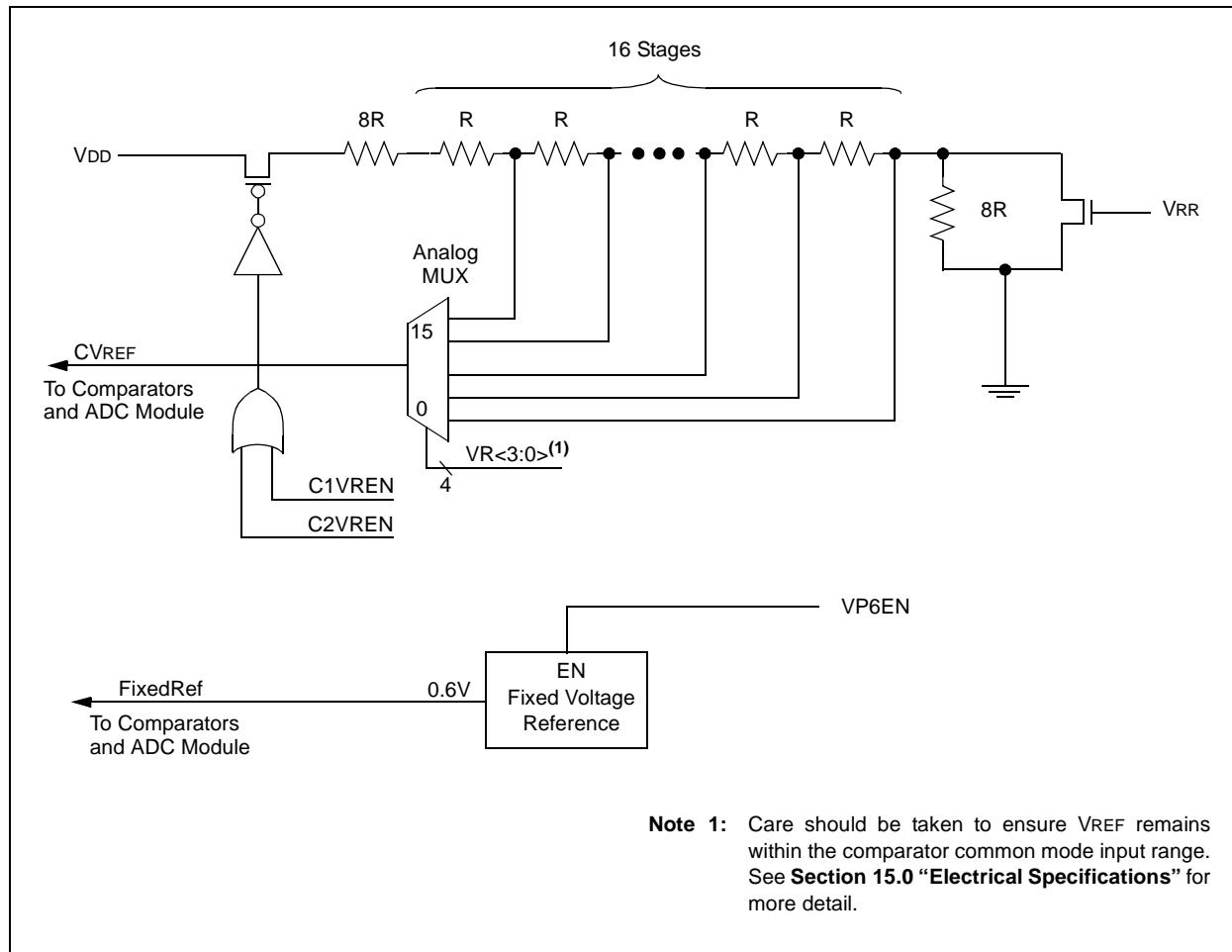
Multiplexers on the output of the voltage reference module enable selection of either the CVREF or fixed voltage reference for use by the comparators.

Setting the C1VREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by C1. Clearing the C1VREN bit selects the fixed voltage for use by C1.

Setting the C2VREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by C2. Clearing the C2VREN bit selects the fixed voltage for use by C2.

When both the C1VREN and C2VREN bits are cleared, current flow in the CVREF voltage divider is disabled minimizing the power drain of the voltage reference peripheral.

FIGURE 8-8: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



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REGISTER 8-6: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1VREN	C2VREN	VRR	VP6EN	VR3	VR2	VR1	VR0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **C1VREN:** Comparator 1 Voltage Reference Enable bit⁽¹⁾

1 = CVREF circuit powered on and routed to C1VREF input of Comparator C1

0 = 0.6 Volt constant reference routed to C1VREF input of Comparator C1

bit 6 **C2VREN:** Comparator 2 Voltage Reference Enable bit⁽¹⁾

1 = CVREF circuit powered on and routed to C2VREF input of Comparator C2

0 = 0.6 Volt constant reference routed to C2VREF input of Comparator C2

bit 5 **VRR:** CVREF Range Selection bit

1 = Low range

0 = High range

bit 4 **VP6EN:** 0.6V Reference Enable bit

1 = Enabled

0 = Disabled

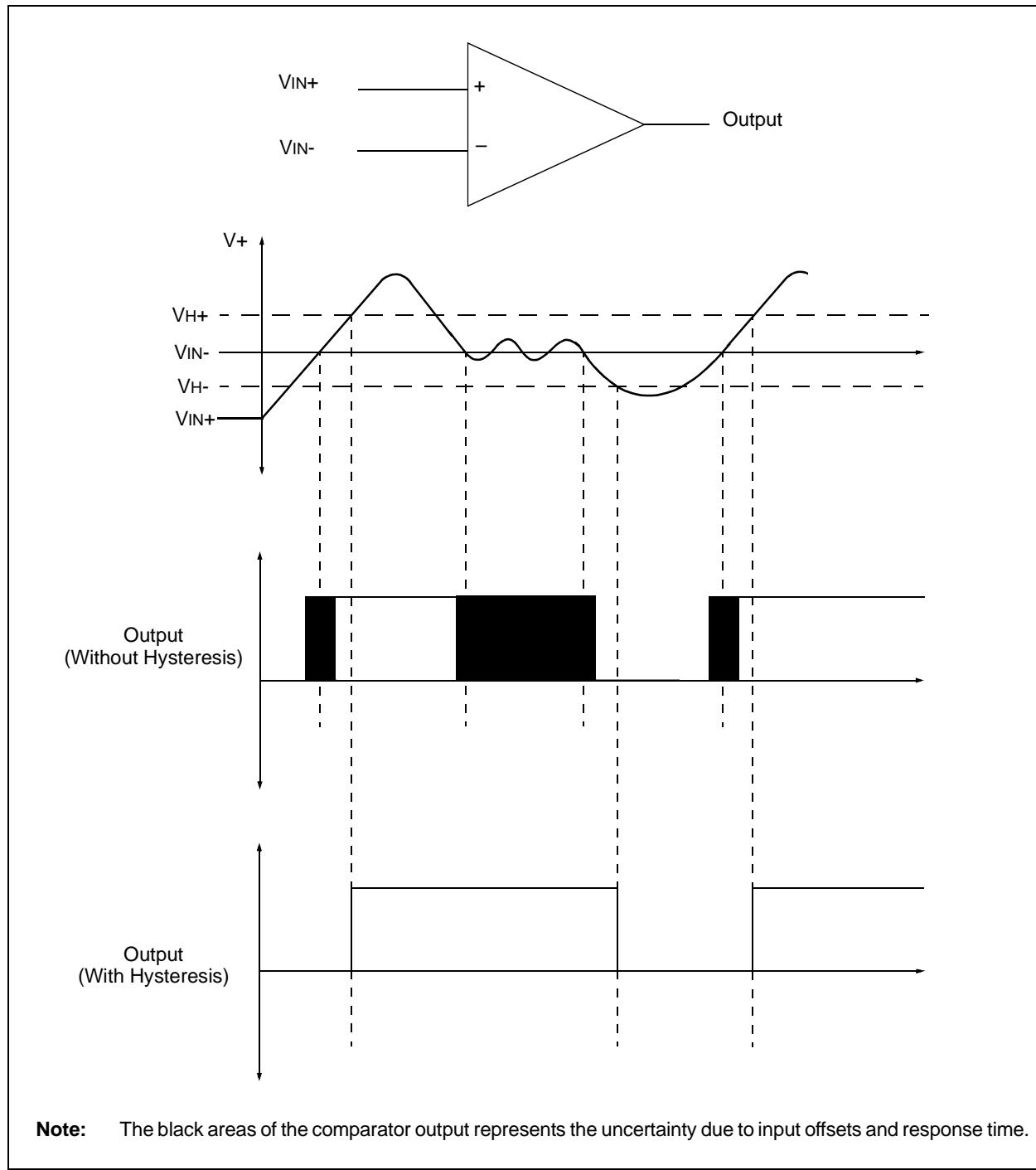
bit 3-0 **VR<3:0>:** Comparator Voltage Reference CVREF Value Selection bits ($0 \leq VR<3:0> \leq 15$)When VRR = 1: CVREF = $(VR<3:0>/24) * VDD$ When VRR = 0: CVREF = $VDD/4 + (VR<3:0>/32) * VDD$

8.11 Comparator Hysteresis

Each comparator has built-in hysteresis that is user enabled by setting the C1HYS or C2HYS bits of the CM2CON1 register. The hysteresis feature can help filter noise and reduce multiple comparator output transitions when the output is changing state.

Figure 8-9 shows the relationship between the analog input levels and digital output of a comparator with and without hysteresis. The output of the comparator changes from a low state to a high state only when the analog voltage at V_{IN+} rises above the upper hysteresis threshold (V_{H+}). The output of the comparator changes from a high state to a low state only when the analog voltage at V_{IN+} falls below the lower hysteresis threshold (V_{H-}).

FIGURE 8-9: COMPARATOR HYSTERESIS



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TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
CM2CON1	MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	00-0 0010
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 000x	0000 000x
PIE1	—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	-000 0-00
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--x0 x000
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	--uu 00uu
SRCON0	SR1	SR0	C1SEN	C2REN	PULSS	PULSR	—	SRCLKEN	0000 00-0	0000 00-0
SRCON1	SRCS1	SRCS2	—	—	—	—	—	—	00-- ----	00-- ----
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
VRCN	C1VREN	C2VREN	VRR	VP6EN	VR3	VR2	VR1	VR0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used for comparator.

9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

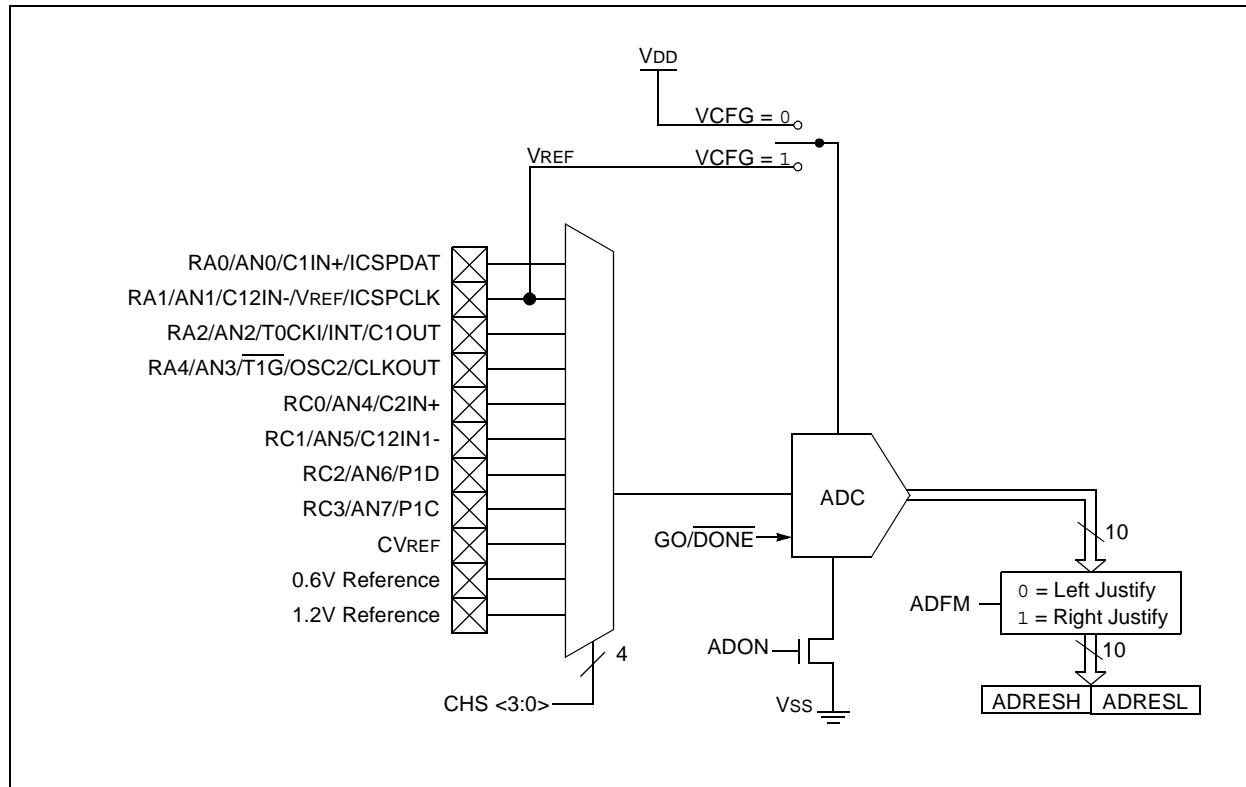
The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 9-1 shows the block diagram of the ADC.

FIGURE 9-1: ADC BLOCK DIAGRAM



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9.1 ADC Configuration

When configuring and using the ADC, the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding Port section for more information.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 “ADC Operation”** for more information.

9.1.3 ADC VOLTAGE REFERENCE

The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either VDD or an external voltage source. The negative voltage reference is always connected to the ground reference.

9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 9-3.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 15.0 “Electrical Specifications”** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

TABLE 9-1: ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES (VDD \geq 3.0V)

ADC Clock Period (TAD)		Device Frequency (Fosc)			
ADC Clock Source	ADCS<2:0>	20 MHz	8 MHz	4 MHz	1 MHz
Fosc/2	000	100 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	2.0 μ s
Fosc/4	100	200 ns ⁽²⁾	500 ns ⁽²⁾	1.0 μ s ⁽²⁾	4.0 μ s
Fosc/8	001	400 ns ⁽²⁾	1.0 μ s ⁽²⁾	2.0 μ s	8.0 μ s ⁽³⁾
Fosc/16	101	800 ns ⁽²⁾	2.0 μ s	4.0 μ s	16.0 μ s ⁽³⁾
Fosc/32	010	1.6 μ s	4.0 μ s	8.0 μ s ⁽³⁾	32.0 μ s ⁽³⁾
Fosc/64	110	3.2 μ s	8.0 μ s ⁽³⁾	16.0 μ s ⁽³⁾	64.0 μ s ⁽³⁾
FRC	x11	2-6 μ s ^(1,4)			

Legend: Shaded cells are outside of recommended range.

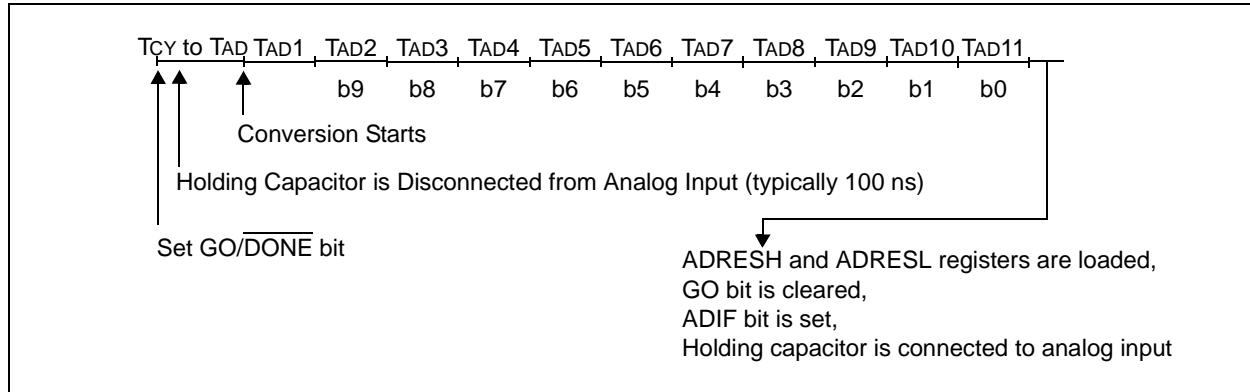
Note 1: The FRC source has a typical TAD time of 4 μ s for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



9.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an analog-to-digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note: The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the interrupt service routine.

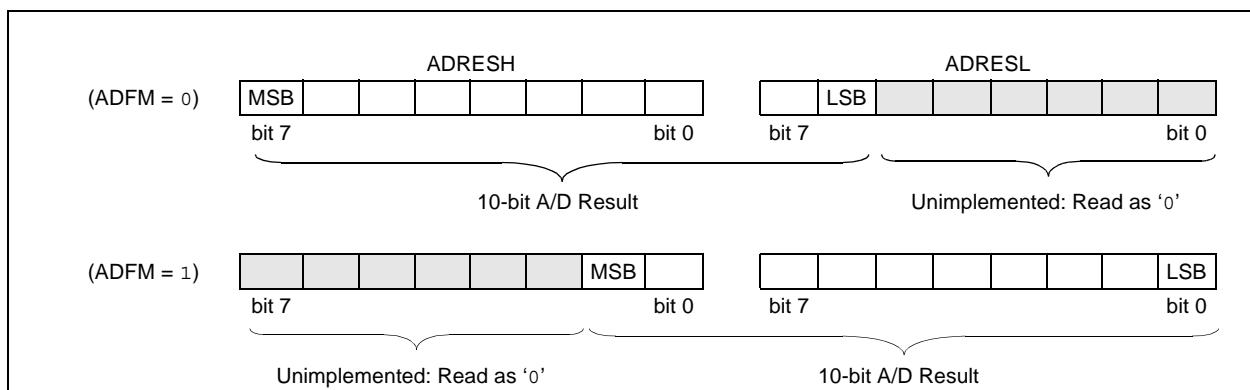
Please see **Section 9.1.5 “Interrupts”** for more information.

9.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 9-4 shows the two output formats.

FIGURE 9-3: 10-BIT A/D CONVERSION RESULT FORMAT



9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the analog-to-digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to [Section 9.2.6 "A/D Conversion Procedure"](#).

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete analog-to-digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The ECCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not ensure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See [Section 10.0 "Enhanced Capture/Compare/PWM \(With Auto-Shutdown and Dead Band\) Module"](#) for more information.

9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an analog-to-digital conversion:

1. Configure Port:
 - Disable pin output driver (See TRIS register)
 - Configure pin as analog
2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Select result format
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt may be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: See [Section 9.3 "A/D Acquisition Requirements"](#).

EXAMPLE 9-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL    ADCON1      ;
MOVLW      B'01110000' ;ADC Frc clock
MOVWF      ADCON1      ;
BANKSEL    TRISA       ;
BSF        TRISA,0    ;Set RA0 to input
BANKSEL    ANSEL       ;
BSF        ANSEL,0    ;Set RA0 to analog
BANKSEL    ADCON0      ;
MOVLW      B'10000001' ;Right justify,
MOVWF      ADCON0      ;Vdd Vref, AN0, On
CALL       SampleTime  ;Acquisiton delay
BSF        ADCON0,GO   ;Start conversion
BTFSR    ADCON0,GO    ;Is conversion done?
GOTO      $-1         ;No, test again
BANKSEL    ADRESH      ;
MOVF      ADRESH,W    ;Read upper 2 bits
MOVWF      RESULTHI    ;store in GPR space
BANKSEL    ADRESL      ;
MOVF      ADRESL,W    ;Read lower 8 bits
MOVWF      RESULTLO    ;Store in GPR space
```

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9.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0						
ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **VCFG:** Voltage Reference bit

1 = VREF pin

0 = VDD

bit 5-2 **CHS<3:0>:** Analog Channel Select bits

0000 = Channel 00 (AN0)

0001 = Channel 01 (AN1)

0010 = Channel 02 (AN2)

0011 = Channel 03 (AN3)

0100 = Channel 04 (AN4)

0101 = Channel 05 (AN5)

0110 = Channel 06 (AN6)

0111 = Channel 07 (AN7)

1000 = Reserved – do not use

1001 = Reserved – do not use

1010 = Reserved – do not use

1011 = Reserved – do not use

1100 = CVREF

1101 = VP6 Reference⁽¹⁾

1110 = V1P2 Reference⁽¹⁾

1111 = Reserved – do not use

bit 1 **GO/DONE:** A/D Conversion Status bit

1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.

This bit is automatically cleared by hardware when the A/D conversion has completed.

0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit

1 = ADC is enabled

0 = ADC is disabled and consumes no operating current

Note 1: When the CHS<3:0> bits change to select the V1P2 or VP6 reference, the reference output voltage will have a transient. If the Comparator module uses this VP6 reference voltage, the comparator output may momentarily change state due to the transient.

REGISTER 9-2: ADCON1: A/D CONTROL REGISTER 1

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = Fosc/2

001 = Fosc/8

010 = Fosc/32

x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

100 = Fosc/4

101 = Fosc/16

110 = Fosc/64

bit 3-0 **Unimplemented:** Read as '0'

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REGISTER 9-3: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

| R-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES9 | ADRES8 | ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 9-4: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Reserved**: Do not use.

REGISTER 9-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 7-2 **Reserved**: Do not use.

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

REGISTER 9-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

| R-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-4. The source impedance (R_s) and the internal sampling switch (R_{ss}) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (R_{ss}) impedance varies over the device voltage (V_{DD}), see Figure 9-4. **The maximum recommended impedance for analog sources is 10 k Ω .** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10k Ω 5.0V VDD

$$\begin{aligned} TACQ &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= TAMP + TC + TCOFF \\ &= 5\mu s + TC + [(Temperature - 25^\circ C)(0.05\mu s/\text{ }^\circ C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{2047} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED} \left(1 - e^{-\frac{TC}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{-\frac{TC}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{2047} \right) \quad ;\text{combining [1] and [2]}$$

Solving for TC :

$$\begin{aligned} TC &= -C_{CHOLD}(R_{IC} + R_{SS} + R_s) \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} TACQ &= 5\mu s + 1.37\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/\text{ }^\circ C)] \\ &= 7.67\mu s \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

- 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- 3: The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

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FIGURE 9-4: ANALOG INPUT MODEL

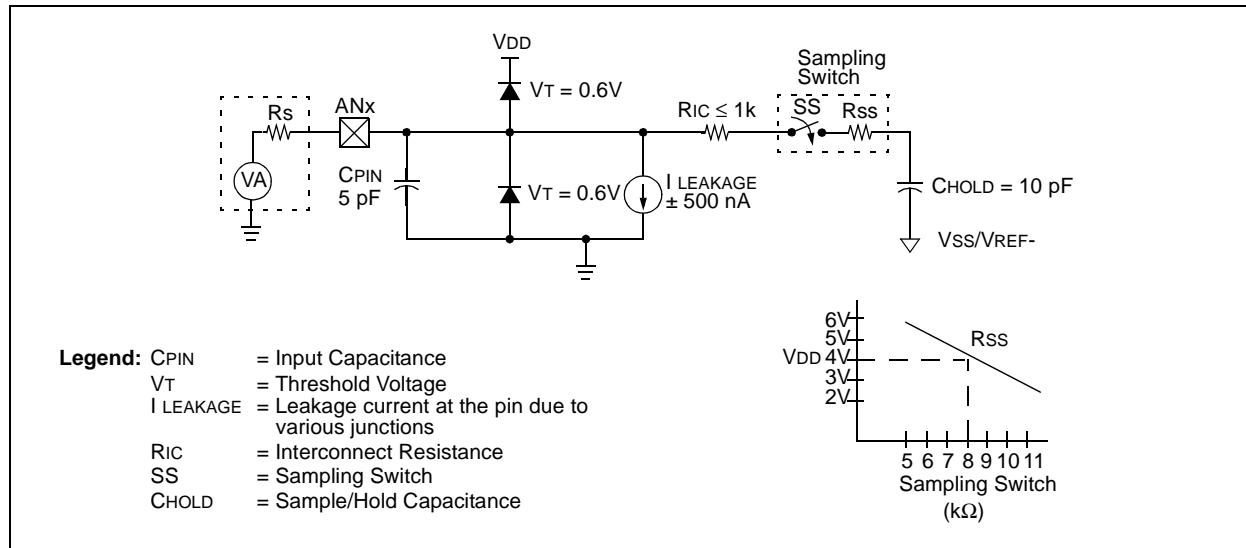


FIGURE 9-5: ADC TRANSFER FUNCTION

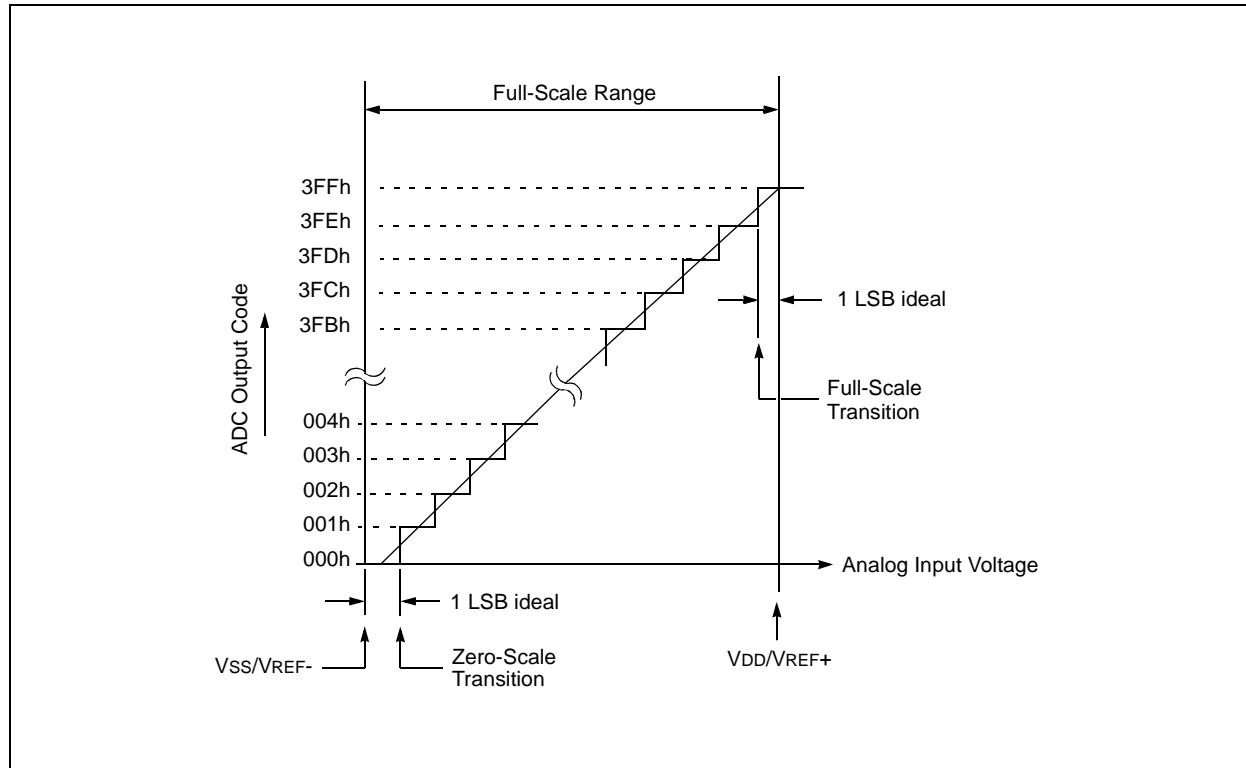


TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	0000 0000	0000 0000
ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE	CCPIE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	-000 0-00
PIR1	—	ADIF	CCPIF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	-000 0-00
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	--u0 u000
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx 00xx	--uu 00uu
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, — = unimplemented read as '0'. Shaded cells are not used for ADC module.

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NOTES:

10.0 ENHANCED CAPTURE/COMPARE/PWM (WITH AUTO-SHUTDOWN AND DEAD BAND) MODULE

The Enhanced Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

Table 10-1 shows the timer resources required by the ECCP module.

TABLE 10-1: ECCP MODE – TIMER RESOURCES REQUIRED

ECCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 10-1: CCP1CON: ENHANCED CCP1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7-6 **P1M<1:0>**: PWM Output Configuration bits
If CCP1M<3:2> = 00, 01, 10:
xx = P1A assigned as Capture/Compare input; P1B, P1C, P1D assigned as Port pins
If CCP1M<3:2> = 11:
00 = Single output; P1A modulated; P1B, P1C, P1D assigned as Port pins
01 = Full-Bridge output forward; P1D modulated; P1A active; P1B, P1C inactive
10 = Half-Bridge output; P1A, P1B modulated with dead-time control; P1C, P1D assigned as Port pins
11 = Full-Bridge output reverse; P1B modulated; P1C active; P1A, P1D inactive
- bit 5-4 **DC1B<1:0>**: PWM Duty Cycle Least Significant bits
Capture mode:
Unused.
Compare mode:
Unused.
PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.
- bit 3-0 **CCP1M<3:0>**: ECCP Mode Select bits
0000 = Capture/Compare/PWM off (resets ECCP module)
0001 = Unused (reserved)
0010 = Compare mode, toggle output on match (CCP1IF bit is set)
0011 = Unused (reserved)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP1IF bit is set)
1001 = Compare mode, clear output on match (CCP1IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 and starts an A/D conversion, if the ADC module is enabled)
1100 = PWM mode; P1A, P1C active-high; P1B, P1D active-high
1101 = PWM mode; P1A, P1C active-high; P1B, P1D active-low
1110 = PWM mode; P1A, P1C active-low; P1B, P1D active-high
1111 = PWM mode; P1A, P1C active-low; P1B, P1D active-low

10.1 Capture Mode

In Capture mode, CCP1H:CCP1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

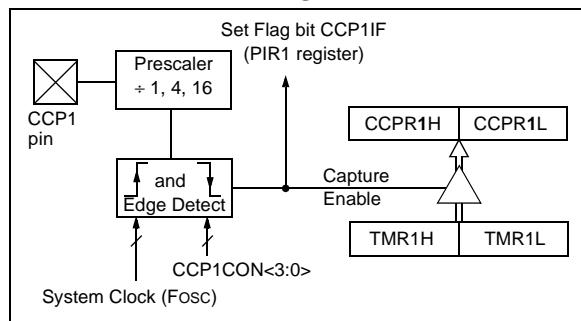
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCP1H, CCP1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 10-1).

10.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note: If the CCP1 pin is configured as an output, a write to the PORT can cause a capture condition.

FIGURE 10-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



10.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

10.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

10.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 10-1).

EXAMPLE 10-1: CHANGING BETWEEN CAPTURE PRESCALERS

```

BANKSEL CCP1CON      ; Set Bank bits to point
                      ; to CCP1CON
CLRF   CCP1CON       ; Turn CCP module off
MOVLW  NEW_CAPT_PS  ; Load the W reg with
                      ; the new prescaler
                      ; move value and CCP ON
MOVWF CCP1CON        ; Load CCP1CON with this
                      ; value

```

10.2 Compare Mode

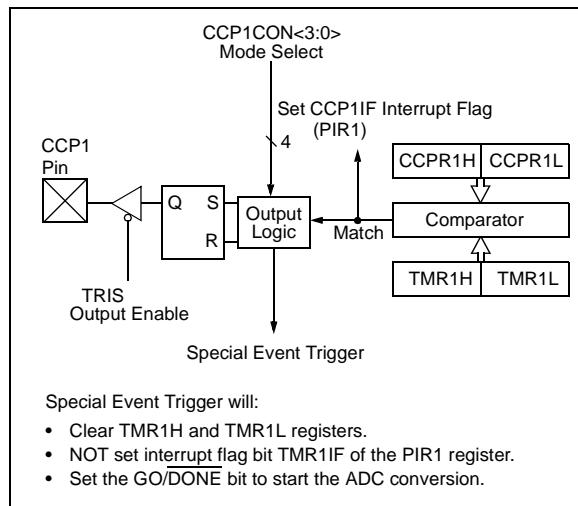
In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

- Toggle the CCP1 output
- Set the CCP1 output
- Clear the CCP1 output
- Generate a Special Event Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register.

All Compare modes can generate an interrupt.

FIGURE 10-2: COMPARE MODE OPERATION BLOCK DIAGRAM



10.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note: Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the Port I/O data latch.

10.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

10.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

10.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (see the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

Note 1: The Special Event Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.

2: Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

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10.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the Port data latch, the TRIS for that pin must be cleared to make the CCP1 pin an output.

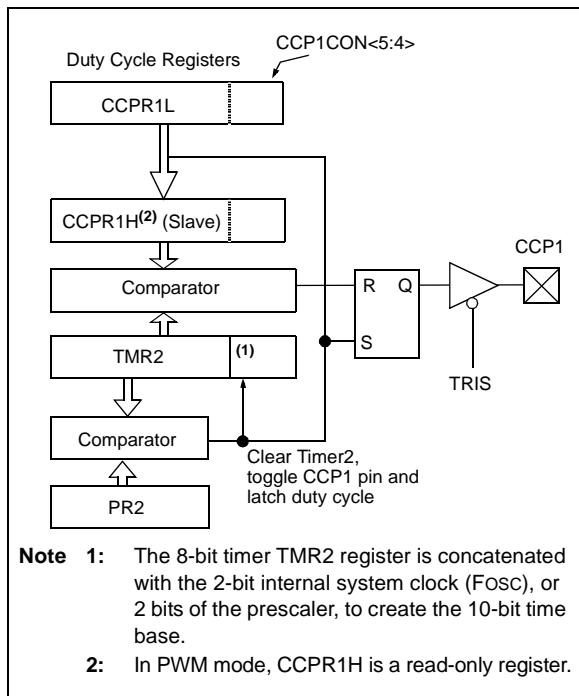
Note: Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

Figure 10-3 shows a simplified block diagram of PWM operation.

Figure 10-4 shows a typical waveform of the PWM signal.

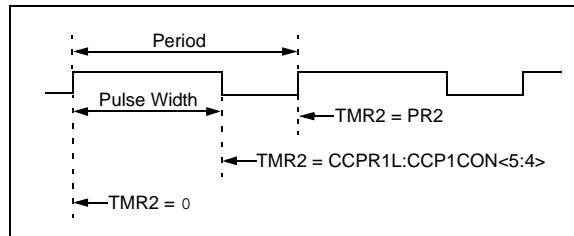
For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 10.3.7 “Setup for PWM Operation”**.

FIGURE 10-3: SIMPLIFIED PWM BLOCK DIAGRAM



The PWM output (Figure 10-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 10-4: CCP PWM OUTPUT



10.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 10-1.

EQUATION 10-1: PWM PERIOD

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (TMR2 \text{ Prescale Value})$$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

Note: The Timer2 postscaler (see **Section 7.1 “Timer2 Operation”**) is not used in the determination of the PWM frequency.

10.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and CCP1<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the CCP1<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and CCP1<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 10-2 is used to calculate the PWM pulse width.

Equation 10-3 is used to calculate the PWM duty cycle ratio.

EQUATION 10-2: PULSE WIDTH

$$\text{Pulse Width} = (CCPR1L:CCP1CON<5:4>) \cdot TOSC \cdot (TMR2 \text{ Prescale Value})$$

EQUATION 10-3: DUTY CYCLE RATIO

$$\text{Duty Cycle Ratio} = \frac{(CCPR1L:CCP1CON<5:4>)}{4(PR2 + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 10-3).

10.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 10-4.

EQUATION 10-4: PWM RESOLUTION

$$\text{Resolution} = \frac{\log[4(PR2 + 1)]}{\log(2)} \text{ bits}$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 10-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 10-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

10.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

10.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 3.0 “Oscillator Module”** for additional details.

10.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

10.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Configure the PWM pin (CCP1) as an input by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and CCP1 bits of the CCP1CON register.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register.
 - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
 - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
 - Enable the CCP1 pin output by clearing the associated TRIS bit.

10.4 PWM (Enhanced Mode)

The Enhanced PWM Mode can generate a PWM signal on up to four different output pins with up to 10-bits of resolution. It can do this through four different PWM Output modes:

- Single PWM
- Half-Bridge PWM
- Full-Bridge PWM, Forward mode
- Full-Bridge PWM, Reverse mode

To select an Enhanced PWM mode, the P1M bits of the CCP1CON register must be set appropriately.

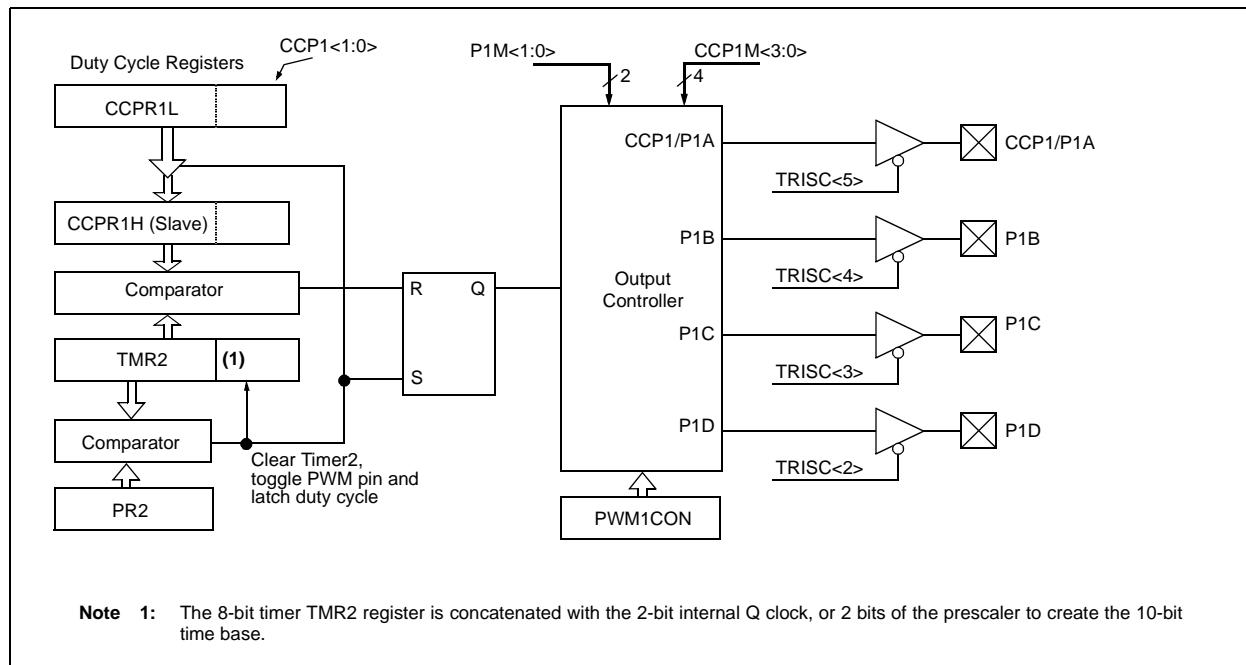
The PWM outputs are multiplexed with I/O pins and are designated P1A, P1B, P1C and P1D. The polarity of the PWM pins is configurable and is selected by setting the CCP1M bits in the CCP1CON register appropriately.

Table 10-4 shows the pin assignments for each Enhanced PWM mode.

Figure 10-5 shows an example of a simplified block diagram of the Enhanced PWM module.

Note: To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

FIGURE 10-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE



Note 1: The TRIS register value for each PWM output must be configured appropriately.

2: Clearing the CCP1CON register will relinquish ECCP control of all PWM output pins.

3: Any pin not used by an Enhanced PWM mode is available for alternate pin functions

TABLE 10-4: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	P1M	CCP1/P1A	P1B	P1C	P1D
Single	00	Yes	No	No	No
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

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FIGURE 10-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)

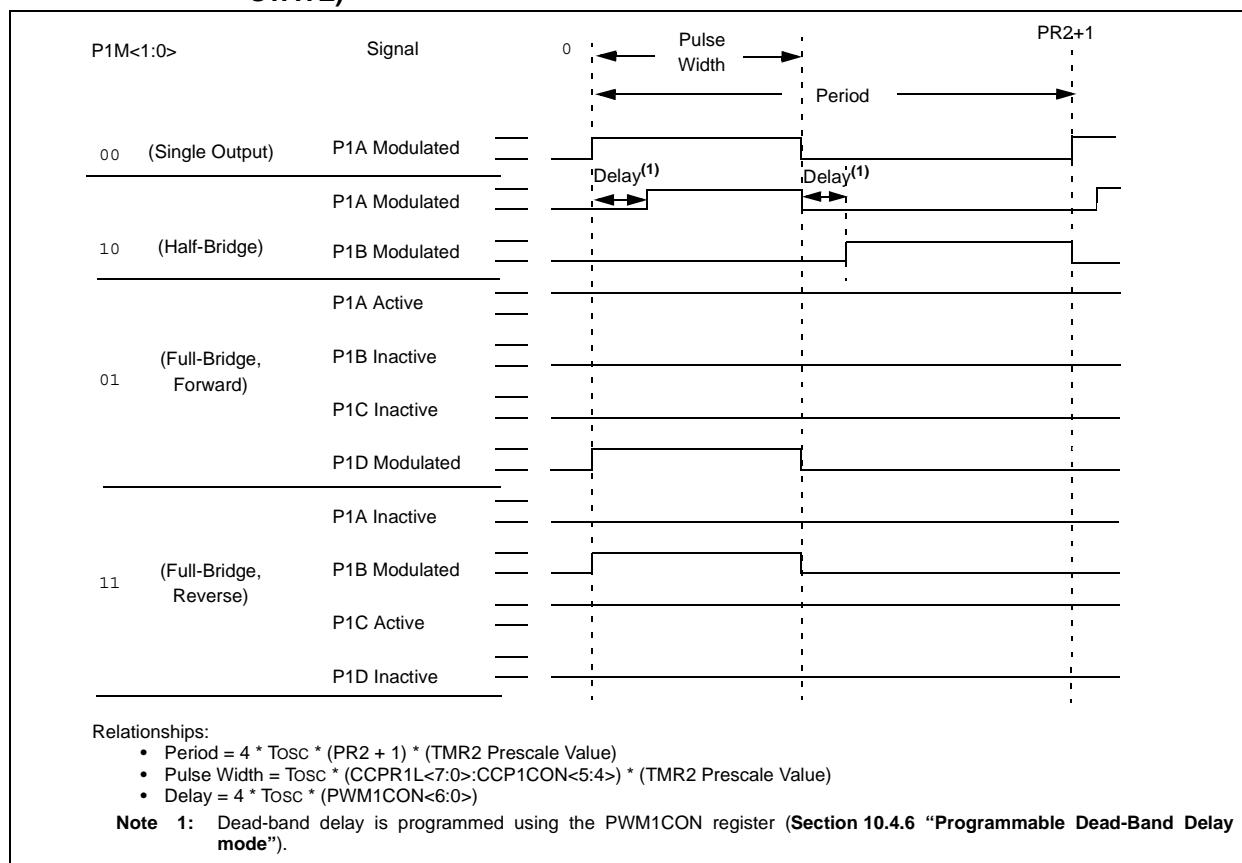
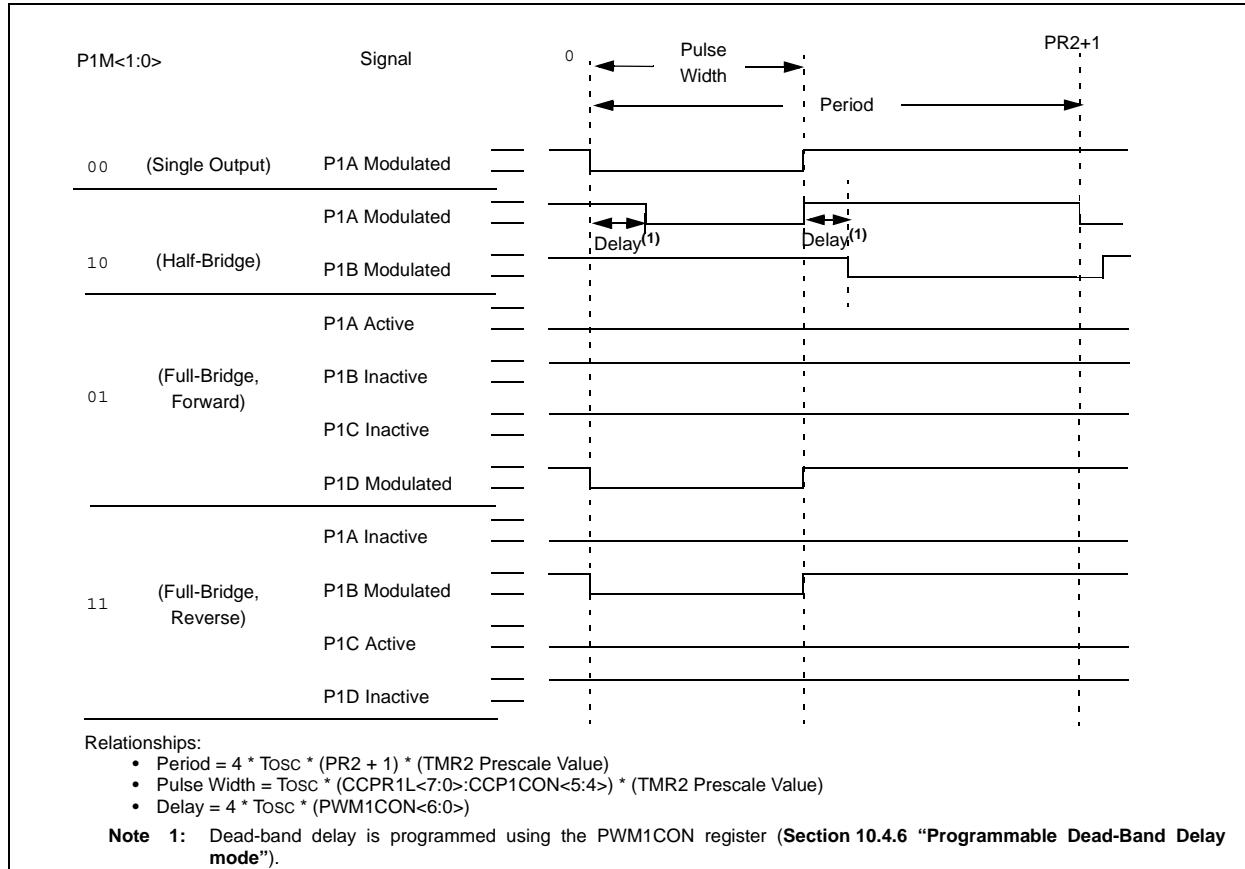


FIGURE 10-7: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)



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10.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 10-8). This mode can be used for half-bridge applications, as shown in Figure 10-9, or for full-bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **10.4.6 “Programmable Dead-Band Delay mode”** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.

FIGURE 10-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

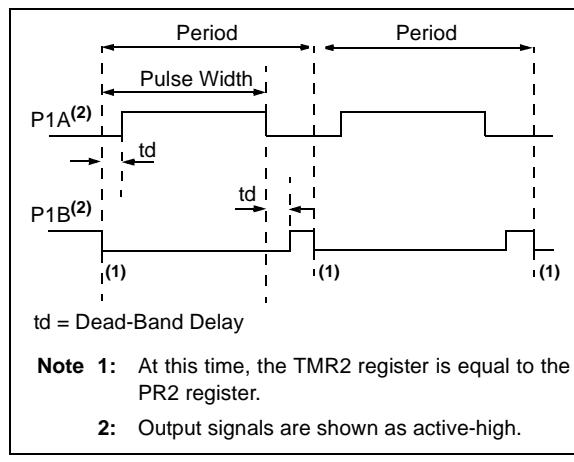
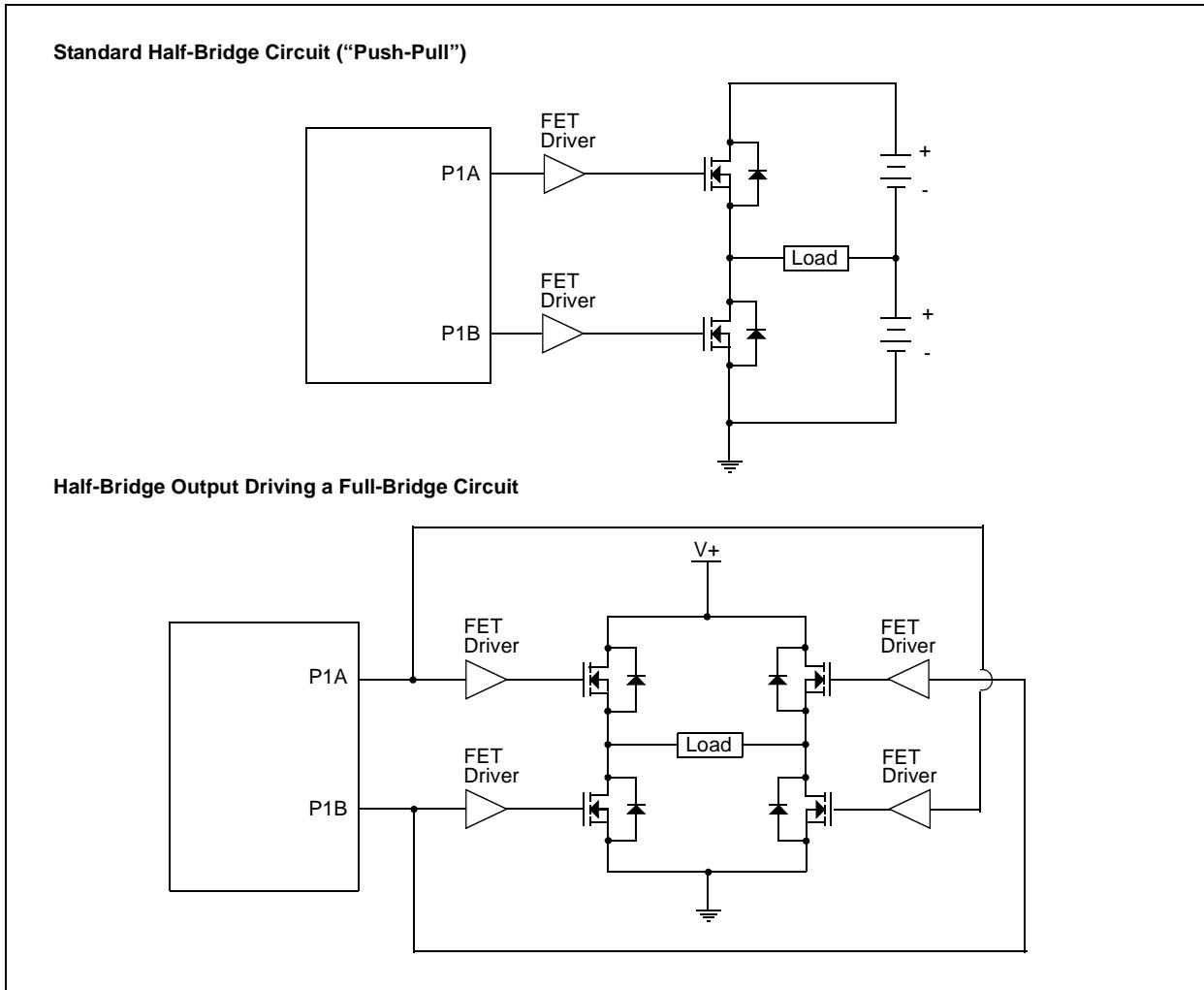


FIGURE 10-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS



10.4.2 FULL-BRIDGE MODE

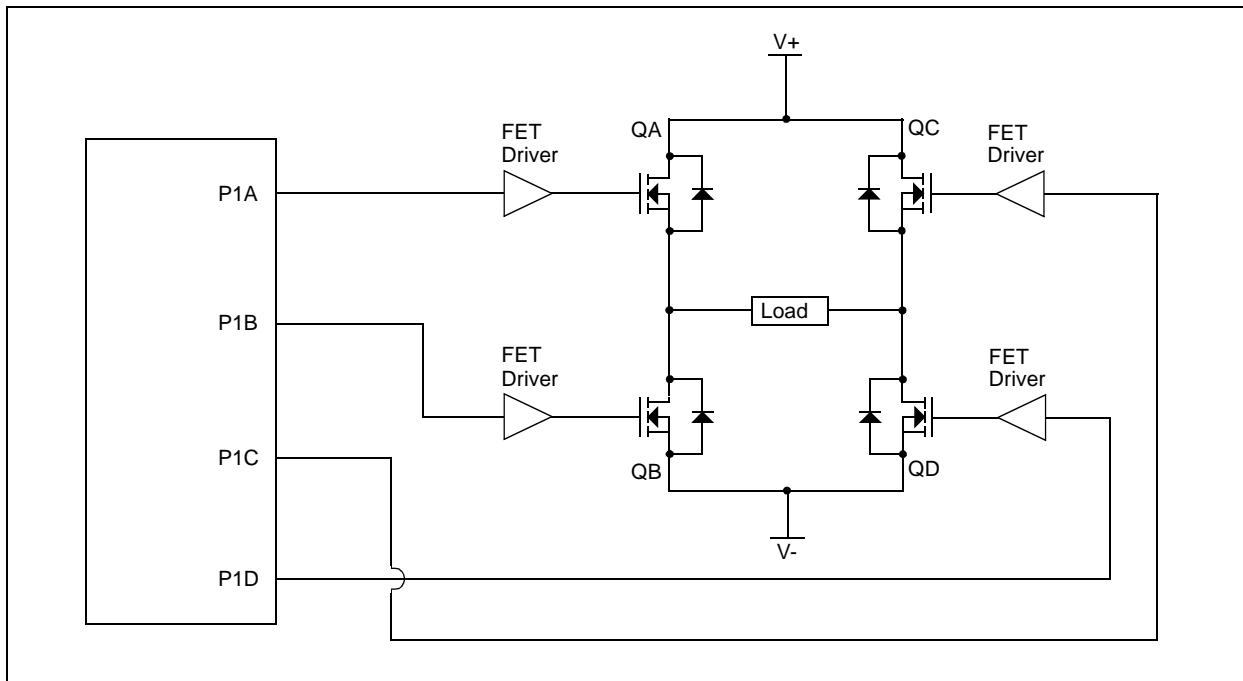
In Full-Bridge mode, all four pins are used as outputs. An example of full-bridge application is shown in Figure 10-10.

In the Forward mode, pin CCP1/P1A is driven to its active state, pin P1D is modulated, while P1B and P1C will be driven to their inactive state as shown in Figure 10-11.

In the Reverse mode, P1C is driven to its active state, pin P1B is modulated, while P1A and P1D will be driven to their inactive state as shown Figure 10-11.

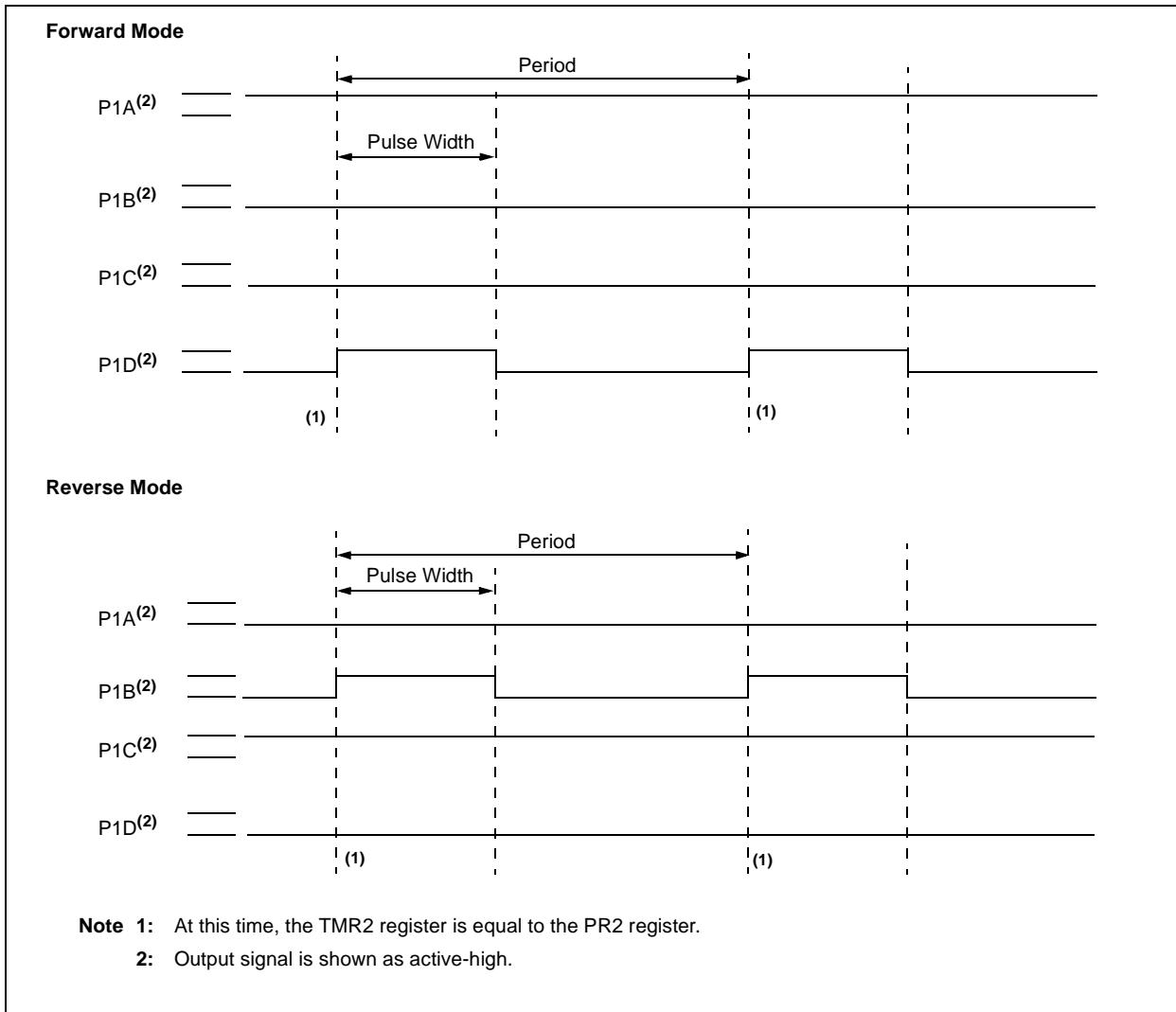
P1A, P1B, P1C and P1D outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the P1A, P1B, P1C and P1D pins as outputs.

FIGURE 10-10: EXAMPLE OF FULL-BRIDGE APPLICATION



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FIGURE 10-11: EXAMPLE OF FULL-BRIDGE PWM OUTPUT



10.4.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the P1M1 bit in the CCP1CON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the P1M1 bit of the CCP1CON register. The following sequence occurs four Timer2 cycles prior to the end of the current PWM period:

- The modulated outputs (P1B and P1D) are placed in their inactive state.
- The associated unmodulated outputs (P1A and P1C) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

See Figure 10-12 for an illustration of this sequence.

The Full-Bridge mode does not provide dead-band delay. As one output is modulated at a time, dead-band delay is generally not required. There is a situation where dead-band delay is required. This situation occurs when both of the following conditions are true:

1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
2. The turn off time of the power switch, including the power device and driver circuit, is greater than the turn on time.

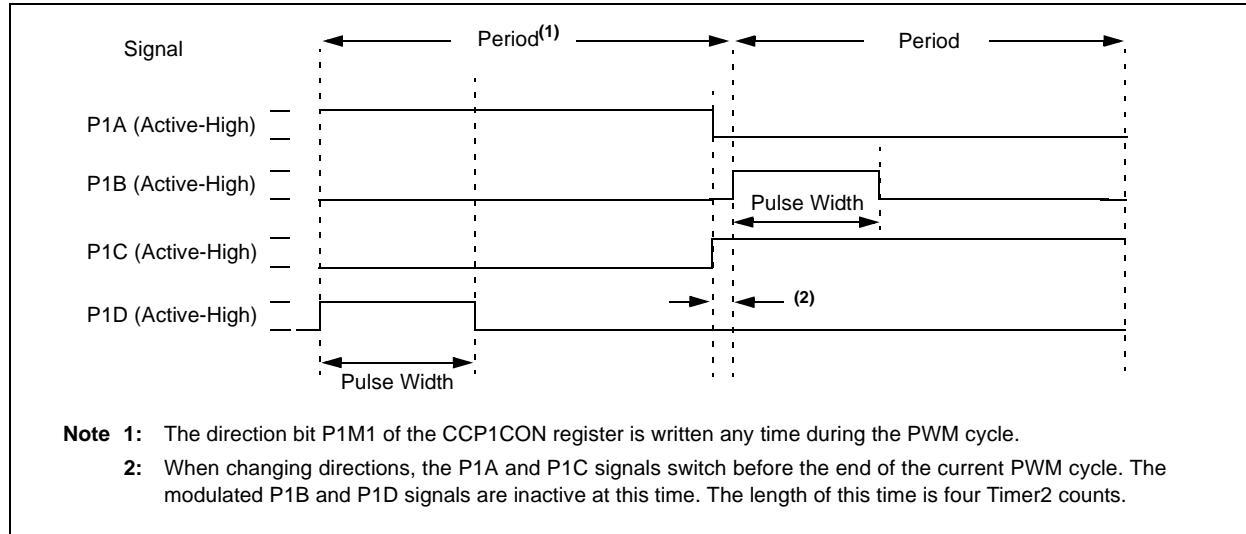
Figure 10-13 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time t_1 , the output P1A and P1D become inactive, while output P1C becomes active. Since the turn off time of the power devices is longer than the turn on time, a shoot-through current will flow through power devices QC and QD (see Figure 10-10) for the duration of ' t '. The same phenomenon will occur to power devices QA and QB for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

1. Reduce PWM duty cycle for one PWM period before changing directions.
2. Use switch drivers that can drive the switches off faster than they can drive them on.

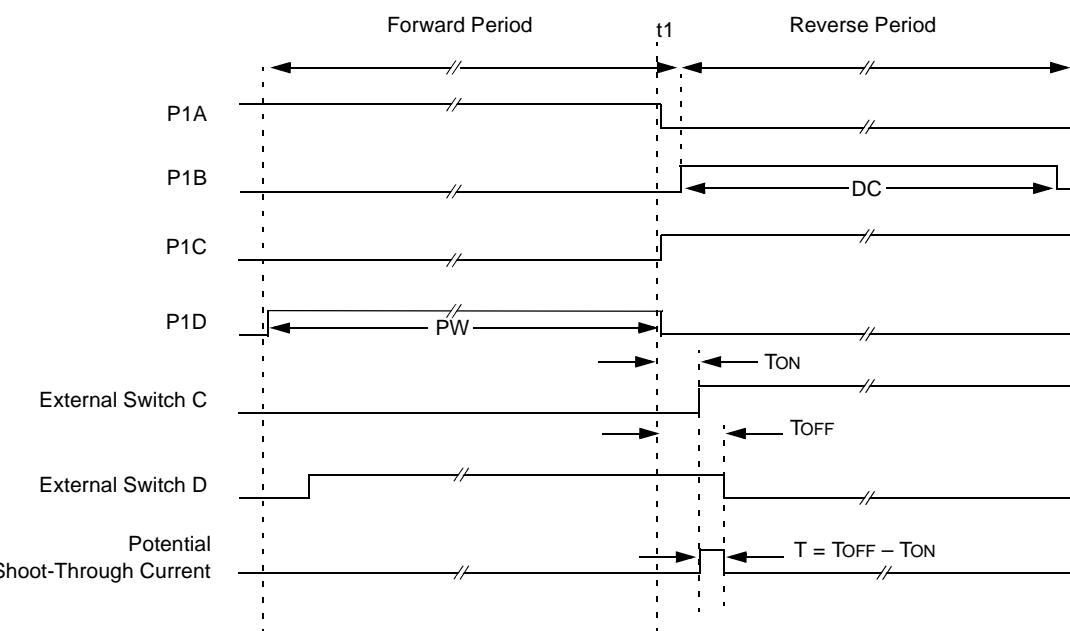
Other options to prevent shoot-through current may exist.

FIGURE 10-12: EXAMPLE OF PWM DIRECTION CHANGE



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FIGURE 10-13: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE



- Note 1:** All signals are shown as active-high.
2: TON is the turn on delay of power switch QC and its driver.
3: TOFF is the turn off delay of power switch QD and its driver.

10.4.3 START-UP CONSIDERATIONS

When any PWM mode is used, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins.

Note: When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the OFF state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

The CCP1M<1:0> bits of the CCP1CON register allow the user to choose whether the PWM output signals are active-high or active-low for each pair of PWM output pins (P1A/P1C and P1B/P1D). The PWM output polarities must be selected before the PWM pins are configured as outputs. Changing the polarity configuration while the PWM pins are configured as outputs is not recommended since it may result in damage to the application circuits.

The P1A, P1B, P1C and P1D output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pins for output at the same time as the Enhanced PWM modes may cause damage to the application circuit. The Enhanced PWM modes must be enabled in the proper Output mode and complete a full PWM cycle before configuring the PWM pins as outputs. The completion of a full PWM cycle is indicated by the TMR2IF bit of the PIR1 register being set as the second PWM period begins.

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10.4.4 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the ECCPASx bits of the ECCPAS register. A shutdown event may be generated by:

- A logic ‘0’ on the INT pin
- Comparator C1
- Comparator C2
- Setting the ECCPASE bit in firmware

A shutdown condition is indicated by the ECCPASE (Auto-Shutdown Event Status) bit of the ECCPAS register. If the bit is a ‘0’, the PWM pins are operating normally. If the bit is a ‘1’, the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The ECCPASE bit is set to ‘1’. The ECCPASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 10.4.5 “Auto-Restart Mode”**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [P1A/P1C] and [P1B/P1D]. The state of each pin pair is determined by the PSSAC and PSSBD bits of the ECCPAS register. Each pin pair may be placed into one of three states:

- Drive logic ‘1’
- Drive logic ‘0’
- Tri-state (high-impedance)

REGISTER 10-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

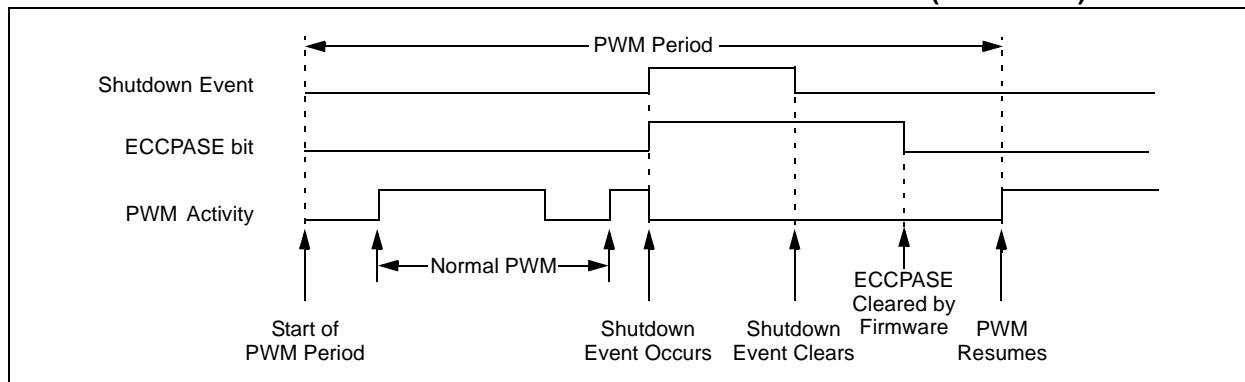
‘0’ = Bit is cleared

x = Bit is unknown

bit 7	ECCPASE: ECCP Auto-Shutdown Event Status bit 1 = A shutdown event has occurred; ECCP outputs are in shutdown state 0 = ECCP outputs are operating
bit 6-4	ECCPAS<2:0>: ECCP Auto-shutdown Source Select bits 000 = Auto-Shutdown is disabled 001 = Comparator C1 output change 010 = Comparator C2 output change 011 = Either Comparator C1 or C2 change 100 = VIL on INT pin 101 = VIL on INT pin or Comparator C1 change 110 = VIL on INT pin or Comparator C2 change 111 = VIL on INT pin or Comparator C1 or Comparator C2 change
bit 3-2	PSSACn: Pins P1A and P1C Shutdown State Control bits 00 = Drive pins P1A and P1C to ‘0’ 01 = Drive pins P1A and P1C to ‘1’ 1x = Pins P1A and P1C tri-state
bit 1-0	PSSBDn: Pins P1B and P1D Shutdown State Control bits 00 = Drive pins P1B and P1D to ‘0’ 01 = Drive pins P1B and P1D to ‘1’ 1x = Pins P1B and P1D tri-state

- Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.
- 2: Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.
 - 3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

FIGURE 10-14: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)

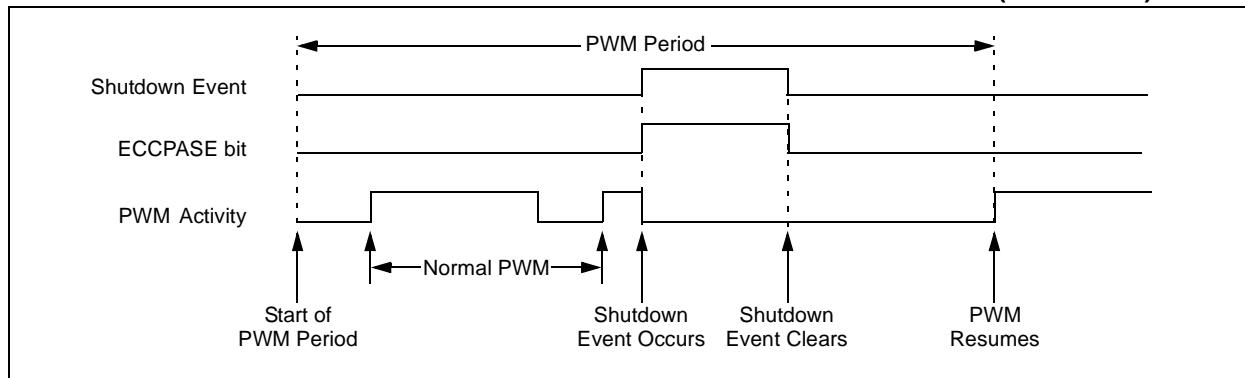


10.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

FIGURE 10-15: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)



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10.4.6 PROGRAMMABLE DEAD-BAND DELAY MODE

In half-bridge applications where all power switches are modulated at the PWM frequency, the power switches normally require more time to turn off than to turn on. If both the upper and lower power switches are switched at the same time (one turned on, and the other turned off), both switches may be on for a short period of time until one switch completely turns off. During this brief interval, a very high current (*shoot-through current*) will flow through both power switches, shorting the bridge supply. To avoid this potentially destructive shoot-through current from flowing during switching, turning on either of the power switches is normally delayed to allow the other switch to completely turn off.

In Half-Bridge mode, a digitally programmable dead-band delay is available to avoid shoot-through current from destroying the bridge power switches. The delay occurs at the signal transition from the non-active state to the active state. See Figure 10-16 for illustration. The lower seven bits of the associated PWM1CON register (Register 10-3) sets the delay period in terms of microcontroller instruction cycles (TCY or 4 Tosc).

FIGURE 10-16: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

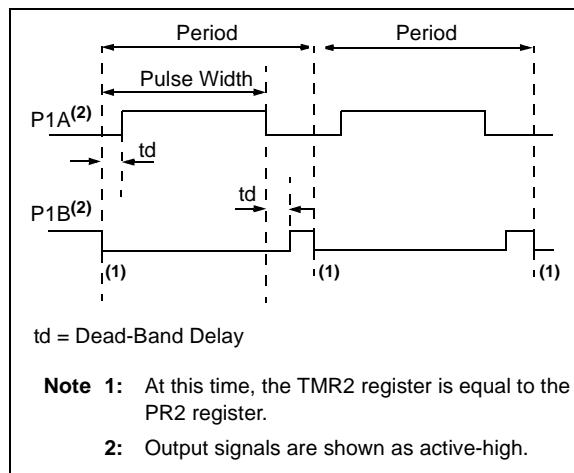
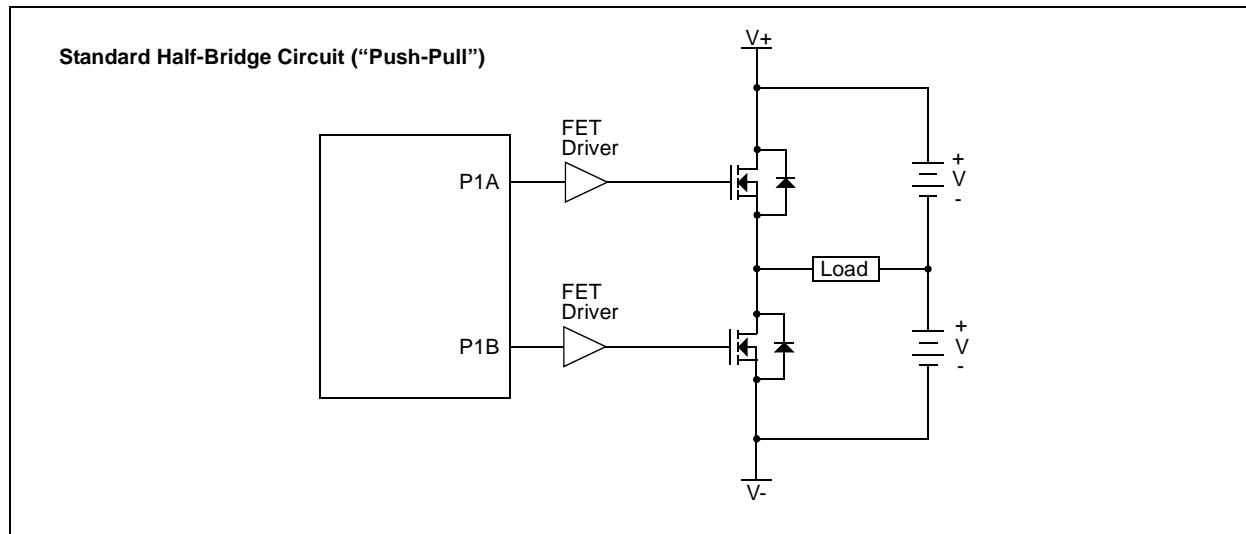


FIGURE 10-17: EXAMPLE OF HALF-BRIDGE APPLICATIONS



REGISTER 10-3: PWM1CON: ENHANCED PWM CONTROL REGISTER

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 |
| bit 7 | bit 0 | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **PRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPASE must be cleared in software to restart the PWM

bit 6-0 **PDC<6:0>:** PWM Delay Count bits

PDCn = Number of Fosc/4 (4 * Tosc) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active

TABLE 10-5: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
CCPR1L	Capture/Compare/PWM Register 1 Low Byte							xxxx xxxx	uuuu uuuu	
CCPR1H	Capture/Compare/PWM Register 1 High Byte							xxxx xxxx	uuuu uuuu	
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1R	C1CH1	C1CH0	0000 -000	0000 -000
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2R	C2CH1	C2CH0	0000 -000	0000 -000
CM2CON1	MC1OUT	MC2OUT	—	T1ACS	C1HYS	C2HYS	T1GSS	C2SYNC	00-0 0010	00-0 0010
ECCPAS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000	0000 0000
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
PIE1	—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	0000 0-00
PIR1	—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	0000 0-00
PR2	Timer2 Module Period Register							1111 1111	1111 1111	
PWM1CON	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000	0000 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register							xxxx xxxx	uuuu uuuu	
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register							xxxx xxxx	uuuu uuuu	
TMR2	Timer2 Module Register							0000 0000	0000 0000	
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare and PWM.

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NOTES:

11.0 SPECIAL FEATURES OF THE CPU

The PIC16F616/16HV616 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC16F616/16HV616 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions-on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 11-1).

11.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 11-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information.

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REGISTER 11-1: CONFIG: CONFIGURATION WORD REGISTER

—	—	—	—	—	—	BOREN1 ⁽¹⁾	BOREN0 ⁽¹⁾
bit 15						bit 8	

IOSCFS	\overline{CP} ⁽²⁾	MCLRE ⁽³⁾	\overline{PWRTE}	WDTE	FOSC2	FOSC1	FOSC0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

P = Programmable'

U = Unimplemented bit,
read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '1'

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits⁽¹⁾

11 = BOR enabled

10 = BOR enabled during operation and disabled in Sleep

0x = BOR disabled

bit 7 **IOSCFS:** Internal Oscillator Frequency Select bit

1 = 8 MHz

0 = 4 MHz

bit 6 **CP:** Code Protection bit⁽²⁾

1 = Program memory code protection is disabled

0 = Program memory code protection is enabled

bit 5 **MCLRE:** \overline{MCLR} Pin Function Select bit⁽³⁾

1 = \overline{MCLR} pin function is \overline{MCLR}

0 = \overline{MCLR} pin function is digital input, \overline{MCLR} internally tied to VDD

bit 4 **PWRTE:** Power-up Timer Enable bit

1 = PWRT disabled

0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits

111 = RC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN

110 = RCIO oscillator: I/O function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN

101 = INTOSC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN

100 = INTOSCO oscillator: I/O function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN

011 = EC: I/O function on RA4/OSC2/CLKOUT pin, CLKIN on RA5/OSC1/CLKIN

010 = HS oscillator: High-speed crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN

001 = XT oscillator: Crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN

000 = LP oscillator: Low-power crystal on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.

2: The entire program memory will be erased when the code protection is turned off.

3: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

11.2 Calibration Bits

The 8 MHz internal oscillator is factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2009h). The Calibration Word is not erased when using the specified bulk erase sequence in the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) and thus, does not require reprogramming.

11.3 Reset

The PIC16F616/16HV616 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- MCLR Reset during normal operation
- MCLR Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

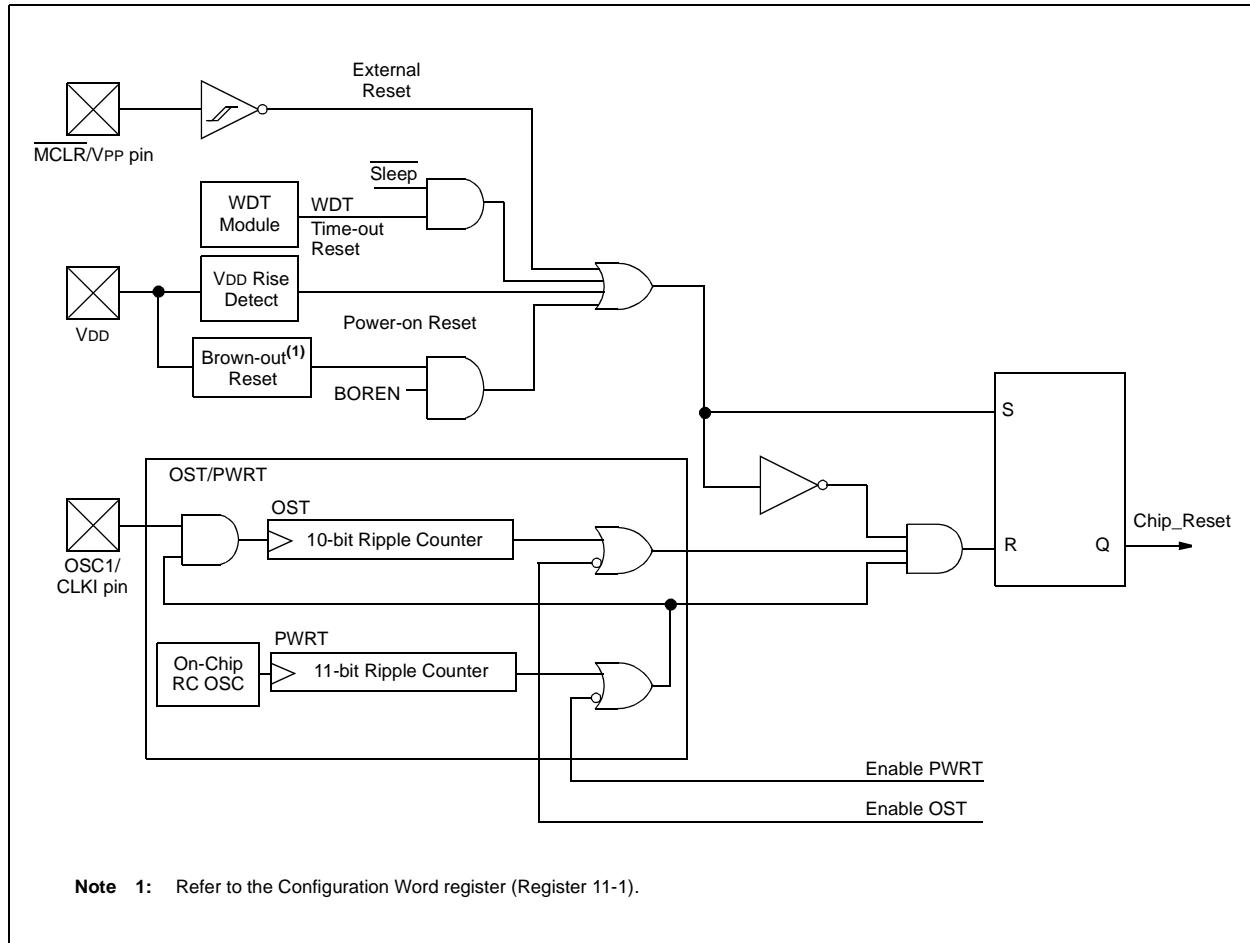
- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. $\overline{T0}$ and \overline{PD} bits are set or cleared differently in different Reset situations, as indicated in Table 11-2. Software can use these bits to determine the nature of the Reset. See Table 11-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 11-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 11-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 11-1).

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11.3.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See **Section 15.0 “Electrical Specifications”** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOR (see **Section 11.3.4 “Brown-out Reset (BOR)”**).

Note: The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach Vss for a minimum of 100 μ s.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure proper operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, “Power-up Trouble Shooting” (DS00607).

11.3.2 MCLR

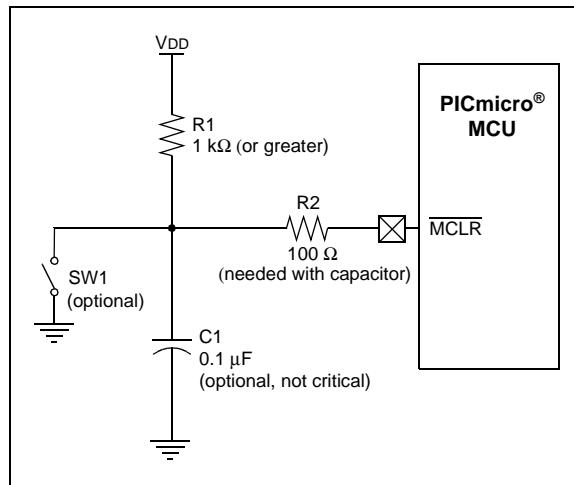
PIC16F616/16HV616 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 11-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the RA3/MCLR pin becomes an external Reset input. In this mode, the RA3/MCLR pin has a weak pull-up to Vdd.

FIGURE 11-2: RECOMMENDED MCLR CIRCUIT



11.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from an internal RC oscillator. For more information, see **Section 3.4 “Internal Clock Modes”**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRTE, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 15.0 “Electrical Specifications”**).

Note: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the MCLR pin, rather than pulling this pin directly to Vss.

11.3.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0> = 10, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 11-1 for the Configuration Word definition.

A brown-out occurs when VDD falls below VBOR for greater than parameter TBOR (see **Section 15.0 "Electrical Specifications"**). The brown-out condition will reset the device. This will occur regardless of VDD slew rate. A Brown-out Reset may not occur if VDD falls below VBOR for less than parameter TBOR.

On any Reset (Power-on, Brown-out Reset, Watchdog timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 11-3). If enabled, the Power-up Timer will be invoked by the Reset and keep the chip in Reset an additional 64 ms.

Note: The Power-up Timer is enabled by the PWRTE bit in the Configuration Word register.

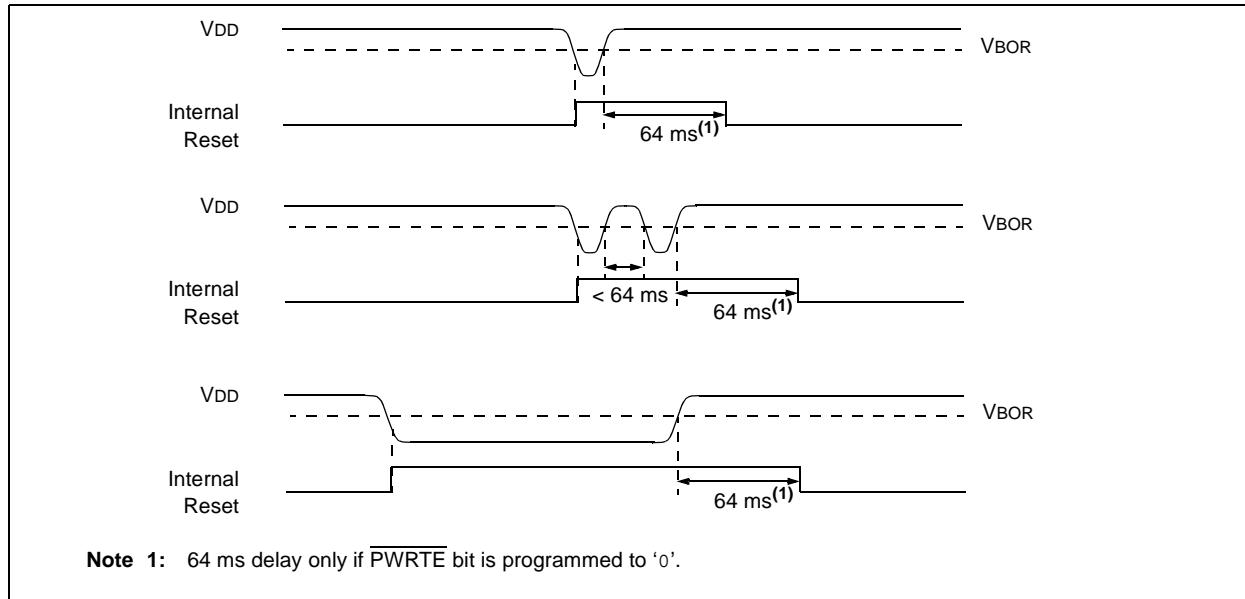
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

11.3.5 BOR CALIBRATION

The PIC16F616/16HV616 stores the BOR calibration values in fuses located in the Calibration Word register (2008h). The Calibration Word register is not erased when using the specified bulk erase sequence in the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) and thus, does not require reprogramming.

Note: Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information.

FIGURE 11-3: BROWN-OUT SITUATIONS



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11.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 11-4, Figure 11-5 and Figure 11-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 11-5). This is useful for testing purposes or to synchronize more than one PIC16F616/16HV616 device operating in parallel.

Table 11-5 shows the Reset conditions for some special registers, while Table 11-4 shows the Reset conditions for all the registers.

11.3.7 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is BOR (Brown-out). BOR is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if BOR = 0, indicating that a Brown-out has occurred. The BOR Status bit is a “don’t care” and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a ‘0’ on Power-on Reset and unaffected otherwise. The user must write a ‘1’ to this bit following a Power-on Reset. On a subsequent Reset, if POR is ‘0’, it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 11.3.4 “Brown-out Reset (BOR)”**.

TABLE 11-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	<u>PWRTE</u> = 0	<u>PWRTE</u> = 1	<u>PWRTE</u> = 0	<u>PWRTE</u> = 1	
XT, HS, LP	TPWRT + 1024 • TOSC	1024 • TOSC	TPWRT + 1024 • TOSC	1024 • TOSC	1024 • TOSC
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 11-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

<u>POR</u>	<u>BOR</u>	<u>TO</u>	<u>PD</u>	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	MCLR Reset during normal operation
u	u	1	0	MCLR Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets ⁽¹⁾
PCON	—	—	—	—	—	—	<u>POR</u>	<u>BOR</u>	---- - -qq	---- - -uu
STATUS	IRP	RP1	RP0	<u>TO</u>	<u>PD</u>	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as ‘0’, q = value depends on condition.
Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

FIGURE 11-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 1

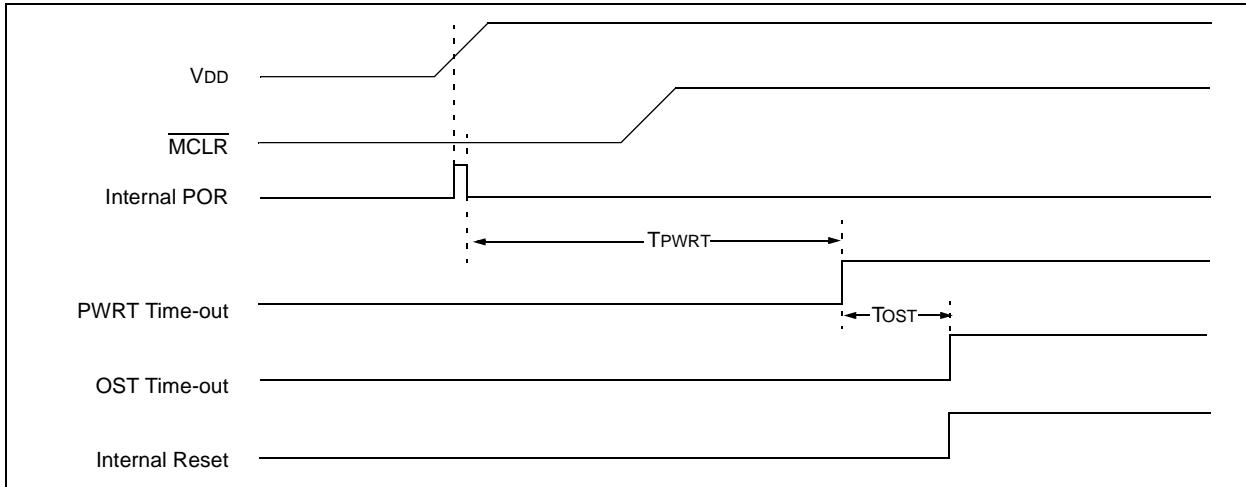


FIGURE 11-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 2

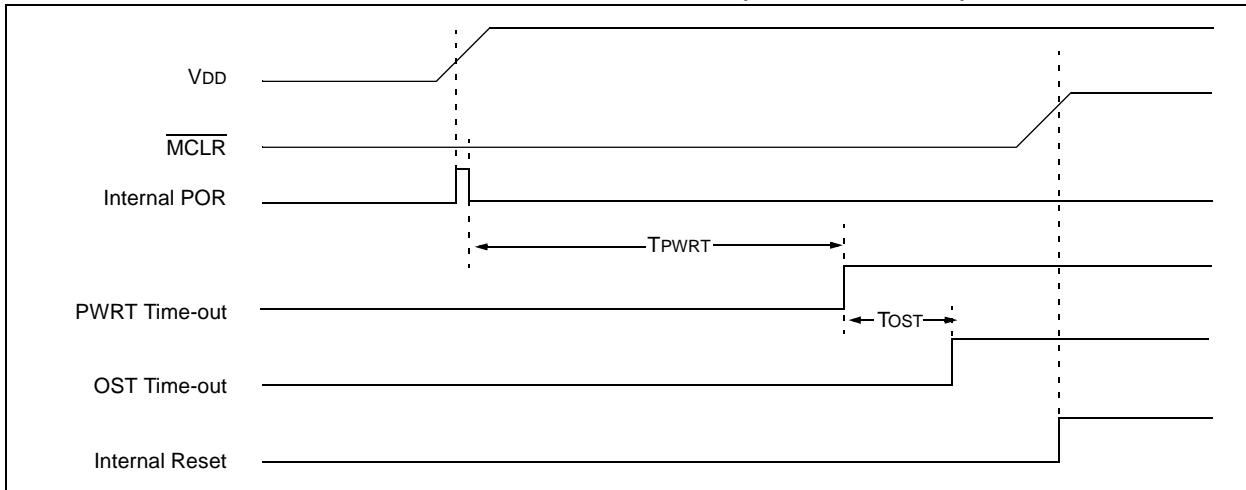
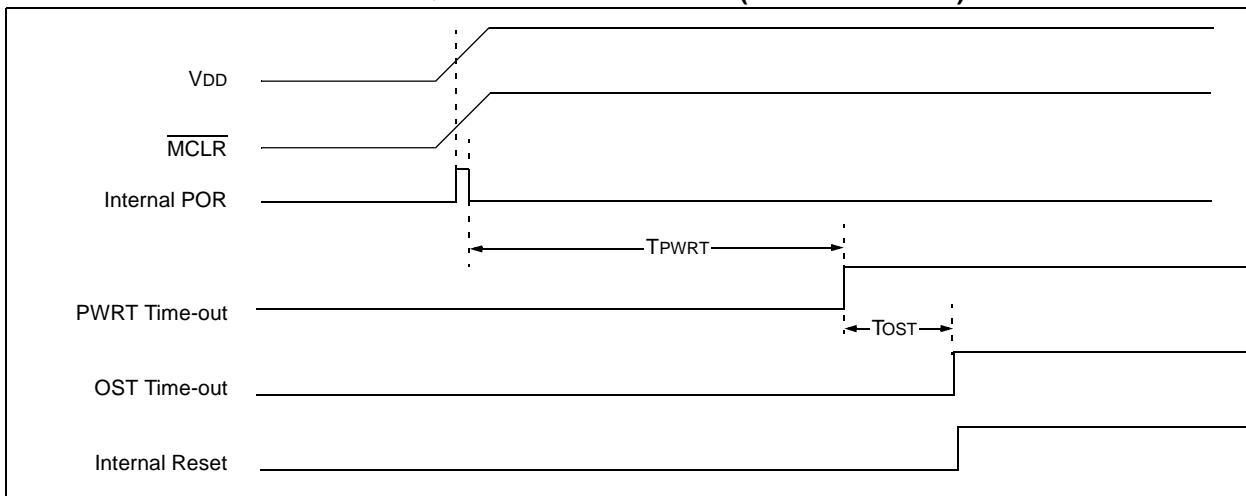


FIGURE 11-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR WITH VDD)



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TABLE 11-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMRO	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--x0 x000	--u0 u000	--uu uuuu
PORTC	07h	--xx xx00	--uu 0uuu	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu ⁽²⁾
PIR1	0Ch	-000 0-00	-000 0-00	-uuu u-uu ⁽²⁾
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	15h	0000 0000	0000 0000	uuuu uuuu
PWM1CON	16h	0000 0000	0000 0000	uuuu uuuu
ECCPAS	17h	0000 0000	0000 0000	uuuu uuuu
VRCON	19h	0000 0000	0000 0000	uuuu uuuu
CM1CON0	1Ah	0000 -000	0000 -000	uuuu -uuu
CM2CON0	1Bh	0000 -000	0000 -000	uuuu -uuu
CM2CON1	1Ch	00-0 0000	00-0 0000	uu-u uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADC0N0	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISC	87h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	-000 0-00	-000 0-00	-uuu u-uu
PCON	8Eh	---- --0x	---- --uu ^(1, 5)	---- --uu
OSCTUNE	90h	---0 0000	---u uuuu	--u uuuu
ANSEL	91h	1111 1111	1111 1111	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 11-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 11-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	MCLR Reset WDT Reset (Continued) Brown-out Reset ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out (Continued)
PR2	92h	1111 1111	1111 1111	1111 1111
WPUA	95h	--11 -111	--11 -111	--uu -uuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
SRCON0	99h	0000 00-0	0000 00-0	uuuu uu-u
SRCON1	9Ah	00-- -----	00-- -----	uu-- -----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000 -----	-000 -----	-uuu -----

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 11-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 11-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
MCLR Reset during normal operation	000h	000u uuuu	---- --uu
MCLR Reset during Sleep	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --10
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

11.4 Interrupts

The PIC16F616/16HV616 has 9 sources of interrupt:

- External Interrupt RA2/INT
- Timer0 Overflow Interrupt
- PORTA Change Interrupts
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 11-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, Enhanced CCP modules, refer to the respective peripheral section.

11.4.1 RA2/INT INTERRUPT

The external interrupt on the RA2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the RA2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 11.7 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 11-9 for timing of wake-up from Sleep through RA2/INT interrupt.

Note: The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’ and cannot generate an interrupt.

11.4.2 TIMER0 INTERRUPT

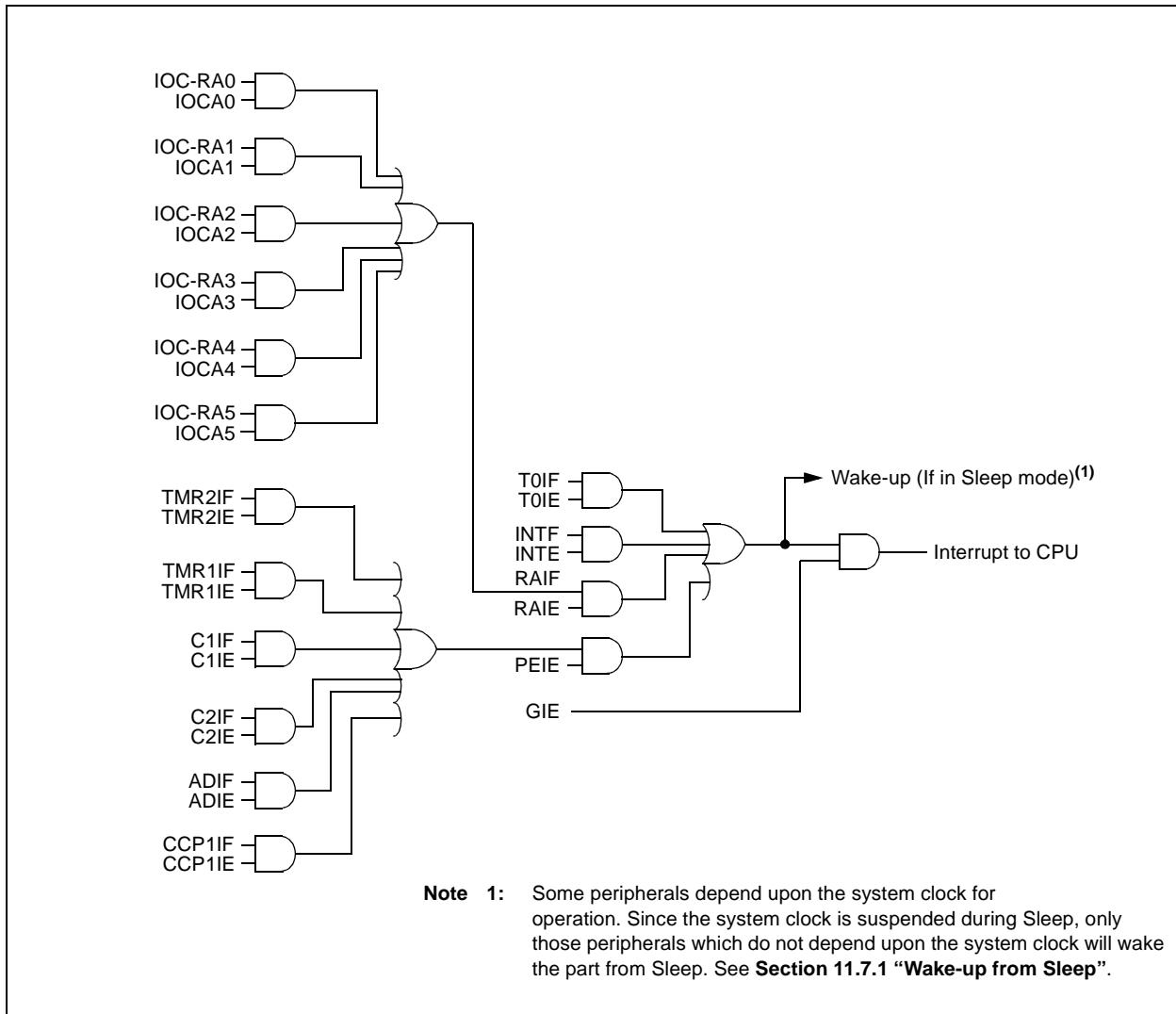
An overflow ($FFh \rightarrow 00h$) in the TMR0 register will set the T0IF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing T0IE bit of the INTCON register. See **Section 5.0 “Timer0 Module”** for operation of the Timer0 module.

11.4.3 PORTA INTERRUPT-ON-CHANGE

An input change on PORTA sets the RAIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the RAIE bit of the INTCON register. Plus, individual pins can be configured through the IOCA register.

Note: If a change on the I/O pin should occur when any PORTA operation is being executed, then the RAIF interrupt flag may not get set.

FIGURE 11-7: INTERRUPT LOGIC



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FIGURE 11-8: INT PIN INTERRUPT TIMING

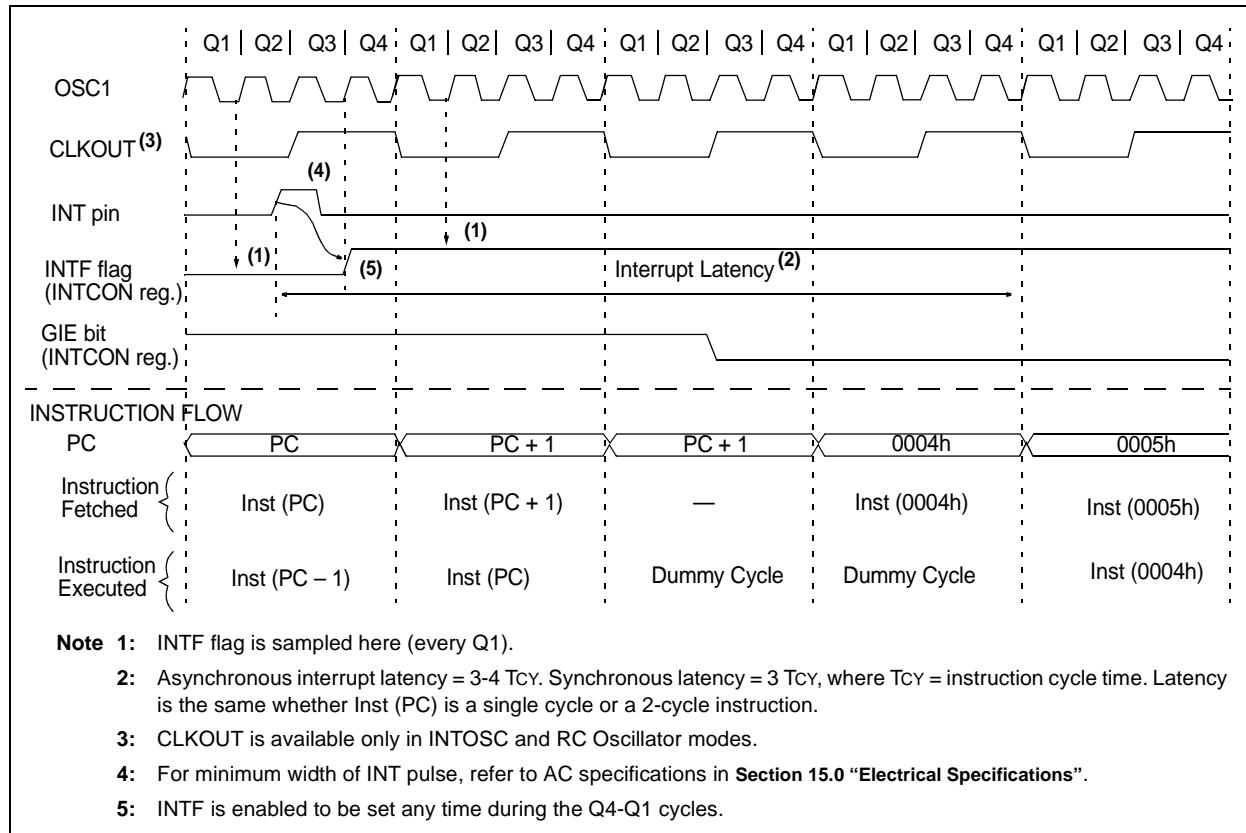


TABLE 11-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: all other Resets
INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
PIR1	—	ADIF	CCP1IF	C2IF	C1IF	—	TMR2IF	TMR1IF	-000 0-00	-000 0-00
PIE1	—	ADIE	CCP1IE	C2IE	C1IE	—	TMR2IE	TMR1IE	-000 0-00	-000 0-00

Legend: x = unknown, u = unchanged, - = unimplemented read as ‘0’, q = value depends upon condition.

Shaded cells are not used by the interrupt module.

11.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-2). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 11-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note: The PIC16F616/16HV616 does not require saving the PCLATH. However, if computed GOTOS are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 11-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF  W_TEMP           ;Copy W to TEMP register
SWAPF  STATUS,W          ;Swap status to be saved into W
                         ;Swaps are used because they do not affect the status bits
MOVWF  STATUS_TEMP        ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                   ;Insert user code here
:
SWAPF  STATUS_TEMP,W     ;Swap STATUS_TEMP register into W
                         ;(sets bank to original state)
MOVWF  STATUS             ;Move W into STATUS register
SWAPF  W_TEMP,F           ;Swap W_TEMP
SWAPF  W_TEMP,W           ;Swap W_TEMP into W
```

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11.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time out generates a device Reset. If the device is in Sleep mode, a WDT time out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (Section 11.1 "Configuration Bits").

11.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The $\overline{T0}$ bit in the STATUS register will be cleared upon a Watchdog Timer time out.

11.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (i.e., $VDD = \text{Min.}$, Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time out occurs.

FIGURE 11-2: WATCHDOG TIMER BLOCK DIAGRAM

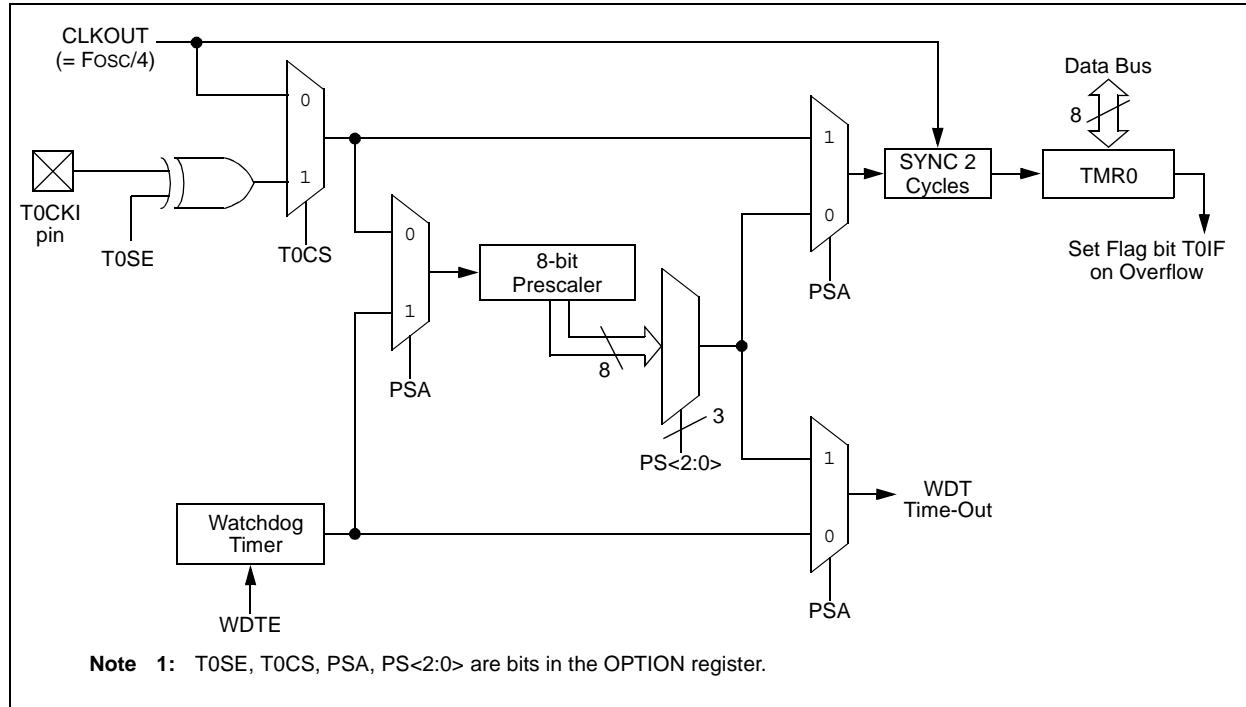


TABLE 11-7: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

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TABLE 11-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
OPTION_REG	RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
CONFIG	IOSCFS	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 11-1 for operation of all Configuration Word register bits.

11.7 Power-Down Mode (Sleep)

The Power-Down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- PD bit in the STATUS register is cleared.
- TO bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or Vss, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The MCLR pin must be at a logic high level.

Note: It should be noted that a Reset generated by a WDT time-out does not drive MCLR pin low.

11.7.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on MCLR pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from RA2/INT pin, PORTA change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device Reset. The PD bit, which is set on power-up, is cleared when Sleep is invoked. TO bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. Timer1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ECCP Capture mode interrupt.
3. A/D conversion (when A/D clock source is RC).
4. Comparator output changes state.
5. Interrupt-on-change.
6. External Interrupt from INT pin.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared) and any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

11.7.2 WAKE-UP USING INTERRUPTS

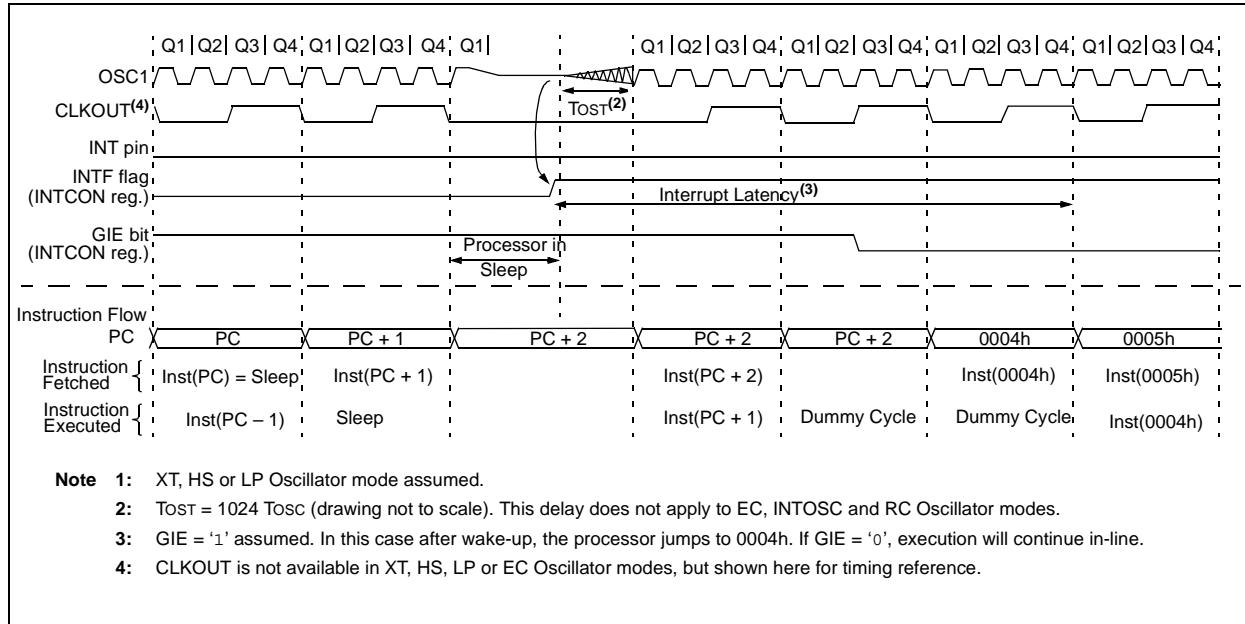
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the TO bit will not be set and the PD bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction is executed. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction. See Figure 11-9 for more details.

FIGURE 11-9: WAKE-UP FROM SLEEP THROUGH INTERRUPT



11.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note: The entire Flash program memory will be erased when the code protection is turned off. See the “PIC12F6XX/16F6XX Memory Programming Specification” (DS41204) for more information.

11.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

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11.10 In-Circuit Serial Programming™

The PIC16F616/16HV616 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

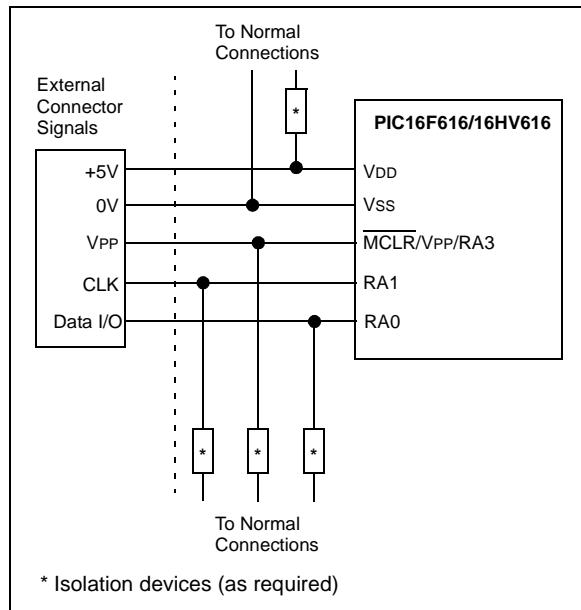
- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (VPP) pin from V_{IL} to V_{IH}. See the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 11-10.

FIGURE 11-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



11.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with an 14-pin device is not practical. A special 20-pin PIC16F616/16HV616 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC16F616/16HV616 device. The debugging adapter is the only source of the ICD device.

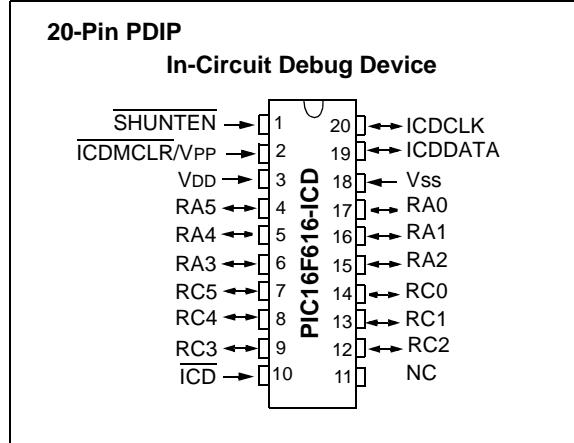
When the ICD pin on the PIC16F616/16HV616 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 11-9 shows which features are consumed by the background debugger.

TABLE 11-9: DEBUGGER RESOURCES

Resource	Description
I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be NOP 700h-7FFh

For more information, see "MPLAB® ICD 2 In-Circuit Debugger User's Guide" (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 11-11: 20-PIN ICD PINOUT



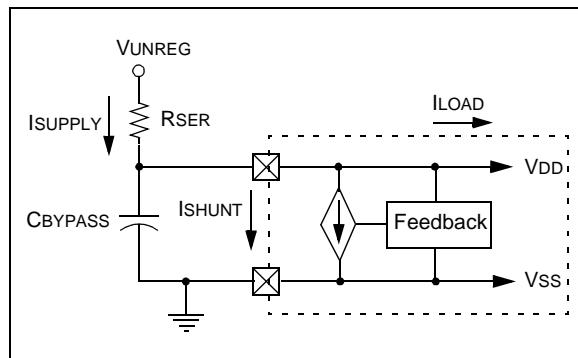
12.0 VOLTAGE REGULATOR

The PIC16HV616 includes a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

12.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 12-1 for voltage regulator schematic.

FIGURE 12-1: VOLTAGE REGULATOR



An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 12-1.

EQUATION 12-1: RSER LIMITING RESISTOR

$$R_{MAX} = \frac{(V_{UMIN} - 5V)}{1.05 \cdot (4\text{ mA} + I_{LOAD})}$$

$$R_{MIN} = \frac{(V_{UMAX} - 5V)}{0.95 \cdot (50\text{ mA})}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

12.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC16HV616 device.

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NOTES:

13.0 INSTRUCTION SET SUMMARY

The PIC16F616/16HV616 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
 - **Bit-oriented** operations
 - **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

Table 13-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal** and **control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μ s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

13.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RAIF flag.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1 .
PC	Program Counter
TO	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
PD	Power-down bit

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations							
13	8	7	6	0			
OPCODE		d	f (FILE #)				
d = 0 for destination W							
d = 1 for destination f							
f = 7-bit file register address							
Bit-oriented file register operations							
13	10	9	7	6	0		
OPCODE		b	(BIT #)	f	(FILE #)		
b = 3-bit bit address							
f = 7-bit file register address							
Literal and control operations							
General							
13	8	7	0				
OPCODE		k (literal)					
k = 8-bit immediate value							
CALL and GOTO instructions only							
13	11	10	0				
OPCODE		k (literal)					
k = 11-bit immediate value							

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TABLE 13-2: PIC16F616/16HV616 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1, 2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1, 2
DECFSZ	f, d	Decrement f	1	00 0011 dfff ffff	Z	1, 2
DECF	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1, 2, 3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1, 2, 3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1, 2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1, 2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1, 2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1, 2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1, 2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1, 2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1, 2
BTFSZ	f, b	Bit Test f, Skip if Clear	1(2)	01 10bb bfff ffff		3
BTFSZ	f, b	Bit Test f, Skip if Set	1(2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call Subroutine	2	10 0kkk kkkk kkkk		
CLRWD	-	Clear Watchdog Timer	1	00 0000 0110 0100	TO, PD	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk		
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into Standby mode	1	00 0000 0110 0011	TO, PD	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF PORTA, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.
- 3:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

13.2 Instruction Descriptions

ADDLW	Add literal and W
Syntax:	[<i>label</i>] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

BCF	Bit Clear f
Syntax:	[<i>label</i>] BCF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$0 \rightarrow (f)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

ADDWF	Add W and f
Syntax:	[<i>label</i>] ADDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow (\text{destination})$
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BSF	Bit Set f
Syntax:	[<i>label</i>] BSF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$1 \rightarrow (f)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

ANDLW	AND literal with W
Syntax:	[<i>label</i>] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .AND. (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[<i>label</i>] BTFSC f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	skip if $(f) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a two-cycle instruction.

ANDWF	AND W with f
Syntax:	[<i>label</i>] ANDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .AND. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

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BTFSS	Bit Test f, Skip if Set	CLRWDT	Clear Watchdog Timer
Syntax:	[<i>label</i>] BTFSS f,b	Syntax:	[<i>label</i>] CLRWDT
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$	Operands:	None
Operation:	skip if $(f < b) = 1$	Operation:	$00h \rightarrow WDT$ $0 \rightarrow WDT$ prescaler, $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$
Status Affected:	None	Status Affected:	$\overline{TO}, \overline{PD}$
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.	Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set.
CALL	Call Subroutine	COMF	Complement f
Syntax:	[<i>label</i>] CALL k	Syntax:	[<i>label</i>] COMF f,d
Operands:	$0 \leq k \leq 2047$	Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(PC)+1 \rightarrow TOS$, $k \rightarrow PC<10:0>$, $(PCLATH<4:3>) \rightarrow PC<12:11>$	Operation:	$(\bar{f}) \rightarrow (\text{destination})$
Status Affected:	None	Status Affected:	Z
Description:	Call Subroutine. First, return address ($PC + 1$) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits $<10:0>$. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.	Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.
CLRF	Clear f	DECFSNZ	Decrement f
Syntax:	[<i>label</i>] CLRF f	Syntax:	[<i>label</i>] DECFSNZ f,d
Operands:	$0 \leq f \leq 127$	Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$00h \rightarrow (f)$ $1 \rightarrow Z$	Operation:	$(f) - 1 \rightarrow (\text{destination})$
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.	Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.
CLRW	Clear W		
Syntax:	[<i>label</i>] CLRW		
Operands:	None		
Operation:	$00h \rightarrow (W)$ $1 \rightarrow Z$		
Status Affected:	Z		
Description:	W register is cleared. Zero bit (Z) is set.		

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$ skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow \text{PC}_{<10:0>}$ $\text{PCLATH}_{<4:3>} \rightarrow \text{PC}_{<12:11>}$
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .\text{OR. } k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

IORWF	Inclusive OR W with f
Syntax:	[<i>label</i>] IORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .\text{OR. } (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

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MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If $d = 0$, destination is W register. If $d = 1$, the destination is file register 'f' itself. $d = 1$ is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
<u>Example:</u>	MOVF FSR, 0
After Instruction	
W = value in FSR register Z = 1	

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
<u>Example:</u>	MOVW OPTION F
Before Instruction	
OPTION = 0xFF W = 0x4F	
After Instruction	
OPTION = 0x4F W = 0x4F	

MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
<u>Example:</u>	MOVLW 0x5A
After Instruction	
W = 0x5A	

NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
<u>Example:</u>	NOP

RETFIE	Return from Interrupt
Syntax:	[<i>label</i>] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	RETFIE

After Interrupt
 PC = TOS
 GIE = 1

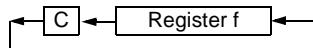
RETLW	Return with literal in W
Syntax:	[<i>label</i>] RETLW <i>k</i>
Operands:	0 ≤ <i>k</i> ≤ 255
Operation:	<i>k</i> → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal ' <i>k</i> '. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre> CALL TABLE;W contains ;table offset ;value GOTO DONE • • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • RETLW kn ;End of table </pre>
	DONE
	Before Instruction <i>W</i> = 0x07 After Instruction <i>W</i> = value of <i>k8</i>

RETURN	Return from Subroutine
Syntax:	[<i>label</i>] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

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RLF Rotate Left f through Carry

Syntax:	[<i>label</i>] RLF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1, 0

Before Instruction

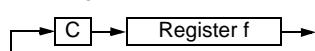
REG1	=	1110 0110
C	=	0

After Instruction

REG1	=	1110 0110
W	=	1100 1100
C	=	1

RRF Rotate Right f through Carry

Syntax:	[<i>label</i>] RRF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP Enter Sleep mode

Syntax:	[<i>label</i>] SLEEP
Operands:	None
Operation:	$00h \rightarrow \text{WDT}$, $0 \rightarrow \text{WDT prescaler}$, $1 \rightarrow \overline{\text{TO}}$, $0 \rightarrow \overline{\text{PD}}$
Status Affected:	$\overline{\text{TO}}, \overline{\text{PD}}$
Description:	The power-down Status bit, $\overline{\text{PD}}$ is cleared. Time-out Status bit, $\overline{\text{TO}}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBWF	Subtract W from f								
Syntax:	[<i>label</i>] SUBWF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(f) - (W) \rightarrow (\text{destination})$								
Status Affected:	C, DC, Z								
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.								
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">C = 0</td> <td style="padding: 2px;">W > f</td> </tr> <tr> <td style="padding: 2px;">C = 1</td> <td style="padding: 2px;">W ≤ f</td> </tr> <tr> <td style="padding: 2px;">DC = 0</td> <td style="padding: 2px;">W<3:0> > f<3:0></td> </tr> <tr> <td style="padding: 2px;">DC = 1</td> <td style="padding: 2px;">W<3:0> ≤ f<3:0></td> </tr> </table>		C = 0	W > f	C = 1	W ≤ f	DC = 0	W<3:0> > f<3:0>	DC = 1	W<3:0> ≤ f<3:0>
C = 0	W > f								
C = 1	W ≤ f								
DC = 0	W<3:0> > f<3:0>								
DC = 1	W<3:0> ≤ f<3:0>								

XORWF	Exclusive OR W with
Syntax:	[<i>label</i>] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .XOR. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SWAPF	Swap Nibbles in f
Syntax:	[<i>label</i>] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (\text{destination}<7:4>),$ $(f<7:4>) \rightarrow (\text{destination}<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW	Exclusive OR literal with W
Syntax:	[<i>label</i>] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .XOR. k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

PIC16F616/16HV616

NOTES:

14.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C18 and MPLAB C30 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD 2
- Device Programmers
 - PICSTART® Plus Development Programmer
 - MPLAB PM3 Device Programmer
 - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (assembly or C)
 - Mixed assembly and C
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

14.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

14.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 family of microcontrollers and the dsPIC30, dsPIC33 and PIC24 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PICmicro MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

14.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.8 MPLAB ICE 4000 High-Performance In-Circuit Emulator

The MPLAB ICE 4000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro MCUs and dsPIC DSCs. Software control of the MPLAB ICE 4000 In-Circuit Emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high-speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, and up to 2 Mb of emulation memory.

The MPLAB ICE 4000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PICmicro MCUs and can be used to develop for these and other PICmicro MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

14.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

14.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PICmicro devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

14.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

14.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PICmicro MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest "Product Selector Guide" (DS00148) for the complete list of demonstration, development and evaluation kits.

15.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^(†)

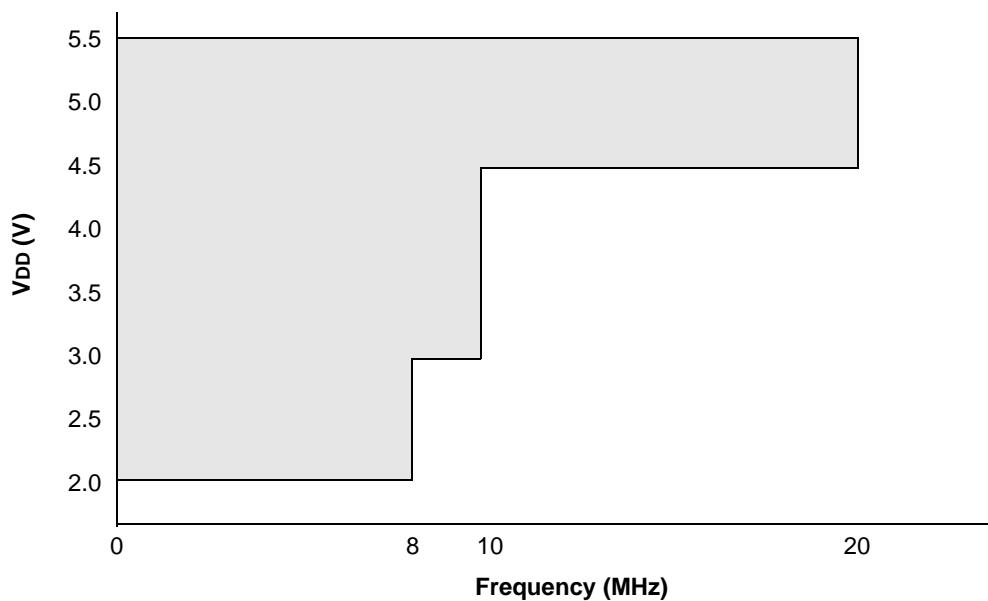
Ambient temperature under bias	-40° to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +6.5V
Voltage on MCLR with respect to Vss	-0.3V to +13.5V
Voltage on all other pins with respect to Vss	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of VSS pin	95 mA
Maximum current into VDD pin	95 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA and PORTC (combined)	90 mA
Maximum current sourced PORTA and PORTC (combined)	90 mA

Note 1: Power dissipation is calculated as follows: P_{DIS} = V_{DD} x {I_{DD} - \sum I_{OH}} + \sum {(V_{DD} - V_{OH}) x I_{OH}} + \sum (V_{OL} x I_{OL}).

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

PIC16F616/16HV616

**FIGURE 15-1: PIC16F616/16HV616 VOLTAGE-FREQUENCY GRAPH,
 $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$**



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

15.1 DC Characteristics: PIC16F616/16HV616-I (Industrial) PIC16F616/16HV616-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	VDD	Supply Voltage	2.0	—	5.5	V	FOSC < = 8 MHz: INTOSC, EC
D001		PIC16F616	2.0	—	5.5	V	FOSC < = 4 MHz
D001		PIC16HV616	2.0	—	5.5	V	FOSC < = 4 MHz
D001C		PIC16F616	3.0	—	5.5	V	FOSC < = 10 MHz
D001C		PIC16HV616	3.0	—	5.5	V	FOSC < = 10 MHz
D001D		PIC16F616	4.5	—	5.5	V	FOSC < = 20 MHz
D001D		PIC16HV616	4.5	—	5.5	V	FOSC < = 20 MHz
D002*	VDR	RAM Data Retention Voltage⁽¹⁾	1.5	—	—	V	Device in Sleep mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	Vss	—	V	See Section 11.3.1 “Power-on Reset (POR)” for details.
D004*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 11.3.1 “Power-on Reset (POR)” for details.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

PIC16F616/16HV616

15.2 DC Characteristics: PIC16F616/16HV616-I (Industrial) PIC16F616/16HV616-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
		VDD				Note	
D010	Supply Current (IDD)^(1, 2)	—	11	16	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	18	28	µA	3.0	
		—	35	54	µA	5.0	
D011*		—	140	240	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	220	380	µA	3.0	
		—	380	550	µA	5.0	
D012		—	260	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	420	650	µA	3.0	
		—	0.8	1.1	mA	5.0	
D013*		—	130	220	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	215	360	µA	3.0	
		—	360	520	µA	5.0	
D014		—	220	340	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	375	550	µA	3.0	
		—	0.65	1.0	mA	5.0	
D016*		—	340	450	µA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	700	µA	3.0	
		—	0.8	1.2	mA	5.0	
D017		—	410	650	µA	2.0	FOSC = 8 MHz INTOSC mode
		—	700	950	µA	3.0	
		—	1.30	1.65	mA	5.0	
D018		—	230	400	µA	2.0	FOSC = 4 MHz EXT RC mode ⁽³⁾
		—	400	680	µA	3.0	
		—	0.63	1.1	mA	5.0	
D019		—	2.6	3.25	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	2.8	3.35	mA	5.0	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula $IR = VDD/2REXT$ (mA) with REXT in kΩ.

15.3 DC Characteristics: PIC16F616

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	Power-down Base Current(IPD)⁽²⁾	—	0.05	1.2	μA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	1.5	μA	3.0	
		—	0.35	1.8	μA	5.0	$-40^{\circ}\text{C} \leq \text{TA} \leq +25^{\circ}\text{C}$
		—	150	500	nA	3.0	
D021		—	1.0	2.2	μA	2.0	WDT Current ⁽¹⁾
		—	2.0	4.0	μA	3.0	
		—	3.0	7.0	μA	5.0	
D022		—	42	60	μA	3.0	BOR Current ⁽¹⁾
		—	85	122	μA	5.0	
D023		—	32	45	μA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024		—	30	36	μA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	55	μA	3.0	
		—	75	95	μA	5.0	
D025*		—	39	47	μA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	72	μA	3.0	
		—	98	124	μA	5.0	
D026		—	4.5	7.0	μA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	5.0	8.0	μA	3.0	
		—	6.0	12	μA	5.0	
D027		—	0.30	1.6	μA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	1.9	μA	5.0	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

PIC16F616/16HV616

15.4 DC Characteristics: PIC16F616/16HV616-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						V _{DD}	Note
D020E	Power-down Base Current (IPD)⁽²⁾	—	0.05	9	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.15	11	µA	3.0	
		—	0.35	15	µA	5.0	
D021E		—	1	17.5	µA	2.0	WDT Current ⁽¹⁾
		—	2	19	µA	3.0	
		—	3	22	µA	5.0	
D022E		—	42	65	µA	3.0	BOR Current ⁽¹⁾
		—	85	127	µA	5.0	
D023E		—	32	45	µA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	µA	3.0	
		—	120	160	µA	5.0	
D024E		—	30	70	µA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	90	µA	3.0	
		—	75	120	µA	5.0	
D025E*		—	39	91	µA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	117	µA	3.0	
		—	98	156	µA	5.0	
D026E		—	4.5	25	µA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	5	30	µA	3.0	
		—	6	40	µA	5.0	
D027E		—	0.30	12	µA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	16	µA	5.0	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD}.

15.5 DC Characteristics: PIC16F616/16HV616-I (Industrial) PIC16F616/16HV616-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D033A	VIL	Input Low Voltage I/O Port: with TTL buffer	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
		with Schmitt Trigger buffer	Vss	—	0.15 VDD	V	2.0V ≤ VDD ≤ 4.5V
		MCLR, OSC1 (RC mode) ⁽¹⁾	Vss	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
		OSC1 (XT and LP modes)	Vss	—	0.2 VDD	V	
		OSC1 (HS mode)	Vss	—	0.3	V	
		OSC1 (RC mode)	Vss	—	0.3 VDD	V	
D040 D040A D041 D042 D043 D043A D043B	VIH	Input High Voltage I/O ports: with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
		with Schmitt Trigger buffer	0.25 VDD + 0.8	—	VDD	V	2.0V ≤ VDD ≤ 4.5V
		MCLR	0.8 VDD	—	VDD	V	2.0V ≤ VDD ≤ 5.5V
		OSC1 (XT and LP modes)	0.8 VDD	—	VDD	V	
		OSC1 (HS mode)	1.6	—	VDD	V	
		OSC1 (RC mode)	0.7 VDD	—	VDD	V	
		OSC1 (RC mode)	0.9 VDD	—	VDD	V	(Note 1)
D060 D061 D063	IIL	Input Leakage Current⁽²⁾ I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
		MCLR ⁽³⁾	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD
		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070*	IPUR	PORTA Weak Pull-up Current	50	250	400	µA	VDD = 5.0V, VPIN = VSS
D080	VOL	Output Low Voltage⁽⁴⁾ I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
D090	VOH	Output High Voltage⁽⁴⁾ I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

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15.5 DC Characteristics: PIC16F616/16HV616-I (Industrial) PIC16F616/16HV616-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100							
D101*	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	
Program Flash Memory							
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 4:** Including OSC2 in CLKOUT mode.

15.6 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$					
Param No.	Sym	Characteristic	Typ	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	69.8	C/W	14-pin PDIP package
			85.0	C/W	14-pin SOIC package
			100.4	C/W	14-pin TSSOP package
			46.3	C/W	16-pin QFN 4x4mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	32.5	C/W	14-pin PDIP package
			31.0	C/W	14-pin SOIC package
			31.7	C/W	14-pin TSSOP package
			2.6	C/W	16-pin QFN 4x4mm package
TH03	TDIE	Die Temperature	150	C	
TH04	PD	Power Dissipation	—	W	$\text{PD} = \text{PINTERNAL} + \text{PI/O}$
TH05	PINTERNAL	Internal Power Dissipation	—	W	$\text{PINTERNAL} = \text{IDD} \times \text{VDD}$ (NOTE 1)
TH06	PI/O	I/O Power Dissipation	—	W	$\text{PI/O} = \sum (\text{IOL} * \text{VOL}) + \sum (\text{IOH} * (\text{VDD} - \text{VOH}))$
TH07	PDER	Derated Power	—	W	$\text{PDER} = \text{PDMAX} (\text{TDIE} - \text{TA}) / \theta_{JA}$ (NOTE 2)

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

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15.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS

T	
F	Frequency

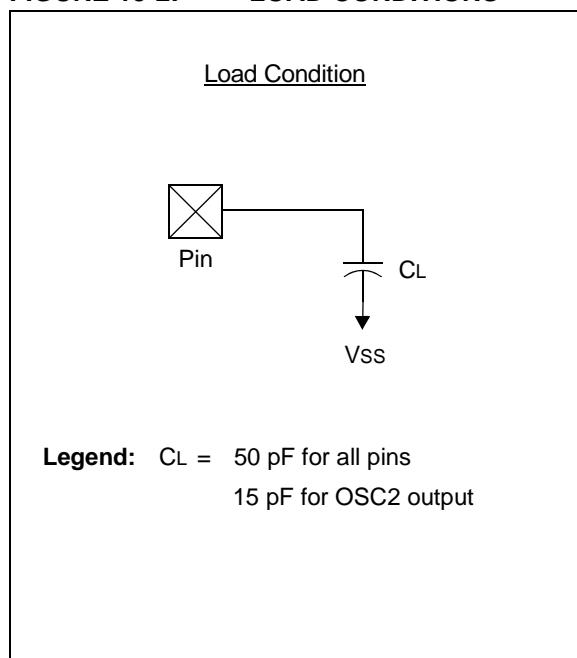
Lowercase letters (pp) and their meanings:

pp	
cc	CCP1
ck	CLKOUT
cs	<u>CS</u>
di	SDI
do	SDO
dt	Data in
io	I/O Port
mc	<u>MCLR</u>
osc	OSC1
rd	<u>RD</u>
rw	<u>RD</u> or <u>WR</u>
sc	SCK
ss	<u>SS</u>
t0	T0CKI
t1	T1CKI
wr	<u>WR</u>

Uppercase letters and their meanings:

S	
F	Fall
H	High
I	Invalid (High-impedance)
L	Low
P	Period
R	Rise
V	Valid
Z	High-impedance

FIGURE 15-2: LOAD CONDITIONS



15.8 AC Characteristics: PIC16F616/16HV616 (Industrial, Extended)

FIGURE 15-3: CLOCK TIMING

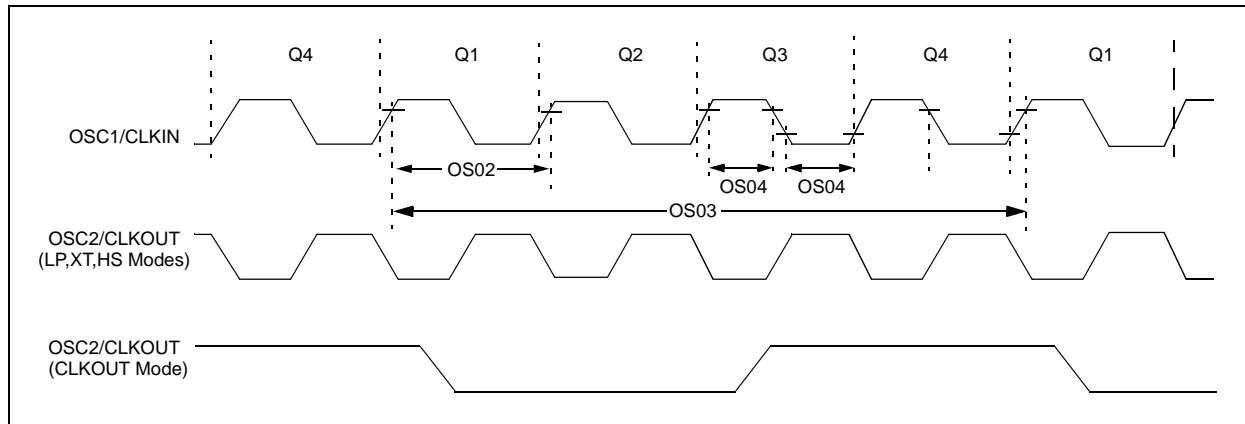


TABLE 15-1: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS01	FOSC	External CLKIN Frequency ⁽¹⁾	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency ⁽¹⁾	—	32.768	—	kHz	LP Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
OS02	TOSC	External CLKIN Period ⁽¹⁾	27	—	∞	μs	LP Oscillator mode
			250	—	∞	ns	XT Oscillator mode
			50	—	∞	ns	HS Oscillator mode
			50	—	∞	ns	EC Oscillator mode
		Oscillator Period ⁽¹⁾	—	30.5	—	μs	LP Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
OS03	T _{CY}	Instruction Cycle Time ⁽¹⁾	200	T _{CY}	DC	ns	T _{CY} = 4/FOSC
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	2	—	—	μs	LP oscillator
			100	—	—	ns	XT oscillator
			20	—	—	ns	HS oscillator
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	0	—	∞	ns	LP oscillator
			0	—	∞	ns	XT oscillator
			0	—	∞	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

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TABLE 15-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic	Freq. Tolerance	Min	Typ†	Max	Units	Conditions
OS06	TWARM	Internal Oscillator Switch when running ⁽³⁾	—	—	—	2	TOSC	Slowest clock
OS08	INTOSC	Internal Calibrated INTOSC Frequency ⁽²⁾	$\pm 1\%$ $\pm 2\%$ $\pm 5\%$	7.92 7.84 7.60	8.0 8.0 8.0	8.08 8.16 8.40	MHz MHz MHz	VDD = 3.5V, 25°C $2.5V \leq \text{VDD} \leq 5.5V$, $0^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ $2.0V \leq \text{VDD} \leq 5.5V$, $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ (Ind.), $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ (Ext.)
OS10*	TOSC ST	INTOSC Oscillator Wake-up from Sleep Start-up Time	—	5.5	12	24	μs	VDD = 2.0V, -40°C to $+85^{\circ}\text{C}$
			—	3.5	7	14		VDD = 3.0V, -40°C to $+85^{\circ}\text{C}$
			—	3	6	11		VDD = 5.0V, -40°C to $+85^{\circ}\text{C}$

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to the OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.
- 2:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.
- 3:** By design.

FIGURE 15-4: CLKOUT AND I/O TIMING

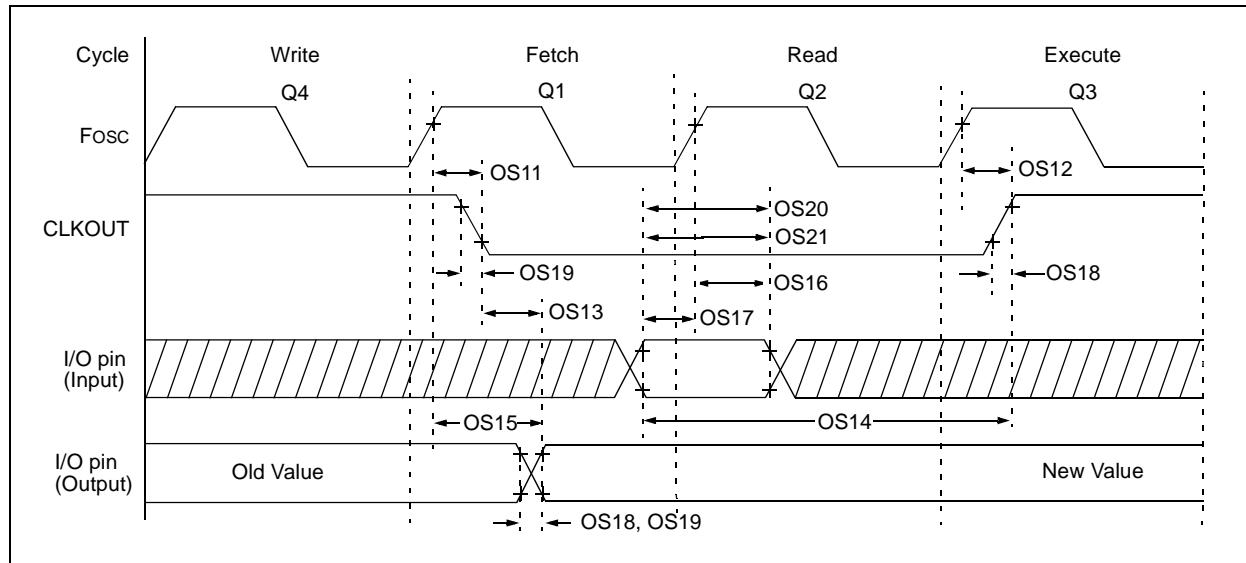


TABLE 15-3: CLKOUT AND I/O TIMING PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typt	Max	Units	Conditions
OS11	TosH2ckL	Fosc \uparrow to CLKOUT \downarrow (1)	—	—	70	ns	VDD = 5.0V
OS12	TosH2ckH	Fosc \uparrow to CLKOUT \uparrow (1)	—	—	72	ns	VDD = 5.0V
OS13	TckL2ioV	CLKOUT \downarrow to Port out valid (1)	—	—	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT \uparrow (1)	Tosc + 200 ns	—	—	ns	
OS15	TosH2ioV	Fosc \uparrow (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 5.0V
OS16	TosH2iol	Fosc \uparrow (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 5.0V
OS17	TioV2osH	Port input valid to Fosc \uparrow (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TioR	Port output rise time (2)	—	15 40	72 32	ns	VDD = 2.0V VDD = 5.0V
OS19	TioF	Port output fall time (2)	—	28 15	55 30	ns	VDD = 2.0V VDD = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TRAP	PORTA interrupt-on-change new input level time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

2: Includes OSC2 in CLKOUT mode.

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FIGURE 15-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

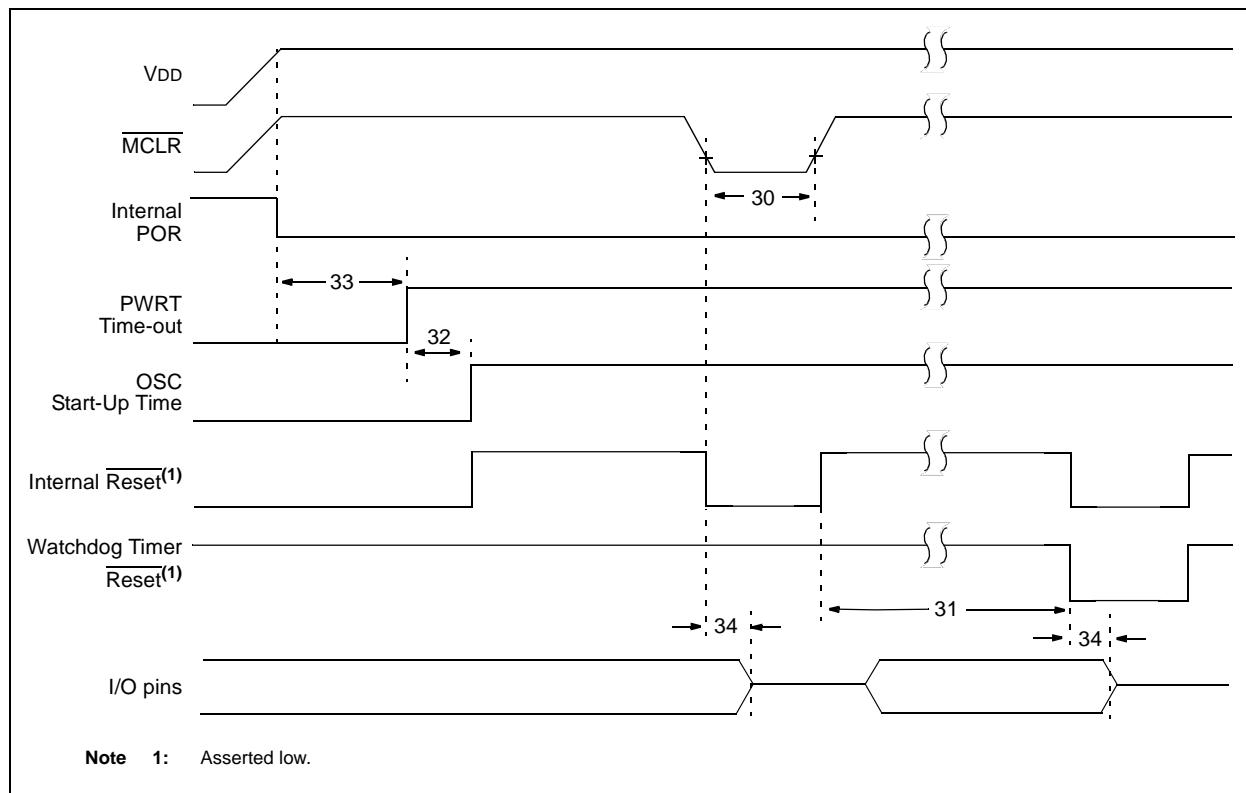


FIGURE 15-6: BROWN-OUT RESET TIMING AND CHARACTERISTICS

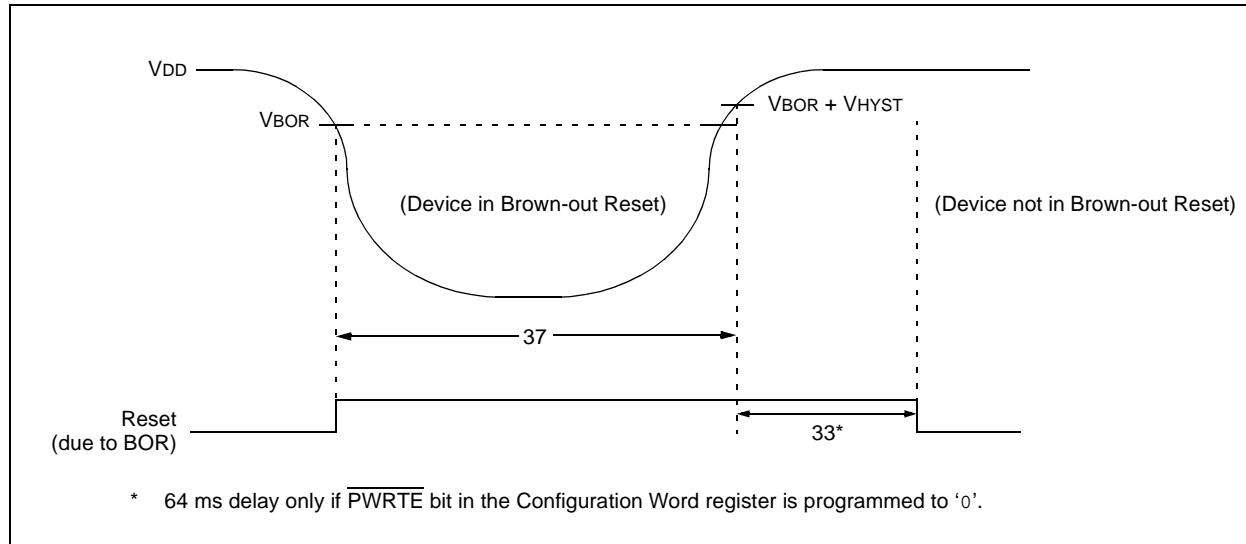


TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 5	— —	— —	μs μs	VDD = 5V, -40°C to $+85^{\circ}\text{C}$ VDD = 5V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	16 16	29 31	ms ms	VDD = 5V, -40°C to $+85^{\circ}\text{C}$ VDD = 5V
32	TOST	Oscillation Start-up Timer Period ^(1, 2)	—	1024	—	Tosc	(NOTE 3)
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
35	VBOR	Brown-out Reset Voltage	2.0	—	2.2	V	(NOTE 4)
36*	VHYST	Brown-out Reset Hysteresis	—	50	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	μs	VDD \leq VBOR

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to the OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

- 2: By design.
- 3: Period of the slower clock.
- 4: To ensure these voltage tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

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FIGURE 15-7: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

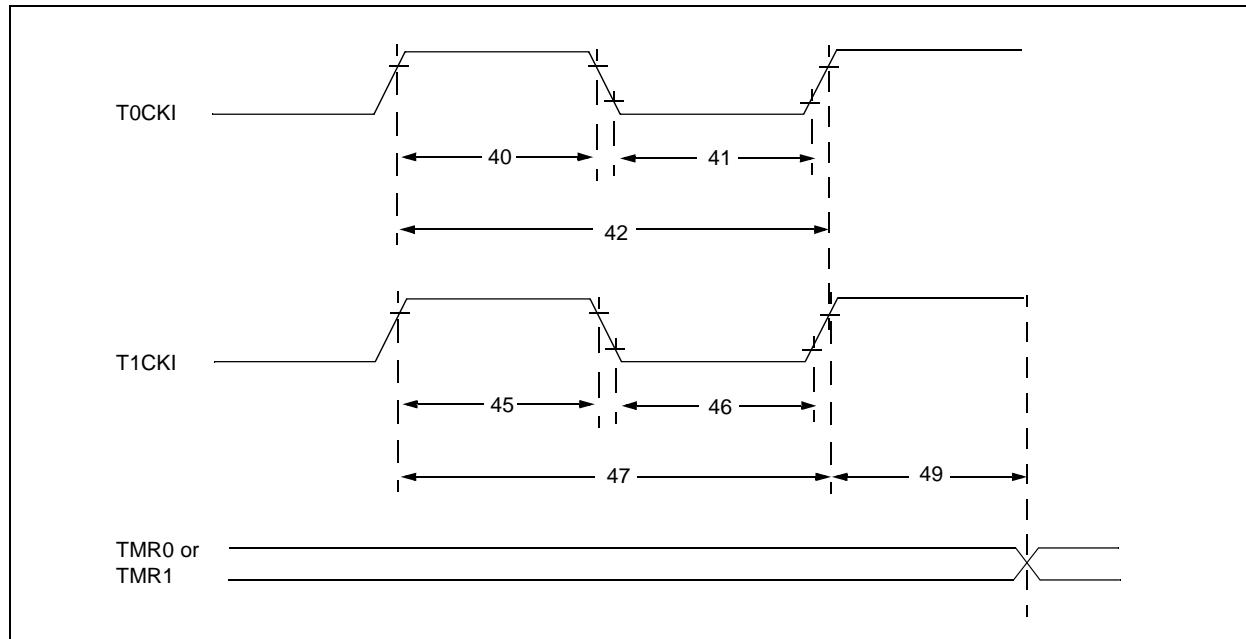


TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or $\frac{\text{TCY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{\text{TCY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 Tosc	—	7 Tosc	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-8: CAPTURE/COMPARE/PWM TIMINGS (ECCP)

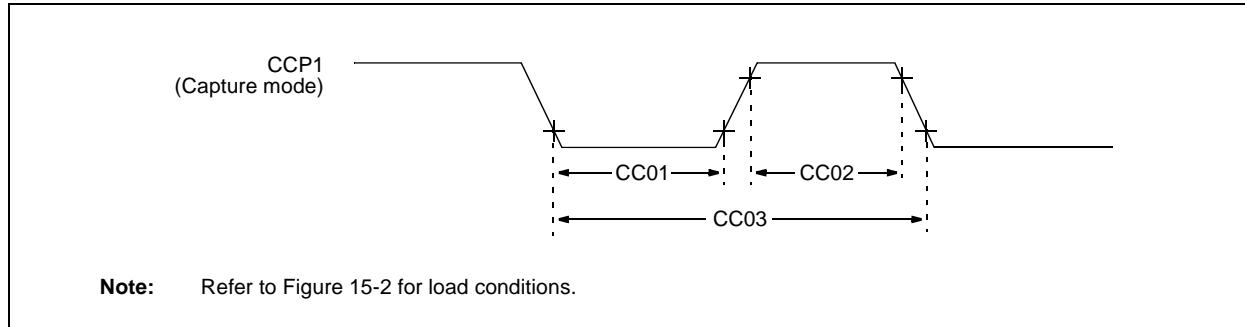


TABLE 15-6: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic		Min	Typt	Max	Units	Conditions
CC01*	TccL	CCP1 Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		$\frac{3\text{TCY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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TABLE 15-7: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristics		Min	Typ†	Max	Units	Comments
CM01	Vos	Input Offset Voltage		—	± 5.0	± 10	mV	(VDD - 1.5)/2
CM02	Vcm	Input Common Mode Voltage		0	—	VDD - 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	TRT	Response Time	Falling	—	150	600	ns	(NOTE 1)
			Rising	—	200	1000	ns	
CM05*	TMC2COV	Comparator Mode Change to Output Valid		—	—	10	μs	
CM06*	VHYS	Input Hysteresis Voltage		—	TBD	—	mV	

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV.

TABLE 15-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristics	Min	Typ†	Max	Units	Comments
CV01*	CLSB	Step Size ⁽²⁾	— —	VDD/24 VDD/32	— —	V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02*	CACC	Absolute Accuracy	— —	— —	$\pm 1/2$ $\pm 1/2$	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03*	CR	Unit Resistor Value (R)	—	2k	—	Ω	
CV04*	CST	Settling Time ⁽¹⁾	—	—	10	μs	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

2: See Section 8.10 "Comparator Voltage Reference" for more information.

TABLE 15-9: VOLTAGE (VP6) REFERENCE SPECIFICATIONS

VR Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$				
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
VR01	VP6OUT	VP6 voltage output	TBD	0.6	TBD	V	
VR02	TCVOUT	Voltage drift temperature coefficient	—	150	TBD	ppm/ $^{\circ}\text{C}$	
VR03	$\Delta\text{VP6OUT}/\Delta\text{VDD}$	Voltage drift with respect to VDD regulation	—	200	—	$\mu\text{V/V}$	
VR04	TSTABLE	Settling Time	—	10	100*	μs	

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

TABLE 15-10: VOLTAGE REFERENCE (V1P2) SPECIFICATIONS

VR Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature	-40°C ≤ TA ≤ +125°C			
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
VR05	V1P2OUT	V1P2 voltage output	1.188 1.182 1.176	1.200 1.200 1.200	1.212 1.218 1.224	V V V	TA = 25°C 0°C ≤ TA ≤ +85°C -40°C ≤ TA ≤ +125°C
VR06	TCVOUT	Voltage drift temperature coefficient	—	150	TBD	ppm/°C	
VR07	ΔV1P2OUT/ ΔVDD	Voltage drift with respect to VDD regulation	—	200	—	μV/V	
VR08	TSTABLE	Settling Time	—	10	100*	μs	
VR09	IV1P2OUT	V1P2 output current	—	—	TBD	μA	Unbuffered 1.2V out

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

TABLE 15-11: SHUNT REGULATOR SPECIFICATIONS (PIC16HV616 only)

SHUNT REGULATOR CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature	-40°C ≤ TA ≤ +125°C			
Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
SR01	VSHUNT	Shunt Voltage	4.25	5	5.25	V	
SR02	ISHUNT	Shunt Current	4	—	50	mA	
SR03*	TSETTLE	Settling Time	—	—	150	ns	To 1% of final value
SR04	CLOAD	Load Capacitance	0.01	—	10	μF	Bypass capacitor on VDD pin
SR05	ΔISNT	Regulator operating current	—	—	180	μA	Includes band gap reference current

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

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TABLE 15-12: PIC16F616/16HV616 A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	± 1	Lsb	VREF = 5.12V
AD03	EDL	Differential Error	—	—	± 1	Lsb	No missing codes to 10 bits VREF = 5.12V
AD04	E _{OFF}	Offset Error	—	—	± 1	Lsb	VREF = 5.12V
AD07	EGN	Gain Error	—	—	± 1	Lsb	VREF = 5.12V
AD06 AD06A	V _{REF}	Reference Voltage ⁽³⁾	2.2 2.5	—	— V _{DD}	V	Absolute minimum to ensure 1 Lsb accuracy
AD07	V _{AIN}	Full-Scale Range	V _{SS}	—	V _{REF}	V	
AD08	Z _{AIN}	Recommended Impedance of Analog Voltage Source	—	—	10	k Ω	
AD09*	I _{REF}	V _{REF} Input Current ⁽³⁾	10	—	1000	μA	During V _{AIN} acquisition. Based on differential of V _{HOLD} to V _{AIN} .
			—	—	50	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

- 2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
- 3: ADC V_{REF} is from external V_{REF} or V_{DD} pin, whichever is selected as reference input.
- 4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

TABLE 15-13: PIC16F616/16HV616 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
AD130*	TAD	A/D Clock Period	1.6	—	9.0	μs	Tosc-based, VREF $\geq 3.0\text{V}$
		A/D Internal RC Oscillator Period	3.0	—	9.0	μs	Tosc-based, VREF full range ADCS<1:0> = 11 (ADRC mode)
AD131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	—	11	—	TAD	Set GO/DONE bit to new data in A/D Result register
AD132*	TACQ	Acquisition Time	—	11.5	—	μs	—
AD133*	TAMP	Amplifier Settling Time	—	—	5	μs	—
AD134	TGO	Q4 to A/D Clock Start	—	Tosc/2	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
				—	Tosc/2 + TCY	—	

* These parameters are characterized but not tested.

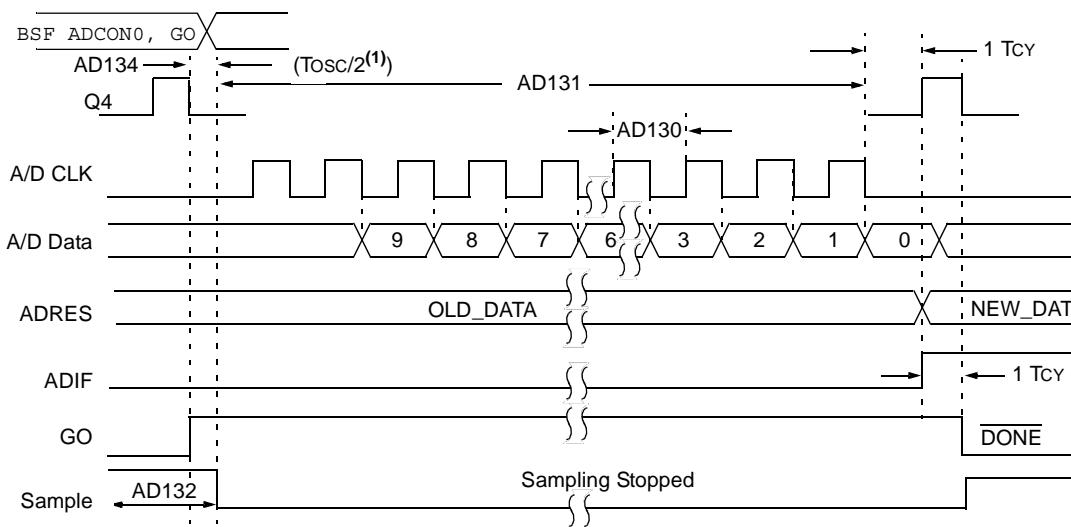
† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See **Section 9.3 “A/D Acquisition Requirements”** for minimum conditions.

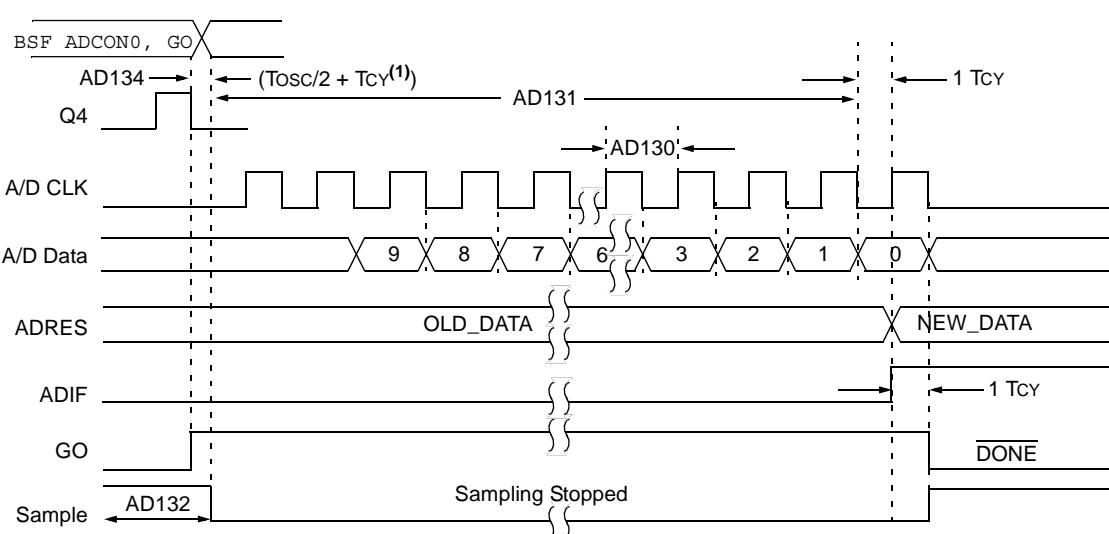
PIC16F616/16HV616

FIGURE 15-9: PIC16F616/16HV616 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

FIGURE 15-10: PIC16F616/16HV616 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs are not available at this time.

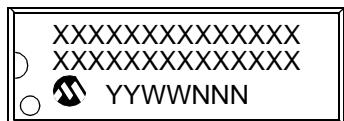
PIC16F616/16HV616

NOTES:

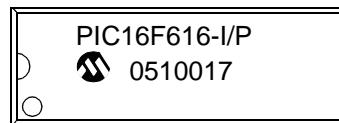
17.0 PACKAGING INFORMATION

17.1 Package Marking Information

14-Lead PDIP



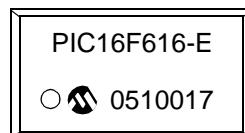
Example



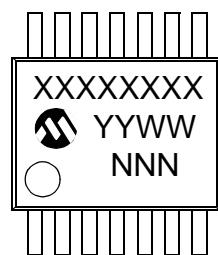
14-Lead SOIC (.150")



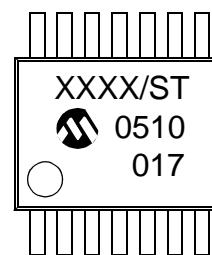
Example



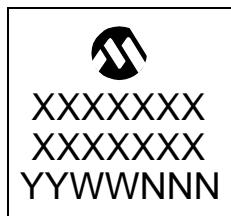
14-Lead TSSOP



Example



16-Lead QFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*		This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

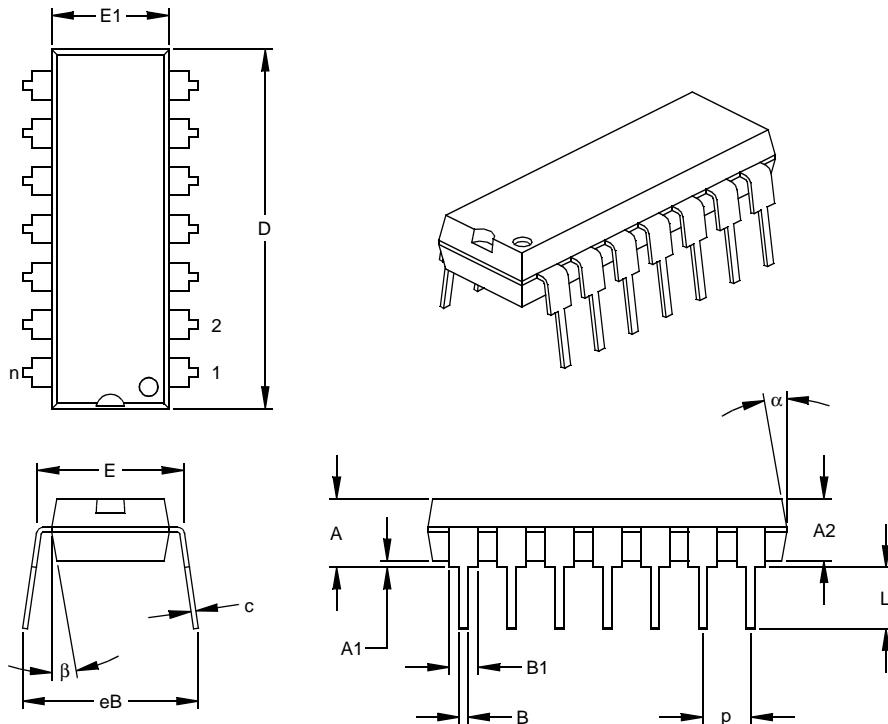
- * Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC16F616/16HV616

17.2 Package Details

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	alpha	5	10	15	5	10	15
Mold Draft Angle Bottom	beta	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

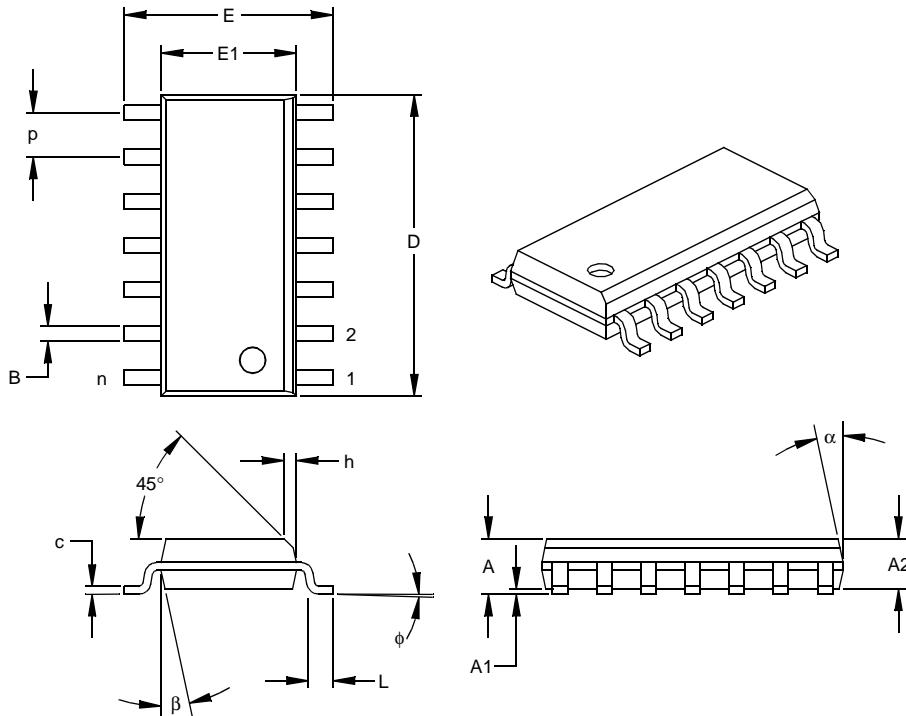
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil Body (SOIC)



Dimension Limits	INCHES*			MILLIMETERS			
	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n	14			14		
Pitch	p	.050			1.27		
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff	§ A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	phi	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	alpha	0	12	15	0	12	15
Mold Draft Angle Bottom	beta	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

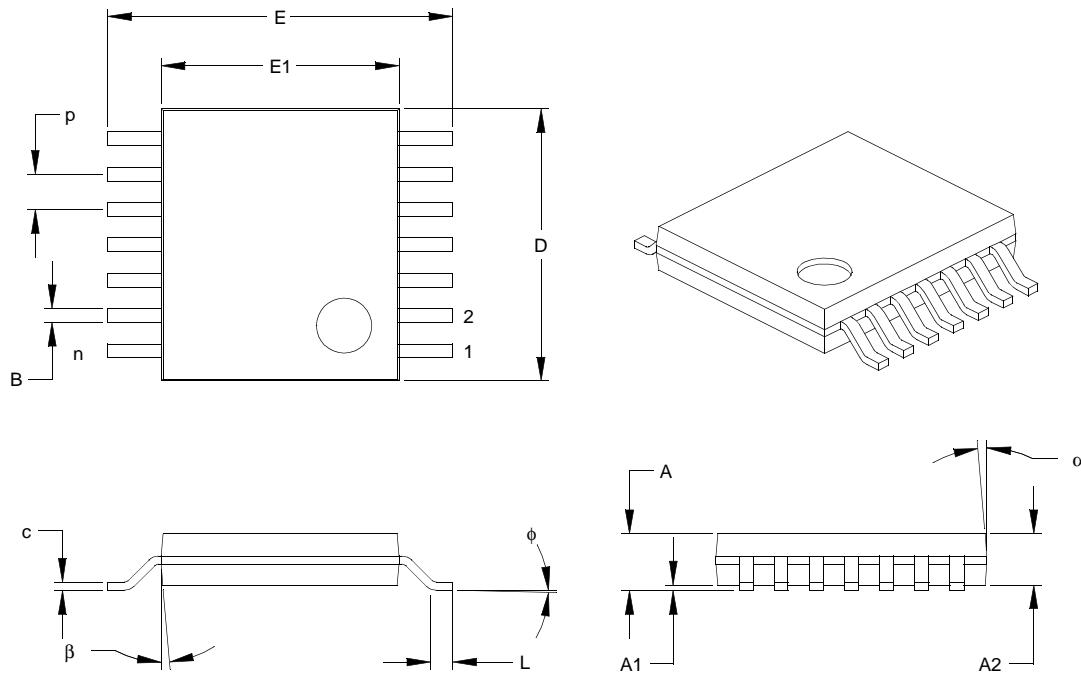
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

PIC16F616/16HV616

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p	.026	BSC		0.65	BSC	
Overall Height	A	.039	.041	.043	1.00	1.05	1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	phi	0°	4°	8°	0°	4°	8°
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	alpha	12° REF			12° REF		
Mold Draft Angle Bottom	beta	12° REF			12° REF		

* Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

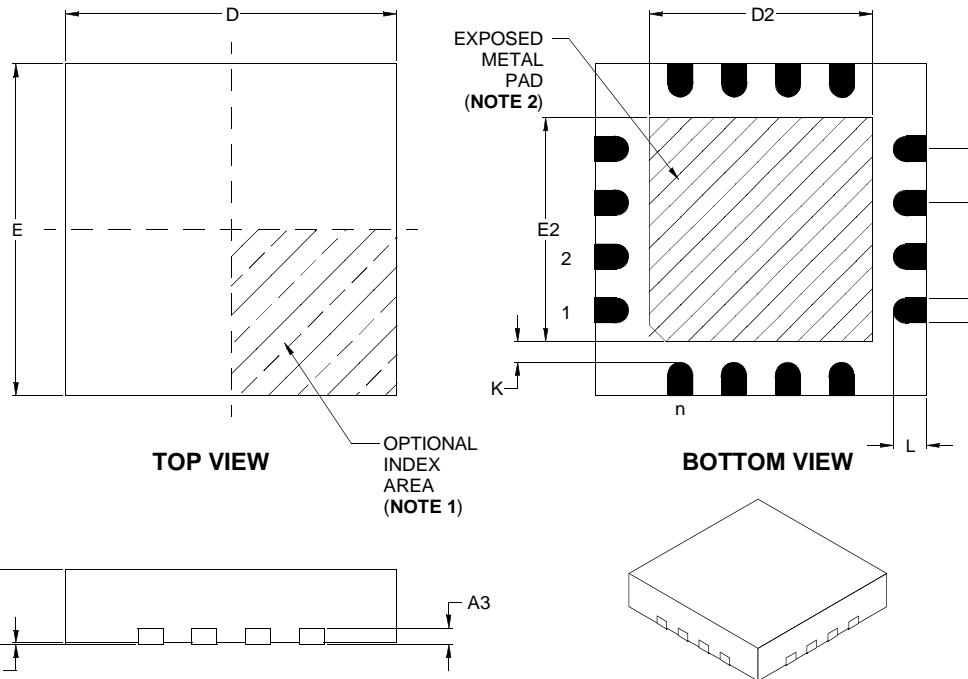
JEDEC Equivalent: MO-153 AB-1

Drawing No. C04-087

Revised: 08-17-05

PIC16F616/16HV616

16-Lead Plastic Quad Flat No Lead Package (ML) 4x4x0.9 mm Body (QFN) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	e		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008 REF			0.20 REF	
Overall Width	E	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Width	E2	.090**	–	.110	2.29**	–	2.80
Overall Length	D	.152	.157	.163	3.85	4.00	4.15
Exposed Pad Length	D2	.090	–	.110	2.29	–	2.80
Contact Width	b	.010	.012	.014	0.25	0.30	0.35
Contact Length §	L	.012	.016	.020	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	.008	–	–	0.20	–	–

* Controlling Parameter

** Outside JEDEC Specification

§ Significant Characteristic

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Exposed pad varies according to die attach paddle size.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

JEDEC equivalent: M0-220 VGGC-3

Drawing No. C04-127

Revised 09-13-05

PIC16F616/16HV616

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

APPENDIX B: MIGRATING FROM OTHER PICmicro® DEVICES

This discusses some of the issues in migrating from other PICmicro devices to the PIC16F6XX Family of devices.

B.1 PIC16F676 to PIC16F616/16HV616

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC16F616/ 16HV616
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	2048
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator	1	2
ECCP	N	Y
INTOSC Frequencies	4 MHz	8 MHz
Internal Shunt Regulator	N	Y (PIC16HV616)

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

PIC16F616/16HV616

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PART NO.	X	XX	XXX		
Device	Temperature Range	Package	Pattern		
Device:	PIC16F616/16HV616, PIC16F616/16HV616T ⁽¹⁾ VDD range 2.0V to 5.5V				
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)				
Package:	ML = Quad Flat No Leads (QFN) P = Plastic DIP SL = 14-lead Small Outline (150 mil) ST = Thin Shrink Small Outline (4.4 mm) ST = Thin Shrink Small Outline (4.4 mm)				
Pattern:	QTP, SQTP or ROM Code; Special Requirements (blank otherwise)				

Examples:

a) PIC16F616/16HV616-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301

b) PIC16F616/16HV616-I/SO = Industrial Temp., SOIC package, 20 MHz

Note 1: T = in tape and reel TSSOP and SOIC packages only.



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