Department - CSE (Second Year) Architecture

Semester - 4th

Roll No. - 37 Date - 10.03.23

Write a verilog program to design simulate and test a circuit of 3 input majority circuit.

Truth Table :-

x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

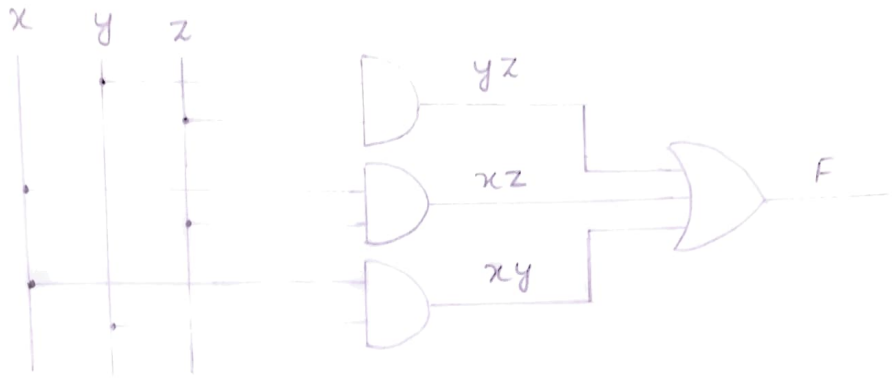
K - Map :-

x \ yz	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Expression :-

$$F = yz + xz + xy$$

Circuit Diagram :-



Code :-

1) Design Module :-

```
module maj(
  input [0:4]sw,
  output led
);
 assign led = (sw[0] & sw[1] & sw[2]) | //ABC
     (sw[0] & sw[1] & sw[3]) | //ABD
     (sw[0] & sw[1] & sw[4]) | // ABE
     (sw[0] & sw[2] & sw[3]) | // ACD
     (sw[0] & sw[2] & sw[4]) | // ACE
     (sw[0] & sw[3] & sw[4]) | // ADE
     (sw[1] & sw[2] & sw[3]) | // BCD
     (sw[1] & sw[2] & sw[4]) | // BCE
     (sw[1] & sw[3] & sw[4]) | // BDE
     (sw[2] & sw[3] & sw[4]); // CDE

endmodule
```

ii) Test Bench :-

```
module maj_testbench;
    reg [0:4] sw;
    wire led;
    maj uut (.sw(sw), .led (led));
    initial begin
        sw [0] = 1;
        sw [1] = 1;
        sw [2] = 0;
        sw [3] = 0;
        sw [4] = 0;
        # 400;
        sw [0] = 1;
        sw [1] = 1;
        sw [2] = 1;
        sw [3] = 0;
        sw [4] = 0;
        # 400;
    end
    initial begin
        $ dumpfile ("dump.vcd");
        $ dump vars ();
          end
end module
```

Majority Circuit - Output Simulation: