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prite a verilog program that includes above
module (4x1 MUX) to describe the functionality of 8-1
multiplexer circuit.
Design module: -
module mux - 4x1 (f, A, sel);
    input [3:07 A;
     input [1:0] sel;
    output f;
    wiref;
     assign f = ((nse1[0]) & (se1[i]) & A[0]) 1 ((nse1
 [0]) & sel [1] & A [1]) I (su [1] & (n sel [0]) & A [2]) I
 (Sel [0] & Sel [1] & A [3]);
 endmodule
 module mux_8(a, sel, d);
      input [7:0] a;
      input [2:0] sel;
      output d;
      wire d, temp1, temp2;
  mux - 4x1 DUTI (a[7:4], sel[1:0], temp1);
             DUT2 (a [3:0], sel [1:0], temp2);
  assign d = Sel [2]? temp 2: temp1;
   endmodule.
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jest bench:
module test;
    reg[7:0] a;
    reg [2:0] sul;
    wouf;
     mux_4x1 DUT (.f(f), . A(a), . sel (sel));
     initial begin
     & dumpfile ("dump. vcd");
     & dumpvars (1);
     a = 8' b 10110100;
      Sel = 3 bill;
      #5;
      a = 8 'b10111111;
      SU = 3' b010;
      #5;
       a = 8'b10101010;
       Sel = 3' 6101;
       #5;
       a = 8' b 0 10 10 10 13
        Sel = 3' 6000;
  end
  endmodule.
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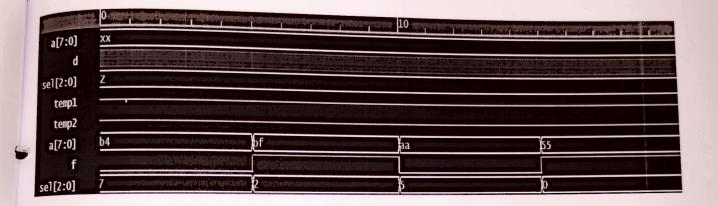
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8X1 MULTIPLEXER:



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