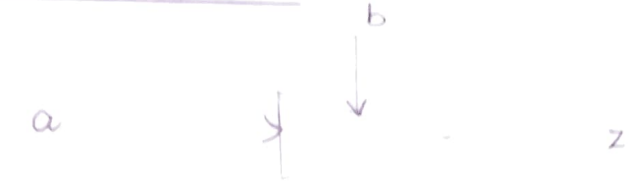
TRISTATE BUFFER :-



Theory:- A tristate buffer is a digital logic gate that allows a signal to pass through when enabled, but when disabled, it sets the output to a high-impedance state, effectively disconnecting it from the rest of the circuit. This allows multiple outputs to share the same signal line without interfering with each other.

Truth Table :-

a	b	z
0	0	z
0	1	z
1	0	0
1	1	1

Code :-

1) **Design module :-**

```
module tristate
 (input a,
  input cnt,
  output z
 );
assign z = (cnt & a) | (~cnt & bz);
  end module
```

Test Bench :-

```
module xnor2_test bench;
reg a, b;
wire z;
xnor2 uut(.a(a), .b(b), .z(z));
initial
    begin
     a=0;
     b=0;
     #100;
     a=0;
     b=1;
     #100;
     a=1;
     b=0;
     #100;
     a=1;
     b=1;
     #100;
  end
initial
    begin
     $dumpfile ("dump.vcd");
     $dumpvars ();
    end
end module
```