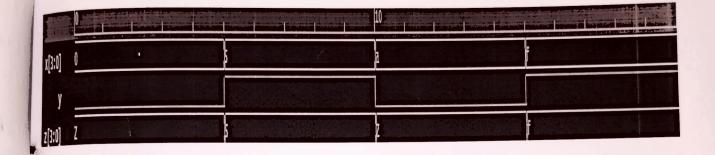
Sub Compuler Name - Hd · Quzal Jawed Architecture Lab Department - CSE (Second Year) Date - 17.03.23 Semester - 4th se ROU NO. - 37 write a verilog program to design, simulate and test a circuit of a 4-bit uniducectional bus circuit having following properties - Take 4-bit Input as I, control Input (CNT), Output is Z (4-bit) Testy benchule:module test; reg [3:0] x; regy; wire [3:0] Z; and-test DUT1( $\overline{I}(x)$ , cNT(y),  $\overline{z}(z)$ ); initial begin Design module: Adumpfile ("dump. vcd"); module and-test (I, (NT, Z); \$ dumpvars (1); x = 4'60000; input [3:0] I; y = 0; input CNT; output [3:0] z; # 5 K = 4' b01013 wire [3:0] Z; assign Z[3:0]= CNT? [3:0] y = 13 : 4'bz; #5 end module x = 4'61010; As Abit x = 0; 2[3:0] 4 6 # 5 x = 4'b11113 y = 1;

end

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## 4 BIT UNIDIRECTIONAL BUS:



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