Write a verilog program to design, simulate and test a circuit of a ternary operation.

Design module :-

```
module ternary(
  input a,
  input b,
  output cab
);
  assign cab = a>b ? a:b;
endmodule
```

Test bench :-

```
module ternary_tb;
   reg a;
   reg b;
   wire cab;
   ternary out(.a(a), .b(b), .cab(cab));
initial begin
     a = 0;
     b = 1;
     #1;
     a = 1;
     b = 0;
     #1;
end
initial begin
     $dumpfile("dump.vcd");
     $dumprars(0, ternary_tb);
end
endmodule
```

TERNARY OPERATOR: