Name - MD Quzal Jawed Sub-Computer Architecture Lab Department - CSE (Second Year) Semester- 4th Date - 03.03.23 se ROII NO. - 37 PY AND GATE :-C = A.B . When added Riviors is Touth Table: seleted time slav nor Input Output oregised in Ede. B C a Grante in defeat test black 0 0 0 0 & design: Con't Create. 0 0 0 Code is Design Module: ii) Test Bench: timescale Ins/10ps module and 2 (input A; module and 2 = tb; input B; reg A, B; wire ci Output (); and 2 wt (. A(A), . B(B), .c(c)); assign C = A & B; initial end module begin Value A = 0; Name 500 B=0 A #10; A=15 B B=0; C # 103 A=1; B=15 #10; end end module

OR GRATE :-

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C = A+B

se

er

## Touth Table :-

Inp	ut	Output
Α	B	C
0	0	0
0	- 1	1
1	0	1
1	1	1

Code

# Design Module:

module ox 2

(input A,

input B,

Output C

);

assign C = AIB;

end module

Name	Volue	ons	1500
A	1		
B	1		
С	1		

## ii) Test Bench:

timescale or 2-tb;

reg A, B;

wire C;

Or 2 UUL (.A(A), .B(B), . C(c));

initial begin

A=0;

B=0; # 10;

A = 0 5 B=1;

#105

A = 1;

3=0;

# 105

A = 1;

B=1;

# 105

end

end module

C = A DB

Touth Table :-

Int	out	Output
Α	В	С
0	0	0
0	1	1
1	0	1
. 1	1	0

Code :-

i) Design Module: -

module xorz

(input A)

input Bs

Output C

);

assign C = AB;

end module

Name	Value	ons , , 500
A	1	
В	1	
C	0	

ii) Test Bench : -

timescale Inslips

module xor2-tb;

reg A, B;

wire c's

xor2 uut (.A(A), .B(B), .c(c));

initial

begin

A = 0;

B=0;

# 103

A = 0;

B=1;

# 10;

A = 1;

B = 0;

# 10;

A = 1;

B=15

# 10;

end

endmodule

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NAND GATE :-

C = A.B

er

A - B .

0-

### Touth Table: -

,		
Inp	ut	Output
A	В	С
0	0	1
O	1	1
t	0	1
. 1	1	0

### Code :-

## i) Design module:

module nand2

(input A, input B,

Output C

);

assign C=! (ABB);

end module

Name	Value	o ns	1500
A	1		
В	1		
С	0		
	She Tu		

### ii) Test Bench :-

timescale Inslips

module nand2\_tb;

reg A,B;

wire C;

nand 2 vot (.A(A), .B(B), .c(c));

initial

begin

A = 0;

B=0;

# 10;

A = 13

B=0;

#10;

A = 0;

B=1;

# 10;

A = 1 ;

B=1;

#10;

end

end module

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NOR GATE ! -

C = A+B

se

AR

#### Touth Table:

Inpu	t	Output
A	В	С
0	0	1
0	1	0
l	0	0
1	1	0

### Code :-

# 1) Design module :

module nor2

(input A)

input B,

Output C

);

assign c = ! (AIB);

end module

Name	Value	Ons	500
A	1		
В	1		
С	0		

## ii) Test bench:

times cale inslipps

module nor2-tb;

reg A, B;

wire c;

nor2 vut (. A(A), . B(B), . c(c));

initial

begin

A=0;

B=0;

# 10;

77 .03

A = 0;

B=1;

# 10; A=1;

B=0;

# 10;

A = 1;

B=1;

#10;

end

end module

 $A \longrightarrow C = A'$ 

# Touth Table :-

Input	Output
Α	C
0	1
1	0

### Code : -

# i) Design module:-

module not 2

(input A,

Output C
);

assign C=!A;

end module

Name	Value	Ons .	500	
٨	٨			
C	0			
Ü				

### ii) Test Bench:

timescale Insliops

module not 2\_tb;

reg A;

wire C;

not 2 vut (A(A), C(C));

initial

begin

A=0;

#10;

A=1;

#10;

end

end module

se

SE

er

B

Touth Table :-

Inpu	ıt	Output
Α	В	Z
0	0	1
0	1	0
1	O	0
1	1	1

### Code :-

# 1) Design module :-

module nnor2 ( input as

input b;

Output Z

assign z = v (a^b);

end module

Name	Value	ð ns	500
A	1		
В	1		
C	1		

#### 11) Test Bench :-

module xnor2-testbench;

stega, b;

wire Zs

xnor2 out (·a(a),·b(b), z(z));

initial

begin

a=0;

b=0;

# 100;

a=0;

b=1;

# 100;

a=1;

b=0;

# 100;

a=1;

b=1;

# 100;

end

initial

begin

\$ dumpfile ("dump.ved");

\$ dump vares ();

end end module

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