Department - CSE (Second Year) Architecture Lab

Semester - 4th

Roll No. - 37 Date - 24.03.23

Write a verilog program that implements multiplexer module (4x1 MUX).

Design module :-

```
module mul4t1(
    input a,
    input b,
    input c,
    input d,
    input s0,
    input s1,
    output mul
);
    assign mul = ((ns0 & ns1) &a) | ((ns0 & s1) &b) | ((s0 & ns1)
                                                &c) | ((s0 & s1) &d);

endmodule.
```

Test bench :-

```
module mul4t1_tb;
    reg a;
    reg b;
    reg c;
    reg d;
    reg s0;
    reg s1;
    wire mul;
```

```
mul4tl uut(.a(a), .b(b), .c(c), .d(d), .s0(s0), .s1
                                    (s1), .mul(mul));

initial begin
    s0 = 0;
    s1 = 0;
    a = 0;
    b = 1;
    c = 0;
    d = 1;
    #1;
    s0 = 0;
    s1 = 1;
    a = 0,
    b = 1;
    c = 0;
    d = 1;
    #1;
    s0 = 1;
    s1 = 0;
    a = 0;
    b = 1;
    c = 0;
    d = 1;
    #1;
    s0 = 1;
    s1 = 1;
    a = 0;
    b = 1;
    c = 0;
    d = 1;
    #1;
end
initial begin
```

```
        $dumpfile ("dump.vcd");
    $dumpvars (0, mul4t1_tb);
end
endmodule.
```

4X1 MULTIPLEXER: