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Department - CSE (Second Year)
                                       Architecture Lab
semester - 4th
                                  Date - 24.03.23
ROU NO. - 37
write a verillog program that implements
multiplexer module (4x1 MUX).
Design module:-
module mul4t1(
   input a,
    input b.
   input Co
   input do
   înput 30,
   input SI,
   output mui
 );
   assign mul = ((ns0 & ns1) &a) ((ns0 & s1) &b) 1 ((s0 & ns1)
                                    &c)1((so & S1) &d);
 endmodule.
  Test bench!
  module mul4t1-tb;
     reg as
```

regbi

reg Co

regdi

reg so;

regs1;

wire mul;

```
mul4t1 vut (·a (a), ·b (b), ·c (c), ·d (d), ·so (so), ·sı
                                    (SI), · mul (mul));
initial begin
    50 = 03
    s1 = 0;
    a = 0;
     b = 13
     C=0;
     d=13
     #15
     50 = 03
     51= 1;
     a = 0,
      b = 1;
      C = 0;
      d= 13
      #13
       50=13
       S1 = 0 3
       a= 0 ;
       b= 13
       c = 0 ; d = 1 ;
       #15
       50=13
       SI = 1;
       a = 0 ;
       b = 15
        C = 0 ;
        d=13
        #1;
   end
```

initial begin

E

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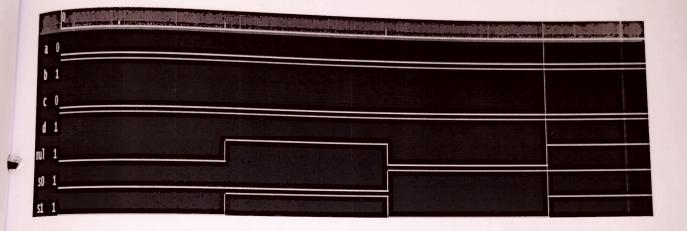
\$ dumpfile ("dump. vcd"); \$ dumpvars (0, mu14H-Hb); end endmodule.

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## 4X1 MULTIPLEXER:



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