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Write a Verilog program to design, simulate and test a circuit of a 4-bit unidirectional bus circuit having following properties - Take 4-bit Input as I, control Input (CNT), Output is Z (4-bit)

Test bench :-

```
module test;
  reg [3:0] x;
  reg y;
  wire [3:0] z;
  and_test DUT1(.I(x), .CNT(y), .z(z));
  initial begin
  $dumpfile("dump.vcd");
  $dumpvars(1);
  x = 4'b0000;
  y = 0;
  #5
   x = 4'b0101;
   y = 1;
   #5
   x = 4'b1010;
   y = 0;
   #5
   x = 4'b1111;
   y = 1;
   end
```

Design module :-

```
module and_test(I, CNT, Z);
  input [3:0] I;
  input CNT;
  output [3:0] z;
  wire [3:0] z;
  assign z[3:0] = CNT ? I[3:0]
                  : 4'bz;
end module
```

As 4-bit z[3:0] 4'b

4 BIT UNIDIRECTIONAL BUS: