dumpvars (0, comp-2 testbench);

end.

3) Statement: Write a verilog program to design stimulate and test a combinatorial circuit 3-bit input as A2A1A0 and 3-bit output as B2B1B0. When the binary input is 0, 1, 2, C the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, binary output is one less than the input.

->

a_0	a_1	a_2		c_0	c_1	c_2
0	0	0		0	0	1
0	0	1		0	1	0
0	1	0		0	1	1
0	1	1		1	0	0
1	0	0		0	1	1
1	0	1		1	0	0
1	1	0		1	0	1
1	1	1		1	1	0

K map:-

C_0 =

	$\bar{a}_1\bar{a}_2$	$\bar{a}_1 a_2$	$a_1 a_2$	$a_1\bar{a}_2$
$\bar{a}_0$	0	1	1 (3)	2
a_0	4	1 (5)	1 (6)	1 (7)

$C_0 = a_0 a_2 + a_1 a_2 + a_0 a_1$

C_1 =

	$\bar{a}_1\bar{a}_2$	$\bar{a}_1 a_2$	$a_1 a_2$	$a_1\bar{a}_2$
$\bar{a}_0$	0	1	3	2
a_0	4	5	7	6

$\bar{a}_0\bar{a}_1 a_2 + \bar{a}_0 a_1\bar{a}_2 + a_0 a_1 a_2 + a_0\bar{a}_1\bar{a}_2$

$a_2(\bar{a}_0\bar{a}_1 + a_0 a_1) + \bar{a}_2(a_0\bar{a}_1 + a_0 a_1)$

$= a_2\overline{(a_0 \oplus a_1)} + \bar{a}_2(a_0 \oplus a_1)$

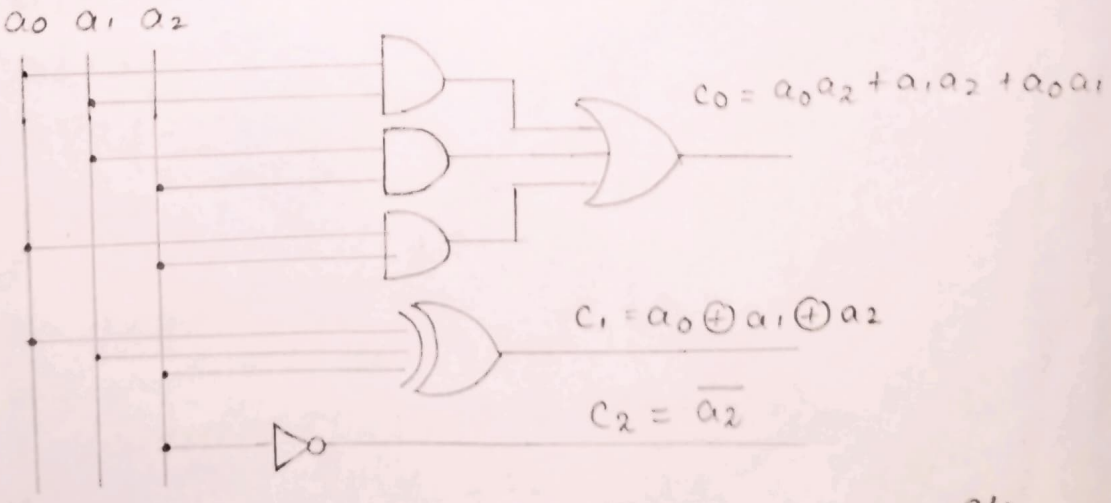
$= a_0 \oplus a_1 \oplus a_2$

C_2 =

	$\bar{a}_1\bar{a}_2$	$\bar{a}_1 a_2$	$a_1 a_2$	$a_1\bar{a}_2$
$\bar{a}_0$	1 0	1	3	1 2
a_0	1 4	5	7	1 6

$= \bar{a}_2$

Circuit Diagram:-



i) Design module :-

```
module boomin(
    input [0:2]a,
    output [0:2]o
);
    assign o[0] = (a[0] & a[1]) | (a[0] & a[2]) | (a[1] & a[2]);
    assign o[1] = a[0] ^ a[1] ^ a[2];
    assign o[2] = ~a[2];
endmodule.
```

ii) Test Bench :-

```
module comp2_testbench;
    reg [0:2] a;
    wire [0:2] o;
    boomin out (.a(a), .o(o));
    initial begin
        a[0] = 1;
        a[1] = 1;
        a[2] = 0;
        # 400;
        a[0] = 0;
        a[1] = 1;
        a[2] = 1;
        # 400
    end
    initial begin
        $ dumpfile ("dump.vcd");
        $ dumpvars (0, comp2_testbench);
    end
endmodule
```

Minimization of Function 2 - Output Simulation: