Write a verilog program that includes above module (4x1 MUX) to describe the functionality of 8-1 multiplexer circuit.

Design module:-

```
module mux_4x1 (f, A, sel);
    input [3:0] A;
    input [1:0] sel;
    output f;
    wire f;
    assign f = ((~sel[0]) & (~sel[1]) & A[0]) | ((~sel[0]) & sel[1] & A[1]) | (sel[1] & (~sel[0]) & A[2]) | (sel[0] & sel[1] & A[3]);
endmodule

module mux_8 (a, sel, d);
    input [7:0] a;
    input [2:0] sel;
    output d;
    wire d, temp1, temp2;
    mux_4x1 DUT1 (a[7:4], sel[1:0], temp1);
            DUT2 (a[3:0], sel[1:0], temp2);
    assign d = sel[2] ? temp2 : temp1;
endmodule.
```

test bench :-

```
module test;
    reg [7:0] a;
    reg [2:0] sel;
    wire f;
    mux_4x1 DUT(.f(f), .A(a), .sel(sel));
    initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
    a = 8'b10110100;
    sel = 3'b111;
    #5;
    a = 8'b10111111;
    sel = 3'b010;
    #5;
    a = 8'b10101010;
    sel = 3'b101;
    #5;
    a = 8'b01010101;
    sel = 3'b000;
end
endmodule.
```

8X1 MULTIPLEXER: