2's complement.

->i) Design module :-

```
module comp2(
    input [0:3] sw,
    output [0:3] comp
);
  assign comp = ~sw+1;
endmodule
```

ii) Test Bench :-

```
module comp2_testbench;
    reg [0:3] sw;
    wire [0:3] comp;
    comp2 uut(.sw(sw),.comp(comp));
    initial begin
        sw[0] = 1;
        sw[1] = 1;
        sw[2] = 0;
        sw[3] = 1;
        #400;
        sw[0] = 1;
        sw[1] = 1;
        sw[2] = 1;
        sw[3] = 0;
        #400;
    end
    initial begin
        $dumpfile("dump.vcd");
        $dumpvars(0, comp2_testbench);
end
```

Two's Complement - Output Simulation: