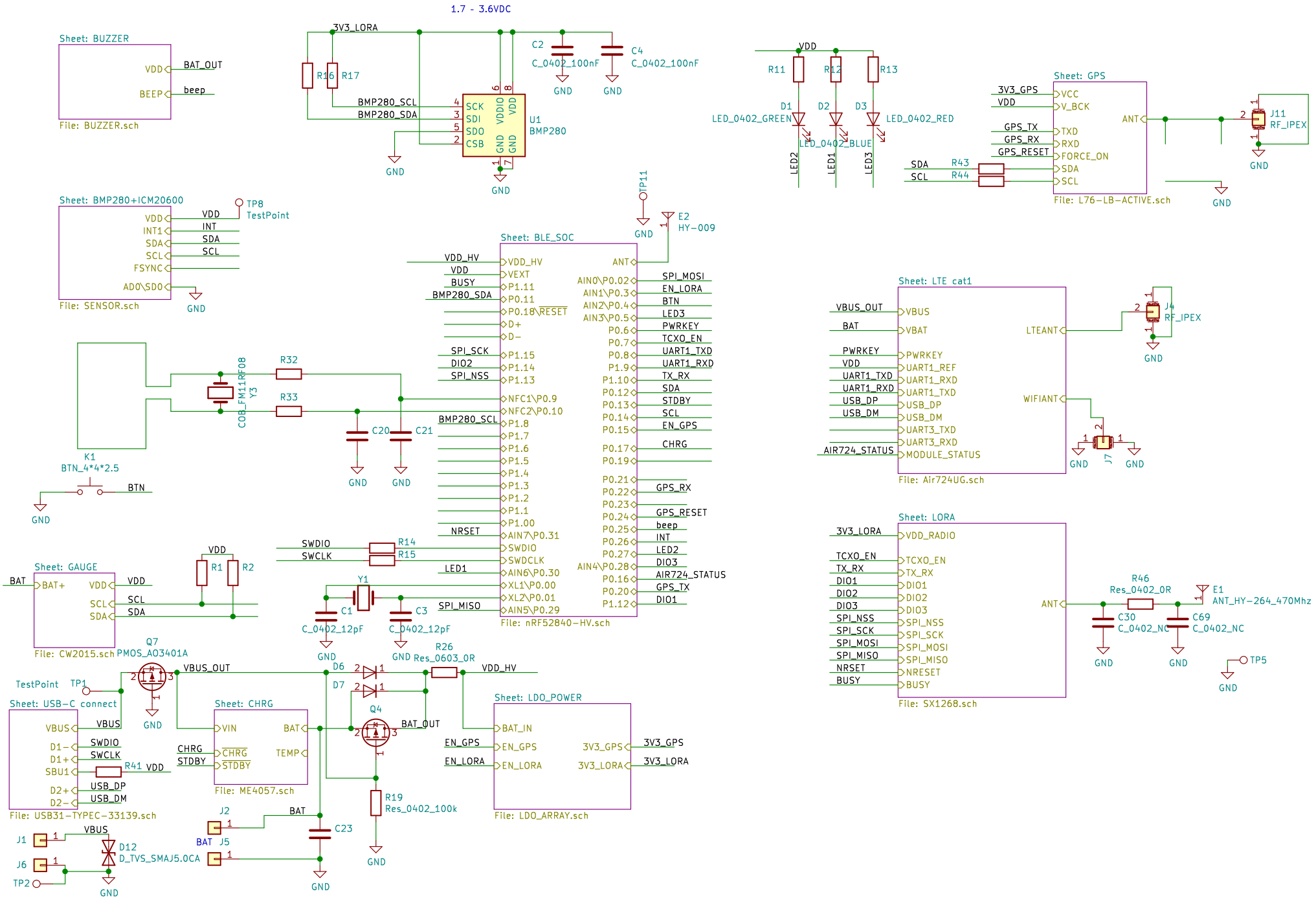

1.7 - 3.6VDC
Sheet: BUZZER
VDD
BEEP
BAT_OUT
beep
File: BUZZER.sch
3V3_LORA
R16
R17
BMP280_SCL
BMP280_SDA
SCK
SDI
SDO
CSB
VDDIO
VDD
GND
U1
BMP280
C2
C_0402_100nF
C4
C_0402_100nF
GND
VDD
R11
R12
R13
D1
D2
D3
LED_0402_GREEN
LED_0402_BLUE
LED_0402_RED
LED2
LED1
LED3
Sheet: GPS
3V3_GPS
VDD
GPS_TX
GPS_RX
GPS_RESET
SDA
SCL
VCC
V_BCK
TXD
RXD
FORCE_ON
ANT
R43
R44
J11
RF_IPEX
File: L76-LB-ACTIVE.sch
Sheet: BMP280+ICM20600
VDD
INT
SDA
SCL
FSYNC
AD0\SDO
TP8
TestPoint
File: SENSOR.sch
TP11
E2
HY-009
Sheet: BLE_SOC
VDD_HV
VDD
BUSY
BMP280_SDA
SPI_SCK
DIO2
SPI_NSS
BMP280_SCL
SWDIO
SWCLK
LED1
SPI_MISO
NRSET
VEXT
P1.11
P0.11
P0.18\RESET
D+
D-
P1.15
P1.14
P1.13
NFC1\P0.9
NFC2\P0.10
P1.8
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.00
AIN7\P0.31
SWDIO
SWDCLK
AIN6\P0.30
XL1\P0.00
XL2\P0.01
AIN5\P0.29
ANT
AIN0\P0.02
AIN1\P0.3
AIN2\P0.4
AIN3\P0.5
P0.6
P0.7
P0.8
P1.9
P1.10
P0.12
P0.13
P0.14
P0.15
P0.17
P0.19
P0.21
P0.22
P0.23
P0.24
P0.25
P0.26
P0.27
AIN4\P0.28
P0.16
P0.20
P1.12
SPI_MOSI
EN_LORA
BTN
LED3
PWRKEY
TCXO_EN
UART1_TXD
UART1_RXD
TX_RX
SDA
STDBY
SCL
EN_GPS
CHRG
GPS_RX
GPS_RESET
beep
INT
LED2
DIO3
AIR724_STATUS
GPS_TX
DIO1
File: nRF52840-HV.sch
R32
R33
Y3
COB_FM11RF08
C20
C21
K1
BTN_4*4*2.5
BTN
R14
R15
Y1
C1
C_0402_12pF
C3
C_0402_12pF
Sheet: LTE cat1
VBUS_OUT
BAT
PWRKEY
VDD
UART1_TXD
UART1_RXD
USB_DP
USB_DM
AIR724_STATUS
VBUS
VBAT
PWRKEY
UART1_REF
UART1_RXD
UART1_TXD
USB_DP
USB_DM
UART3_TXD
UART3_RXD
MODULE_STATUS
LTEANT
WIFIANT
J4
RF_IPEX
J7
File: Air724UG.sch
Sheet: GAUGE
BAT
BAT+
VDD
SCL
SDA
R1
R2
File: CW2015.sch
Q7
PMOS_AO3401A
TestPoint
TP1
Sheet: USB-C connect
VBUS
D1-
D1+
SBU1
D2+
D2-
SWDIO
SWCLK
R41
USB_DP
USB_DM
File: USB31-TYPEC-33139.sch
VBUS_OUT
D6
D7
R26
Res_0603_0R
VDD_HV
Q4
BAT_OUT
Sheet: CHRG
VIN
CHRG
STDBY
BAT
TEMP
File: ME4057.sch
Sheet: LDO_POWER
BAT_IN
EN_GPS
EN_LORA
3V3_GPS
3V3_LORA
File: LDO_ARRAY.sch
R19
Res_0402_100k
J2
J5
C23
J1
J6
TP2
D12
D_TVS_SMAJ5.0CA
Sheet: LORA
3V3_LORA
TCXO_EN
TX_RX
DIO1
DIO2
DIO3
SPI_NSS
SPI_SCK
SPI_MOSI
SPI_MISO
NRSET
BUSY
VDD_RADIO
TCXO_EN
TX_RX
DIO1
DIO2
DIO3
SPI_NSS
SPI_SCK
SPI_MOSI
SPI_MISO
NRESET
BUSY
ANT
R46
Res_0402_0R
E1
ANT_HY-264_470Mhz
C30
C_0402_NC
C69
C_0402_NC
TP5
File: SX1268.sch

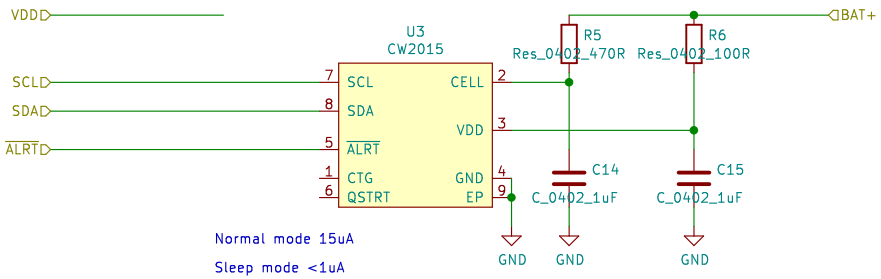
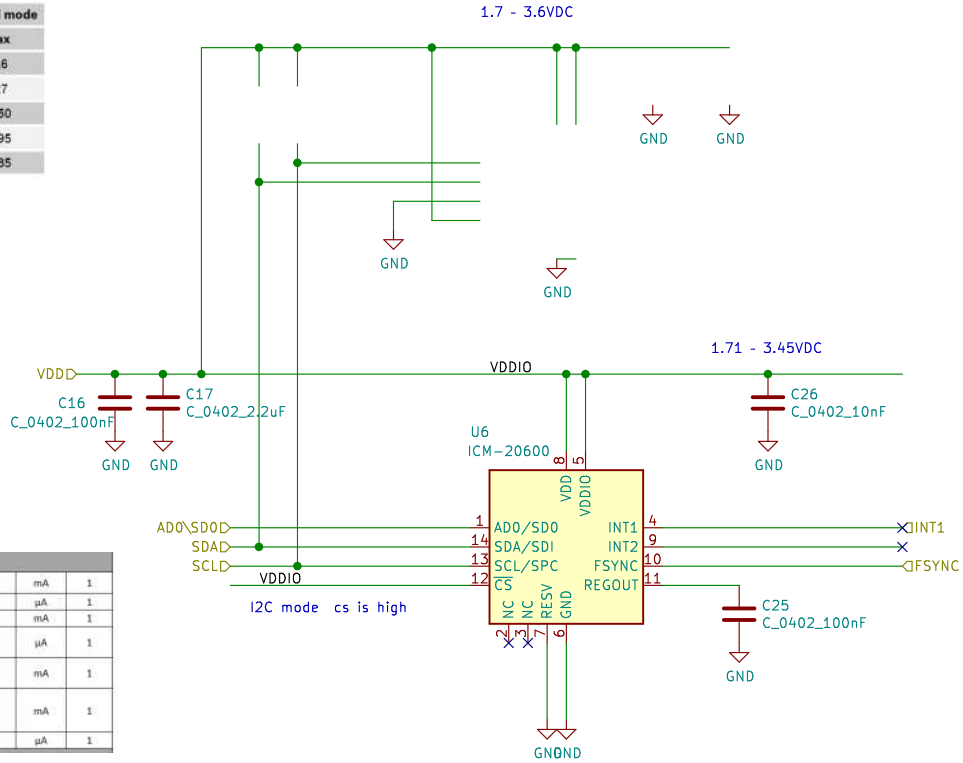

VDD
SCL
SDA
ALRT
U3
CW2015
SCL
SDA
ALRT
CTG
QSTRT
CELL
VDD
GND
EP
7
8
5
1
6
2
3
4
9
R5
Res_0402_470R
R6
Res_0402_100R
BAT+
C14
C_0402_1uF
C15
C_0402_1uF
GND
GND
GND
Normal mode 15uA
Sleep mode <1uA

Table 12: Current consumption

Oversampling setting	Pressure oversampling	Temperature oversampling	I_{DD} [µA] @ 1 Hz forced mode	
			Typ	Max
Ultra low power	×1	×1	2.74	4.16
Low power	×2	×1	4.17	6.27
Standard resolution	×4	×1	7.02	10.50
High resolution	×8	×1	12.7	18.95
Ultra high resolution	×16	×2	24.8	36.85



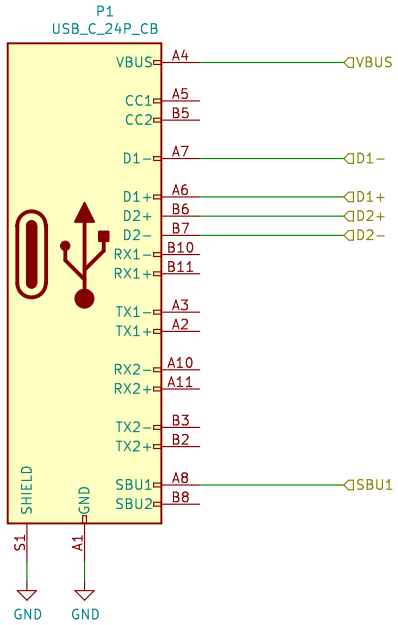
SUPPLY CURRENTS & BOOT TIME						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		2.79		mA	1
	3-Axis Accelerometer		321		µA	1
	3-Axis Gyroscope		2.55		mA	1
Accelerometer Low -Power Mode (Gyroscope disabled)	100 Hz ODR, 1x averaging		40		µA	1
Gyroscope Low-Power Mode (Accelerometer disabled)	100 Hz ODR, 1x averaging		1.08		mA	1
6-Axis Low-Power Mode (Gyroscope Low-Power Mode; Accelerometer Low-Noise Mode)	100 Hz ODR, 1x averaging		1.33		mA	1
Full-Chip Sleep Mode	At 25ºC		6		µA	1

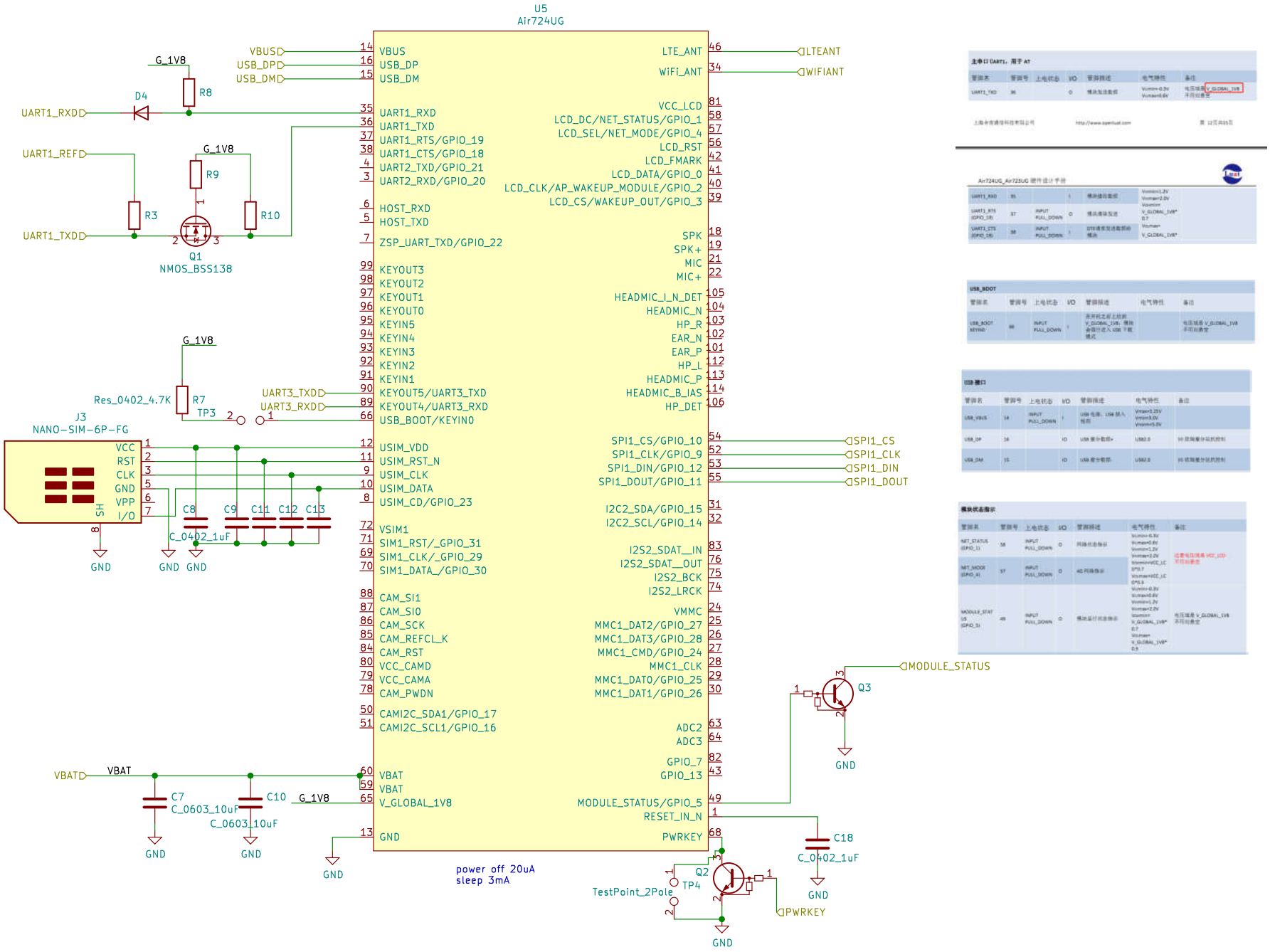
Interrupts carried on INT1 and INT2 pins are shown in the table below. If INT2 is not enabled, all interrupts are mapped to INT1.

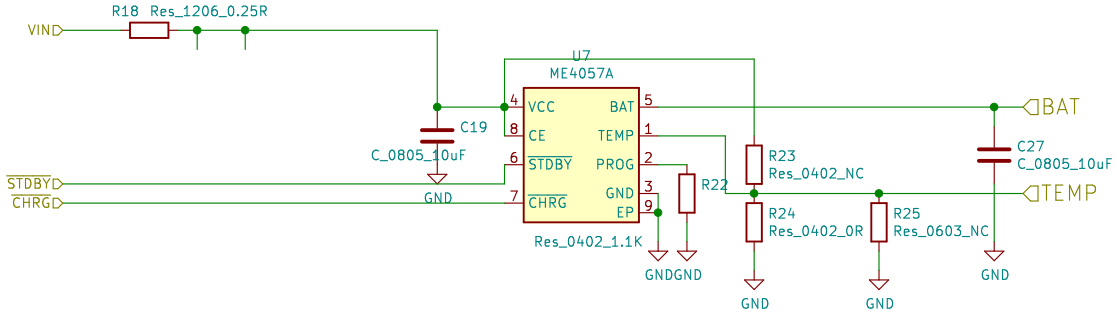
the address of one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

INTERRUPT NAME	MODULE
Motion Detection	INT2
FIFO Overflow	INT2
FIFO Watermark	INT1
Data Ready	INT1
FSYNC	INT2

Table 12. Table of Interrupt Sources


P1
USB_C_24P_CB
VBUS
A4
VBUS
CC1
A5
CC2
B5
D1−
A7
D1−
D1+
A6
D1+
D2+
B6
D2+
D2−
B7
D2−
RX1−
B10
RX1+
B11
TX1−
A3
TX1+
A2
RX2−
A10
RX2+
A11
TX2−
B3
TX2+
B2
SBU1
A8
SBU1
SBU2
B8
SHIELD
GND
S1
A1
GND
GND


U5
Air724UG
VBUS
USB_DP
USB_DM
UART1_RXD
UART1_TXD
UART2_TXD/GPIO_21
UART2_RXD/GPIO_20
HOST_RXD
HOST_TXD
ZSP_UART_TXD/GPIO_22
KEYOUT3
KEYOUT2
KEYOUT1
KEYOUT0
KEYIN5
KEYIN4
KEYIN3
KEYIN2
KEYIN1
KEYOUT5/UART3_TXD
KEYOUT4/UART3_RXD
USB_BOOT/KEYIN0
USIM_VDD
USIM_RST_N
USIM_CLK
USIM_DATA
USIM_CD/GPIO_23
VSIM1
SIM1_RST/_GPIO_31
SIM1_CLK/_GPIO_29
SIM1_DATA_/GPIO_30
CAM_SI1
CAM_SI0
CAM_SCK
CAM_REFCL_K
CAM_RST
VCC_CAMD
VCC_CAMA
CAM_PWDN
CAMI2C_SDA1/GPIO_17
CAMI2C_SCL1/GPIO_16
VBAT
VBAT
V_GLOBAL_1V8
GND
LTE_ANT
WiFi_ANT
VCC_LCD
LCD_DC/NET_STATUS/GPIO_1
LCD_SEL/NET_MODE/GPIO_4
LCD_RST
LCD_FMARK
LCD_DATA/GPIO_0
LCD_CLK/AP_WAKEUP_MODULE/GPIO_2
LCD_CS/WAKEUP_OUT/GPIO_3
SPK
SPK+
MIC
MIC+
HEADMIC_I_N_DET
HEADMIC_N
HP_R
EAR_N
EAR_P
HP_L
HEADMIC_P
HEADMIC_B_IAS
HP_DET
SPI1_CS/GPIO_10
SPI1_CLK/GPIO_9
SPI1_DIN/GPIO_12
SPI1_DOUT/GPIO_11
I2C2_SDA/GPIO_15
I2C2_SCL/GPIO_14
I2S2_SDAT__IN
I2S2_SDAT__OUT
I2S2_BCK
I2S2_LRCK
VMMC
MMC1_DAT2/GPIO_27
MMC1_DAT3/GPIO_28
MMC1_CMD/GPIO_24
MMC1_CLK
MMC1_DAT0/GPIO_25
MMC1_DAT1/GPIO_26
ADC2
ADC3
GPIO_7
GPIO_13
MODULE_STATUS/GPIO_5
RESET_IN_N
PWRKEY
power off 20uA
sleep 3mA
G_1V8
R8
D4
R9
R3
R10
Q1
NMOS_BSS138
Res_0402_4.7K
R7
TP3
J3
NANO-SIM-6P-FG
VCC
RST
CLK
GND
VPP
I/O
SH
C8
C9
C11
C12
C13
C_0402_1uF
C7
C_0603_10uF
C10
C_0603_10uF
Q3
MODULE_STATUS
C18
C_0402_1uF
Q2
TP4
TestPoint_2Pole
PWRKEY



产品型号	产品说明
ME4057ASPG	V_{FLOAT} =4.2V
ME4057DSPG	V_{FLOAT} =4.34V
ME4057ESPG	V_{FLOAT} =4.4V

脚位说明

序号	名称	功　　能
1	TEMP	**电池温度检测** TEMP外部连接一个温度检测电阻，用来监视电池温度。当TEMP脚电压低于45%或高于80%VCC电压时，意味着电池温度过低或者过高，充电停止。当外部不用温度检测功能时，可将TEMP直接接到GND.
2	PROG	**恒流电流设置和充电电流监测引脚** 充电电流可以通过外接一个电阻R_{PROG} 到地，来设置充电电流。充电电流公式： $I_{BAT} = \frac{V_{PROG}}{R_{PROG}} * 1100$
3	GND	地
4	V_{CC}	**芯片输入引脚** 提供电源给内部电路，当电源比BAT较电压低至80mV以内时，芯片内部关闭，进入睡眠模式，电池漏电流低至 2μA.
5	BAT	**电池连接引脚** 连接电池到BAT引脚，BAT 引脚充电截止电压为4.2V /4.34V.
6	$\overline{STDBY}$	**充电截止状态指示** $\overline{STDBY}$ 当检测到充电截止时，内部开关下拉。其他状态此引脚为高阻态。
7	$\overline{CHRG}$	**开漏充电状态指示** 当检测到电池正在充电时，$\overline{CHRG}$ 引脚内部开关下拉，其他状态此引脚高阻态。
8	CE	**芯片使能引脚** 引脚拉高芯片开始正常工作，引脚拉低，芯片停止工作。CE引脚可以被TTL或CMOS逻辑电路驱动。

I_{BAT}	充电电流(电流模式 V_{BAT}=3.9V)	●R_{PROG}=2.2KΩ，电流模式		450	500	550	mA
		●R_{PROG}=1.1KΩ，电流模式		950	1000	1050	mA
		●待机模式	V_{BAT}=4.2V (ME4057ASPG /ME4057BSP)	0	-2.5	-6	μA
			V_{BAT}=4.34V (ME4057DSPG)				
		R_{PROG} 悬空		-	±1	±2	μA
		睡眠模式，V_{CC}=0V		-	-1	-2	μA
I_{TRIKL}	涓流充电电流	●V_{BAT}<V_{TRIKL}, R_{PROG}=1.1KΩ		120	130	140	mA

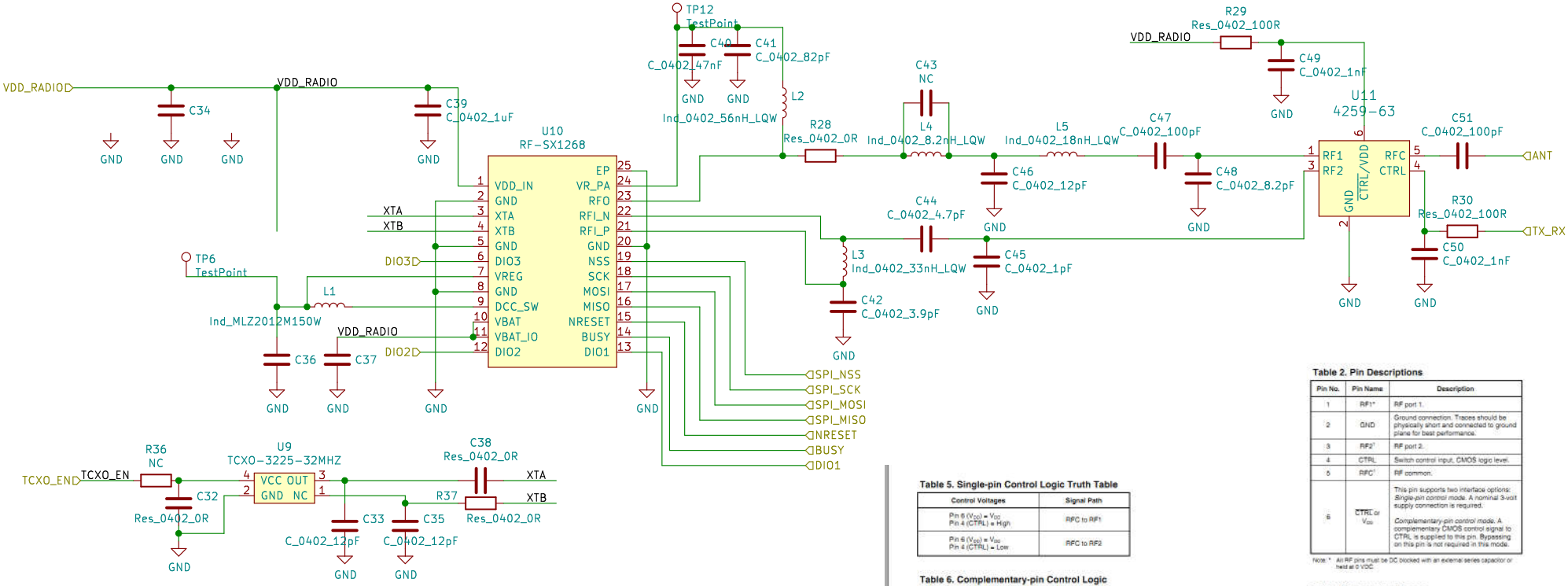


Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 ($\overline{CTRL}$ or V_{DD}) = Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 ($\overline{CTRL}$ or V_{DD}) = High Pin 4 (CTRL) = Low	RFC to RF2

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1*	RF port 1.
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2*	RF port 2.
4	CTRL	Switch control input, CMOS logic level.
5	RFC*	RF common.
6	$\overline{CTRL}$ or V_{DD}	This pin supports two interface options: *Single-pin control mode.* A nominal 3-volt supply connection is required. *Complementary-pin control mode.* A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Power supply voltage	1.8	3.0	3.3	V
I_{DD} Power supply current (V_{DD} = 3V, V_{DIO} = 3V)		8	20	µA
Control voltage high	0.7x V_{DD}			V
Control voltage low			0.3x V_{DD}	V

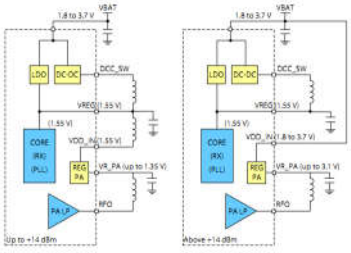


Figure 4-3: PA Supply Scheme in DC-DC Mode

4.4.3 Power Amplifier Summary

The following table summarizes the power amplifier optimization keys between both PA supply modes:

Table 4-4: Power Amplifier Summary

PA Summary	Conditions	Up to +14 dBm	Above +14 dBm
Max Power	with relevant matching and settings	+14 dBm	+22 dBm
IDDTX	at +22 dBm and 490 MHz at +10 dBm and 780 MHz	- 20 mA	107 mA -
Output Power vs VBAT		flat from VBAT = 1.8 V to 3.7 V	in DC-DC mode, flat from 3.3 V to 3.7 V VBAT = 3.1 V for +22 dBm VBAT = 2.7 V for +20 dBm VBAT = 1.8 V for +16 dBm
IDDTX vs VBAT		inversely proportional to VBAT, DC-DC buck converter is used for PA supply	-

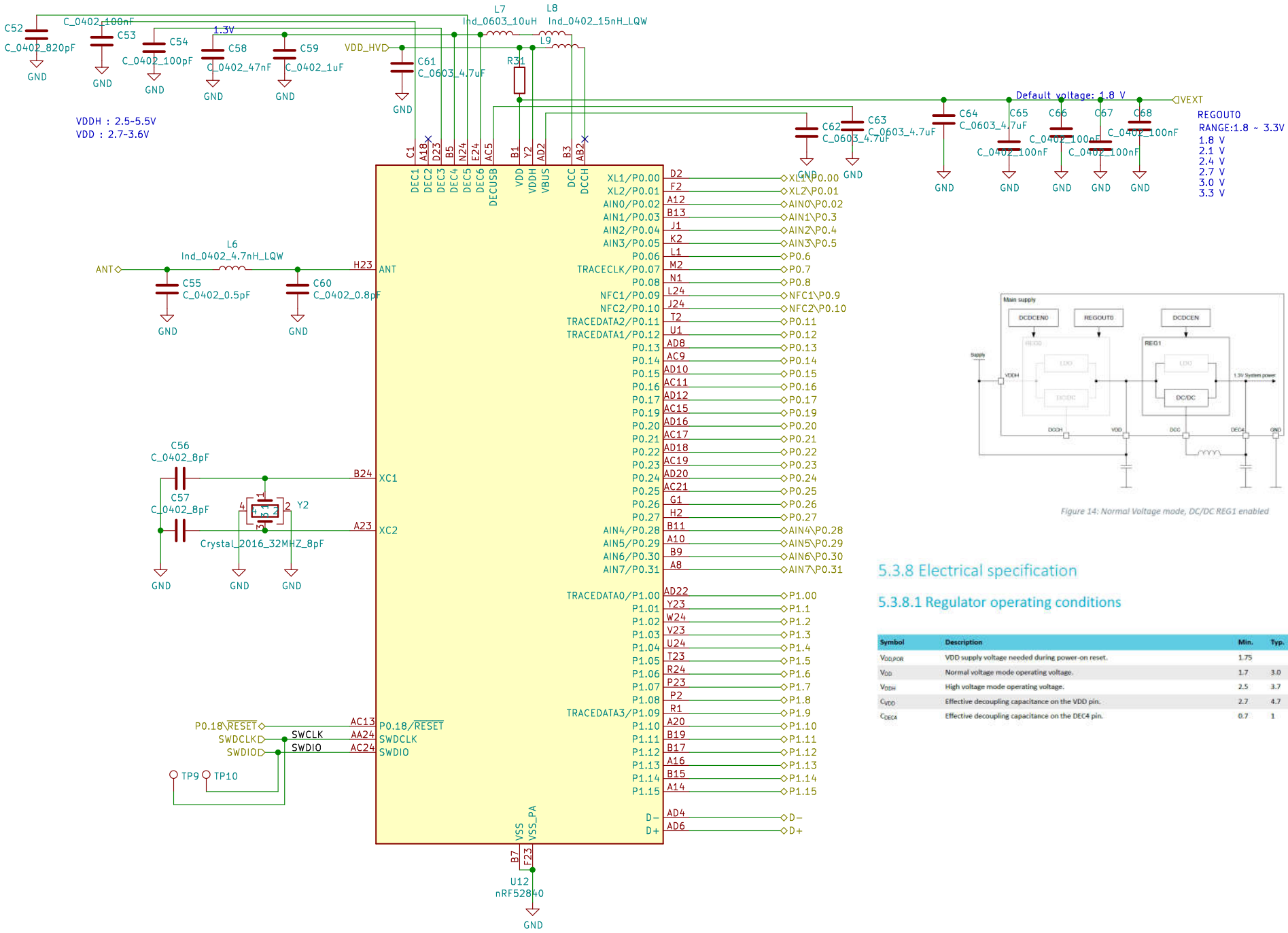
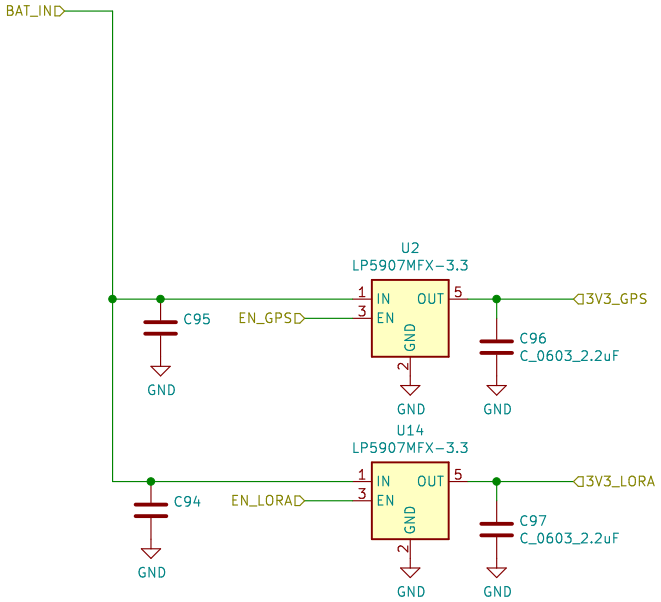


Figure 14: Normal Voltage mode, DC/DC REG1 enabled

5.3.8 Electrical specification

5.3.8.1 Regulator operating conditions

Symbol	Description	Min.	Typ.	Max.	Units
$V_{DD,POR}$	VDD supply voltage needed during power-on reset.	1.75			V
V_{DD}	Normal voltage mode operating voltage.	1.7	3.0	3.6	V
V_{DDH}	High voltage mode operating voltage.	2.5	3.7	5.5	V
C_{VDD}	Effective decoupling capacitance on the VDD pin.	2.7	4.7	5.5	µF
C_{DEC4}	Effective decoupling capacitance on the DEC4 pin.	0.7	1	1.3	µF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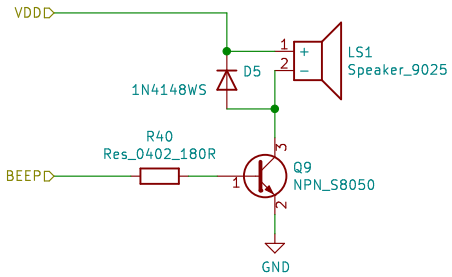
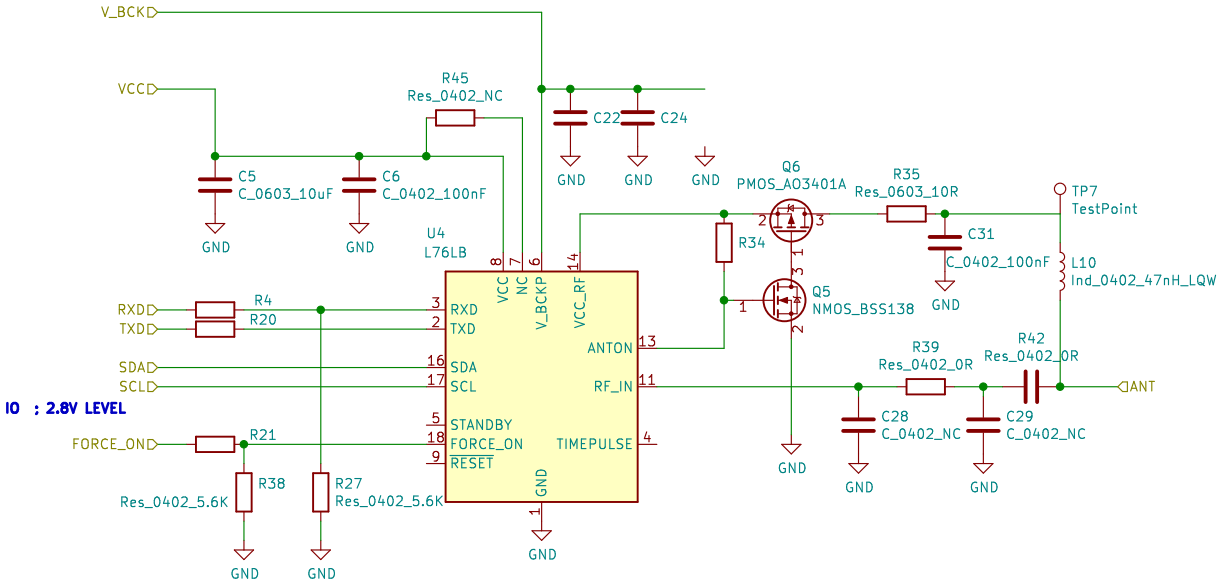
U2
LP5907MFX-3.3
1
IN
OUT
5
3
EN
GND
2
C95
EN_GPS
3V3_GPS
C96
C_0603_2.2uF
GND
GND
GND
U14
LP5907MFX-3.3
1
IN
OUT
5
3
EN
GND
2
C94
EN_LORA
3V3_LORA
C97
C_0603_2.2uF
GND
GND
GND


VDD
1
2
LS1
Speaker_9025
D5
1N4148WS
R40
Res_0402_180R
BEEP
3
Q9
NPN_S8050
1
2
GND


V_BCKD
VCCD
R45
Res_0402_NC
C22
C24
C5
C_0603_10uF
C6
C_0402_100nF
GND
U4
L76LB
VCC
NC
V_BCKP
VCC_RF
RXD
TXD
SDA
SCL
STANDBY
FORCE_ON
RESET
ANTON
RF_IN
TIMEPULSE
GND
R4
R20
R21
R38
Res_0402_5.6K
R27
Res_0402_5.6K
IO : 2.8V LEVEL
Q6
PMOS_AO3401A
R34
Q5
NMOS_BSS138
R35
Res_0603_10R
C31
C_0402_100nF
TP7
TestPoint
L10
Ind_0402_47nH_LQW
R39
Res_0402_0R
R42
Res_0402_0R
C28
C_0402_NC
C29
C_0402_NC
ANT