Contents

1. Specifications 2
1.1 Features 2
1.2 Mechanical Specifications 2
1.3 Absolute Maximum Ratings 2
1.4 DC Electrical Characteristics 3
1.5 Optical Characteristics 3
1.6 Backlight Characteristics 4
2. Module Structure 5
2.1 Counter Drawing 5
2.2 Interface Pin Description 6
2.3 Timing Characteristics 7
2.4 Display Command 9
2.4.1 Write Display Data 9
2.4.2 Read Display Data 9
2.4.3 Read-Modify-Write 10
2.4.4 The END Command 12
2.4.5 Software RESET Command 12

1. Specifications

1.1 Features

Item	Standard Value
Display Type	120 * 32 dots
LCD Type	STN, Gray, Transflective, Positive, Extended Temp
Driver Condition	LCD-Module: 1/32 Duty, 1/5Bias
Viewing Direction	12 O'clock
Backlight	YG LED B/L
Weight	26.4g
Interface	-

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	68.1(L) * 32.9(W) * 7.6(H)(Max)	mm
Viewing Area	62.0(L) * 22.5(W)	mm
Active Area	56.35(L) * 20.75(W)	mm
Dot Size	0.42(L) * 0.6(w)	mm
Dot Pitch	0.47(L) * 0.65(w)	mm

Note: For detailed information please refer to LCM drawing.

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit
Power Supply Voltage	V_{DD}	-	-0.3	7.0	V
LCD Driver Supply Voltage	V_{DD}- V_{EE}	-	-	13	V
Input Voltage	V_{IN}	-	-0.3	V_{DD} +0.3	V
Operating Temperature	T_{OP}	Excluded B/L	-20	70	°C
Storage Temperature	T_{ST}	Excluded B/L	-30	80	°C
Storage Humidity	H_D	Ta<40°C	0	90	%RH

1.4 DC Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Logic Supply Voltage	V_{DD}	-	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	-	V_{DD} -2.2	-	V_{DD}	V
"L" Input Voltage	V_{IL}	-	0	-	0.8	V
"H" Output Voltage	V_{OH}	I_{OH}=-2.0mA	V_{DD} -0.3	-	V_{DD}	V
"L" Output Voltage	V_{OL}	I_{OL}=-2.0mA	0.0	-	0.3	V
Supply Current	I_{DD}	V_{DD}=5.0V	-	73	100	mA
LCM Driver Voltage	V_{OP}	V_{DD}-V_O (-20°C)	-	-	-	V
		V_{DD}-V_O (25°C)	5.3	5.5	5.7	
		V_{DD}-V_O (70°C)	-	-	-	

1.5 Optical Characteristics

LCD Panel: 1/32 Duty, 1/5 Bias, VLCD=5.8V, Ta=25°C

Item	Symbol	Conditions	Min	Typ.	Max
View Angle	θ	C≥2.0, Ø=0°	35°	-	-
Contrast Ratio	C	θ=5°, Ø=0°	2	3	-
Response Time (rise)	tr	θ=5°, Ø=0°	-	150ms	225ms
Response Time (fall)	tf	θ=5°, Ø=0°	-	300ms	450ms

1.6 Backlight Characteristics

LCD Module with LED Backlight

Maximum Ratings

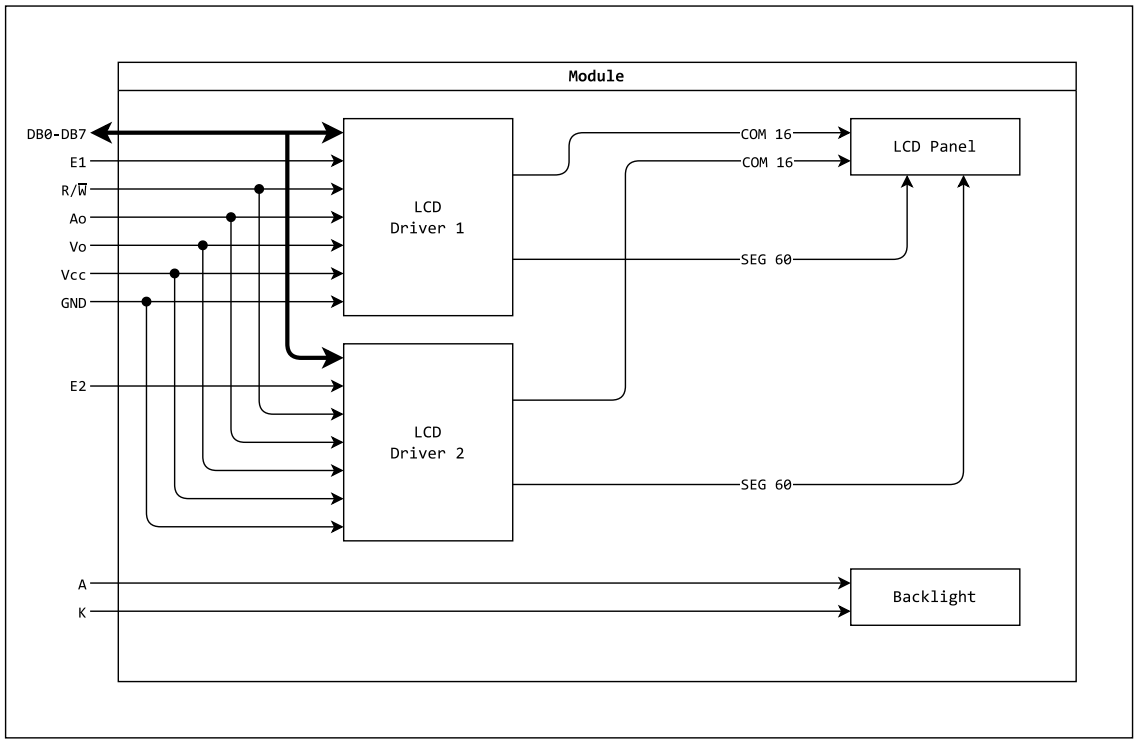
Item	Symbol	Condition	Min	Max	Unit
Forward Current	IF	Ta=25°C	-	250	mA
Reverse Voltage	VR	Ta=25°C	-	10	V
Power Dissipation	PO	Ta=25°C	-	1.15	W

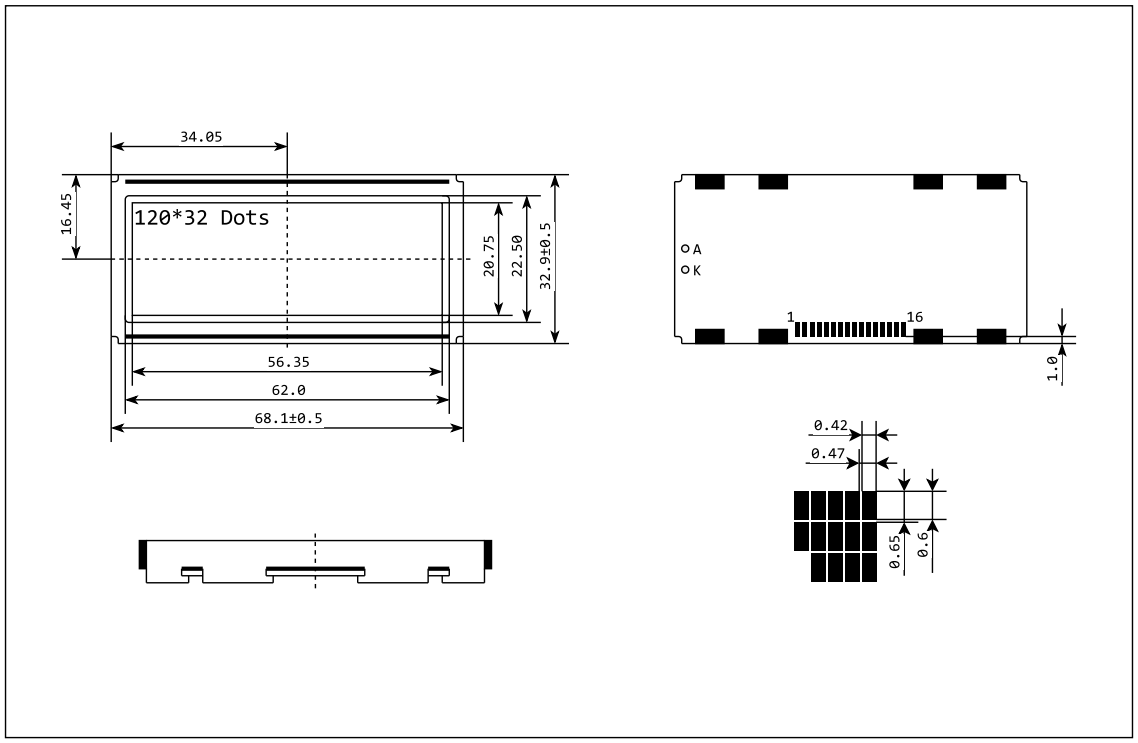
Electrical / Optical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Forward Voltage	VF	IF=100mA	-	4.2	4.6	V
Reverse Current	IR	VR=10V	-	-	0.1	mA
Average Brightness (with LCD)	IV	IF=100mA	12	17	-	cd/m^2
Wavelength	λ_p	IF=100mA	569	-	576	Nm
Luminous Intensity (without LCD)	IV	IF=100mA	24	30	-	cd/m^2
Color	Yellow-green					

2. Module Structure

2.1 Counter Drawing

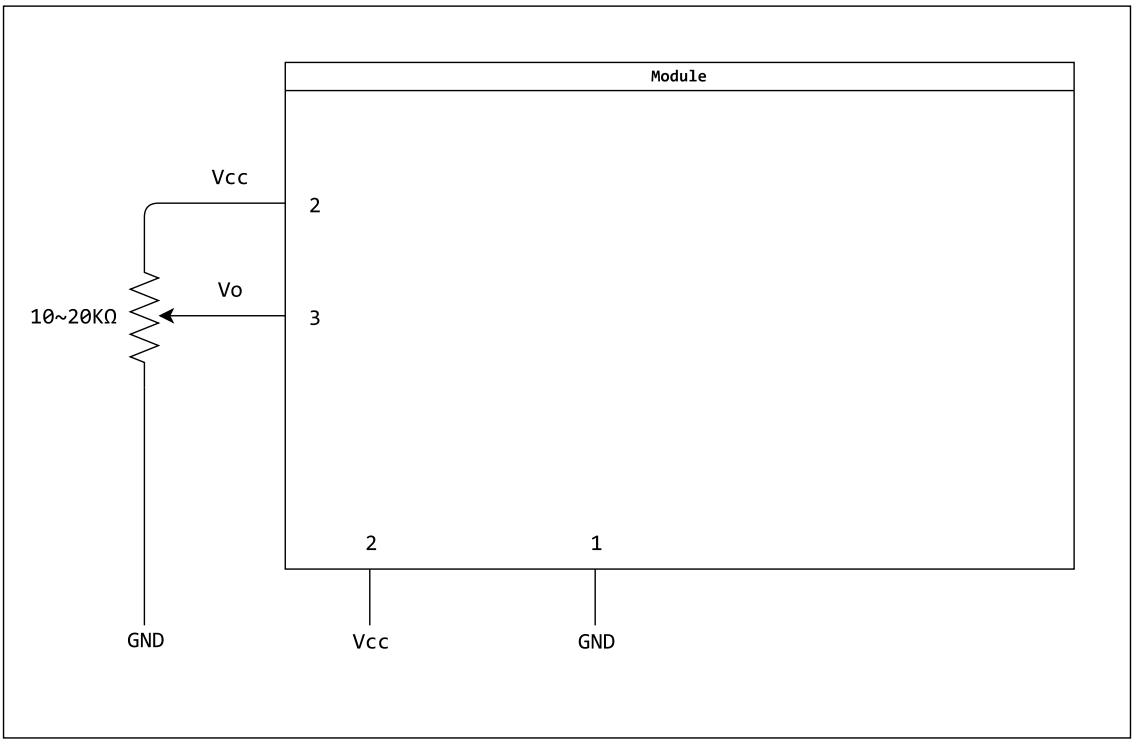




2.2 Interface Pin Description

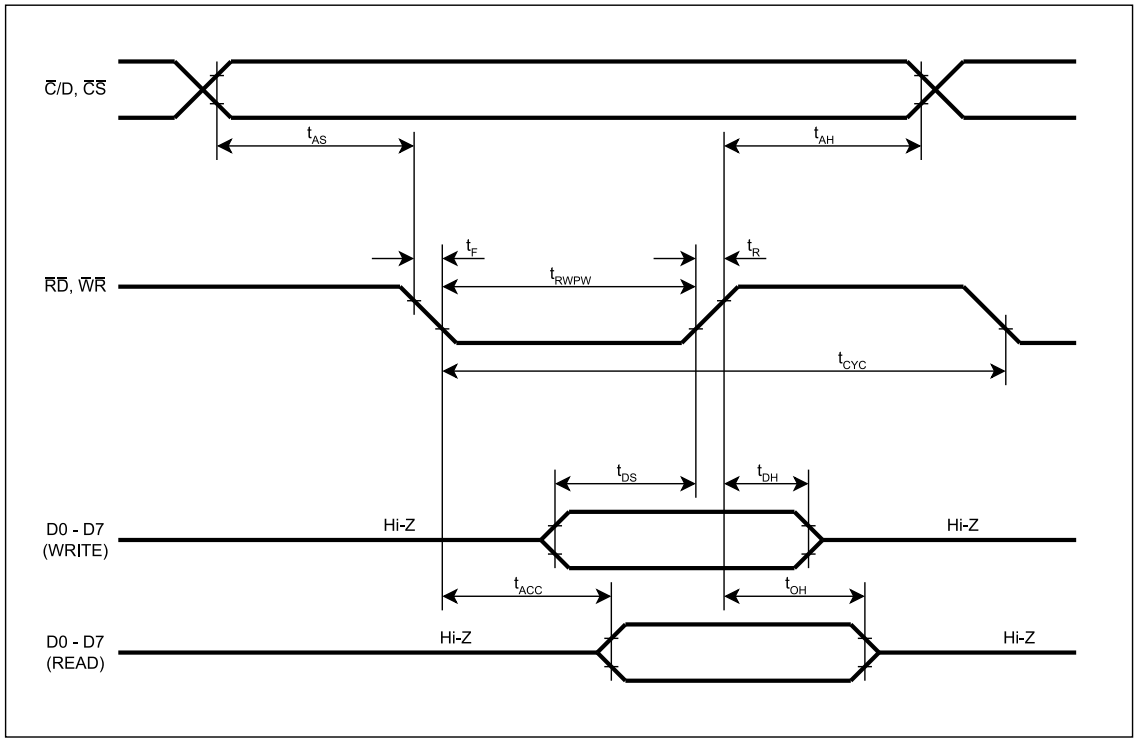
Pin No	Symbol	Function
1	GND	- Signal ground for LCM - Power supply for LED B/L(-)
2	Vcc	- Power supply for logic - Power supply for LED B/L(+)
3	Vo	Contrast adjustment
4	Ao	Register selection input High => Data register Low => Instruction register (for write) Busy flag address counter (for read)
5	R/$\overline{W}$	R/$\overline{W}$ signal input is used to select the read/write mode High => Read mode Low => Write mode
6	E1	Chip enable active “L” (segment 1 ~ 60)
7	E2	Chip enable active “L” (segment 61 ~ 120)
8	-	No connection
9-16	DB0-DB7	Data bus line

Contrast Adjustment



2.3 Timing Characteristics

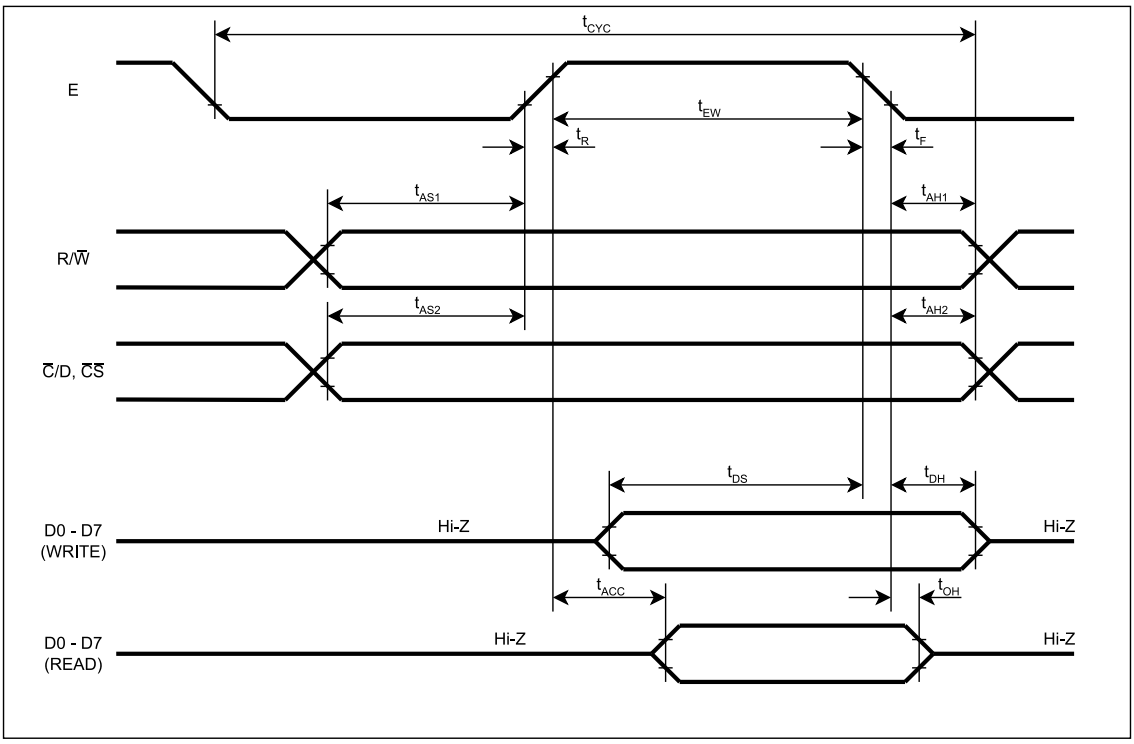
MPU Bus Read/Write I (80-family MPU)



V_{DD}=5V±10%; V_{SS}=0V; T_{amb}=-20°C to +75°C

Symbol	Parameter	Test Conditions	Min	Max	Unit
t_{AS}	Address set-up time		20	-	ns
t_{AH}	Address hold time		10	-	ns
t_F, t_R	Read/Write pulse falling/rising time		-	15	ns
t_{RWPW}	Read/Write pulse width		200	-	ns
t_{CYC}	System cycle time		1000	-	ns
t_{DS}	Data setup time		80	-	ns
t_{DH}	Data hold time		10	-	ns
t_{ACC}	Data READ access time	CL=100pF	-	90	ns
t_{OH}	Data READ output hold time		10	60	ns

MPU Bus Read/Write II (68-family MPU)



V_{DD}=5V±10%; V_{SS}=0V; T_{amb}=-20°C to +75°C

Symbol	Parameter	Test Conditions	Min	Max	Unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$		20	-	ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$		20	-	ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$		10	-	ns
t_{AH2}	Address hold time with respect to $\overline{C}$/D, $\overline{CS}$		10	-	ns
t_F, t_R	Enable (E) pulse falling/rising time		-	15	ns
t_{CYC}	System cycle time		1000	-	ns
t_{EWR}	Enable pulse width for READ		100	-	ns
t_{EWW}	Enable pulse width for WRITE		80	-	ns
t_{DS}	Data setup time		80	-	ns
t_{DH}	Data hold time		10	-	ns
t_{ACC}	Data access time	CL=100pF	-	90	ns
t_{OH}	Data output hold time		10	60	ns

2.4 Display Command

Command	Command Code								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
Write Display Data	Data to be written into the Display Data Memory.								Write a byte of data to the Display Data Memory.
Read Display Data	Data to read from the Display Data Memory.								Read a byte of data from the Display Data Modify.
Read-Modify-Write	1	1	1	0	0	0	0	0	Start Read-Modify-Write
END	1	1	1	0	1	1	1	0	Stop Read-Modify-Write
Software reset	1	1	1	0	0	0	1	0	Software Reset

2.4.1 Write Display Data

The Write Display Data command writes a byte (8 bits) of data to the Display Data Memory. Data is put on the data bus by the host microcontroller. The location which accepts this byte of data, is pointed to the Page Address Register and Column Address Register. At end of the command operation, the content of the Column Address Register is automatically incremented by 1.

For page address and column address of the Display Data Memory, please refer to Fig. 12.

Table 28 gives the control bus setting for this command.

The setting of the control bus for issuing Write Display Data command.

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
1	1	0

2.4.2 Read Display Data

The Read Display Data command Starts a 3-step operation

1. First, the current data of the internal 8-bitoutput latch of the Display Data Memory is read by the microcontroller, via the 8-bit data bus DEO-037,
2. Then a byte of data of the Display Data Memory is transferred to the 8-bit output latch from a location specified by the Page Address Register and the Column Address Register.
3. Finally, the content of the Column Address Register is automatically incremented by one.

Fig. 16 shows the internal 8-bit output latch located between the 8-bit I/O data bus and the Display Data Memory cell array. Because of this internal 8-bit output latch, a dummy read is needed to obtain correct data from the Display Data Memory.

For Display Data Write operation, a dummy write **is not** needed, because data can be directly written from the data bus to internal memory cells.

The setting of the control bus for issuing Read Display Data command.

C/D	E/(RD)	R/W(WR)
1	0	1

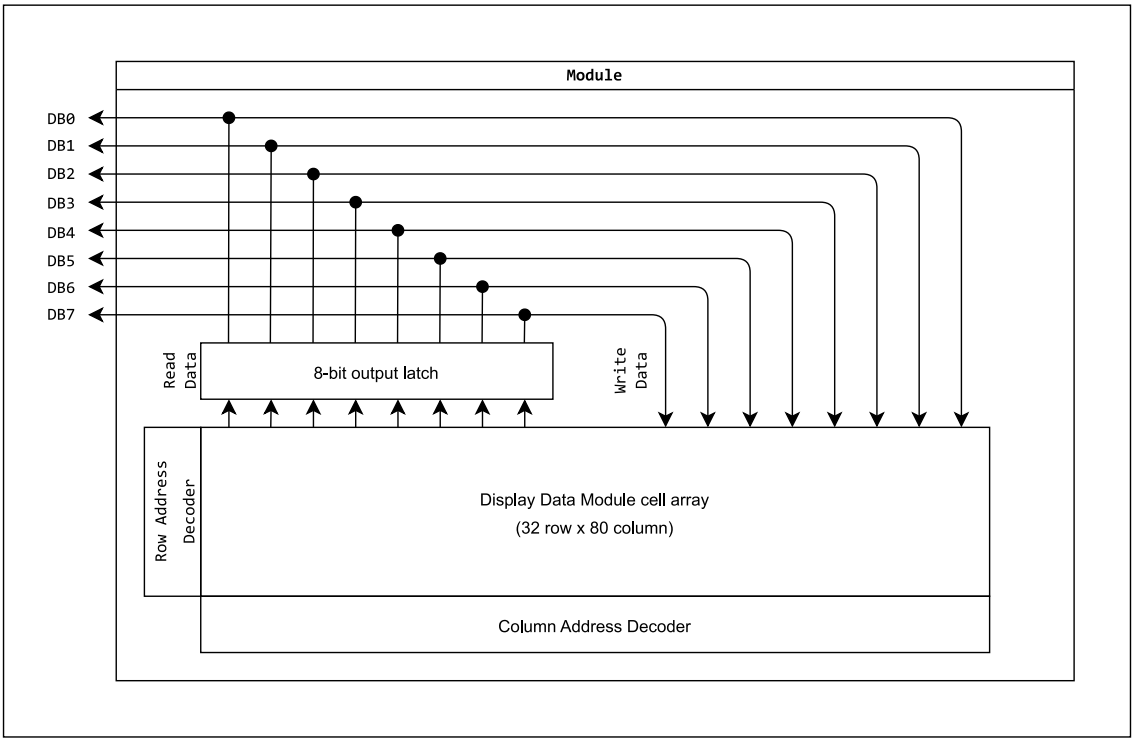


Fig. 16 Read Display Data Memory

2.4.3 Read-Modify-Write

When the Read-Modify-Write command is issued, the SBN1661G X enters into Read-Modify-Write mode.

In normal operation, when a Read Display Data command or a Write Display Data command is issued, the content of the Column Address Register is automatically incremented by one after the command operation is finished. However, during Read-Modify-Write mode, the content of the Column Address Register is not incremented by one after a Read Display Data command is finished; only the Write Display Data command can make the content of the Column Address Register automatically incremented by one after tie command operation is finished.

During Read-Modify-Write mode, any other registers, except the Column Address Register, can be modified. This command is useful when a block of the Display Data Memory needs to be repeatedly read and updated.

Fig. 17 gives the change sequence of the Column Address Register during Read-Modify-Write mode. Figure 18 gives the flow Chart for Read-Modify-Write command.

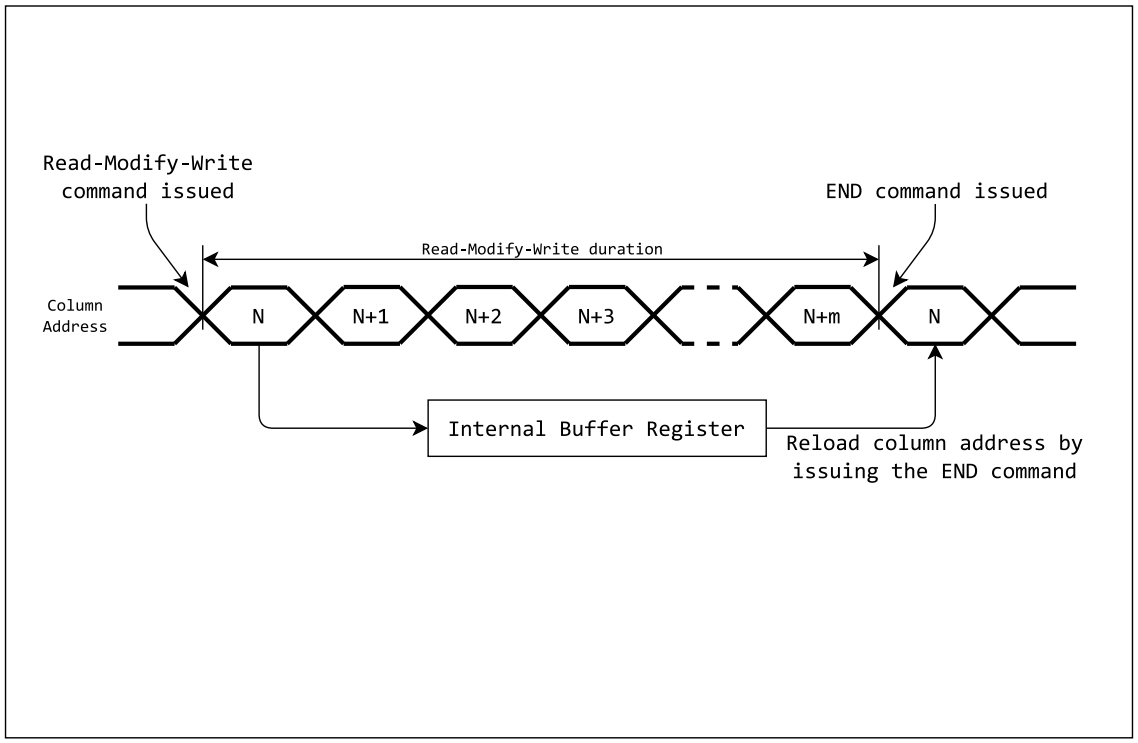


Fig. 17 Column address change during Read-Modify-Write

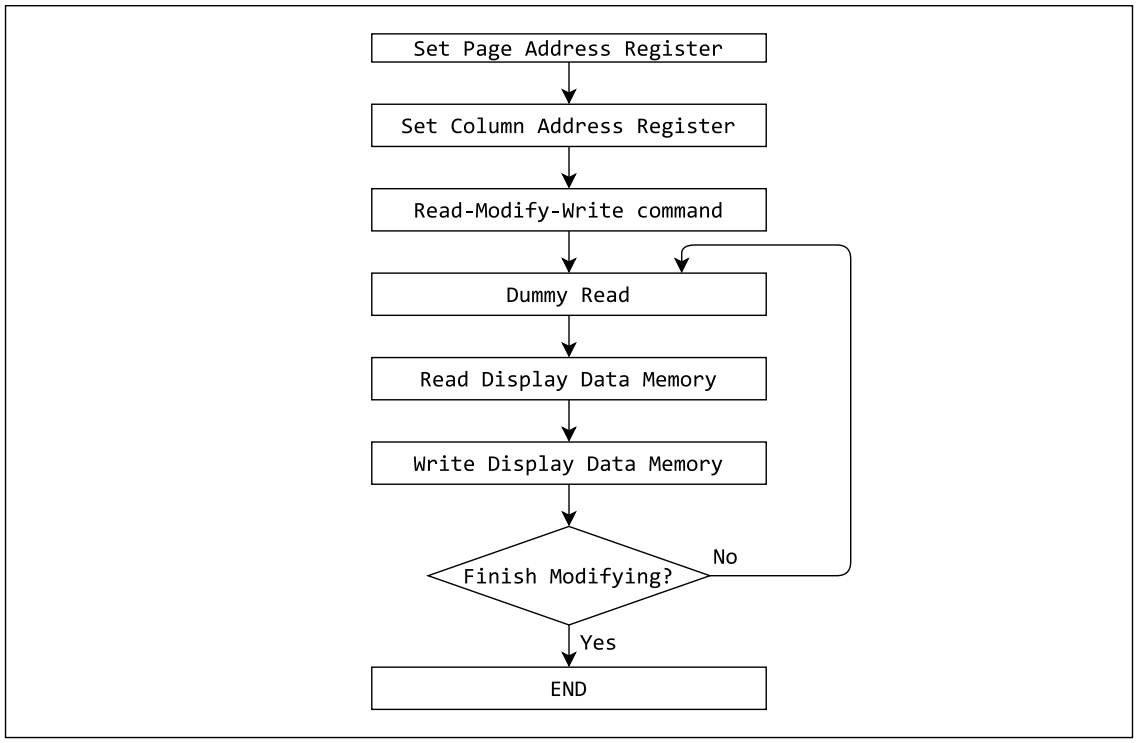


Fig. 18 The flowchart for Read-Modify-Write

The setting of the control bus for the Read-Modify-Write command.

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
1	0	1

The setting of the data bus for the Read-Modify-Write command.

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
1	1	1	0	0	0	0	0

The command code is E0 Hex.

2.4.4 The END Command

The END command releases the Read-Modify-Write mode and re-loads the Column Address Register With the value previously stored in the internal buffer (refer to Fig. 17) when the Read-Modify-Write command was issued.

Table 32 gives the setting for the control bus and the setting of the data bus is given in Table 33.

The setting of the control bus for the END command.

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for the END command.

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
1	1	1	0	1	1	1	0

The command code is EE Hex.

2.4.5 Software RESET Command

The Software Reset command is different from the hardware reset and cannot be used to replace hardware reset.

When Software Reset is issued by the host microcontroller,

- the content of the Display Start Line Register is cleared to zero (A4~A0=00000),
- the Page Address Register is set to 3 (A1 AO = 11),
- the content of the Display Data Memory remains unchanged, and
- the content of all other registers remains unchanged.

Table 34 gives the setting for the control bus and the setting of the data bus is given in table 35.

The setting of the control bus for the Software RESET command.

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for the Software RESET command.

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
1	1	1	0	0	0	1	0

The command code is E2 Hex.