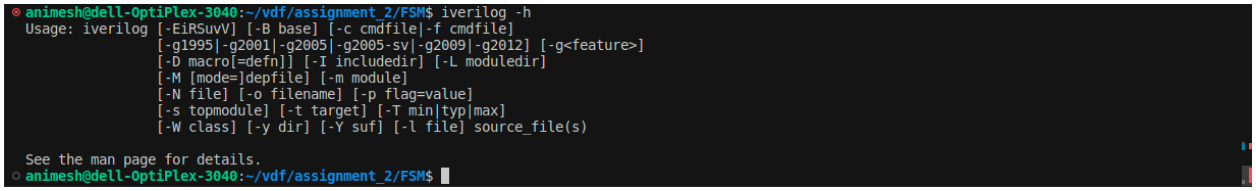
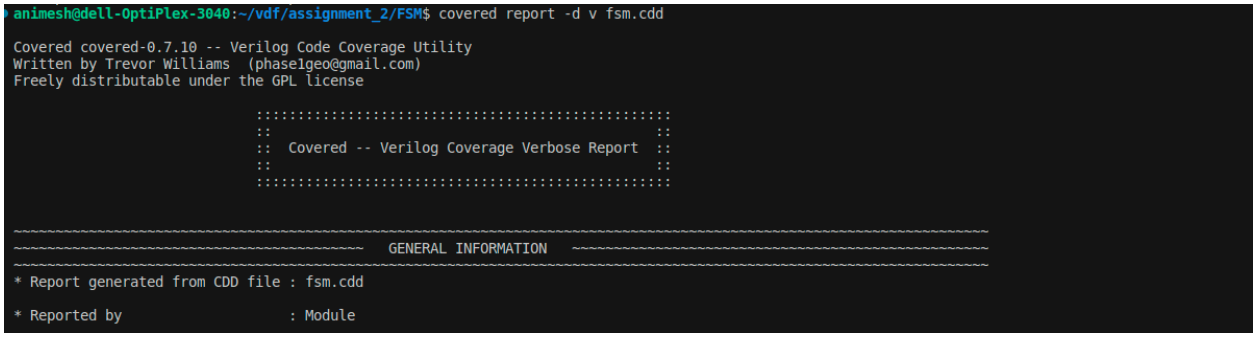
VDF Assignment-2 Report
By Animesh Pareek { BTech-ECE 2021131 }

Part-1 →

Iverilog Tool Run Screenshot >>



Covered Tool Run Screenshot >>

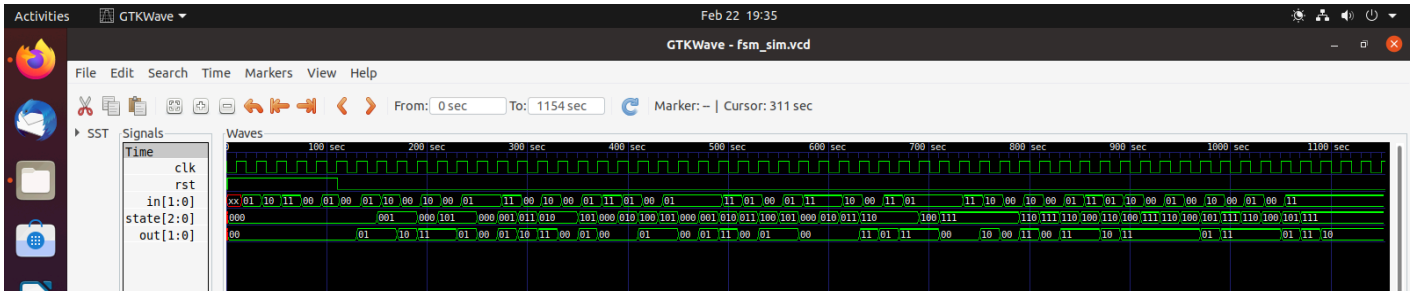


Yosys Tool Run Screenshot >>

Part-2 →

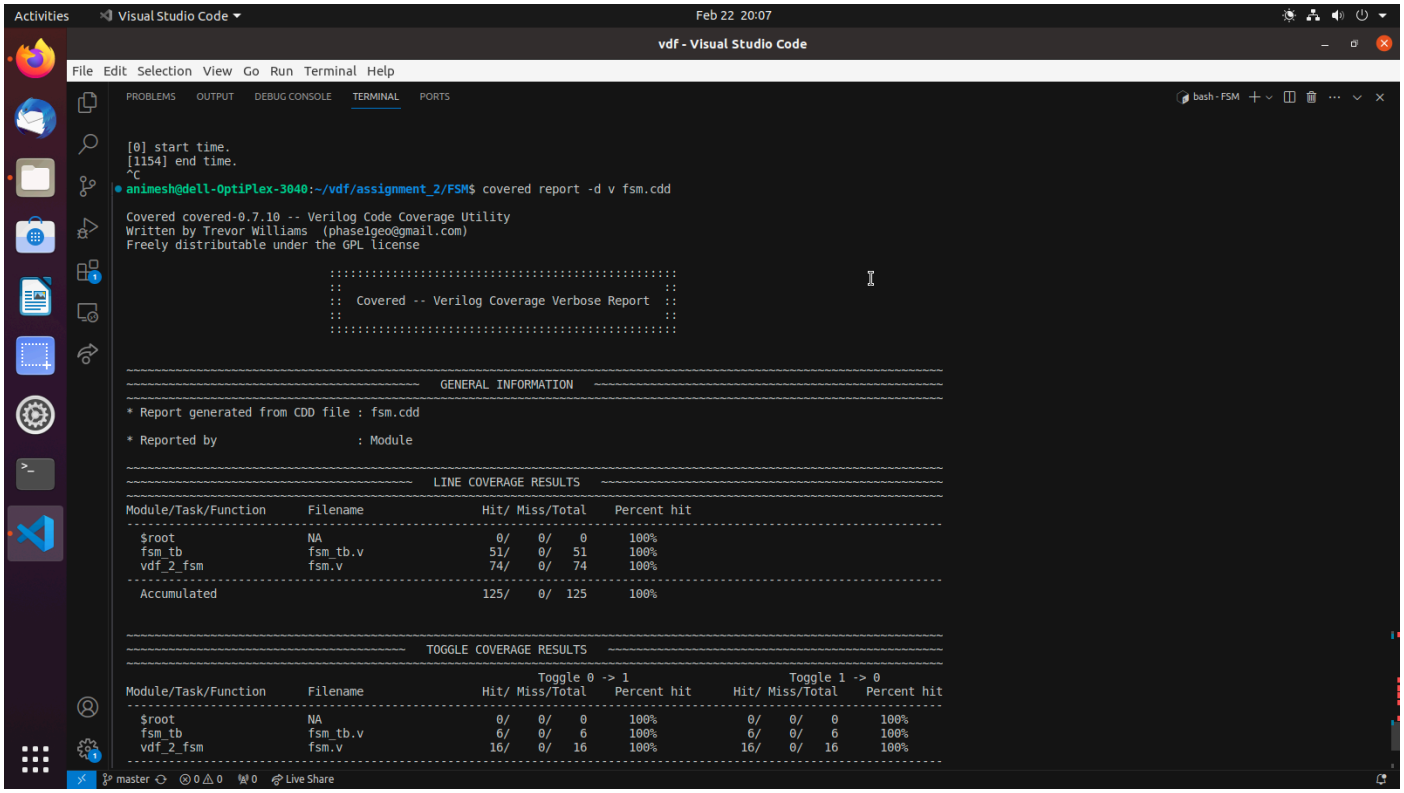
(a) Please refer to the ‘fsm.v’ file for code in the FSM directory.
(b) Please refer to the ‘fsm_tb.v’ file for code in the FSM directory.

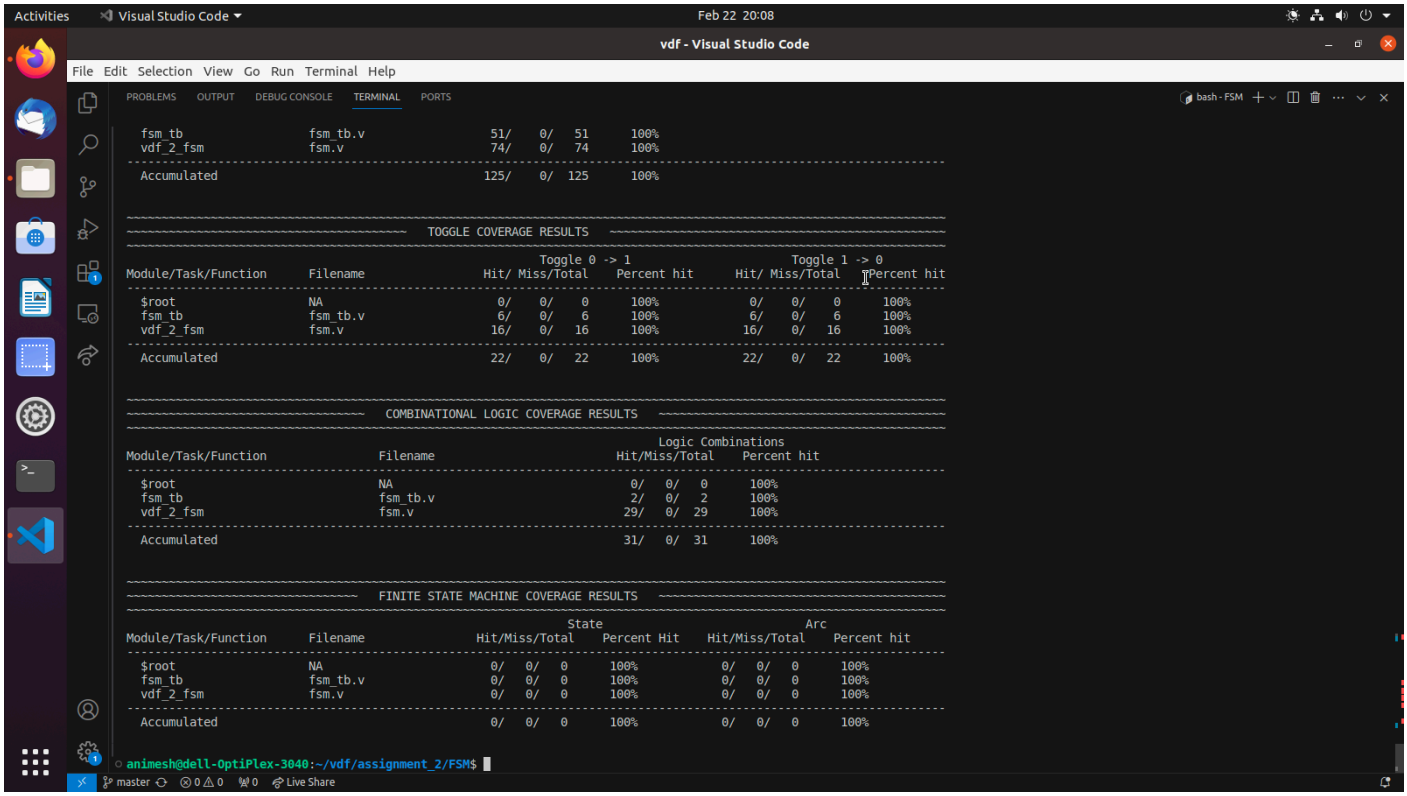
(c) Simulation Waveform →



In the above Simulation waveform we have tested for fsm given in the assignment pdf. We started with a basic toggling clock signal and then gave the reset signal (not at clock edge) which spontaneously resets our fsm. While the reset (asynchronous) was high, we tried to vary input but the output and state did not change. Clearly this shows that reset is working perfectly fine. Now when we deserted the reset the next state change was observed at the positive edge of the clock. After this we gave different inputs and verified the state changes and output changes via manual checks. The results of manual checks completely verified the simulation results (including correct outputs and states) and complete coverage of the code.

(d) Line coverage Report →





This Report indicates that we have written a perfect testbench for our fsm. It perfectly covers all lines, combinational logics, toggles and fsm logics.

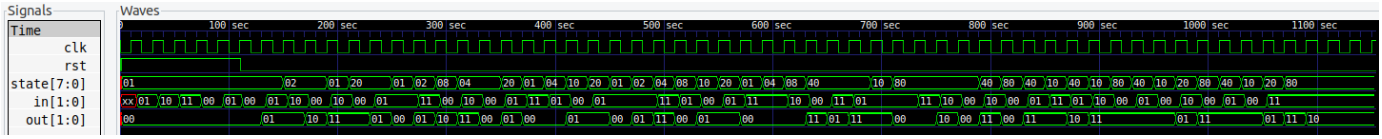
(e) Please refer to the ‘synth_fsm.v’ and ‘synth_fsm.sp’ files for netlist in the FSM directory. The usage Report for this result is the following :

```
=== vdf_2_fsm ===

   Number of wires:                 67
   Number of wire bits:             75
   Number of public wires:           8
   Number of public wire bits:      16
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 64
     AND2_X1                         1
     AND3_X1                         2
     AOI211_X1                       1
     AOI21_X1                        2
     AOI221_X1                       2
     AOI22_X1                        1
     DFFR_X1                         5
     INV_X1                         11
     NAND2_X1                        5
     NAND3_X1                        5
     NAND4_X1                        7
     NOR2_X1                         5
     NOR3_X1                         1
     OAI211_X1                       5
     OAI21_X1                        3
     OR2_X1                          5
     OR3_X1                          2
     XNOR2_X1                        1

   Chip area for module '\vdf_2_fsm': 87.248000
```

(f) For hot encoding refer to the folder ‘Hot_Encodding_FSM’.
Fsm file is ‘fsm_hot.v’.
Testbench file is ‘fsm_tb.v’
Simulation file is ‘fsm_sim.vcd’
Simulation waveform was as follows :



Again the results of manual checks completely verified the simulation results (including correct outputs and states) and complete coverage of the code.
Covered report file is ‘fsm.ccd’
Report is :

```
animesh@dell-OptiPlex-3040:~/vdf/assignment_2/Hot_Encodding_FSM$ covered report -d v fsm.cdd

 Covered covered-0.7.10 -- Verilog Code Coverage Utility
 Written by Trevor Williams  (phase1geo@gmail.com)
 Freely distributable under the GPL license

                              ::::::::::::::::::::::::::::::::::::::::::::::::::
                              ::                                              ::
                              ::  Covered -- Verilog Coverage Verbose Report  ::
                              ::                                              ::
                              ::::::::::::::::::::::::::::::::::::::::::::::::::


 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   GENERAL INFORMATION   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 * Report generated from CDD file : fsm.cdd

 * Reported by                    : Module

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 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   LINE COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 Module/Task/Function      Filename                Hit/ Miss/Total    Percent hit
 ------------------------------------------------------------------------------------------------------------------------
   $root                   NA                        0/    0/    0      100%
   fsm_tb                  fsm_tb.v                 51/    0/   51      100%
   vdf_2_fsm               fsm_hot.v                74/    0/   74      100%
 ------------------------------------------------------------------------------------------------------------------------
   Accumulated                                     125/    0/  125      100%


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 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   TOGGLE COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
                                                           Toggle 0 -> 1                       Toggle 1 -> 0
 Module/Task/Function      Filename                Hit/ Miss/Total    Percent hit      Hit/ Miss/Total    Percent hit
 ------------------------------------------------------------------------------------------------------------------------
   $root                   NA                        0/    0/    0      100%             0/    0/    0      100%
   fsm_tb                  fsm_tb.v                  6/    0/    6      100%             6/    0/    6      100%
   vdf_2_fsm               fsm_hot.v                26/    0/   26      100%            26/    0/   26      100%
 ------------------------------------------------------------------------------------------------------------------------
   Accumulated                                      32/    0/   32      100%            32/    0/   32      100%
```

```
   Accumulated                                      32/    0/   32      100%            32/    0/   32      100%


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 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   COMBINATIONAL LOGIC COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
                                                                    Logic Combinations
 Module/Task/Function                Filename                          Hit/Miss/Total    Percent hit
 ------------------------------------------------------------------------------------------------------------------------
   $root                             NA                                  0/    0/    0      100%
   fsm_tb                            fsm_tb.v                            2/    0/    2      100%
   vdf_2_fsm                         fsm_hot.v                          27/    2/   29       93%
 ------------------------------------------------------------------------------------------------------------------------
   Accumulated                                                          29/    2/   31       94%
 ------------------------------------------------------------------------------------------------------------------------

     Module: vdf_2_fsm, File: fsm_hot.v
     --------------------------------------------------------------------------------------------------------------------
     Missed Combinations  (* = missed value)

       =========================================================================================================
        Line #     Expression
       =========================================================================================================
              22:    state <= new_state
                              |---1---|

         Expression 1   (1/2)
         ^^^^^^^^^^^^^ -
          E | E
         =0=|=1=
          *

       =========================================================================================================
        Line #     Expression
       =========================================================================================================
              29:    case( state )
                           |-1-|
                      s1 :

         Expression 1   (1/2)
         ^^^^^^^^^^^^^ -
          E | E
         =0=|=1=
          *
```

```
          *


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 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   FINITE STATE MACHINE COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
 ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
                                                          State                              Arc
Module/Task/Function       Filename                Hit/Miss/Total    Percent Hit      Hit/Miss/Total    Percent hit
 ------------------------------------------------------------------------------------------------------------------------
  $root                    NA                        0/    0/    0      100%             0/    0/    0      100%
  fsm_tb                   fsm_tb.v                  0/    0/    0      100%             0/    0/    0      100%
  vdf_2_fsm                fsm_hot.v                 0/    0/    0      100%             0/    0/    0      100%
 ------------------------------------------------------------------------------------------------------------------------
  Accumulated                                        0/    0/    0      100%             0/    0/    0      100%
```

The reason why this report is throwing 2 uncoverage issues in combinational check is because it sees that we don't happen to evaluate ‘state’ when either state is 8’b0 or ‘new_state’ is 8’b0. This is not an issue because in our hot encoding scheme there is no state which is represented by 8’b0. Apart from this, this Report indicates that we have written a perfect testbench for our fsm which covers all lines, toggles situations, and combinational and fsm logics.
Finally the netlist files synthesized by yosys are ‘synth_fsm_hot.v’ and ‘synth_fsm_hot.sp’.
The Usage Report for this synthesis is :

```
=== vdf_2_fsm ===

   Number of wires:                 81
   Number of wire bits:             99
   Number of public wires:           8
   Number of public wire bits:      26
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                 83
     AND2_X1                         2
     AND3_X1                         1
     AND4_X1                         5
     AOI21_X1                        4
     AOI222_X1                       1
     AOI22_X1                        2
     DFFR_X1                         9
     DFFS_X1                         1
     INV_X1                         21
     NAND2_X1                        4
     NAND3_X1                        1
     NAND4_X1                        6
     NOR2_X1                        10
     NOR3_X1                         2
     NOR4_X1                         2
     OAI211_X1                       1
     OAI21_X1                        3
     OAI221_X1                       4
     OAI22_X1                        1
     OR2_X1                          1
     OR4_X1                          1
     XNOR2_X1                        1

   Chip area for module '\vdf_2_fsm': 126.350000
```

To re-run the model , Refer to the Readme.txt

End of the Report