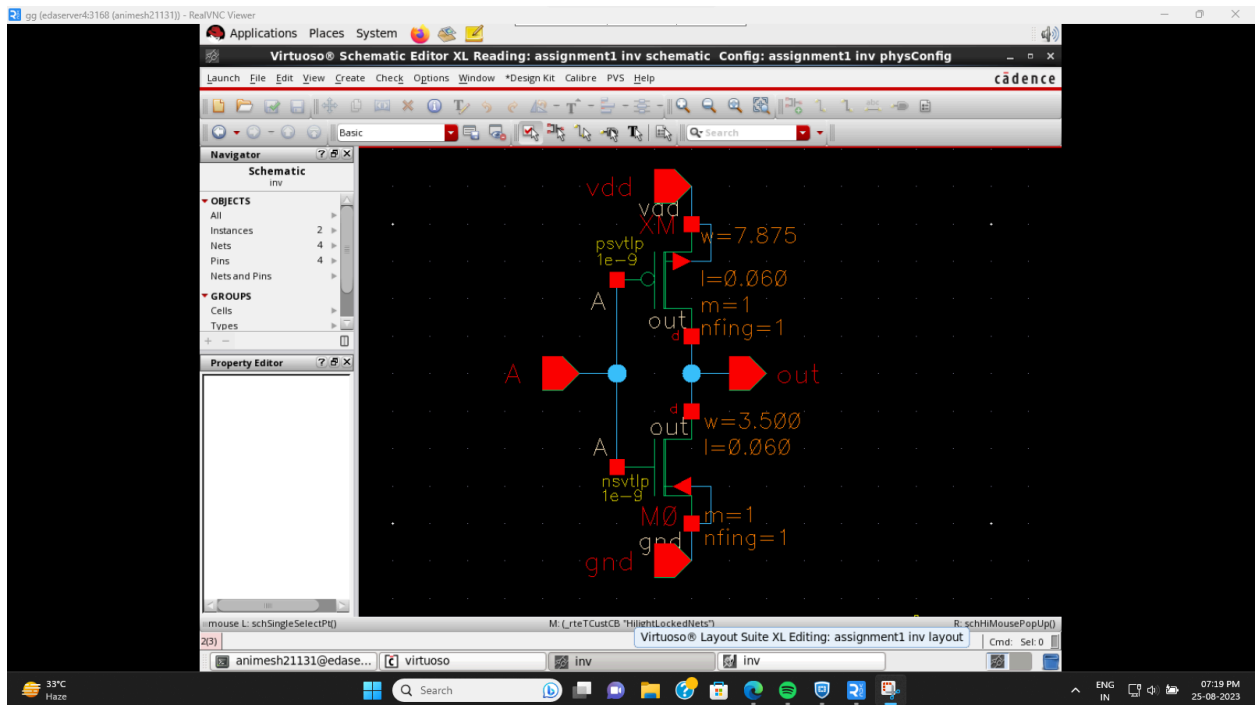


- 1) For Slow-Slow case->
Schematic =>



Pre layout Report =>

```
animesh21131@edaserver4:inv
File Edit View Search Terminal Help
Simulation progress : 90% (t = 90.0000 N)
Elapsed CPU time   : 0h 0mn 0s 0 ( 0h 0mn 0s 10)
CPU Usage         : 0% ( 66%)
.....
Simulation progress : 100% (t = 100.0000 N)
Elapsed CPU time   : 0h 0mn 0s 0 ( 0h 0mn 0s 10)
CPU Usage         : 0% ( 62%)

***>Current simulation completed

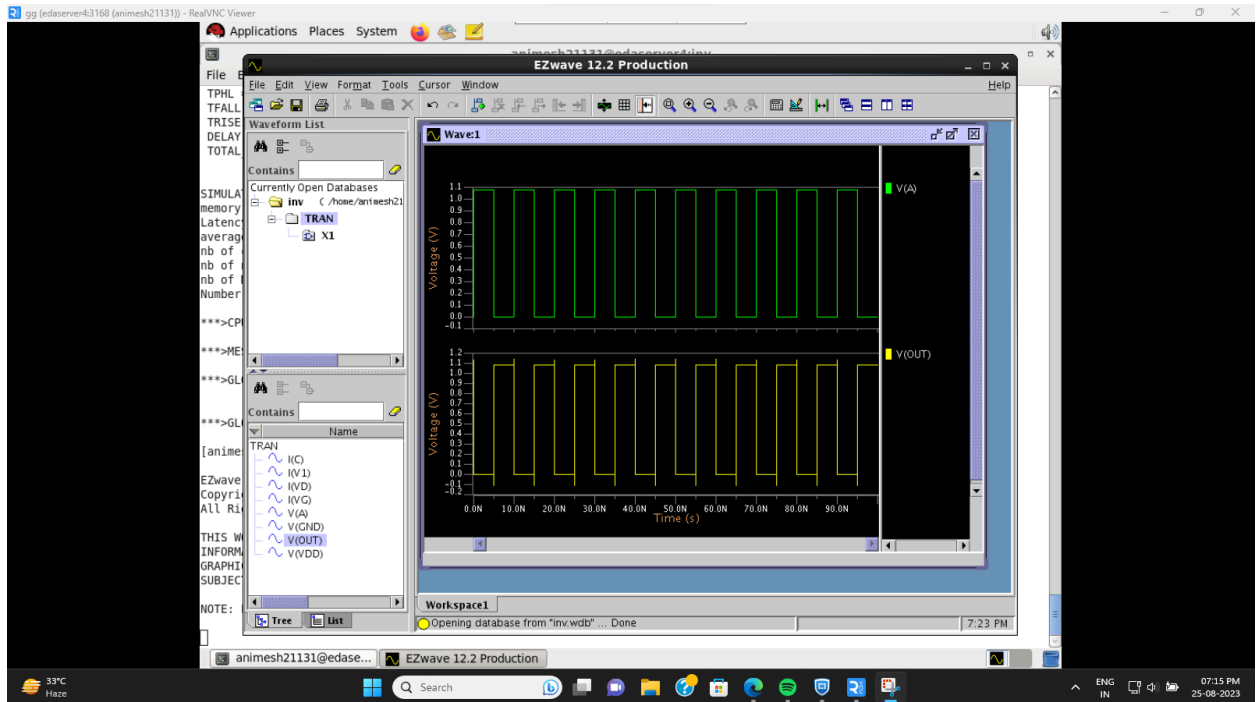
TPLH = 2.5271E-11
TPHL = 2.2115E-11
TFALL = 2.5118E-11
TRISE = 2.5062E-11
DELAY = 2.3693E-11
TOTAL_POWER = 3.8500E-06

SIMULATION INFORMATION
memory size allocated in Mbytes 260.3
Latency: 0.000000%
average number of newton iterations: 2.619490
nb of components: 6
nb of nodes: 6
nb of MOS or BIP calls: 1296
Number of steps computed: 431

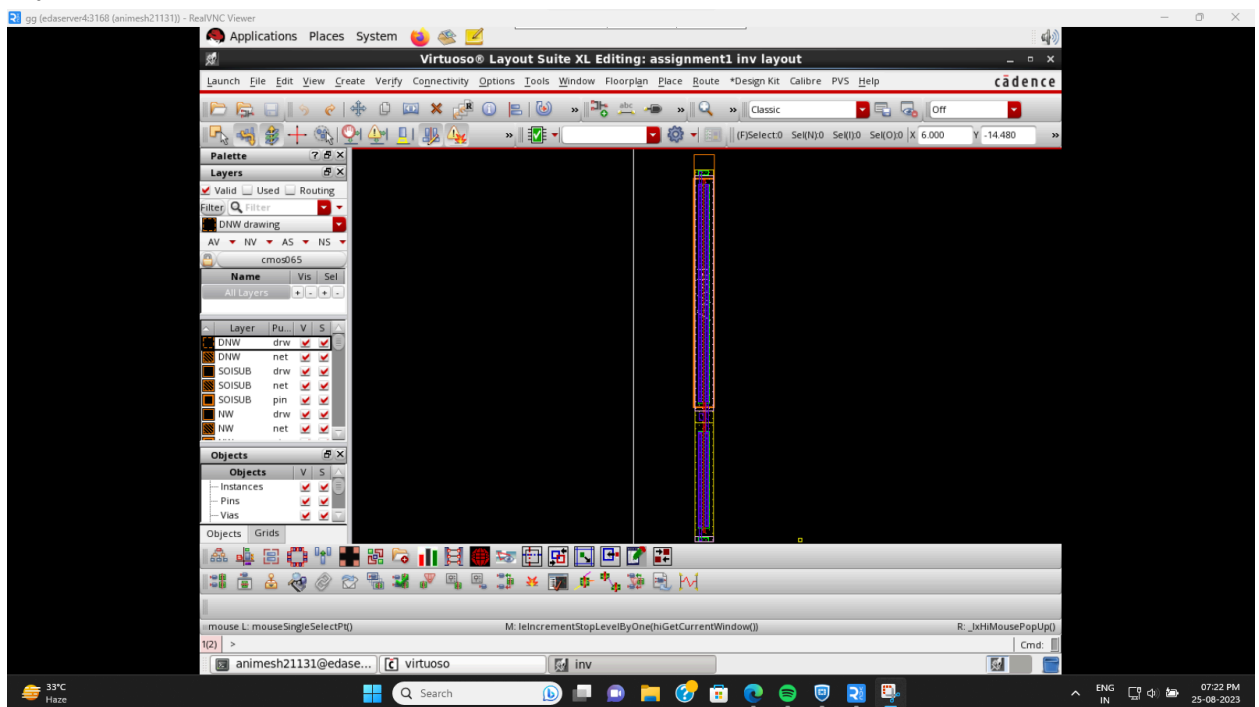
***>CPU TIME 0s 010ms <***
***>MESSAGE SUMMARY: 7 warnings
***>GLOBAL CPU TIME 0s 200ms <***

***>GLOBAL ELAPSED TIME 0s <***

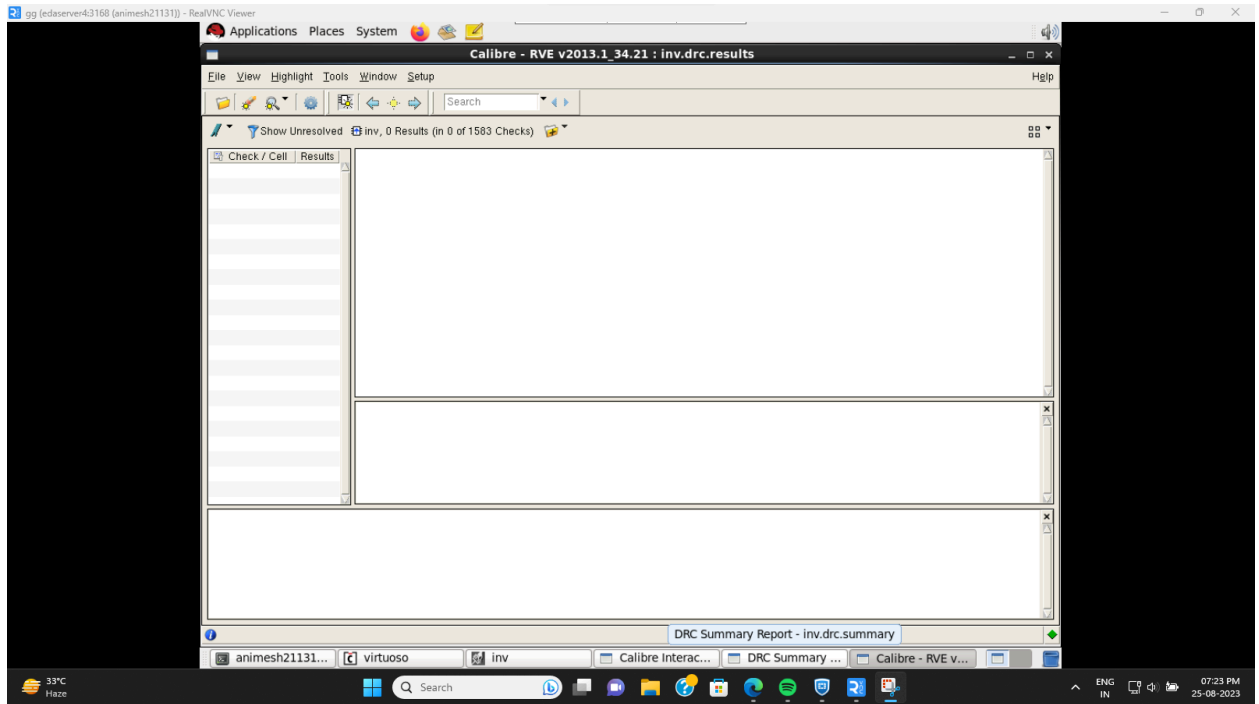
[animesh21131@edaserver4 inv]$
```



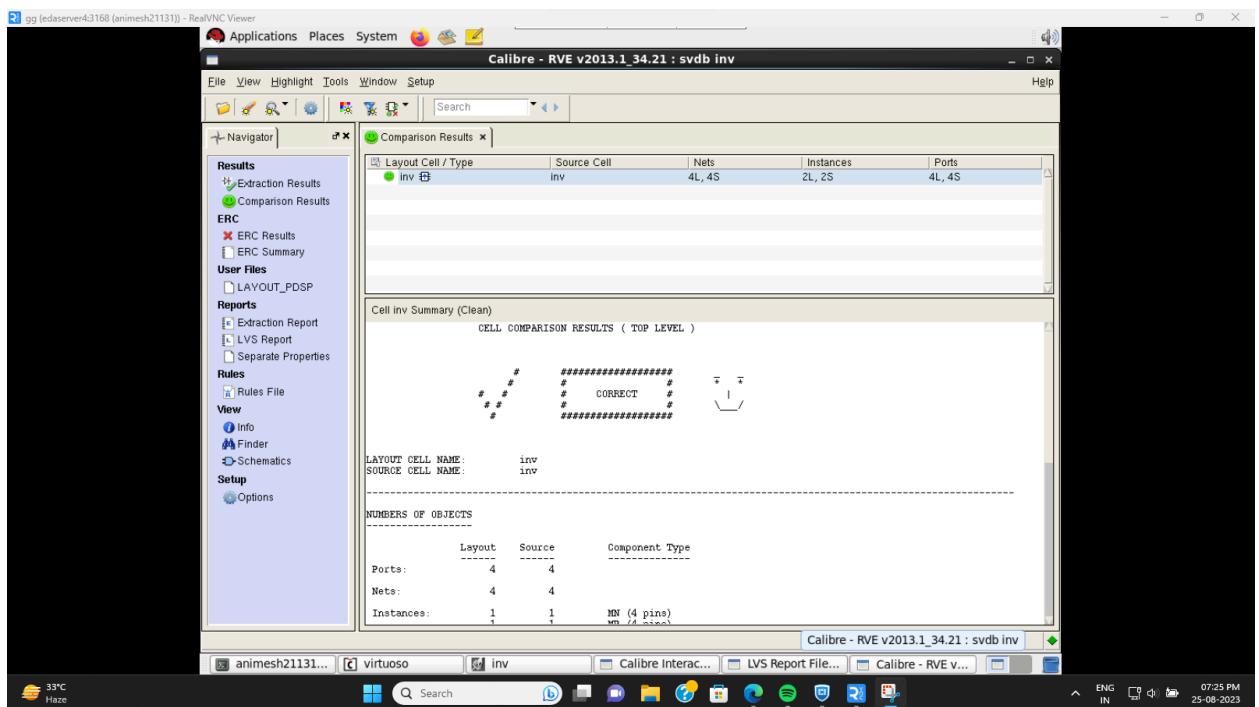
Layout ⇒



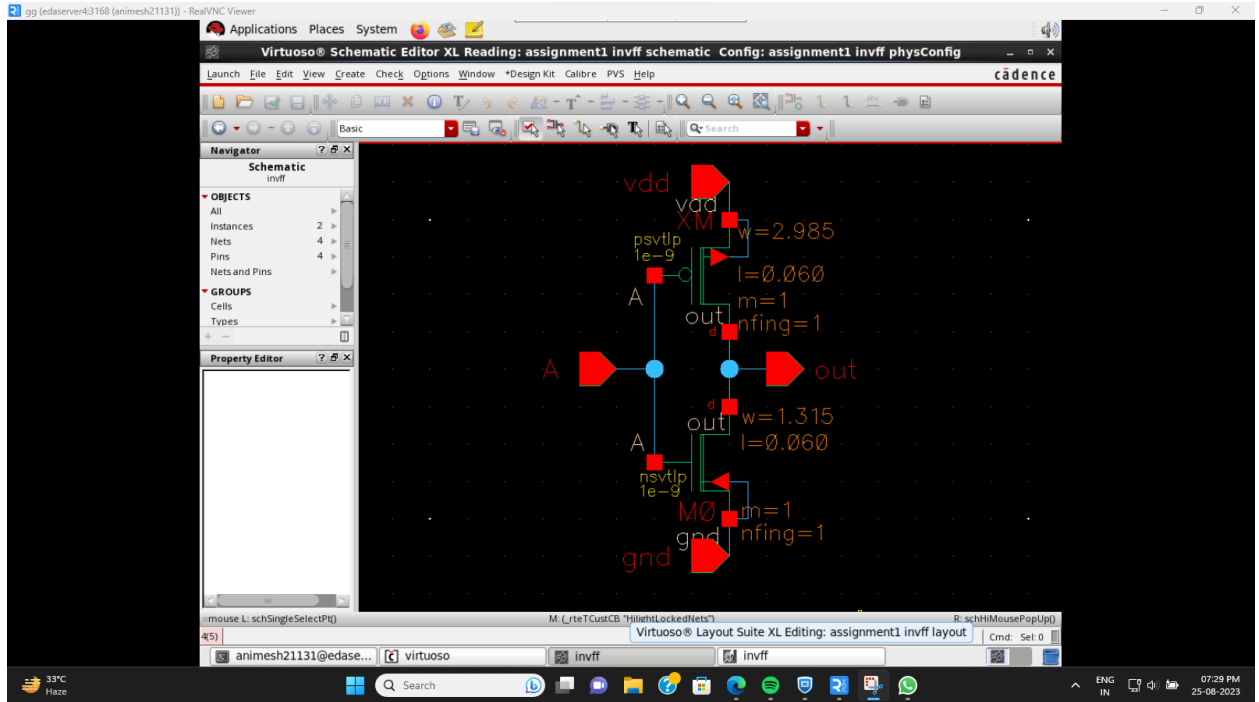
DRC Clearance ⇒



LVS Clearance ⇒



- 2) For Fast- Fast case->
Schematic ⇒



Pre layout Report ⇒

```

animesh21131@edaserver4:invff
File Edit View Search Terminal Help
Elapsed CPU time      : 0h 0mn 0s 0 ( 0h 0mn 0s 10)
CPU Usage             : 0% ( 50%)
.....
Simulation progress   : 100% (t = 100.0000 N)
Elapsed CPU time      : 0h 0mn 0s 10 ( 0h 0mn 0s 20)
CPU Usage             : 100% ( 95%)

***>Current simulation completed

TPLH = 1.7784E-11
TPHL = 1.9820E-11
TFALL = 2.5004E-11
TRISE = 2.5003E-11
DELAY = 1.8802E-11
TOTAL_POWER = 4.3651E-06

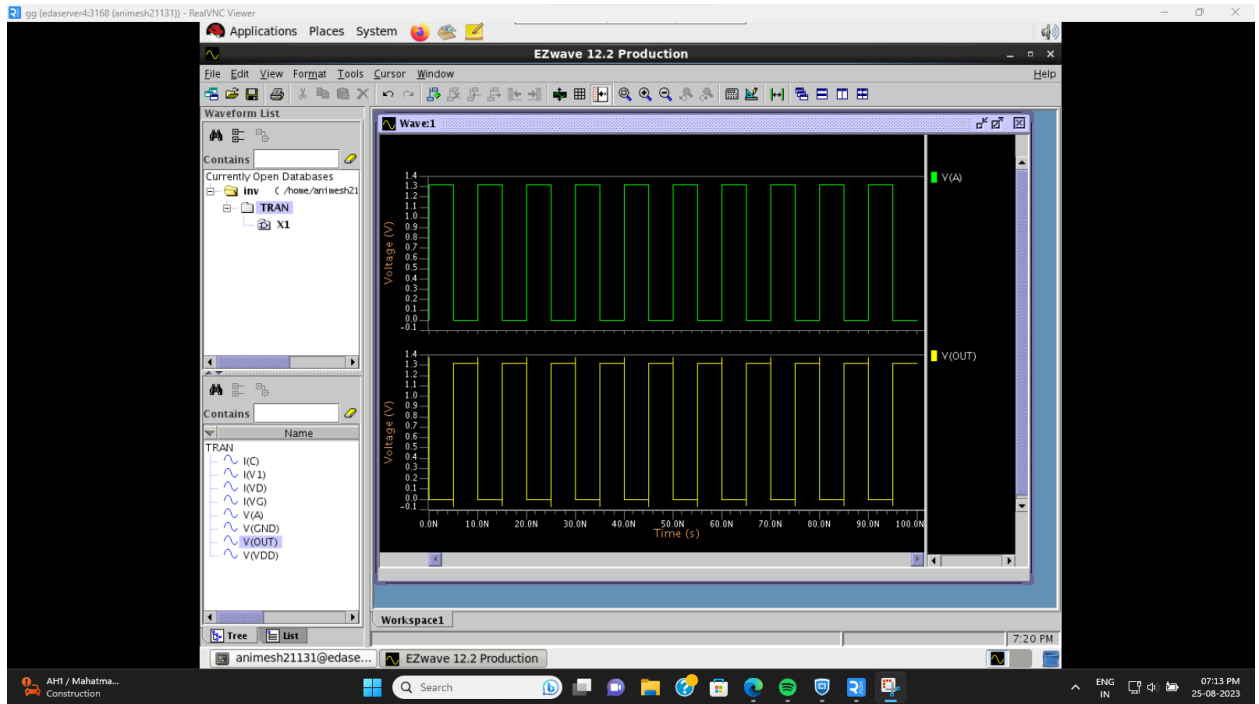
SIMULATION INFORMATION
memory size allocated in Mbytes 260.3
Latency: 0.000000%
average number of newton iterations: 2.351544
nb of components: 6
nb of nodes: 6
nb of MOS or BIP calls: 1365
Number of steps computed: 421

***>CPU TIME 0s 020ms <***
***>MESSAGE SUMMARY: 7 warnings
***>GLOBAL CPU TIME 0s 210ms <***

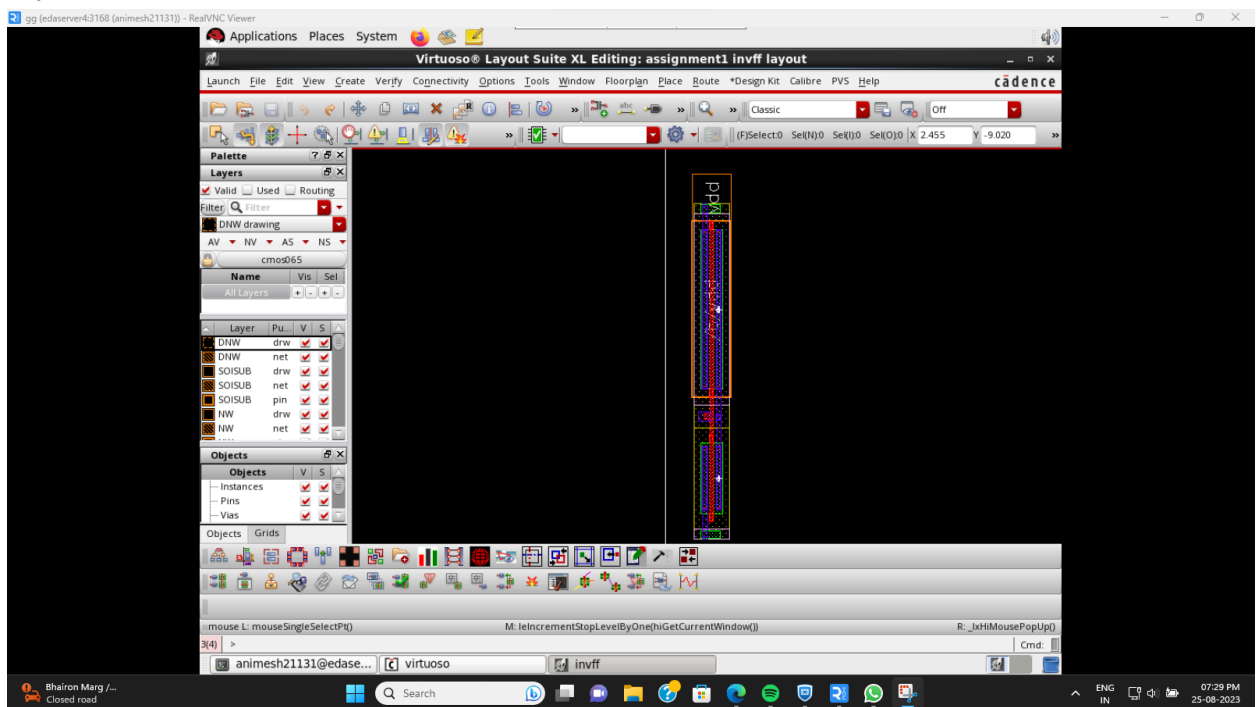
***>GLOBAL ELAPSED TIME 1s <***

[animesh21131@edaserver4 invff]$ ezwave inv.wdb
animesh21131@edase...

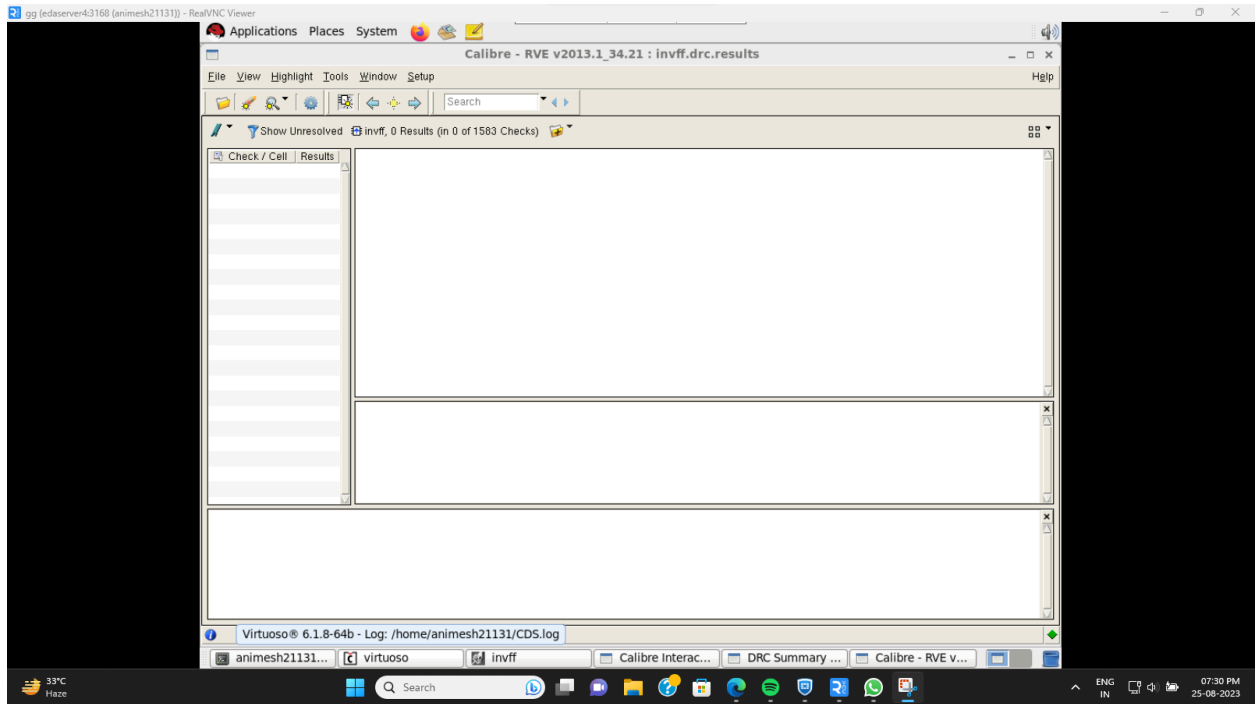
```



Layout ⇒



DRC Clearance ⇒



LVS Clearance ⇒

