

VDF Assignment-2 Report

By Animesh Pareek { BTech-ECE 2021131 }

Part-1 →

Iverilog Tool Run Screenshot >>

```
animesh@dell-OptiPlex-3040:~/vdf/assignment_2/FSM$ iverilog -h
Usage: iverilog [-EiRSuvV] [-B base] [-c cmdfile|-f cmdfile]
             [-g1995|-g2001|-g2005|-g2005-sv|-g2009|-g2012] [-g<feature>]
             [-D macro[=defn]] [-I includedir] [-L moduledir]
             [-M [mode=]depfile] [-m module]
             [-N file] [-o filename] [-p flag=value]
             [-s topmodule] [-t target] [-T min|typ|max]
             [-W class] [-y dir] [-Y suf] [-l file] source_file(s)

See the man page for details.
animesh@dell-OptiPlex-3040:~/vdf/assignment_2/FSM$
```

Covered Tool Run Screenshot >>

```
animesh@dell-OptiPlex-3040:~/vdf/assignment_2/FSM$ covered report -d v fsm.cdd

Covered covered-0.7.10 -- Verilog Code Coverage Utility
Written by Trevor Williams (phaselgeo@gmail.com)
Freely distributable under the GPL license

:::
::
:: Covered -- Verilog Coverage Verbose Report ::
::
:::

-----
GENERAL INFORMATION
-----

* Report generated from CDD file : fsm.cdd

* Reported by           : Module
```

Yosys Tool Run Screenshot >>

```
animesh@dell-OptiPlex-3040:~/vdf/assignment_2/FSM$ yosys

/-----/
|
| yosys -- Yosys Open SYnthesis Suite
|
| Copyright (C) 2012 - 2020 Claire Xenia Wolf <claire@yosyshq.com>
|
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|
| THE SOFTWARE IS PROVIDED "AS IS" AND THE AUTHOR DISCLAIMS ALL WARRANTIES
| WITH REGARD TO THIS SOFTWARE INCLUDING ALL IMPLIED WARRANTIES OF
| MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR
| ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES
| WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN
| ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF
| OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.
|
|-----/

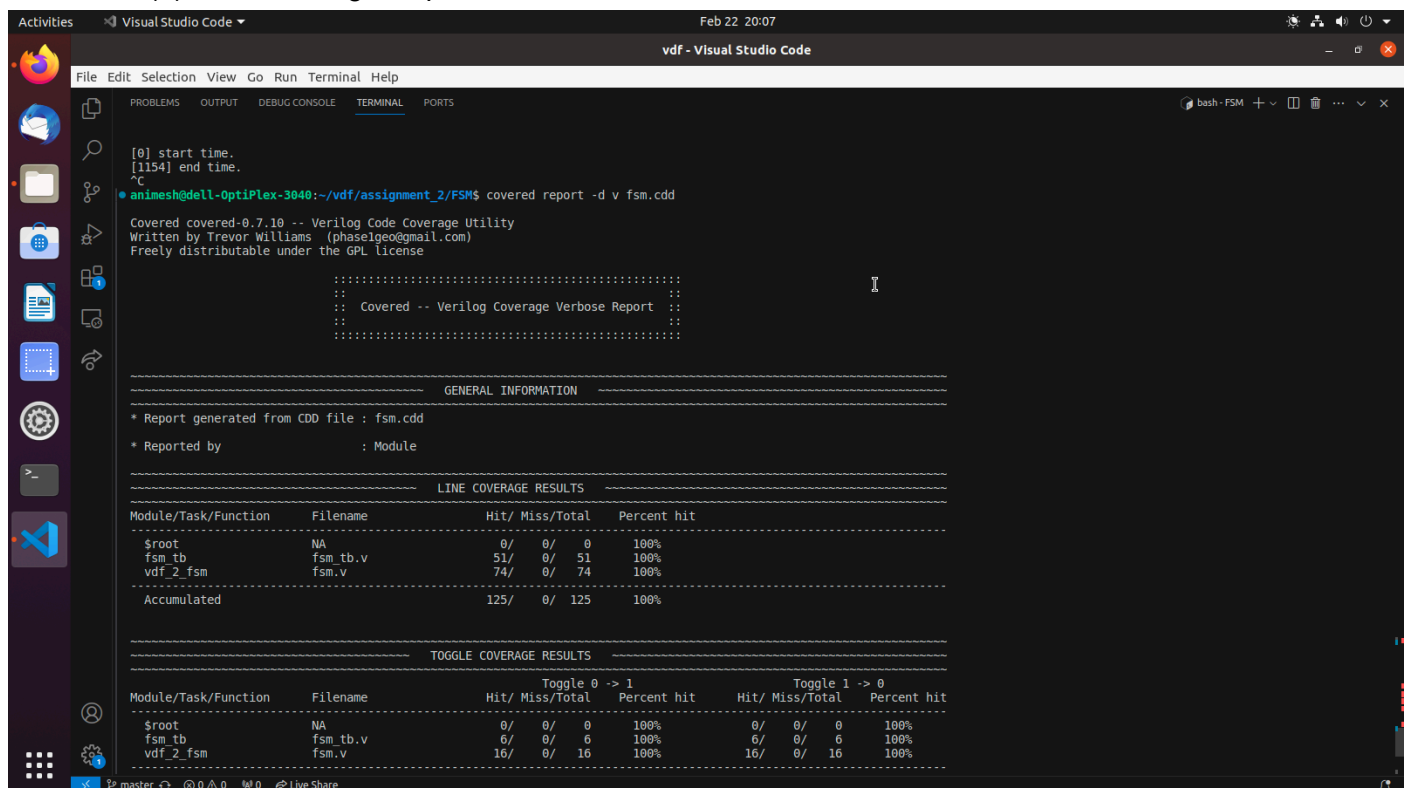
Yosys 0.37+27 (git sha1 ebf6128d9, clang 10.0.0-4ubuntu1 -fPIC -Os)

yosys> ^C
animesh@dell-OptiPlex-3040:~/vdf/assignment_2/FSM$
```

Part-2 →

- Please refer to the 'fsm.v' file for code in the FSM directory.
- Please refer to the 'fsm_tb.v' file for code in the FSM directory.

(d) Line coverage Report →



```

Feb 22 20:08
vdf - Visual Studio Code

File Edit Selection View Go Run Terminal Help
PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL PORTS
bash - FSM

fsm_tb          fsm_tb.v      51/ 0/ 51    100%
vdf_2_fsm      fsm.v        74/ 0/ 74    100%
-----
Accumulated          125/ 0/ 125    100%

=====
TOGGLE COVERAGE RESULTS
=====
Module/Task/Function  Filename      Toggle 0 -> 1  Percent hit  Toggle 1 -> 0  Percent hit
-----
$root                NA            0/ 0/ 0      100%         0/ 0/ 0      100%
fsm_tb               fsm_tb.v      6/ 0/ 6      100%         6/ 0/ 6      100%
vdf_2_fsm             fsm.v        16/ 0/ 16     100%        16/ 0/ 16     100%
-----
Accumulated          22/ 0/ 22     100%        22/ 0/ 22     100%

=====
COMBINATIONAL LOGIC COVERAGE RESULTS
=====
Module/Task/Function  Filename      Logic Combinations
Hit/Miss/Total      Percent hit
-----
$root                NA            0/ 0/ 0      100%
fsm_tb               fsm_tb.v      2/ 0/ 2      100%
vdf_2_fsm             fsm.v        29/ 0/ 29     100%
-----
Accumulated          31/ 0/ 31     100%

=====
FINITE STATE MACHINE COVERAGE RESULTS
=====
Module/Task/Function  Filename      State      Percent Hit  Arc      Percent hit
-----
$root                NA            0/ 0/ 0      100%         0/ 0/ 0      100%
fsm_tb               fsm_tb.v      0/ 0/ 0      100%         0/ 0/ 0      100%
vdf_2_fsm             fsm.v        0/ 0/ 0      100%         0/ 0/ 0      100%
-----
Accumulated          0/ 0/ 0      100%         0/ 0/ 0      100%

animesh@dell-OptiPlex-3040:~/vdf/assignment_2/FSM$

```

- This Report indicates that we have written a perfect testbench for our fsm. It perfectly covers all lines, combinational logics, toggles and fsm logics.
- (e) Please refer to the 'synth_fsm.v' and 'synth_fsm.sp' files for netlist in the FSM directory. The usage Report for this result is the following :

```

=== vdf_2_fsm ===

Number of wires:          67
Number of wire bits:      75
Number of public wires:   8
Number of public wire bits: 16
Number of memories:       0
Number of memory bits:    0
Number of processes:      0
Number of cells:          64
    AND2_X1                1
    AND3_X1                2
    AOI211_X1              1
    AOI21_X1               2
    AOI221_X1              2
    AOI22_X1               1
    DFFR_X1                5
    INV_X1                 11
    NAND2_X1               5
    NAND3_X1               5
    NAND4_X1               7
    NOR2_X1                5
    NOR3_X1                1
    OAI211_X1              5
    OAI21_X1               3
    OR2_X1                 5
    OR3_X1                 2
    XNOR2_X1               1

Chip area for module 'vdf_2_fsm': 87.248000

```

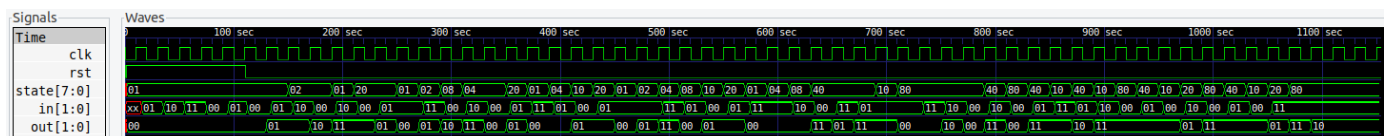
(f) For hot encoding refer to the folder 'Hot_Encodding_FSM'.

Fsm file is 'fsm_hot.v'.

Testbench file is 'fsm_tb.v'

Simulation file is 'fsm_sim.vcd'

Simulation waveform was as follows :



Again the results of manual checks completely verified the simulation results (including correct outputs and states) and complete coverage of the code.

Covered report file is 'fsm.ccd'

Report is :

```

animesh@de11-OptiPlex-3040:~/vdf/assignment_2/Hot_Encodding_FSM$ covered report -d v fsm.cdd

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Written by Trevor Williams (phaselgeo@gmail.com)
Freely distributable under the GPL license

:::
::
:: Covered -- Verilog Coverage Verbose Report ::
::
:::

-----
GENERAL INFORMATION
-----

* Report generated from CDD file : fsm.cdd

* Reported by      : Module

-----
LINE COVERAGE RESULTS
-----

Module/Task/Function  Filename      Hit/ Miss/Total  Percent hit
-----
$root                 NA            0/   0/   0      100%
fsm_tb                fsm_tb.v      51/   0/  51      100%
vdf_2_fsm             fsm_hot.v     74/   0/   74      100%
-----
Accumulated           125/   0/  125      100%

-----
TOGGLE COVERAGE RESULTS
-----

Module/Task/Function  Filename      Hit/ Miss/Total  Toggle 0 -> 1  Percent hit  Hit/ Miss/Total  Toggle 1 -> 0  Percent hit
-----
$root                 NA            0/   0/   0      100%           0/   0/   0      100%
fsm_tb                fsm_tb.v      6/   0/   6      100%           6/   0/   6      100%
vdf_2_fsm             fsm_hot.v     26/   0/  26      100%          26/   0/  26      100%
-----
Accumulated           32/   0/   32      100%           32/   0/   32      100%

```

```

Accumulated           32/   0/   32      100%           32/   0/   32      100%

-----
COMBINATIONAL LOGIC COVERAGE RESULTS
-----

Module/Task/Function  Filename      Logic Combinations
Hit/Miss/Total  Percent hit
-----
$root                 NA            0/   0/   0      100%
fsm_tb                fsm_tb.v      2/   0/   2      100%
vdf_2_fsm             fsm_hot.v     27/   2/  29      93%
-----
Accumulated           29/   2/  31      94%

Module: vdf_2_fsm, File: fsm_hot.v
Missed Combinations (* = missed value)

=====
Line #      Expression
=====
      22:  state <= new_state
           |--1--|

Expression 1 (1/2)
~~~~~
E | E
=0|=1=
*

=====
Line #      Expression
=====
      29:  case( state )
           |-1-|
           s1 :

Expression 1 (1/2)
~~~~~
E | E
=0|=1=
*

=====

```

```

*

-----
FINITE STATE MACHINE COVERAGE RESULTS
-----

Module/Task/Function  Filename      State
Hit/Miss/Total  Percent Hit  Hit/Miss/Total  Arc  Percent hit
-----
$root                 NA            0/   0/   0      100%           0/   0/   0      100%
fsm_tb                fsm_tb.v      0/   0/   0      100%           0/   0/   0      100%
vdf_2_fsm             fsm_hot.v      0/   0/   0      100%           0/   0/   0      100%
-----
Accumulated           0/   0/   0      100%           0/   0/   0      100%

```

The reason why this report is throwing 2 uncoverage issues in combinational check is because it sees that we don't happen to evaluate 'state' when either state is 8'b0 or 'new_state' is 8'b0. This is not an issue because in our hot encoding scheme there is no state which is represented by 8'b0. Apart from this, this Report indicates that we have written a perfect testbench for our fsm which covers all lines, toggles situations, and combinational and fsm logics. Finally the netlist files synthesized by yosys are 'synth_fsm_hot.v' and 'synth_fsm_hot.sp'.

The Usage Report for this synthesis is :

```
=== vdf_2_fsm ===  
  
Number of wires:                81  
Number of wire bits:            99  
Number of public wires:         8  
Number of public wire bits:     26  
Number of memories:             0  
Number of memory bits:          0  
Number of processes:            0  
Number of cells:                83  
  AND2_X1                        2  
  AND3_X1                        1  
  AND4_X1                        5  
  AOI21_X1                       4  
  AOI222_X1                      1  
  AOI22_X1                       2  
  DFFR_X1                        9  
  DFFS_X1                        1  
  INV_X1                        21  
  NAND2_X1                      4  
  NAND3_X1                      1  
  NAND4_X1                      6  
  NOR2_X1                       10  
  NOR3_X1                       2  
  NOR4_X1                       2  
  OAI211_X1                     1  
  OAI21_X1                      3  
  OAI221_X1                     4  
  OAI22_X1                      1  
  OR2_X1                        1  
  OR4_X1                        1  
  XNOR2_X1                      1  
  
Chip area for module '\vdf_2_fsm': 126.350000
```

To re-run the model , Refer to the Readme.txt

****End of the Report****