

VDF Assignment-4 Report

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Q1 →

ATPG Tool Run Screenshot :

```
animesh@dell-OptiPlex-3040:~/vdf/assignment_4$ atalanta
Invalid command line options.
To see on-line manual, use the following commands:
  For the user's guide, type "atalanta -h g"
  For the netlist format, type "atalanta -h n"
  For the test file format, type "atalanta -h t"
  For the fault list file format, type "atalanta -h f"
  For the entire manual, type "atalanta -h a"
animesh@dell-OptiPlex-3040:~/vdf/assignment_4$
```

Q-2 →

Bench Netlist, Test Patterns Generated (Patterns and analysis) and Undetected Faults:

The screenshot displays the ATPG tool interface with three main panels:

- netlist1.v.bench:** Contains the circuit description in Verilog format, including inputs A, B, C, D, and output Z, along with logic equations for w1 through w5.
- netlist1.vec:** Shows the generated test vectors for the circuit, including the primary inputs A, B, C, D and the primary output Z.
- netlist1.test:** Displays the test patterns and fault-free responses for the circuit, including the primary inputs A, B, C, D and the primary output Z.

The bottom panel shows the results of the fault analysis, indicating that there are 1 undetected faults.

Undetected Faults = 1

Manual fault analysis : (single fault)

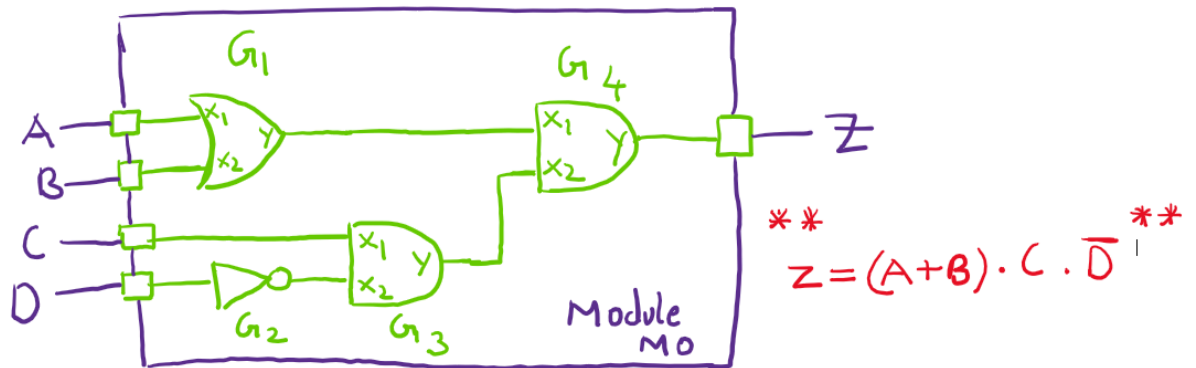
Required test vectors(A,B,C,D) => 1111, 1010,0110, 0010, 1100

Table** : ** (x stands for don't cares) { x = 0 or 1 } (A,B,C,D) (Z)

| Fault Site | Fault Type | Test Pattern reported by Tool | Test Pattern Manually Computed |
|---|------------|----------------------------------|---|
| A or G1(X1) | SA0 | 1010 (1) | 1010 (1) |
| | SA1 | NO REPORT | 0010 (0) |
| B or G1(X2) | SA0 | 0110 (1) | 0110 (1) |
| | SA1 | NO REPORT | 0010 (0) |
| C (input to design) or (G2(X1) && G3(X2)) | SA0 | 1x10 (1) | 1x10 or x110 (1) |
| | SA1 | 1x00 (0) | 1x00 or x100 (0) |
| G2(X1) | SA0 | 1x11 or 0111 (0) | 1x11 or x111 (0) |
| | SA1 | U Fault Site | CAN'T Be TESTED (No Impact on functionality) |
| G3(X2) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | NO REPORT | 1x00 or x100 or 1x01 or x101 (0) |
| D or G2(X2) | SA0 | NO REPORT | 1x11 or x111 (0) |
| | SA1 | 1x10 (1) | 1x10 or x110 (1) |
| G1(Y) or G3(X1) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | 0010 (0) | 0010 (0) |
| G2(Y) or G4(X2) | SA0 | NO REPORT | 1x11 or x111 (0) |
| | SA1 | NO REPORT | 1x10 or x110 (1) |
| G3(Y) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | 1x0x or 010x (0) | 0010 or xx0x (0) |
| G3(~Y) or G4(X1) | SA0 | 0010 or xx0x (0) | 0010 or xx0x (0) |
| | SA1 | NO REPORT | 1x10 or x110 (1) |
| G4(Y) | SA0 | 1x11 or 0111 (0) | 0010 or xxx1 or xx00 (0) |
| | SA1 | NO REPORT | 1x10 or x110 (1) |
| Z or G4(~Y) | SA0 | 1x10 or 0110 (1) | 1x10 or x110 (1) |
| | SA1 | xx11 or xx01 or xx00 or 0010 (0) | 0010 or xxx1 or xx00 (0) |

Q-3 →

New schematic :



Bench Netlist, Test Patterns Generated (Patterns and analysis) and Undetected Faults:

```

File Edit Selection View Go Run Terminal Help

netlist2.v.bench x
assignment_4 > netlist2.v.bench
1 #bench format
2 INPUT(A)
3 INPUT(B)
4 INPUT(C)
5 INPUT(D)
6 w1=OR(A,B)
7 w2=NOT(D)
8 w3=AND(w2,C)
9 Z=AND(w1,w3)
10 OUTPUT(Z)

netlist2.vec x
assignment_4 > netlist2.vec
1 1011
2 0110
3 0010
4 1000
5 1010
6 END

netlist2.test x
assignment_4 > netlist2.test
1 * Name of circuit: netlist2.v.bench
2 * Primary inputs :
3 | A B C D
4
5 * Primary outputs:
6 | Z
7
8 * Test patterns and fault free responses:
9
10 w1 /1
11 | 1: 0010 0
12 C /1
13 | 1: 1x00 0
14 w3 /1
15 | 1: 1x0x 0
16 | 2: 1x11 0
17 | 3: 010x 0
18 | 4: 0111 0
19 Z /1
20 | 1: 00xx 0
21 | 2: 100x 0
22 | 3: 1011 0
23 | 4: x10x 0
24 | 5: x111 0
25 A /0
26 | 1: 1010 1
27 B /0
28 | 1: 0110 1
29 w2 /1
30 | 1: 1x11 0
31 | 2: 0111 0
32 Z /0
33 | 1: 1x10 1
34 | 2: 0110 1
35
  
```

Undetected Faults = 0

Manual fault analysis : (single fault)

Required test vectors(A,B,C,D) => 1111, 1010,0110, 0010, 1100

Table** :

** (x stands for don't cares) { x = 0 or 1 }

| Fault Site | Fault Type | Test Pattern reported by Tool | Test Pattern Manually Computed (A,B,C,D) |
|----------------------|------------|----------------------------------|--|
| A or G1(X1) | SA0 | 1010 (1) | 1010 (1) |
| | SA1 | NO REPORT | 0010 (0) |
| B or G1(X2) | SA0 | 0110 (1) | 0110 (1) |
| | SA1 | NO REPORT | 0010 (0) |
| C or G3(X1) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | 1x00 (0) | 1x00 or x100 (0) |
| D or G2(Input) | SA0 | NO REPORT | 1x11 or x111 (0) |
| | SA1 | NO REPORT | 1x10 or x110 (1) |
| G1(Y) or G4(X1) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | 0010 (0) | 0010 (0) |
| G3(X2) or G2(Output) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | 1x11 or 0111 (0) | 1x11 or x111 (0) |
| G3(Y) or G4(X2) | SA0 | NO REPORT | 1x10 or x110 (1) |
| | SA1 | 1x0x or 1x11 or 010x or 0111 (0) | 1x00 or x100 or 1x01 or x101 or 1x11 or x111 (0) |
| Z or G4(Y) | SA0 | 1x10 or 0110 (1) | 1x10 or x110 (1) |
| | SA1 | xx11 or xx01 or xx00 or 0010 (0) | 0010 or xxx1 or xx00 (0) |

To re-run the model , Refer to the Readme.txt

****End of the Report****