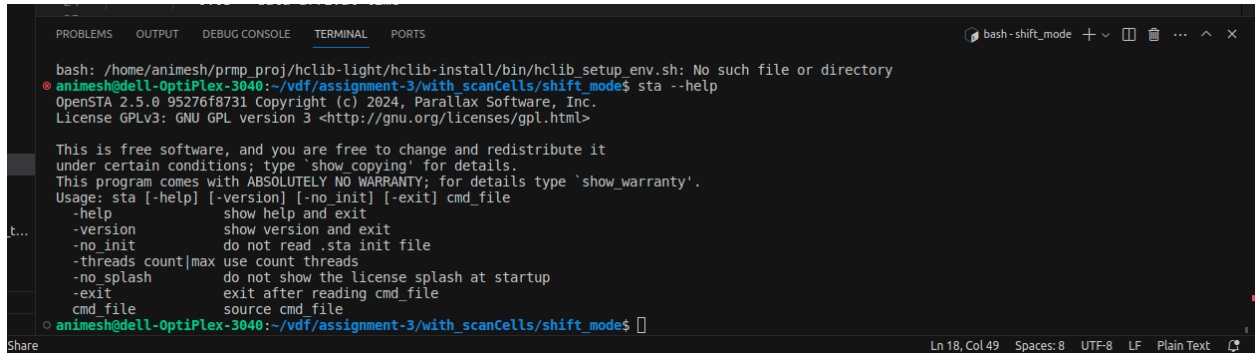


VDF Assignment-3 Report

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Q1 →

STA Tool Run Screenshot >>



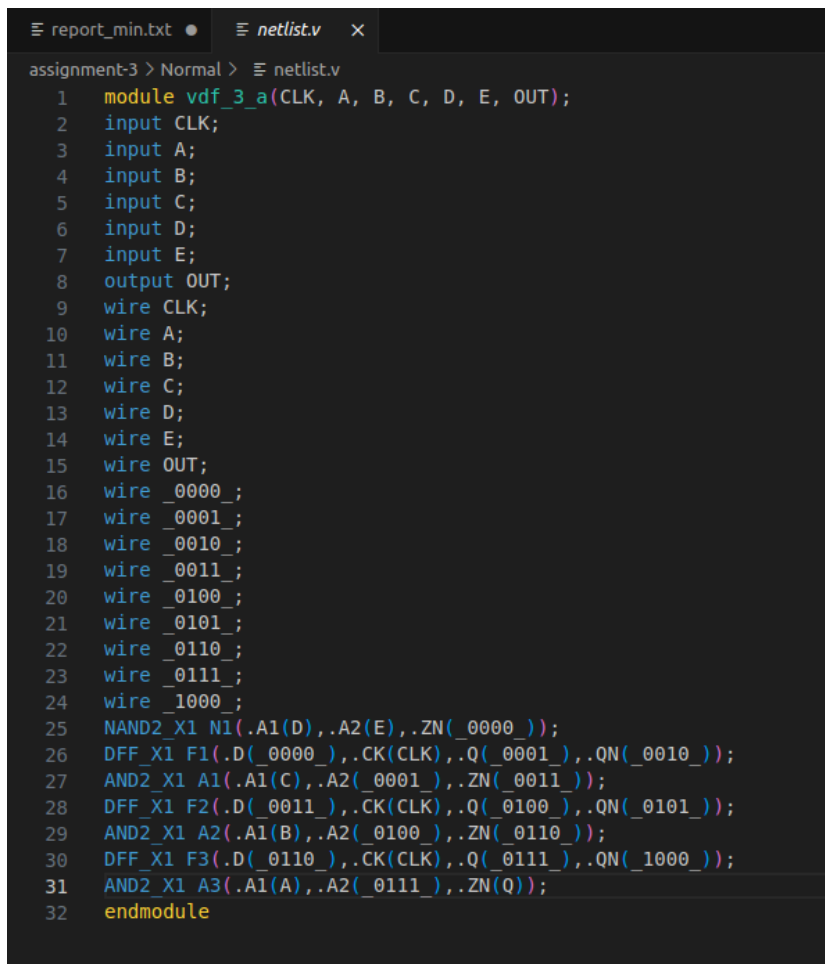
```
bash: /home/animesh/prmp_proj/hclib-light/hclib-install/bin/hclib_setup_env.sh: No such file or directory
animesh@dell-OptiPlex-3040:~/vdf/assignment-3/with_scanCells/shift_mode$ sta --help
OpenSTA 2.5.0 95276f8731 Copyright (c) 2024, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
Usage: sta [-help] [-version] [-no_init] [-exit] cmd_file
       -help          show help and exit
       -version       show version and exit
       -no_init       do not read .sta init file
       -threads count|max use count threads
       -no_splash     do not show the license splash at startup
       -exit          exit after reading cmd_file
       cmd_file       source cmd_file

animesh@dell-OptiPlex-3040:~/vdf/assignment-3/with_scanCells/shift_mode$
```

Q-2 →

Netlist



```
report_min.txt netlist.v
assignment-3 > Normal > netlist.v
1  module vdf_3_a(CLK, A, B, C, D, E, OUT);
2  input CLK;
3  input A;
4  input B;
5  input C;
6  input D;
7  input E;
8  output OUT;
9  wire CLK;
10 wire A;
11 wire B;
12 wire C;
13 wire D;
14 wire E;
15 wire OUT;
16 wire _0000_;
17 wire _0001_;
18 wire _0010_;
19 wire _0011_;
20 wire _0100_;
21 wire _0101_;
22 wire _0110_;
23 wire _0111_;
24 wire _1000_;
25 NAND2_X1 N1(.A1(D),.A2(E),.ZN(_0000_));
26 DFF_X1 F1(.D(_0000_),.CK(CLK),.Q(_0001_),.QN(_0010_));
27 AND2_X1 A1(.A1(C),.A2(_0001_),.ZN(_0011_));
28 DFF_X1 F2(.D(_0011_),.CK(CLK),.Q(_0100_),.QN(_0101_));
29 AND2_X1 A2(.A1(B),.A2(_0100_),.ZN(_0110_));
30 DFF_X1 F3(.D(_0110_),.CK(CLK),.Q(_0111_),.QN(_1000_));
31 AND2_X1 A3(.A1(A),.A2(_0111_),.ZN(Q));
32 endmodule
```

Constraints

```
netlist.sdc x
assignment-3 > Normal > netlist.sdc
1 create_clock -name CLOCK -period 0.2 [get_ports CLK]
2 set_clock_transition 0.03 [get_clocks CLOCK]
3 set_clock_uncertainty 0.05 [get_clocks CLOCK]
4 set_input_delay -max 0.07 -clock CLOCK [get_ports A]
5 set_input_delay -max 0.07 -clock CLOCK [get_ports B]
6 set_input_delay -max 0.07 -clock CLOCK [get_ports C]
7 set_input_delay -max 0.07 -clock CLOCK [get_ports D]
8 set_input_delay -max 0.07 -clock CLOCK [get_ports E]
9 set_output_delay -max 0.15 -clock CLOCK [get_ports OUT]
10 set_load 0.6 [get_ports OUT]
11
```

Sta tcl file

```
sta_script.tcl x
assignment-3 > Normal > sta_script.tcl
1 read_liberty NangateOpenCellLibrary_low_temp.lib
2 read_verilog netlist.v
3 link_design vdf_3_a
4 read_sdc netlist.sdc
5 report_checks -path_delay max -from [get_pins F1/CK] -to [get_pins F2/D] > report_max.txt
6 report_checks -path_delay min -from [get_pins F1/CK] -to [get_pins F2/D] > report_min.txt
7 report_net -connection -verbose _0001 > report_net_load.txt
```

Path delay reports (max, min)= slacks (0.07,0.00) ns

```
sta_script.tcl x report_max.txt x ... report_min.txt x
assignment-3 > Normal > report_max.txt
1 Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK)
2 Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
3 Path Group: CLOCK
4 Path Type: max
5
6 Delay Time Description
7 -----
8 0.00 0.00 clock CLOCK (rise edge)
9 0.00 0.00 clock network delay (ideal)
10 0.00 0.00 ^ F1/CK (DFF_X1)
11 0.04 0.04 ^ F1/Q (DFF_X1)
12 0.02 0.06 ^ A1/ZN (AND2_X1)
13 0.00 0.06 ^ F2/D (DFF_X1)
14 0.00 0.06 data arrival time
15
16 0.20 0.20 clock CLOCK (rise edge)
17 0.00 0.20 clock network delay (ideal)
18 -0.05 0.15 clock uncertainty
19 0.00 0.15 clock reconvergence pessimism
20 0.15 ^ F2/CK (DFF_X1)
21 -0.02 0.13 library setup time
22 0.13 0.13 data required time
23 -----
24 0.13 0.13 data required time
25 -0.06 -0.06 data arrival time
26 -----
27 0.07 0.07 slack (MET)
28

assignment-3 > Normal > report_min.txt
1 Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK)
2 Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
3 Path Group: CLOCK
4 Path Type: min
5
6 Delay Time Description
7 -----
8 0.00 0.00 clock CLOCK (rise edge)
9 0.00 0.00 clock network delay (ideal)
10 0.00 0.00 ^ F1/CK (DFF_X1)
11 0.04 0.04 ^ F1/Q (DFF_X1)
12 0.02 0.06 ^ A1/ZN (AND2_X1)
13 0.00 0.06 ^ F2/D (DFF_X1)
14 0.00 0.06 data arrival time
15
16 0.00 0.00 clock CLOCK (rise edge)
17 0.00 0.00 clock network delay (ideal)
18 0.05 0.05 clock uncertainty
19 0.00 0.05 clock reconvergence pessimism
20 0.05 ^ F2/CK (DFF_X1)
21 0.01 0.06 library hold time
22 0.06 0.06 data required time
23 -----
24 0.06 0.06 data required time
25 -0.06 -0.06 data arrival time
26 -----
27 0.00 0.00 slack (MET)
28
```

Net Report

```
report_net_load.txt x
assignment-3 > Normal > report_net_load.txt
1 Warning: sta_script.tcl line 7, report_net -connections is deprecated.
2 Warning: sta_script.tcl line 7, report_net -verbose is deprecated.
3 Net _0001
4 Pin capacitance: 0.94-0.98
5 Wire capacitance: 0.00
6 Total capacitance: 0.94-0.98
7 Number of drivers: 1
8 Number of loads: 1
9 Number of pins: 2
10
11 Driver pins
12 | F1/Q output (DFF_X1)
13
14 Load pins
15 | A1/A2 input (AND2_X1) 0.94-0.98
16
```

Q-3 →

Netlist

```
report_net_load.txt netlist.v x
assignment-3 > with_scanCells > netlist.v
1  module vdf_3_b(CLK, A, B, C, D, E, SI, SE, OUT, S0);
2  input CLK;
3  input A;
4  input B;
5  input C;
6  input D;
7  input E;
8  input SI;
9  input SE;
10 output OUT;
11 output S0;
12 wire CLK;
13 wire A;
14 wire B;
15 wire C;
16 wire D;
17 wire E;
18 wire SI;
19 wire SE;
20 wire OUT;
21 wire S0;
22 wire _000_;
23 wire _001_;
24 wire _010_;
25 wire _011_;
26 wire _100_;
27 wire _101_;
28 wire _110_;
29 wire _111_;
30 NAND2_X1 N1(.A1(D),.A2(E),.ZN(_000_));
31 SDFF_X1 F1(.D(_000_),.SE(SE),.SI(SI),.CK(CLK),.Q(_001_),.QN(_010_));
32 AND2_X1 A1(.A1(C),.A2(_001_),.ZN(_011_));
33 SDFF_X1 F2(.D(_011_),.SE(SE),.SI(_001_),.CK(CLK),.Q(_100_),.QN(_101_));
34 AND2_X1 A2(.A1(B),.A2(_100_),.ZN(_110_));
35 SDFF_X1 F3(.D(_110_),.SE(SE),.SI(_100_),.CK(CLK),.Q(S0),.QN(_111_));
36 AND2_X1 A3(.A1(A),.A2(S0),.ZN(Q));
37 endmodule
```

Q-4 →

New constraints

```

≡ netlist.sdc X
assignment-3 > with_scanCells > Functional_mode > ≡ netlist.sdc
1  create_clock -name CLOCK -period 0.2 [get_ports CLK]
2  set_clock_transition 0.03 [get_clocks CLOCK]
3  set_clock_uncertainty 0.05 [get_clocks CLOCK]
4  set_input_delay -max 0.07 -clock CLOCK [get_ports SE]
5  set_case_analysis 0 [get_ports SE]
6  set_input_delay -max 0.07 -clock CLOCK [get_ports SI]
7  set_input_delay -max 0.07 -clock CLOCK [get_ports A]
8  set_input_delay -max 0.07 -clock CLOCK [get_ports B]
9  set_input_delay -max 0.07 -clock CLOCK [get_ports C]
10 set_input_delay -max 0.07 -clock CLOCK [get_ports D]
11 set_input_delay -max 0.07 -clock CLOCK [get_ports E]
12 set_output_delay -max 0.15 -clock CLOCK [get_ports OUT]
13 set_output_delay -max 0.15 -clock CLOCK [get_ports S0]
14 set_load 0.6 [get_ports OUT]

```

New tcl script

```

≡ sta_script.tcl X
assignment-3 > with_scanCells > Functional_mode > ≡ sta_script.tcl
1  read_liberty ../NangateOpenCellLibrary_low_temp.lib
2  read_verilog ../netlist.v
3  link_design vdf_3_b
4  read_sdc netlist.sdc
5  report_checks -path_delay max -from [get_pins F1/CK] -to [get_pins F2/D] > report_max.txt
6  report_checks -path_delay min -from [get_pins F1/CK] -to [get_pins F2/D] > report_min.txt
7  report_net -connection -verbose _001 > report_net_load.txt

```

Report (Delay (max,min))

≡ report_max.txt X				≡ report_min.txt X			
assignment-3 > with_scanCells > Functional_mode > ≡ report_max.txt				assignment-3 > with_scanCells > Functional_mode > ≡ report_min.txt			
1	Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK)			1	Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK)		
2	Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)			2	Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)		
3	Path Group: CLOCK			3	Path Group: CLOCK		
4	Path Type: max			4	Path Type: min		
5				5			
6	Delay	Time	Description	6	Delay	Time	Description
7	-----			7	-----		
8	0.00	0.00	clock CLOCK (rise edge)	8	0.00	0.00	clock CLOCK (rise edge)
9	0.00	0.00	clock network delay (ideal)	9	0.00	0.00	clock network delay (ideal)
10	0.00	0.00	^ F1/CK (SDFF_X1)	10	0.00	0.00	^ F1/CK (SDFF_X1)
11	0.03	0.03	v F1/Q (SDFF_X1)	11	0.03	0.03	v F1/Q (SDFF_X1)
12	0.01	0.05	v A1/ZN (AND2_X1)	12	0.01	0.05	v A1/ZN (AND2_X1)
13	0.00	0.05	v F2/D (SDFF_X1)	13	0.00	0.05	v F2/D (SDFF_X1)
14		0.05	data arrival time	14		0.05	data arrival time
15				15			
16	0.20	0.20	clock CLOCK (rise edge)	16	0.00	0.00	clock CLOCK (rise edge)
17	0.00	0.20	clock network delay (ideal)	17	0.00	0.00	clock network delay (ideal)
18	-0.05	0.15	clock uncertainty	18	0.05	0.05	clock uncertainty
19	0.00	0.15	clock reconvergence pessimism	19	0.00	0.05	clock reconvergence pessimism
20		0.15	^ F2/CK (SDFF_X1)	20		0.05	^ F2/CK (SDFF_X1)
21	-0.04	0.11	library setup time	21	0.00	0.05	library hold time
22		0.11	data required time	22		0.05	data required time
23	-----			23	-----		
24		0.11	data required time	24		0.05	data required time
25		-0.05	data arrival time	25		-0.05	data arrival time
26	-----			26	-----		
27		0.07	slack (MET)	27		0.00	slack (MET)
28				28			

Explanation (max,min = 0.06ns,0ns)

In our case the setup slack decreases by 0.1 ns, this happens because for scan cells the setup time increases by 0.02 ns as compared to normal DFF also the ck to ff Delay and decreases from 0.04ns to 0.03ns.

In our case the hold slack almost remains because for scan cells the hold time decreased by 0.01 ns as compared to normal DFF also the ck to ff Delay and decreases from 0.04ns to 0.03ns. (Almost equal amount of delay transition)

Report load on net

```
report_net_load.txt x
assignment-3 > with_scanCells > Functional_mode > report_net_load.txt
1 Warning: sta_script.tcl line 7, report_net -connections is deprecated.
2 Warning: sta_script.tcl line 7, report_net -verbose is deprecated.
3 Net _001_
4 Pin capacitance: 1.85-1.90
5 Wire capacitance: 0.00
6 Total capacitance: 1.85-1.90
7 Number of drivers: 1
8 Number of loads: 2
9 Number of pins: 3
10
11 Driver pins
12 F1/Q output (SDFF_X1)
13
14 Load pins
15 A1/A2 input (AND2_X1) 0.94-0.98
16 F2/SI input (SDFF_X1) 0.91-0.92
17
```

Explanation

Overall capacitance decreases because of two loads (sharing of load) on this net (F1/D to F2/SI), This is also the main reason, i.e the capacitance sharing, which leads to decrease in FF CK to Q delay.

Q-5 →

New constraints

```
netlist.sdc x
assignment-3 > with_scanCells > shift_mode > netlist.sdc
1 create_clock -name CLOCK -period 0.2 [get_ports CLK]
2 set_clock_transition 0.03 [get_clocks CLOCK]
3 set_clock_uncertainty 0.05 [get_clocks CLOCK]
4 set_input_delay -max 0.07 -clock CLOCK [get_ports SE]
5 set_case_analysis 1 [get_ports SE]
6 set_input_delay -max 0.07 -clock CLOCK [get_ports SI]
7 set_input_delay -max 0.07 -clock CLOCK [get_ports A]
8 set_input_delay -max 0.07 -clock CLOCK [get_ports B]
9 set_input_delay -max 0.07 -clock CLOCK [get_ports C]
10 set_input_delay -max 0.07 -clock CLOCK [get_ports D]
11 set_input_delay -max 0.07 -clock CLOCK [get_ports E]
12 set_output_delay -max 0.15 -clock CLOCK [get_ports OUT]
13 set_output_delay -max 0.15 -clock CLOCK [get_ports S0]
14 set_load 0.6 [get_ports OUT]
```

New tcl script

```
sta_script.tcl X
assignment-3 > with_scanCells > shift_mode > sta_script.tcl
1 read_liberty ../NangateOpenCellLibrary_low_temp.lib
2 read_verilog ../netlist.v
3 link_design vdf_3_b
4 read_sdc netlist.sdc
5 report_checks -path_delay max -from [get_pins F1/CK] -to [get_pins F2/SI] > report_max.txt
6 report_checks -path_delay min -from [get_pins F1/CK] -to [get_pins F2/SI] > report_min.txt
7 report_net -connection -verbose _001_ > report_net_load.txt
```

Report load on net

```
report_net_load.txt X
assignment-3 > with_scanCells > shift_mode > report_net_load.txt
1 Warning: sta_script.tcl line 7, report_net -connections is deprecated.
2 Warning: sta_script.tcl line 7, report_net -verbose is deprecated.
3 Net _001_
4 Pin capacitance: 1.85-1.90
5 Wire capacitance: 0.00
6 Total capacitance: 1.85-1.90
7 Number of drivers: 1
8 Number of loads: 2
9 Number of pins: 3
10
11 Driver pins
12 F1/Q output (SDFF_X1)
13
14 Load pins
15 A1/A2 input (AND2_X1) 0.94-0.98
16 F2/SI input (SDFF_X1) 0.91-0.92
17
```

Report (Delay (max,min))

```
report_max.txt X
assignment-3 > with_scanCells > shift_mode > report_max.txt
1 Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK)
2 Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
3 Path Group: CLOCK
4 Path Type: max
5
6 Delay Time Description
7 -----
8 0.00 0.00 clock CLOCK (rise edge)
9 0.00 0.00 clock network delay (ideal)
10 0.00 0.00 ^ F1/CK (SDFF_X1)
11 0.03 0.03 v F1/Q (SDFF_X1)
12 0.00 0.03 v F2/SI (SDFF_X1)
13 0.00 0.03 data arrival time
14
15 0.20 0.20 clock CLOCK (rise edge)
16 0.00 0.20 clock network delay (ideal)
17 -0.05 0.15 clock uncertainty
18 0.00 0.15 clock reconvergence pessimism
19 0.15 0.11 ^ F2/CK (SDFF_X1)
20 -0.04 0.11 library setup time
21 0.11 0.11 data required time
22 -----
23 0.11 0.11 data required time
24 -0.03 0.08 data arrival time
25 -----
26 0.08 0.08 slack (MET)
27
```

```
report_min.txt X
assignment-3 > with_scanCells > shift_mode > report_min.txt
1 Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK)
2 Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
3 Path Group: CLOCK
4 Path Type: min
5
6 Delay Time Description
7 -----
8 0.00 0.00 clock CLOCK (rise edge)
9 0.00 0.00 clock network delay (ideal)
10 0.00 0.00 ^ F1/CK (SDFF_X1)
11 0.03 0.03 v F1/Q (SDFF_X1)
12 0.00 0.03 v F2/SI (SDFF_X1)
13 0.00 0.03 data arrival time
14
15 0.00 0.00 clock CLOCK (rise edge)
16 0.00 0.00 clock network delay (ideal)
17 0.05 0.05 clock uncertainty
18 0.00 0.05 clock reconvergence pessimism
19 0.05 0.05 ^ F2/CK (SDFF_X1)
20 0.00 0.05 library hold time
21 0.05 0.05 data required time
22 -----
23 0.05 0.05 data required time
24 -0.03 0.02 data arrival time
25 -----
26 -0.01 0.02 slack (VIOLATED)
27
```

Explanation (max,min = 0.08ns,-0.01ns)

In both the cases of the setup and hold time analysis we see a change in path: why?

This is because when set to shift mode, scan cells do not use input from D pin whereas they use input from SI pin. As a result, the path through and gate which was used in the previous case doesn't add to delay. Since this path does not have an intermediate combinational logic we see a drop in the path delays as compared to previous slacks.

Thus setup slack increases and hold slack decreases.(in fact gets violated)

To re-run the model , Refer to the Readme.txt

****End of the Report****