VDF Assignment-3 Report
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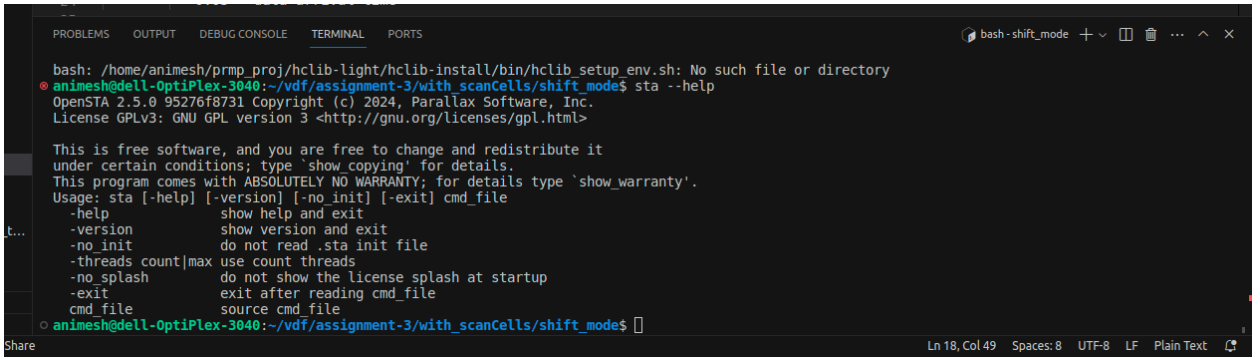
Q1 →

STA Tool Run Screenshot >>



Q-2 →

Netlist

report_min.txt ● netlist.v ×

assignment-3 > Normal > netlist.v

```
1  module vdf_3_a(CLK, A, B, C, D, E, OUT);
2  input CLK;
3  input A;
4  input B;
5  input C;
6  input D;
7  input E;
8  output OUT;
9  wire CLK;
10 wire A;
11 wire B;
12 wire C;
13 wire D;
14 wire E;
15 wire OUT;
16 wire _0000_;
17 wire _0001_;
18 wire _0010_;
19 wire _0011_;
20 wire _0100_;
21 wire _0101_;
22 wire _0110_;
23 wire _0111_;
24 wire _1000_;
25 NAND2_X1 N1(.A1(D),.A2(E),.ZN(_0000_));
26 DFF_X1 F1(.D(_0000_),.CK(CLK),.Q(_0001_),.QN(_0010_));
27 AND2_X1 A1(.A1(C),.A2(_0001_),.ZN(_0011_));
28 DFF_X1 F2(.D(_0011_),.CK(CLK),.Q(_0100_),.QN(_0101_));
29 AND2_X1 A2(.A1(B),.A2(_0100_),.ZN(_0110_));
30 DFF_X1 F3(.D(_0110_),.CK(CLK),.Q(_0111_),.QN(_1000_));
31 AND2_X1 A3(.A1(A),.A2(_0111_),.ZN(Q));
32 endmodule
```

Constraints

netlist.sdc

assignment-3 > Normal > netlist.sdc

```
create_clock -name CLOCK -period 0.2 [get_ports CLK]
set_clock_transition 0.03 [get_clocks CLOCK]
set_clock_uncertainty 0.05 [get_clocks CLOCK]
set_input_delay -max 0.07 -clock CLOCK [get_ports A]
set_input_delay -max 0.07 -clock CLOCK [get_ports B]
set_input_delay -max 0.07 -clock CLOCK [get_ports C]
set_input_delay -max 0.07 -clock CLOCK [get_ports D]
set_input_delay -max 0.07 -clock CLOCK [get_ports E]
set_output_delay -max 0.15 -clock CLOCK [get_ports OUT]
set_load 0.6 [get_ports OUT]

```

Sta tcl file

sta_script.tcl

assignment-3 > Normal > sta_script.tcl

```
read_liberty NangateOpenCellLibrary_low_temp.lib
read_verilog netlist.v
link_design vdf_3_a
read_sdc netlist.sdc
report_checks -path_delay max -from [get_pins F1/CK] -to [get_pins F2/D] > report_max.txt
report_checks -path_delay min -from [get_pins F1/CK] -to [get_pins F2/D] > report_min.txt
report_net -connection -verbose _0001_ > report_net_load.txt
```

Path delay reports (max, min)= slacks (0.07,0.00) ns

report_max.txt

assignment-3 > Normal > report_max.txt

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
Path Group: CLOCK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFF_X1)
   0.04    0.04 ^ F1/Q (DFF_X1)
   0.02    0.06 ^ A1/ZN (AND2_X1)
   0.00    0.06 ^ F2/D (DFF_X1)
           0.06   data arrival time

   0.20    0.20   clock CLOCK (rise edge)
   0.00    0.20   clock network delay (ideal)
  -0.05    0.15   clock uncertainty
   0.00    0.15   clock reconvergence pessimism
           0.15 ^ F2/CK (DFF_X1)
  -0.02    0.13   library setup time
           0.13   data required time
---------------------------------------------------------
           0.13   data required time
          -0.06   data arrival time
---------------------------------------------------------
           0.07   slack (MET)
```

report_min.txt

assignment-3 > Normal > report_min.txt

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
Path Group: CLOCK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFF_X1)
   0.04    0.04 ^ F1/Q (DFF_X1)
   0.02    0.06 ^ A1/ZN (AND2_X1)
   0.00    0.06 ^ F2/D (DFF_X1)
           0.06   data arrival time

   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.05    0.05   clock uncertainty
   0.00    0.05   clock reconvergence pessimism
           0.05 ^ F2/CK (DFF_X1)
   0.01    0.06   library hold time
           0.06   data required time
---------------------------------------------------------
           0.06   data required time
          -0.06   data arrival time
---------------------------------------------------------
           0.00   slack (MET)
```

Net Report

report_net_load.txt

assignment-3 > Normal > report_net_load.txt

```
Warning: sta_script.tcl line 7, report_net -connections is deprecated.
Warning: sta_script.tcl line 7, report_net -verbose is deprecated.
Net _0001_
 Pin capacitance: 0.94-0.98
 Wire capacitance: 0.00
 Total capacitance: 0.94-0.98
 Number of drivers: 1
 Number of loads: 1
 Number of pins: 2

Driver pins
 F1/Q output (DFF_X1)

Load pins
 A1/A2 input (AND2_X1) 0.94-0.98
```

Q-3 →

Netlist

report_net_load.txt | netlist.v

assignment-3 > with_scanCells > netlist.v

```
module vdf_3_b(CLK, A, B, C, D, E, SI, SE, OUT, SO);
input CLK;
input A;
input B;
input C;
input D;
input E;
input SI;
input SE;
output OUT;
output SO;
wire CLK;
wire A;
wire B;
wire C;
wire D;
wire E;
wire SI;
wire SE;
wire OUT;
wire SO;
wire _000_;
wire _001_;
wire _010_;
wire _011_;
wire _100_;
wire _101_;
wire _110_;
wire _111_;
NAND2_X1 N1(.A1(D),.A2(E),.ZN(_000_));
SDFF_X1 F1(.D(_000_),.SE(SE),.SI(SI),.CK(CLK),.Q(_001_),.QN(_010_));
AND2_X1 A1(.A1(C),.A2(_001_),.ZN(_011_));
SDFF_X1 F2(.D(_011_),.SE(SE),.SI(_001_),.CK(CLK),.Q(_100_),.QN(_101_));
AND2_X1 A2(.A1(B),.A2(_100_),.ZN(_110_));
SDFF_X1 F3(.D(_110_),.SE(SE),.SI(_100_),.CK(CLK),.Q(SO),.QN(_111_));
AND2_X1 A3(.A1(A),.A2(SO),.ZN(Q));
endmodule
```

Q-4 →

New constraints

netlist.sdc

assignment-3 > with_scanCells > Functional_mode > netlist.sdc

```
create_clock -name CLOCK -period 0.2 [get_ports CLK]
set_clock_transition 0.03 [get_clocks CLOCK]
set_clock_uncertainty 0.05 [get_clocks CLOCK]
set_input_delay -max 0.07 -clock CLOCK [get_ports SE]
set_case_analysis 0 [get_ports SE]
set_input_delay -max 0.07 -clock CLOCK [get_ports SI]
set_input_delay -max 0.07 -clock CLOCK [get_ports A]
set_input_delay -max 0.07 -clock CLOCK [get_ports B]
set_input_delay -max 0.07 -clock CLOCK [get_ports C]
set_input_delay -max 0.07 -clock CLOCK [get_ports D]
set_input_delay -max 0.07 -clock CLOCK [get_ports E]
set_output_delay -max 0.15 -clock CLOCK [get_ports OUT]
set_output_delay -max 0.15 -clock CLOCK [get_ports SO]
set_load 0.6 [get_ports OUT]
```

New tcl script

sta_script.tcl

assignment-3 > with_scanCells > Functional_mode > sta_script.tcl

```
read_liberty ../NangateOpenCellLibrary_low_temp.lib
read_verilog ../netlist.v
link_design vdf_3_b
read_sdc netlist.sdc
report_checks -path_delay max -from [get_pins F1/CK] -to [get_pins F2/D] > report_max.txt
report_checks -path_delay min -from [get_pins F1/CK] -to [get_pins F2/D] > report_min.txt
report_net -connection -verbose _001_ > report_net_load.txt
```

Report (Delay (max,min))

report_max.txt

assignment-3 > with_scanCells > Functional_mode > report_max.txt

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
Path Group: CLOCK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (SDFF_X1)
   0.03    0.03 v F1/Q (SDFF_X1)
   0.01    0.05 v A1/ZN (AND2_X1)
   0.00    0.05 v F2/D (SDFF_X1)
           0.05   data arrival time

   0.20    0.20   clock CLOCK (rise edge)
   0.00    0.20   clock network delay (ideal)
  -0.05    0.15   clock uncertainty
   0.00    0.15   clock reconvergence pessimism
           0.15 ^ F2/CK (SDFF_X1)
  -0.04    0.11   library setup time
           0.11   data required time
---------------------------------------------------------
           0.11   data required time
          -0.05   data arrival time
---------------------------------------------------------
           0.07   slack (MET)
```

report_min.txt

assignment-3 > with_scanCells > Functional_mode > report_min.txt

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
Path Group: CLOCK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (SDFF_X1)
   0.03    0.03 v F1/Q (SDFF_X1)
   0.01    0.05 v A1/ZN (AND2_X1)
   0.00    0.05 v F2/D (SDFF_X1)
           0.05   data arrival time

   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.05    0.05   clock uncertainty
   0.00    0.05   clock reconvergence pessimism
           0.05 ^ F2/CK (SDFF_X1)
   0.00    0.05   library hold time
           0.05   data required time
---------------------------------------------------------
           0.05   data required time
          -0.05   data arrival time
---------------------------------------------------------
           0.00   slack (MET)
```

Explanation (max,min = 0.06ns,0ns)

In our case the setup slack decreases by 0.1 ns, this happens because for scan cells the setup time increases by 0.02 ns as compared to normal DFF also the ck to ff Delay and decreases from 0.04ns to 0.03ns.

In our case the hold slack almost remains because for scan cells the hold time decreased by 0.01 ns as compared to normal DFF also the ck to ff Delay and decreases from 0.04ns to 0.03ns. (Almost equal amount of delay transition)

Report load on net

report_net_load.txt

assignment-3 > with_scanCells > Functional_mode > report_net_load.txt

```
Warning: sta_script.tcl line 7, report_net -connections is deprecated.
Warning: sta_script.tcl line 7, report_net -verbose is deprecated.
Net _001_
 Pin capacitance: 1.85-1.90
 Wire capacitance: 0.00
 Total capacitance: 1.85-1.90
 Number of drivers: 1
 Number of loads: 2
 Number of pins: 3

Driver pins
 F1/Q output (SDFF_X1)

Load pins
 A1/A2 input (AND2_X1) 0.94-0.98
 F2/SI input (SDFF_X1) 0.91-0.92

```

Explanation

Overall capacitance decreases because of two loads (sharing of load) on this net (F1/D to F2/SI), This is also the main reason, i.e the capacitance sharing, which leads to decrease in FF CK to Q delay.

Q-5 →

New constraints

netlist.sdc

assignment-3 > with_scanCells > shift_mode > netlist.sdc

```
create_clock -name CLOCK -period 0.2 [get_ports CLK]
set_clock_transition 0.03 [get_clocks CLOCK]
set_clock_uncertainty 0.05 [get_clocks CLOCK]
set_input_delay -max 0.07 -clock CLOCK [get_ports SE]
set_case_analysis 1 [get_ports SE]
set_input_delay -max 0.07 -clock CLOCK [get_ports SI]
set_input_delay -max 0.07 -clock CLOCK [get_ports A]
set_input_delay -max 0.07 -clock CLOCK [get_ports B]
set_input_delay -max 0.07 -clock CLOCK [get_ports C]
set_input_delay -max 0.07 -clock CLOCK [get_ports D]
set_input_delay -max 0.07 -clock CLOCK [get_ports E]
set_output_delay -max 0.15 -clock CLOCK [get_ports OUT]
set_output_delay -max 0.15 -clock CLOCK [get_ports SO]
set_load 0.6 [get_ports OUT]
```

New tcl script

sta_script.tcl

assignment-3 > with_scanCells > shift_mode > sta_script.tcl

```
read_liberty ../NangateOpenCellLibrary_low_temp.lib
read_verilog ../netlist.v
link_design vdf_3_b
read_sdc netlist.sdc
report_checks -path_delay max -from [get_pins F1/CK] -to [get_pins F2/SI] > report_max.txt
report_checks -path_delay min -from [get_pins F1/CK] -to [get_pins F2/SI] > report_min.txt
report_net -connection -verbose _001_ > report_net_load.txt
```

Report load on net

report_net_load.txt

assignment-3 > with_scanCells > shift_mode > report_net_load.txt

```
Warning: sta_script.tcl line 7, report_net -connections is deprecated.
Warning: sta_script.tcl line 7, report_net -verbose is deprecated.
Net _001_
 Pin capacitance: 1.85-1.90
 Wire capacitance: 0.00
 Total capacitance: 1.85-1.90
 Number of drivers: 1
 Number of loads: 2
 Number of pins: 3

Driver pins
 F1/Q output (SDFF_X1)

Load pins
 A1/A2 input (AND2_X1) 0.94-0.98
 F2/SI input (SDFF_X1) 0.91-0.92

```

Report (Delay (max,min))

report_max.txt

assignment-3 > with_scanCells > shift_mode > report_max.txt

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
Path Group: CLOCK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (SDFF_X1)
   0.03    0.03 v F1/Q (SDFF_X1)
   0.00    0.03 v F2/SI (SDFF_X1)
           0.03   data arrival time

   0.20    0.20   clock CLOCK (rise edge)
   0.00    0.20   clock network delay (ideal)
  -0.05    0.15   clock uncertainty
   0.00    0.15   clock reconvergence pessimism
           0.15 ^ F2/CK (SDFF_X1)
  -0.04    0.11   library setup time
           0.11   data required time
---------------------------------------------------------
           0.11   data required time
          -0.03   data arrival time
---------------------------------------------------------
           0.08   slack (MET)

```

report_min.txt

assignment-3 > with_scanCells > shift_mode > report_min.txt

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by CLOCK
Endpoint: F2 (rising edge-triggered flip-flop clocked by CLOCK)
Path Group: CLOCK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (SDFF_X1)
   0.03    0.03 v F1/Q (SDFF_X1)
   0.00    0.03 v F2/SI (SDFF_X1)
           0.03   data arrival time

   0.00    0.00   clock CLOCK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.05    0.05   clock uncertainty
   0.00    0.05   clock reconvergence pessimism
           0.05 ^ F2/CK (SDFF_X1)
   0.00    0.05   library hold time
           0.05   data required time
---------------------------------------------------------
           0.05   data required time
          -0.03   data arrival time
---------------------------------------------------------
          -0.01   slack (VIOLATED)

```

Explanation (max,min = 0.08ns,-0.01ns)
In both the cases of the setup and hold time analysis we see a change in path: why? This is because when set to shift mode, scan cells do not use input from D pin whereas they use input from SI pin. As a result, the path through and gate which was used in the previous case doesn't add to delay. Since this path does not have an intermediate combinational logic we see a drop in the path delays as compared to previous slacks. Thus setup slack increases and hold slack decreases.(in fact gets violated)

To re-run the model , Refer to the Readme.txt

End of the Report