VDF Group Project: Part II

Objective

The objective of this part of the project is to gain a hands-on experience on the state-of-the-art CAD tool used for Physical Design and understanding various trade-offs that are involved in Physical Design. The focus should not only be on running of the tools, but also on the analysis/interpretation of the results.

This project is a continuation of VDF Group Project: Part I.

Read the following instructions carefully. Marks may be deducted if the instructions are not followed.

Problem Solving

- This assignment will be done in groups as in VDF Group Project: Part I
- Input used in VDF Group Project: Part II is the same netlist which was generated after Scan Cell Insertion in VDF Group Project: Part I.
- Keep focus on the objective mentioned above and try fulfilling this objective in the best possible manner. Evaluation will be based on how good this objective is fulfilled by the student. **Note that for evaluation your interpretation/analysis of the result is very important.**

Choice of Tools

Use Cadence Innovus for Physical Design

Design Steps

Following design steps need to be completed in this Assignment

1. Floorplanning
2. Power Network Design
3. Placement
4. Clock-Tree Synthesis
5. Routing
6. Writing out final GDS

   You need to perform these steps for the following two conditions:

   1. Floorplanning is done with small utilization (say 0.5) or large die area
   2. Floorplanning is done with large utilization (say 0.8) or small die area

You should choose reasonably tight timing constraint.

Submission Requirements

Two files need to be submitted:
1. One PDF file
2. One Zipped/tarred (archived) files

You should also keep your setup ready for a demo throughout the VDF course. Your setup may be archived for future use.

The first few pages of the PDF file should contain the following:

1. Your interpretation of the results obtained in various steps of Physical Design (Timing/Area/Power trade-offs)
2. Your interpretation of the routability on the change in floorplan.

(The above description should be in your own words, citing the observations made in your design).

For each of the above two floorplans you need to report the following in the PDF file. These information are the minimum information that you need to provide. You can give additional information that you consider important for analysing the results.

Design Step	Information that should be contained in PDF
Before starting Physical Design	• Timing report of Worst Path with analysis of each component and how it is computed. Explain the effect of slew, load, positive/negative unate-ness, PBA/GBA in the computation of timing of each stage. • Area of Standard Cells (breakup of different kinds of cells such as buffers/inverters/flip-flops/other-combo-cells) • Power
After Placement	• Timing report of Worst Path with analysis of each component and how it is computed. Explain the effect of placement on timing. • Area of Standard Cells (breakup of different kinds of cells such as buffers/inverters/flip-flops/other-combo-cells) • Power • Snap-shot of layout of design and connectivity showing Fly-Lines
After Clock Tree Synthesis	• Timing report of Worst Path with analysis of each component and how it is computed. Explain the effect of the timing of the clock-path on overall slack. • Area of Standard Cells (breakup of different kinds of cells such as buffers/inverters/flip-flops/other-combo-cells) • Power • Snap-shot of layout of design showing Clock-Tree

After Detailed Routing	• Timing report of Worst Path. Explain the effect of different metal layers on the timing of the path.
	• Area of Standard Cells (breakup of different kinds of cells such as buffers/inverters/flip-flops/other-combo-cells)
	• Power
	• Snap-shot of layout of design and connectivity showing different metal layers

In the Zipped/tarred (archived) files following should be uploaded:

1. The command file (TCL script) that was used. If you have used GUI, put all the commands corresponding to the GUI operations in the command file.
2. All the logfiles
3. GDS output of the design

Library to be used

Use the same library that was used in VDF Group Project: Part I. Use the LEF files corresponding to the library used in VDF Group Project: Part I. In case the library used in Project Part I does not have physical information, you can change the library.

Doubts

All doubts/confusion can be cleared by email.

Plagiarism/Cheating

Institute rule will apply.