Memristor Overview

Prepared by:
Sherief Fathi Ibrahim
Lecturer Assistant – Faculty of Engineering (SCU)

Outline

- What is Memristor?
- Basic Operation
- Why Memristor?
- Memristor Fabrication
- Memristor Modeling & Emulating
- Applications of Memristors in
  a) Memories
  b) Logic and FPGA
  c) Neural Networks
  d) Analog circuits

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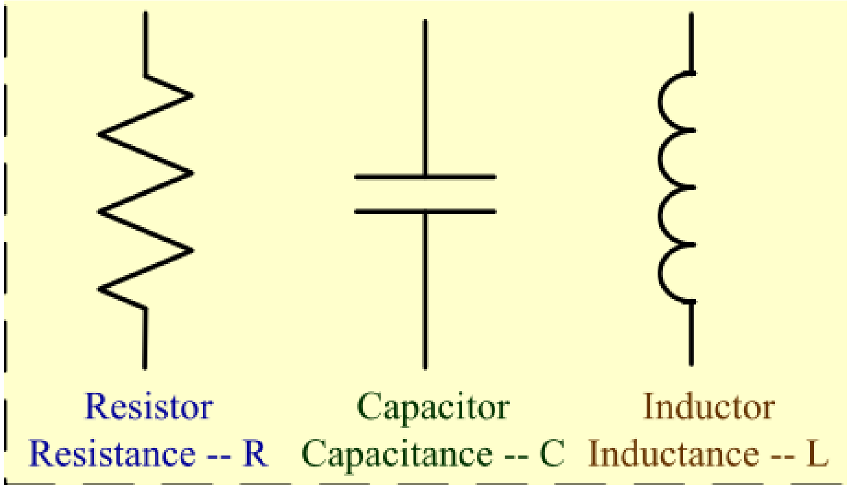
What is Memristor?

Fundamental passive elements:

Resistor (R)

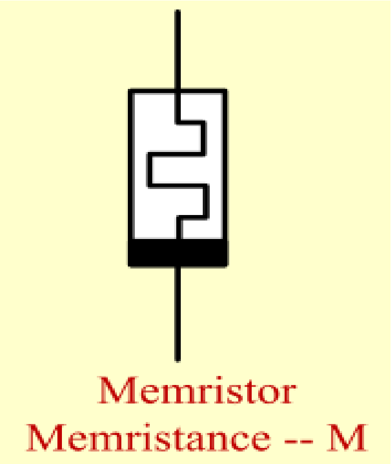
Inductor (L)

Capacitor (C)

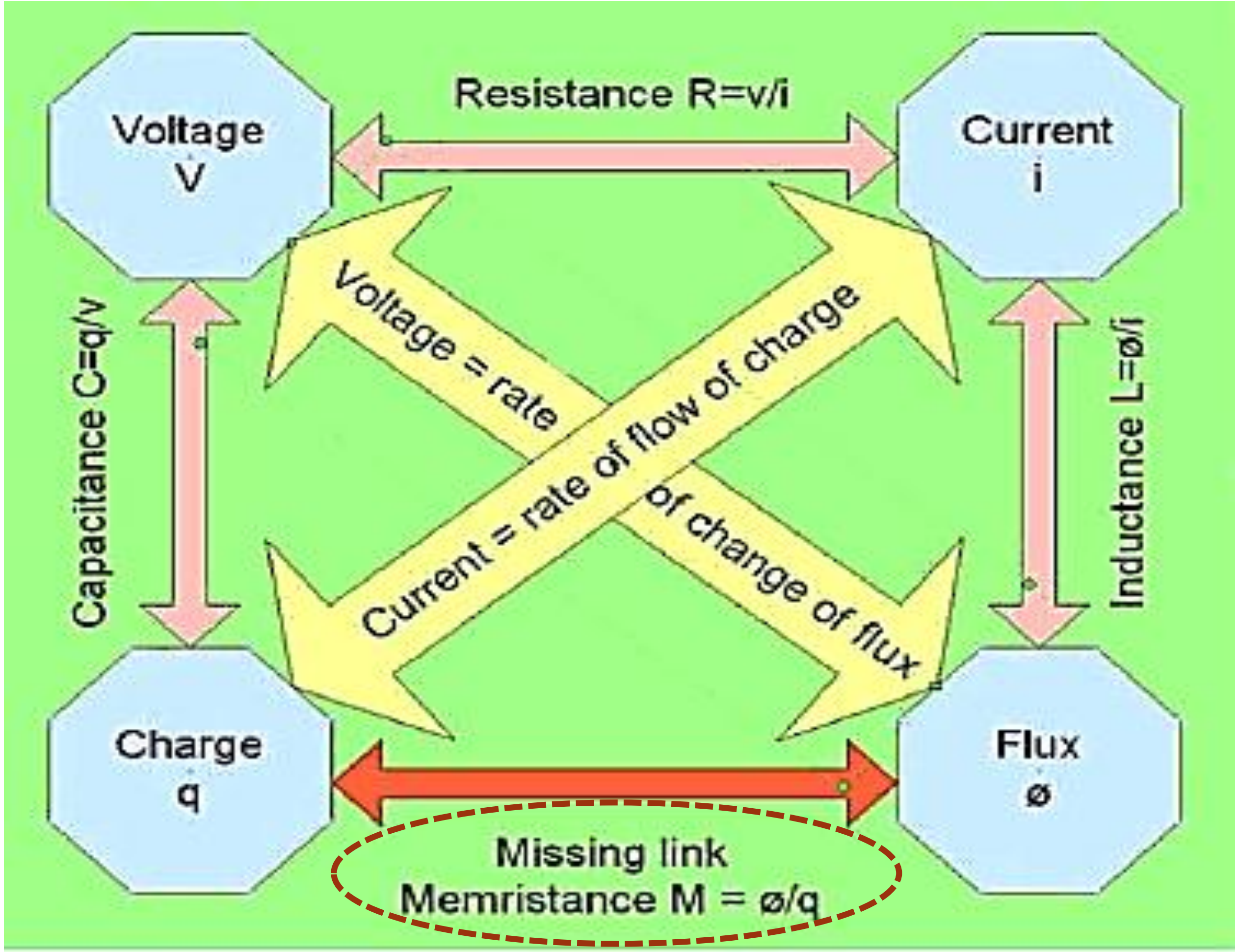


In 1971, Professor Leon predicted that there should be a fourth fundamental element:

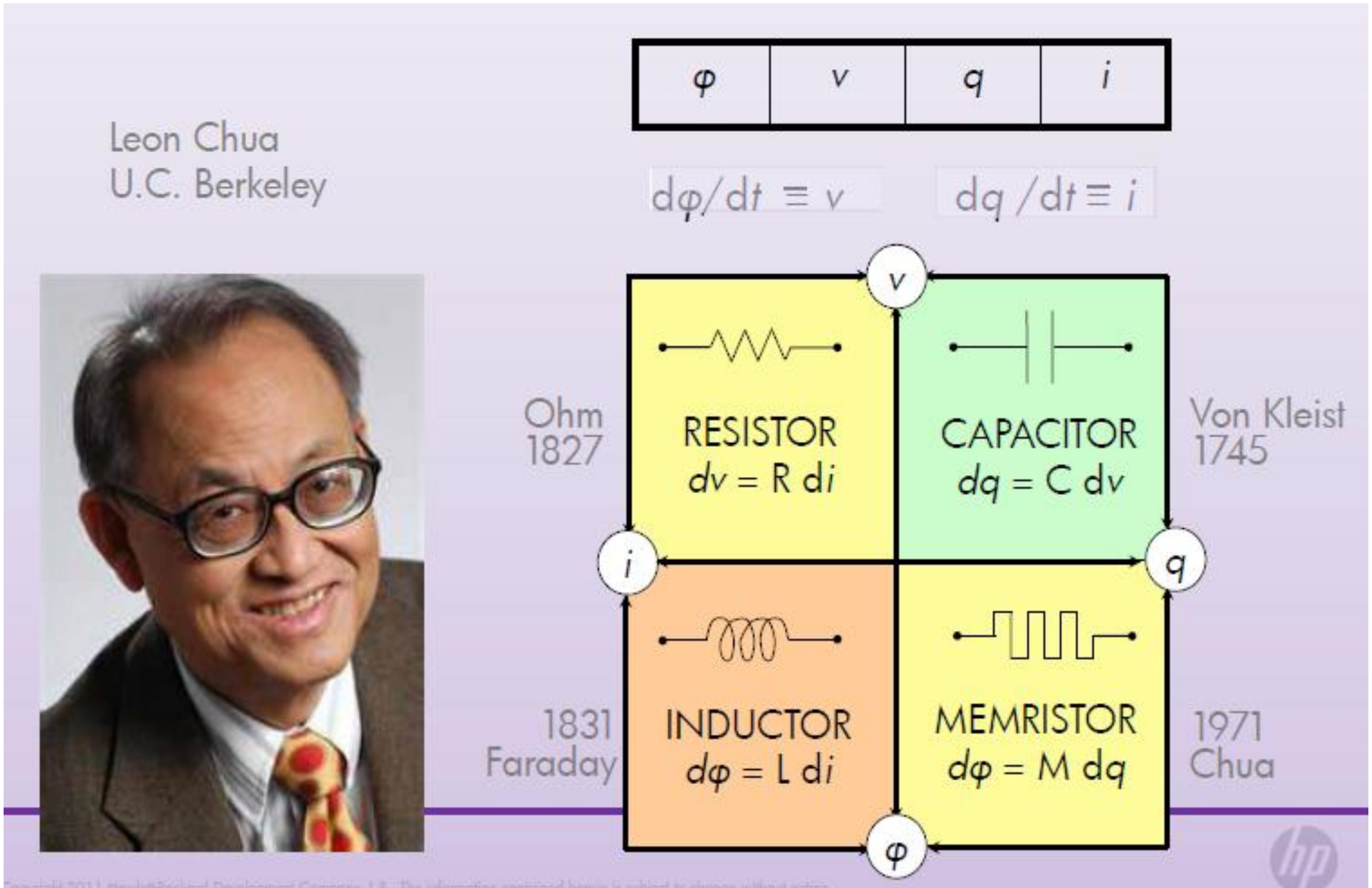
Memristor (M)



What is Memristor?



What is Memristor?



What is Memristor?

Memristor combines the behavior of a memory and a resistor:

(i.e. memory+resistor)

The first fabricated devices exhibiting the characteristics of a memristor:

(by HP labs in 2008)

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Basic Operation

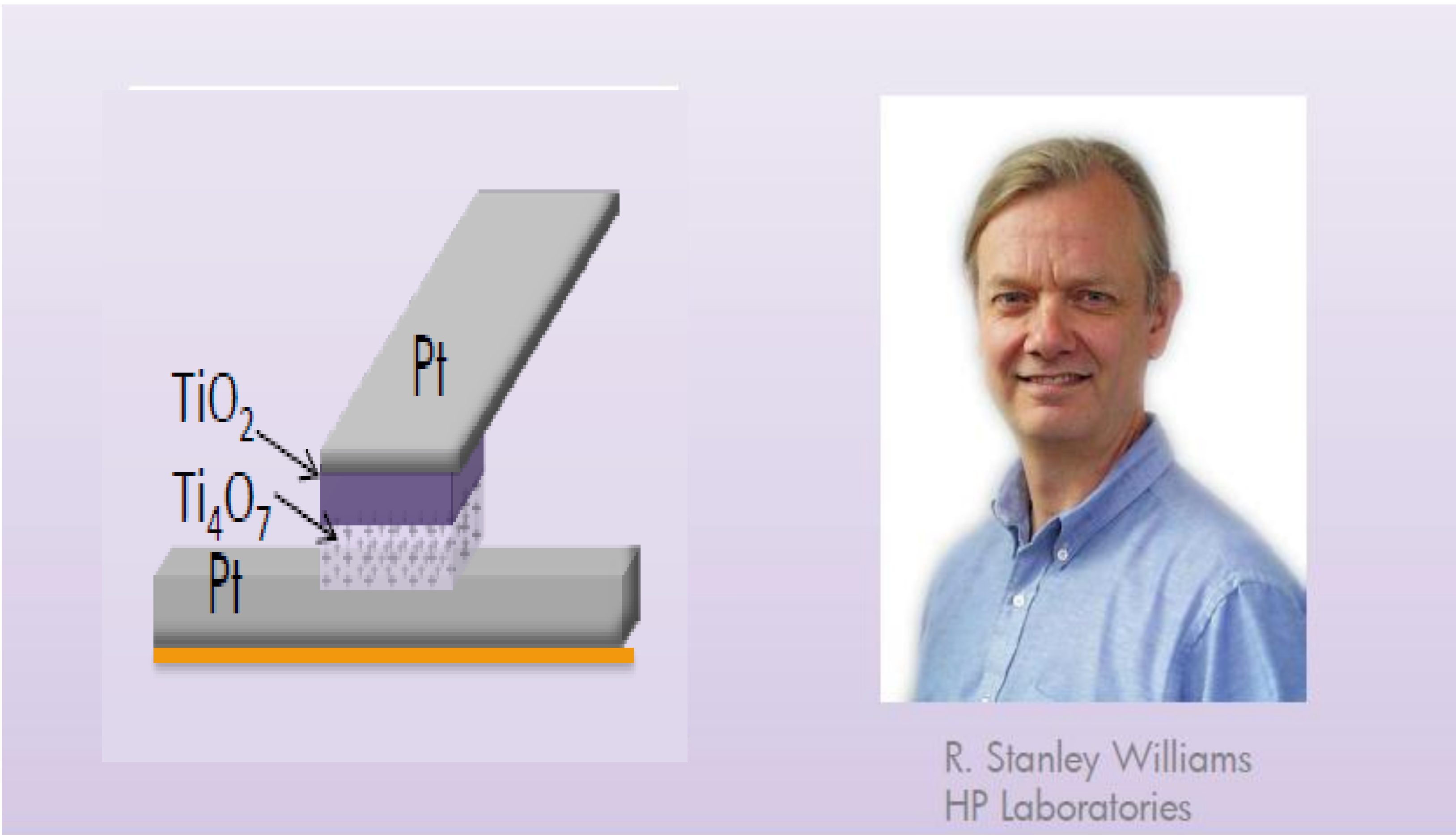
- **The memristor-with memristance M- provides a relation between charge and flux :**

$$d\varphi = M\,dq$$

Memristance(M): is a property of the memristor

The Memristor: Found

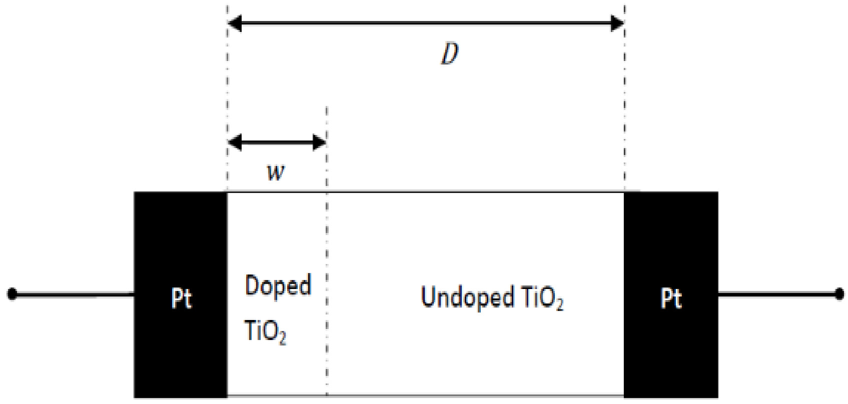
- Reduced to Practice in 2008 by HP Labs:

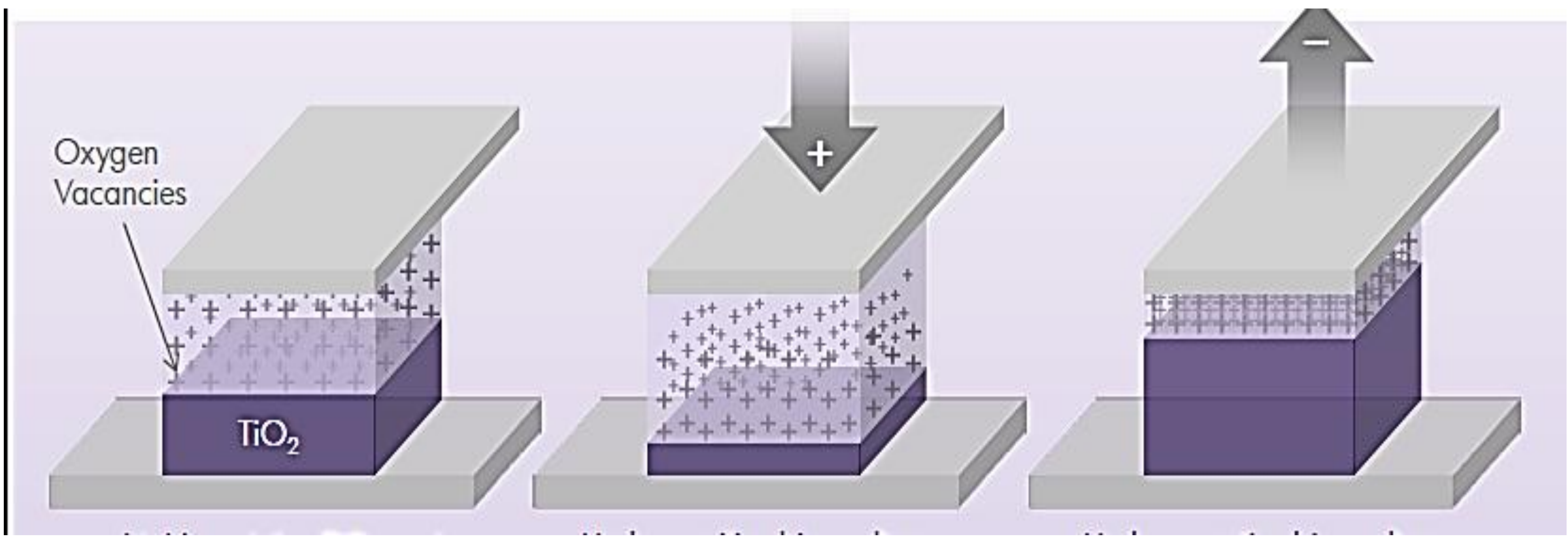


Basic Operation

- **<u>HP memristor:</u>**

  very thin film of titanium dioxide (TiO_{2-x}) between two platinum(Pt) plates





Basic Operation

- **When the charge flows in one direction through a circuit:**

(the resistance of the memristor increases)

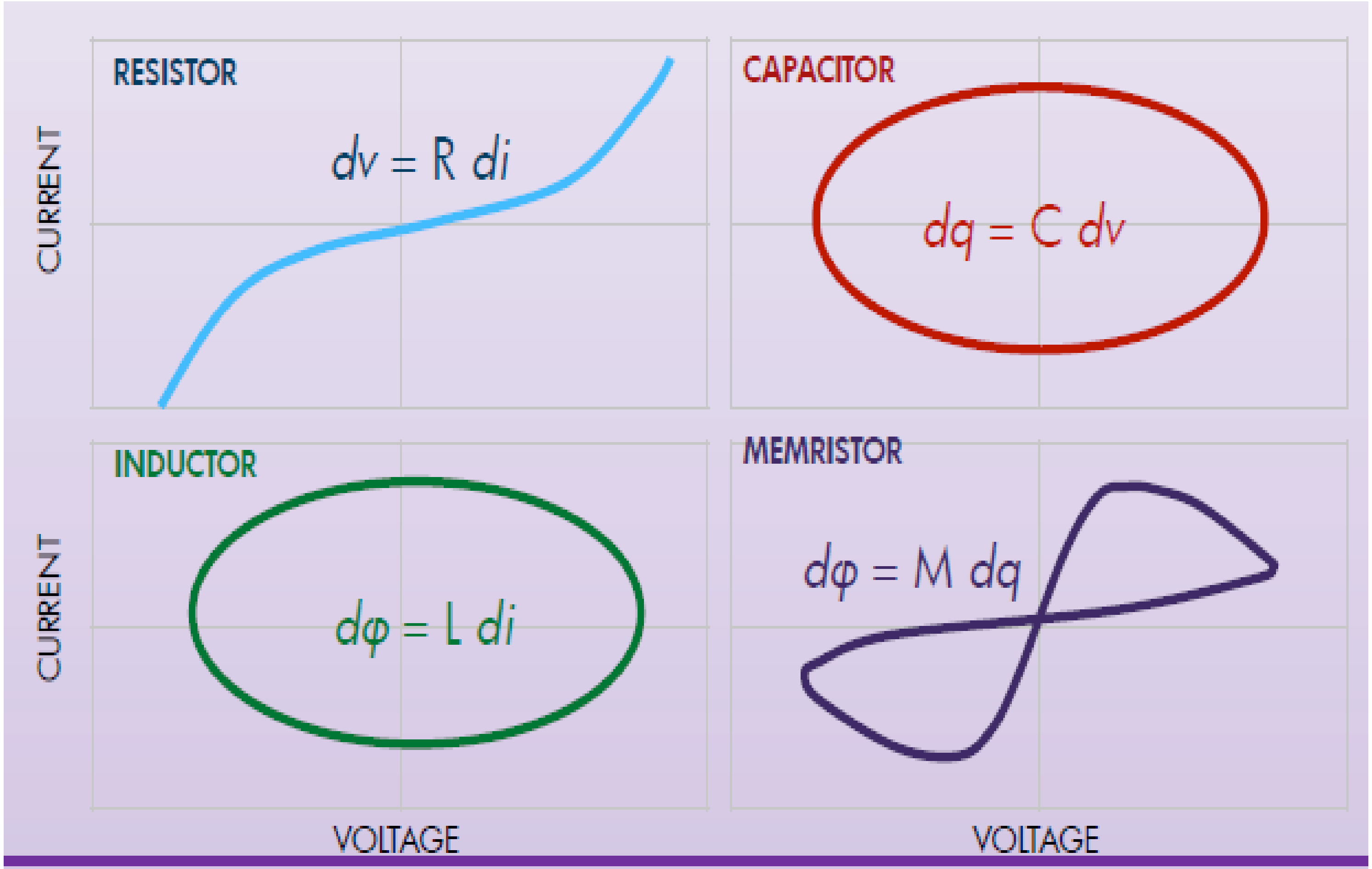
- **when the charge flows in the opposite direction in the circuit:**

(the resistance of the memristor decreases)

- **Thus, we can say that the memristor "remembers" the history of the applied voltage on it .**

which give it the name "memory-resistor"

Unique I-V characteristic:



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Why Memristor?

There are many advantageous of Memristor that makes it a very promising candidate in the future of electronic design:

1. The property of "**remembering**" input can be used in many innovated circuits and memory devices.
2. Memristor can be designed in the **metal layer over chips** and thus save the area on chip.
3. Ability of **combining** logic operation with memory cells on the same chip, and in different places through the chip.
4. It can act as a **configurable switch** in FPGA chips .

Reliable supply of scalable memory technology

FLASH scalability is approaching it's limit

Multi-level cells have low realistic endurance

DRAM is fast approaching their limit also

DRAM architectures and circuitry are adapted to

25 fF cell capacitance

Shrinking geometries threaten industry ability to maintain 25fF

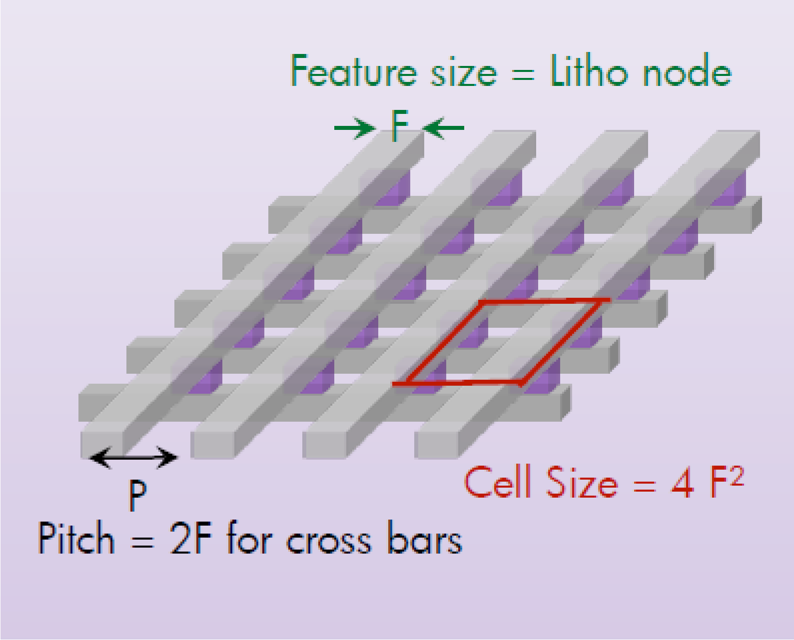
Taller cell capacitor / Thinner cell dielectric<32 nm:

50:1 aspect ratio / < 3 Angstroms

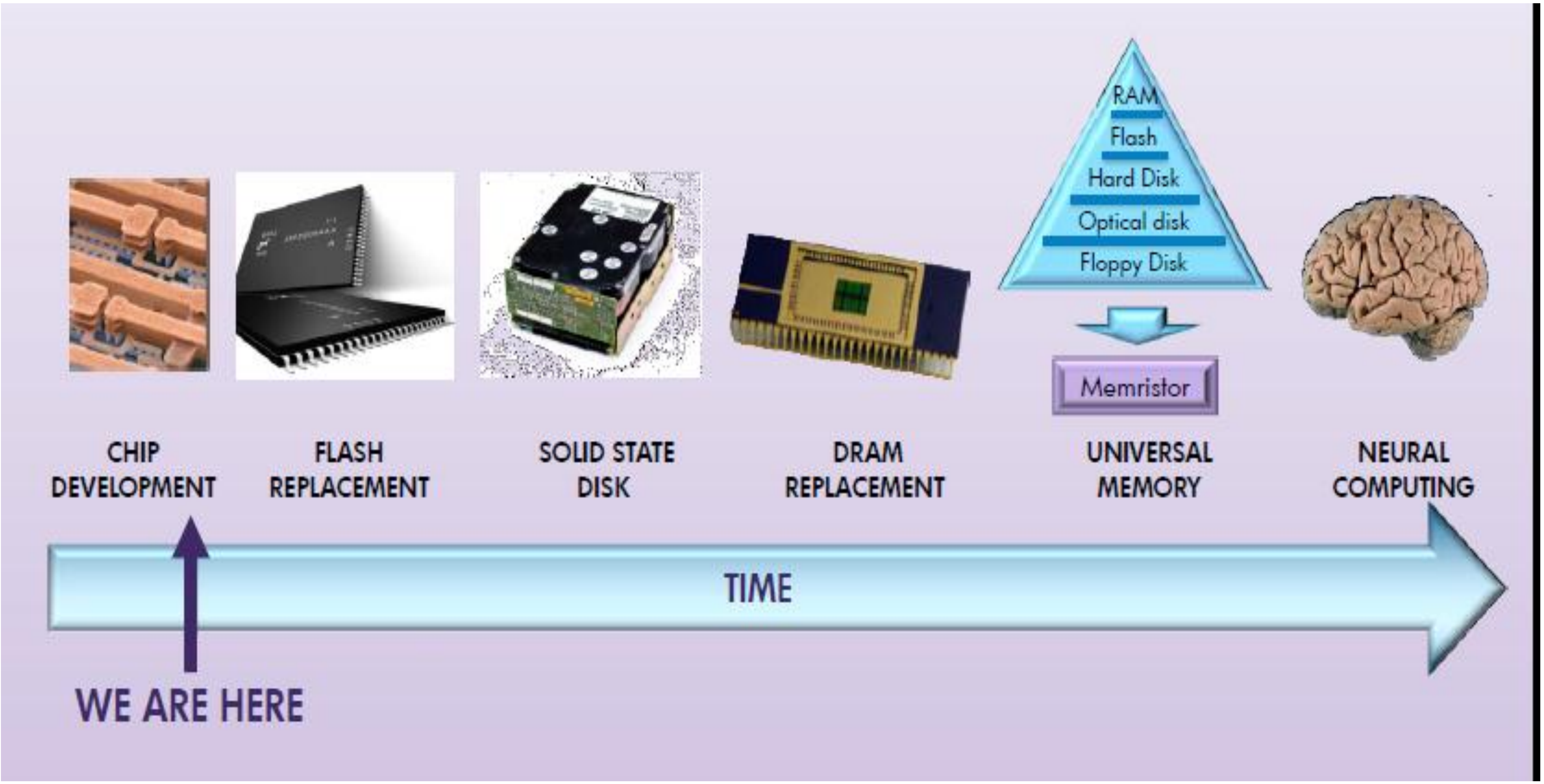
Currently no physical mechanism to create such large trenches with such high precision

Enables true crossbar structures

- **Does not require transistors or other access devices**
- **Removes Silicon requirement**
- **Stack arrays on top of each other:**
- **cell sizes < 4F^2**
- **Improve density**
- **Reduce power consumption**
- **Reduce total area**



HP memristor opportunities



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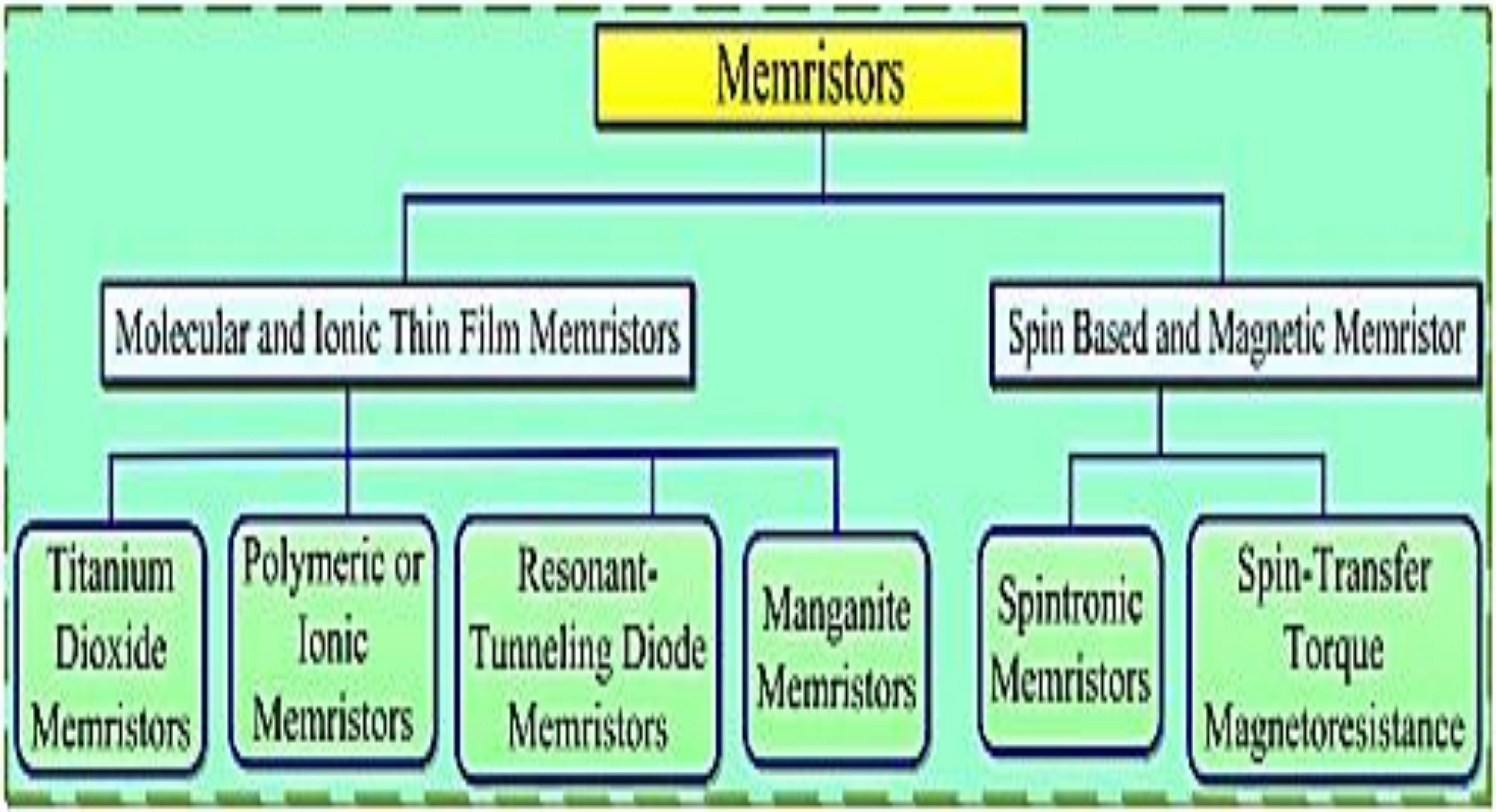
Memristor Fabrication



Memristor Fabrication

Molecular and Ionic Thin Film memristors:

This type of memristors mainly depends on thin film atomic lattices of different materials that shows hysteresis under the application of charge.

- **Titanium Dioxide Memristor:**
- **Polymeric Memristor**
- **Ferroelectric Memristor**

Polymeric Memristor

- **In 2004, Krieger and Spitzer described dynamic doping of polymer and inorganic dielectric-like materials to construct Polymeric memristor for nonvolatile memories.**
- **They used a passive layer between electrode and active thin films, which enhanced the extraction of ions from the electrode.**

Ferroelectric Memristor

- **The ferroelectric memristor is based on a thin ferroelectric barrier sandwiched between two metallic electrodes.**
- **Switching the polarization of the ferroelectric material by applying a positive or negative voltage across the junction can lead to a two order of magnitude resistance variation: $R_{OFF} >> R_{ON}$ (an effect called Tunnel Electro-Resistance).**
- **In general, the polarization does not switch abruptly. The reversal occurs gradually through the nucleation and growth of ferroelectric domains with opposite polarization.**

Memristor Fabrication

Spin-based Memristors:

- **In one device resistance occurs when the spin of electrons in one section of the device points in a different direction from those in another section, creating a boundary between the two sections called a "domain wall".**
- **Electrons flowing into the device have a certain spin, which alters the device's magnetization state.**
- **Changing the magnetization of the device moves the domain wall and changes its resistance.**

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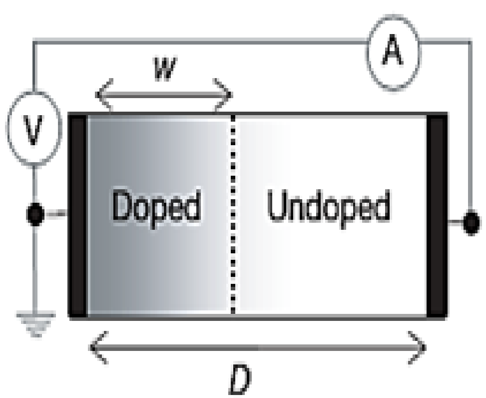
Memristor Modeling & Emulating

Linear Ion Drift Model

- Based on the HP memristor
- A **uniform electric field** across the device is assumed; thus, there is a **linear relationship** between drift–diffusion velocity and the net electric field.

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t)$$

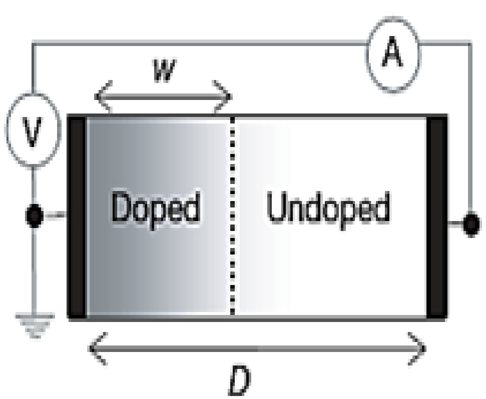


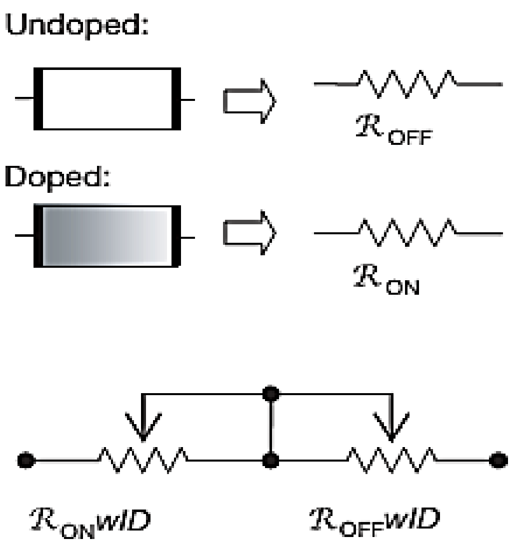
Memristor Modeling & Emulating

- According to the linear ion drift; the memristor can be modelled as a coupled variable-resistor mode
- $v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t)$

where Ron & R_{OFF} are the equivalent resistance of the memristor when the whole device is undoped & the whole device is doped respectively.

- $M(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2} q(t)\right)$





Memristor Modeling & Emulating

Nonlinear Ion Drift Model

- **The nanometre dimensions of memristor causes a high electric field with only applying a few volts.**
- **The electric field can easily exceed 10^6V/cm, and it is reasonable to expect a high nonlinearity in the ionic drift-diffusion.**
- **To consider this nonlinearity in the state equation different papers proposed different 'window functions F(w/D)' multiplied by the right-hand side of the state equation.**

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t) F\left(\frac{w}{D}\right)$$

Memristor Modeling & Emulating

Window function

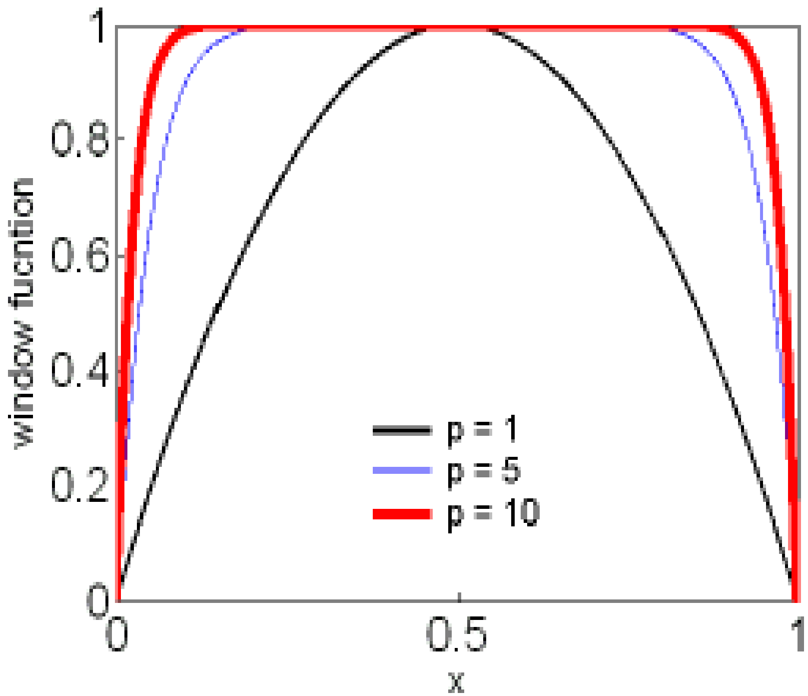


Fig. 2. Plot of non-linear window function proposed by Joglekar *et al.* for $p = 1, 5$, and 10.

$$f(x) = 1 - (2x - 1)^{2p}$$

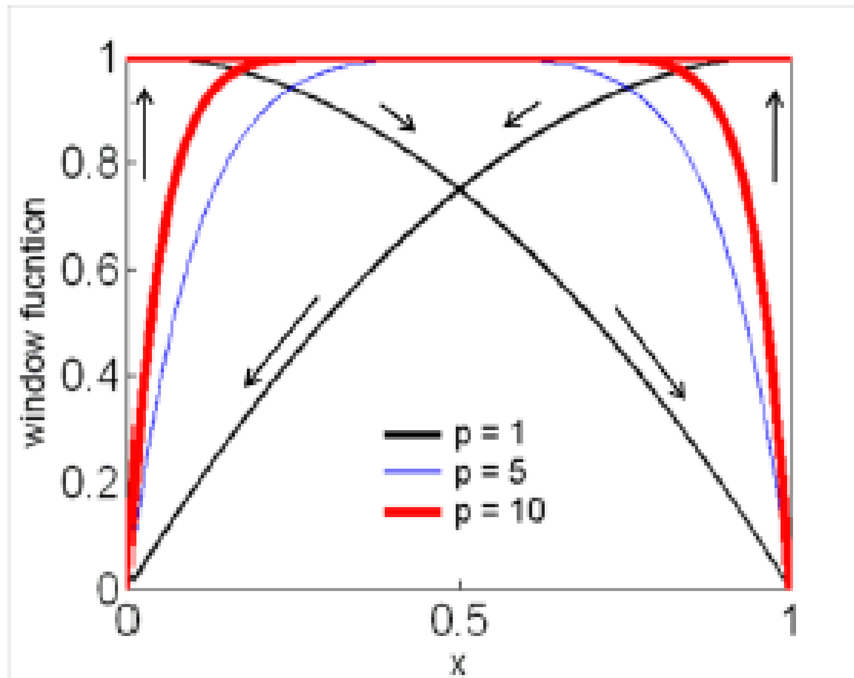


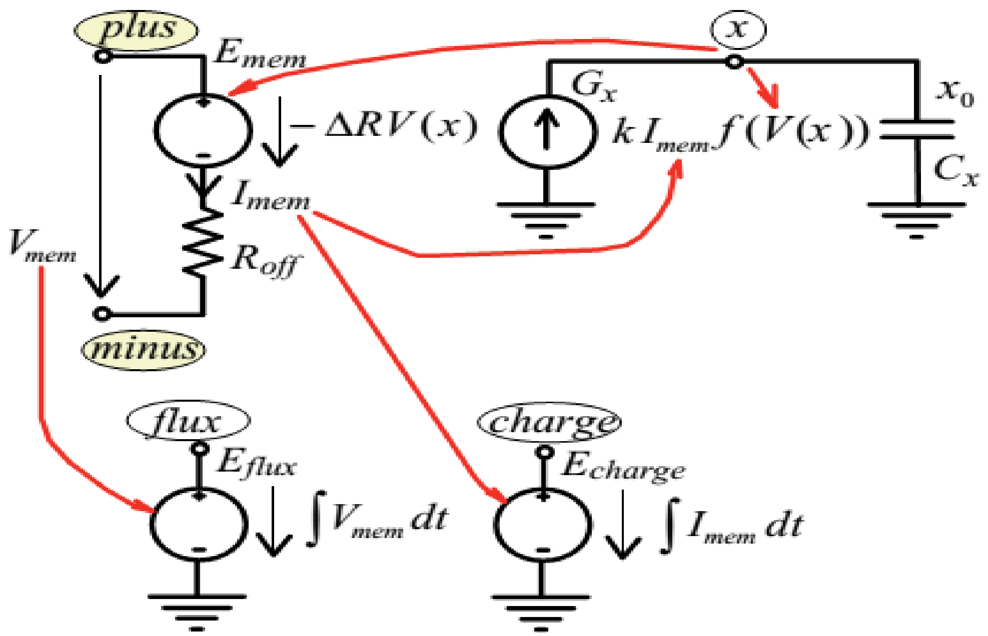
Fig. 3. Plot of non-linear window function proposed by Biolek *et al.* for $p = 1, 5$, and 10.

$$f_p(x) = 1 - \left(x - u(-i)\right)^{2p}$$

Memristor Modeling & Emulating

SPICE Macro-modeling:

Example
:

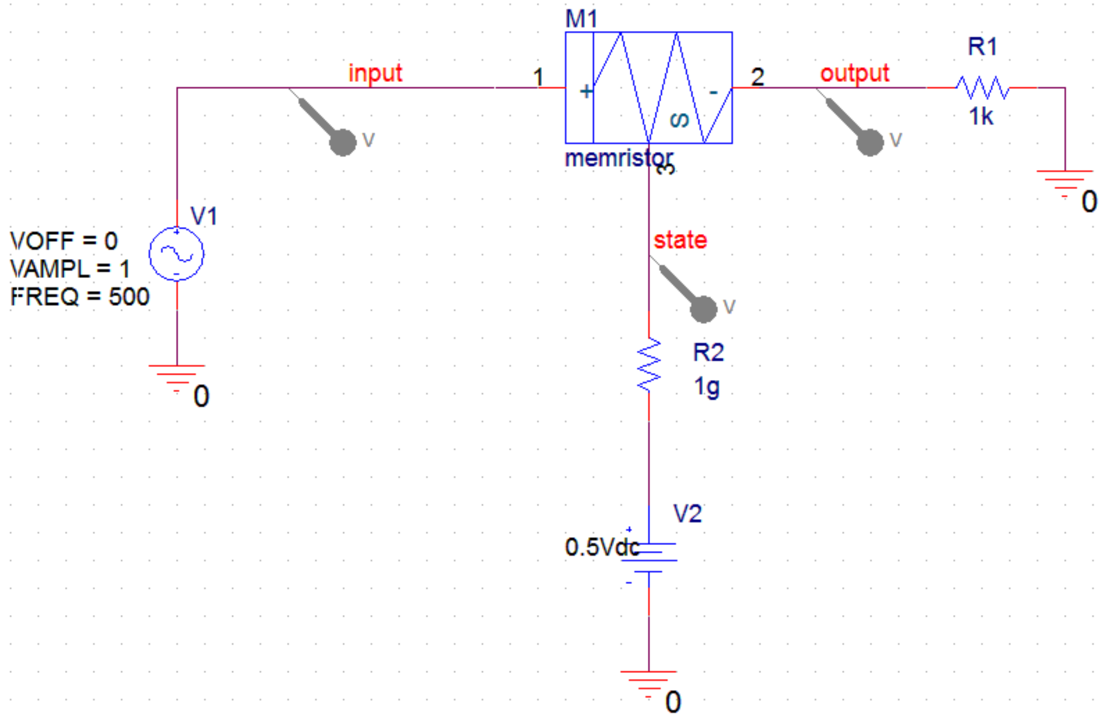


A memristor SPICE model

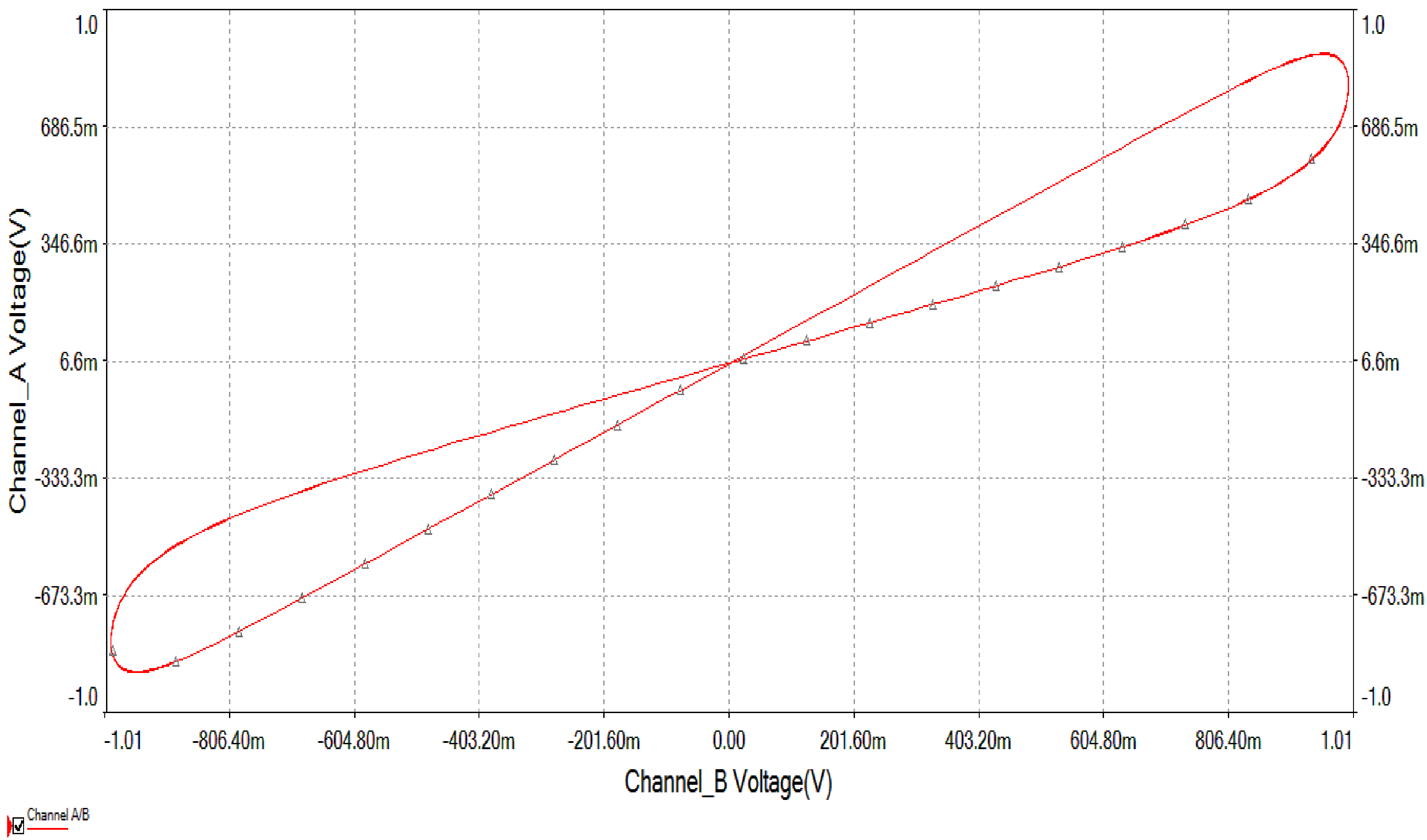
$$f(x) = 1 - (2x - 1)^{2p}$$

Simulation using different SPICE simulators

- ORCAD(PSPICE):
  Using HP PSPICE Model

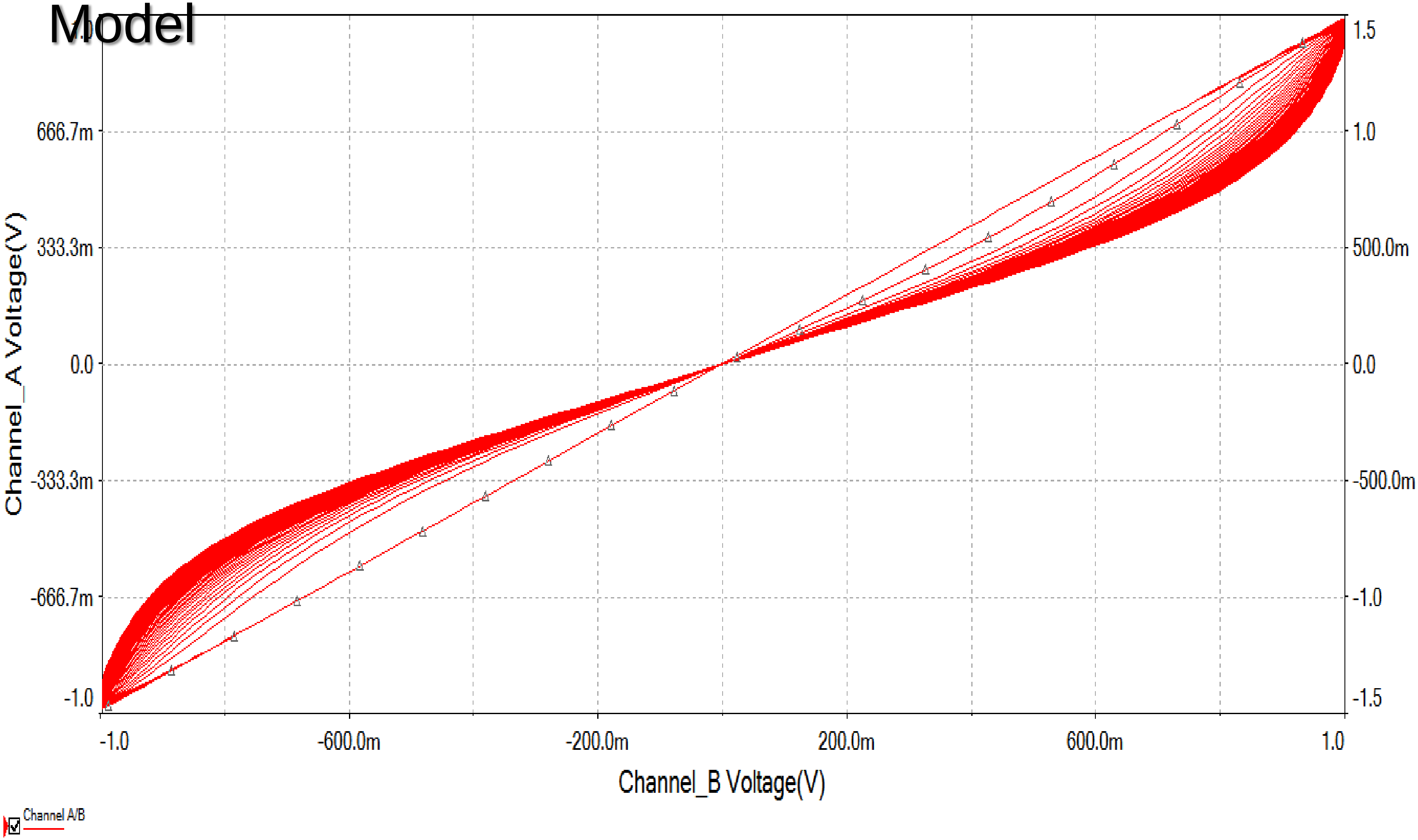


Simulation using different SPICE simulators



Simulation using different SPICE simulators

- NI Multisim12 (SPICE 3f5): Using HP PSPICE Model



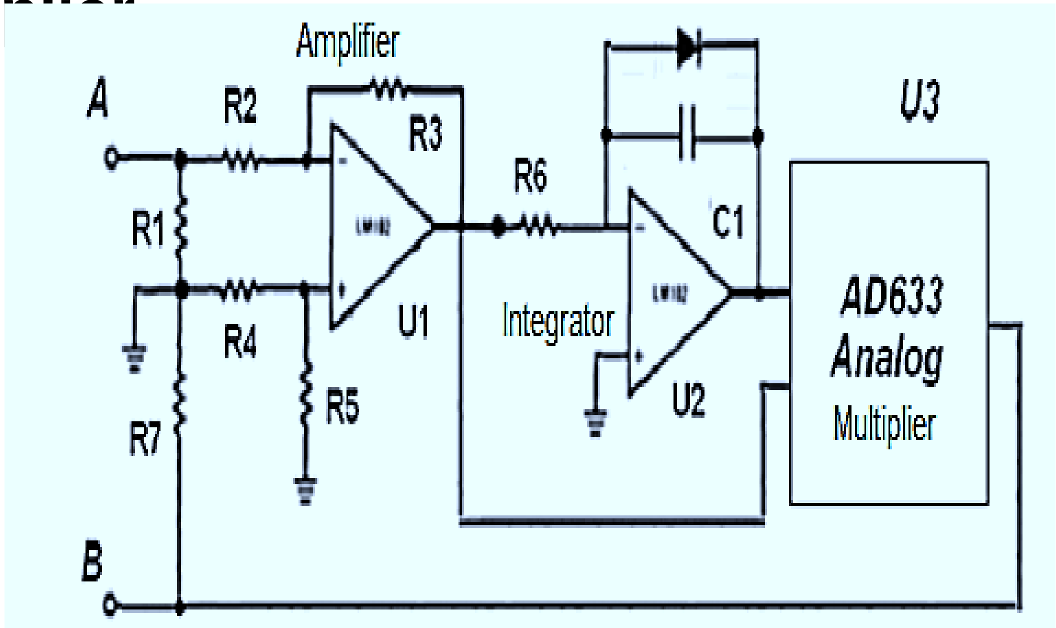
Memristor Modeling & Emulating

Memristor Emulation

- The fabrication technology of memristor devices is still not available for most of the researchers.
- Thus, it would be helpful if we can use an emulator circuit using existing devices to study the main characteristics of memristor devices and applications.

Memristor Modeling & Emulating

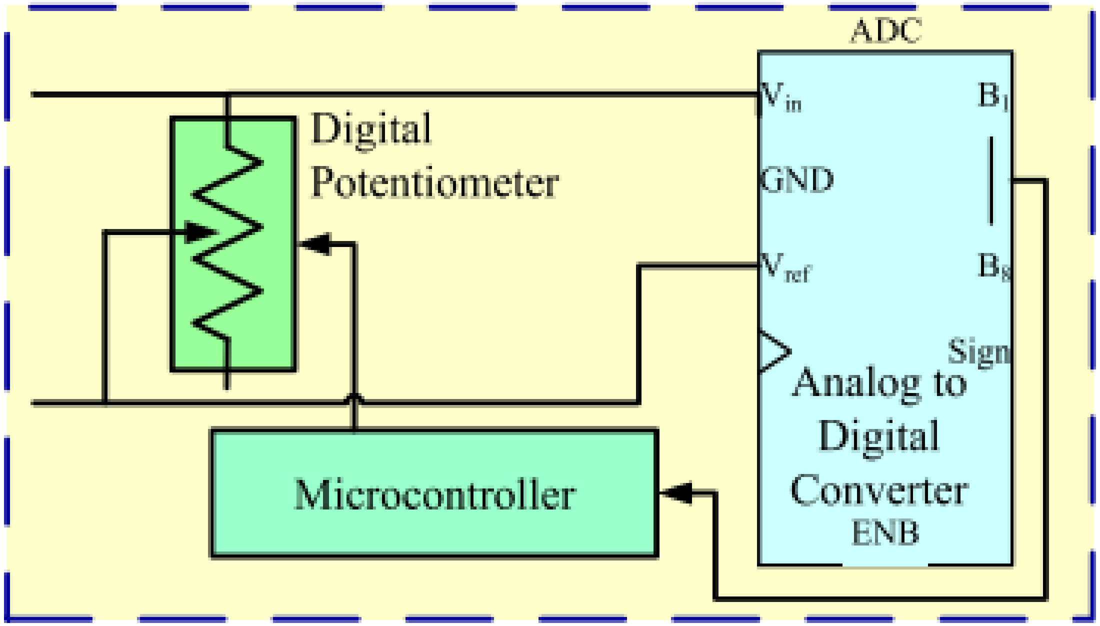
- **Mutlu proposed an emulator circuit to the TiO2 memristor with linear dopant drift using analog multiplier**



Memristor Mutlu Emulator circuit

Memristor Modeling & Emulating

Pershin proposed a memristor emulator usind A-to-D converter and microcontroller.



Pershin memristor emulator

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Applications of Memristors in Memories

MEMRISTORS MEMORIES

1 Resistive Random-Access Memory

2 Sneak Path Problem*

3 Memristor-based Content Addressable Memory (MCAM)

***Memristor issue (not memory topology)**

Applications of Memristors in Memories

	Traditional Memories				Other Emerging Technologies			Redox
	DRAM	SRAM	NOR Flash	NAND Flash	FeRAM	MRAM	PCRAM	Including Memristor
Cell Element	1T1C	6T	1T	1T	1T1C	1(2)T1R	1T(D)1R	(1D)(1T)1R
Feature Size (nm)	36-65	45	90	22	180	65	45	**9**
Density (Gbit/cm^2)	0.8 - 13	0.4	1.2	52	0.14	1.2	12	**154 - 309**
Read Time (ns)	2-10	**0.2**	15	100	45	35	12	<50
Write Time (ns)	2-10	**0.2**	10^7	10^6	65	35	100	0.3
Retention Time	4-64 ms	N/A	10 years	10 years	10 years	>10 years	>10 years	>10 years

International technology roadmap for semiconductors.
URL http://www.itrs.net/

Applications of Memristors in Memories

Memristors Memories

1 Resistive Random-Access Memory

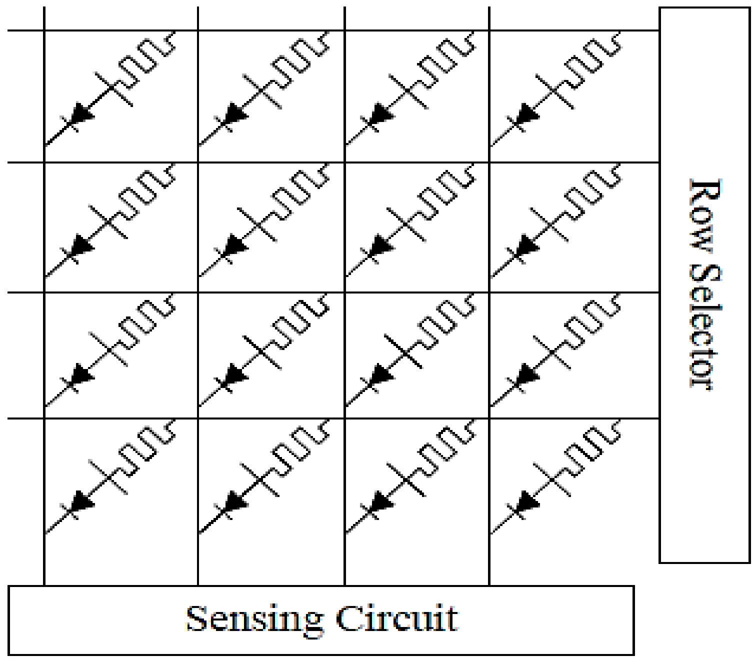
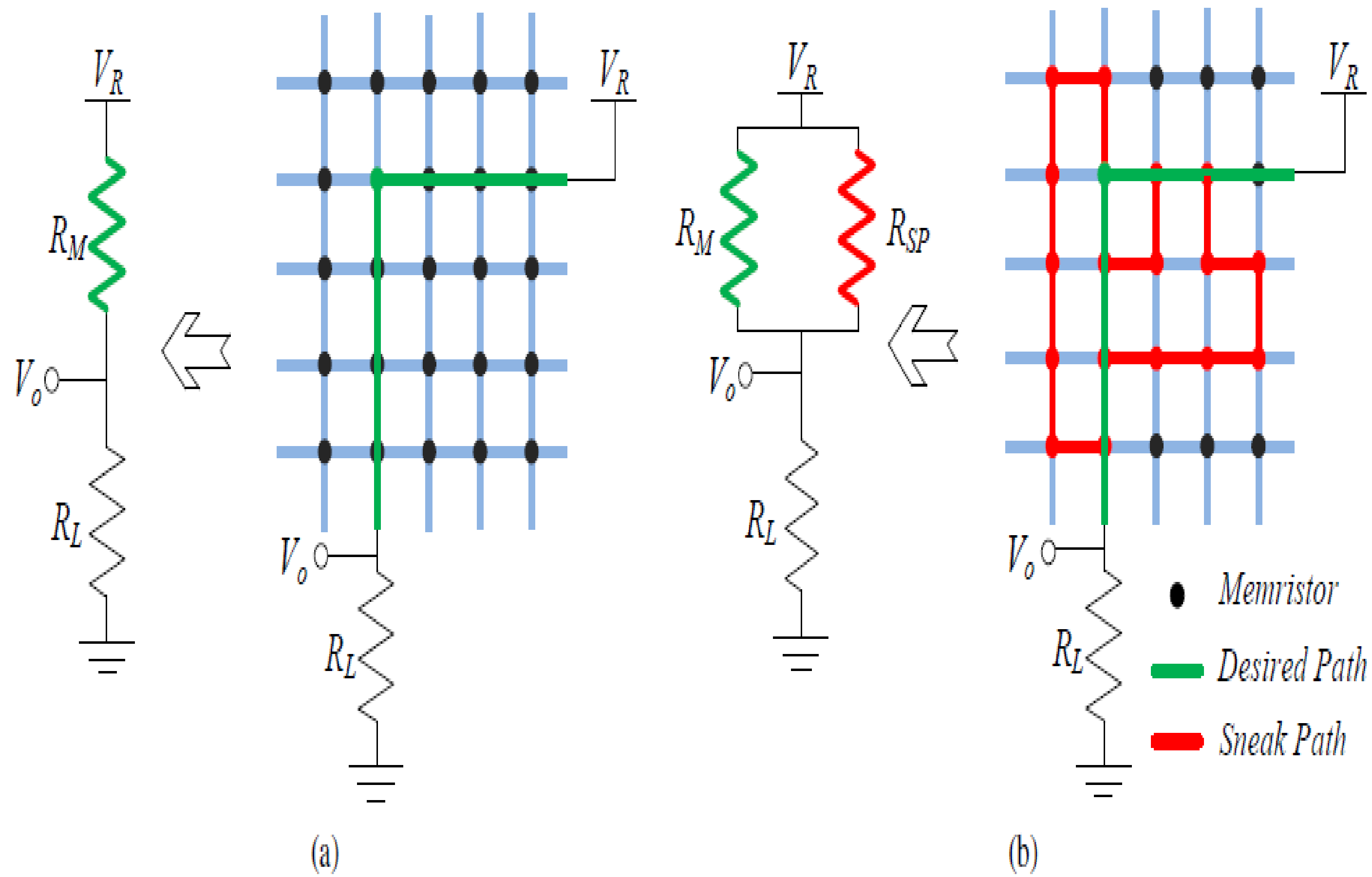


Figure 9: Simple memory array with 1D1M used for each memory cell.

Applications of Memristors in Memories

2 Sneak Path Problem



Applications of Memristors in Memories

1. ***Sneak paths are undesired paths for current, parallel to the intended path.***
2. **The source of the sneak paths is the fact that the crossbar architecture is based on the memristor as the only memory element, without gating.**
3. **These paths act as an unknown parallel resistance to the desired cell resistance .**
4. **What makes the sneak paths problem harder to solve is the fact that the paths depend on the content of the memory.**
5. **The added resistance of the sneak paths significantly narrows the noise margin and reduces the maximum possible size of a memristor array.**

Applications of Memristors in Memories

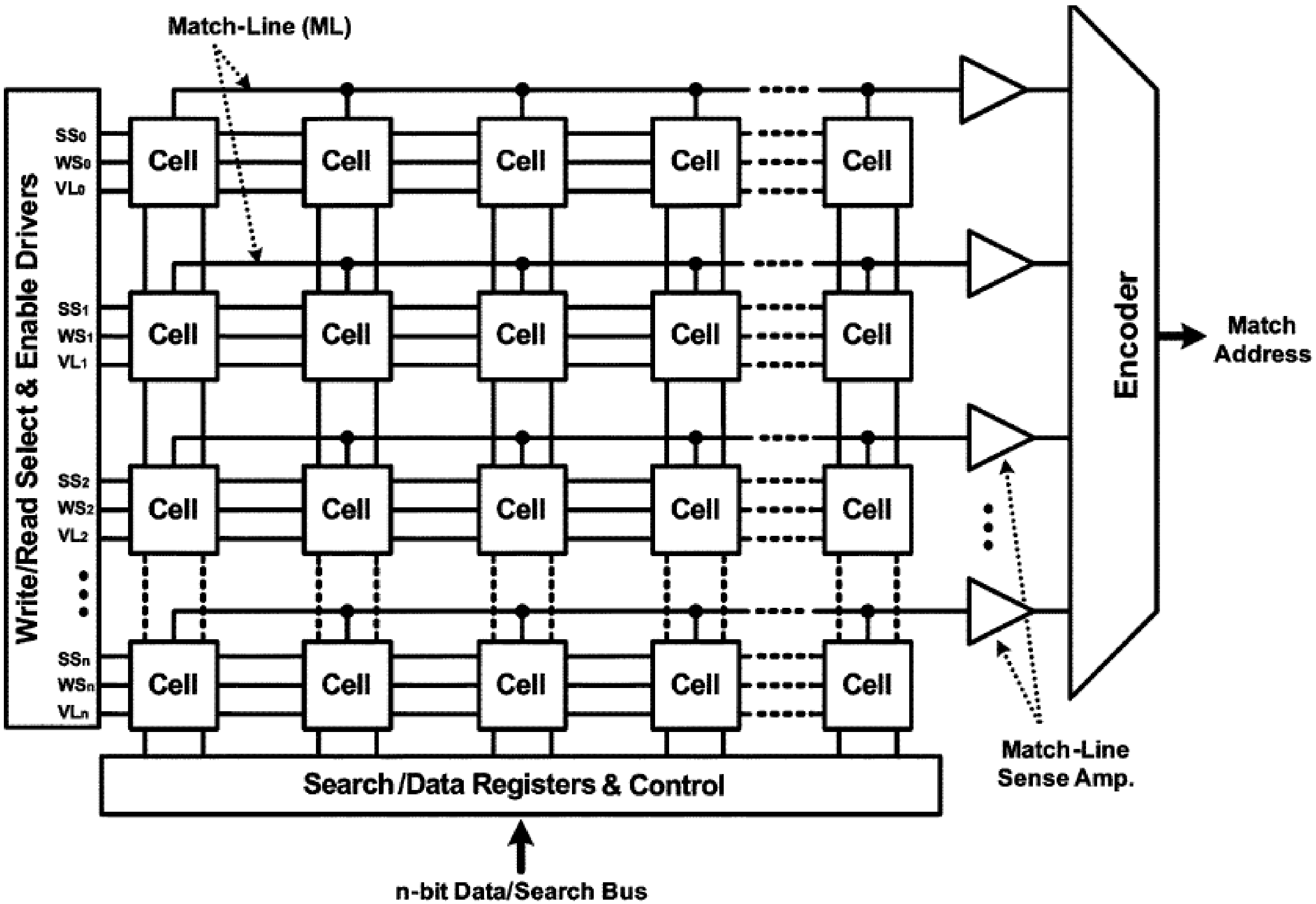
3 Content-addressable memory (CAM):

CAM is a type of associative memory that is used in high speed searching applications.

It compares input search data (tag) against a table of stored data, and returns the address of matching data (or in the case of associative memory, the matching data).

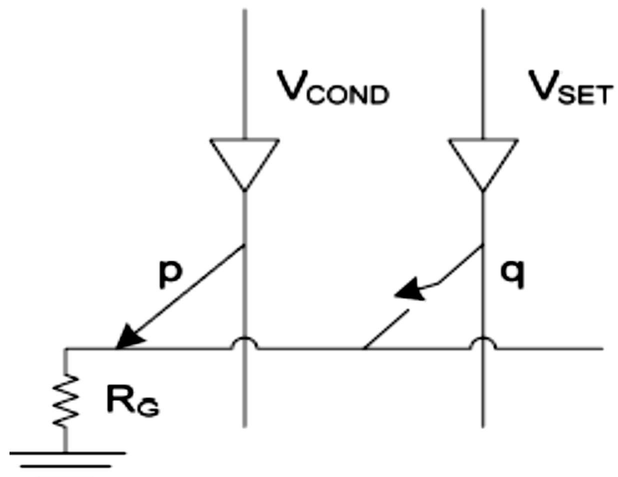
Applications of Memristors in Memories

- **<u>Generic CAM Topology:</u>**



Applications of Memristors in Logic & FPGA

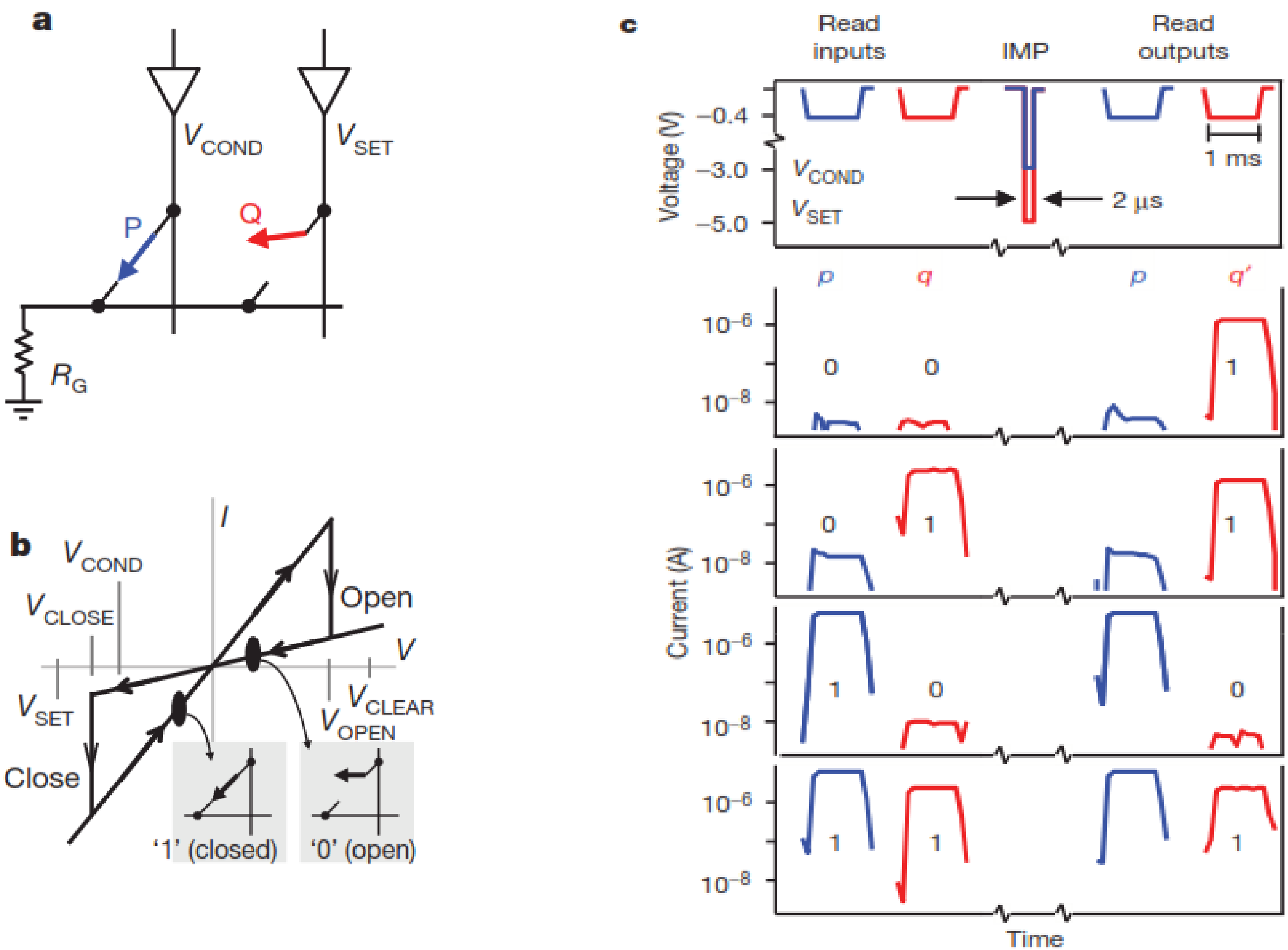
- **<u>Implication Logic:</u>**



p	q	q
0	0	1
0	1	1
1	0	0
1	1	1

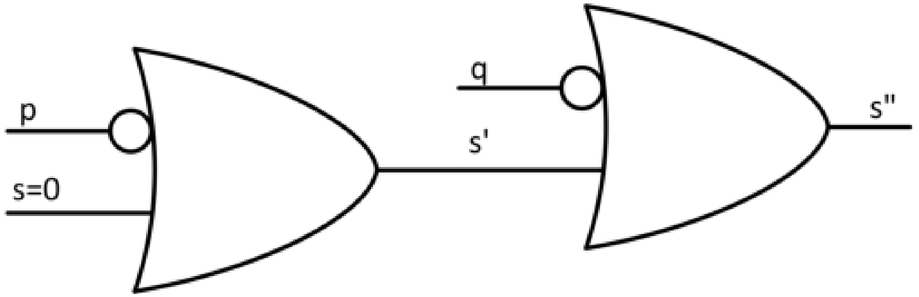
Figure 5: Memristor Implication Logic

Material Implication with Memristors



Building NAND from IMPLY

- IMPLY & FALSE is a computationally complete set of operators
- 2 input memristors and one work memristor can build NAND gate
  - Having NAND we are creating a link to known logic synthesis algorithms



Step 1
s=FALSE

s
0
0
0
0

Step 2
p→s=s'

p	s	s'
0	0	1
0	0	1
1	0	0
1	0	0

Step 3
q→s'=s''

q	s'	s''
0	1	1
1	1	1
0	0	1
1	0	0

Applications of Memristors in Logic & FPGA

- **<u>Implication Logic:</u>**

Table 2 Counts of IMP operations and devices for Boolean logic

Operation	IMP Operations (latency)	Devices (area)
$s \leftarrow p\,\mathrm{NAND}\,q$	2	3
$s \leftarrow p\,\mathrm{AND}\,q$	3	4
$s \leftarrow p\,\mathrm{NOR}\,q$	5	6
$s \leftarrow p\,\mathrm{OR}\,q$	4	6
$s \leftarrow p\,\mathrm{XOR}\,q$	8	7
$s \leftarrow \mathrm{NOT}\,p$	1	2

Applications of Memristors in Logic & FPGA

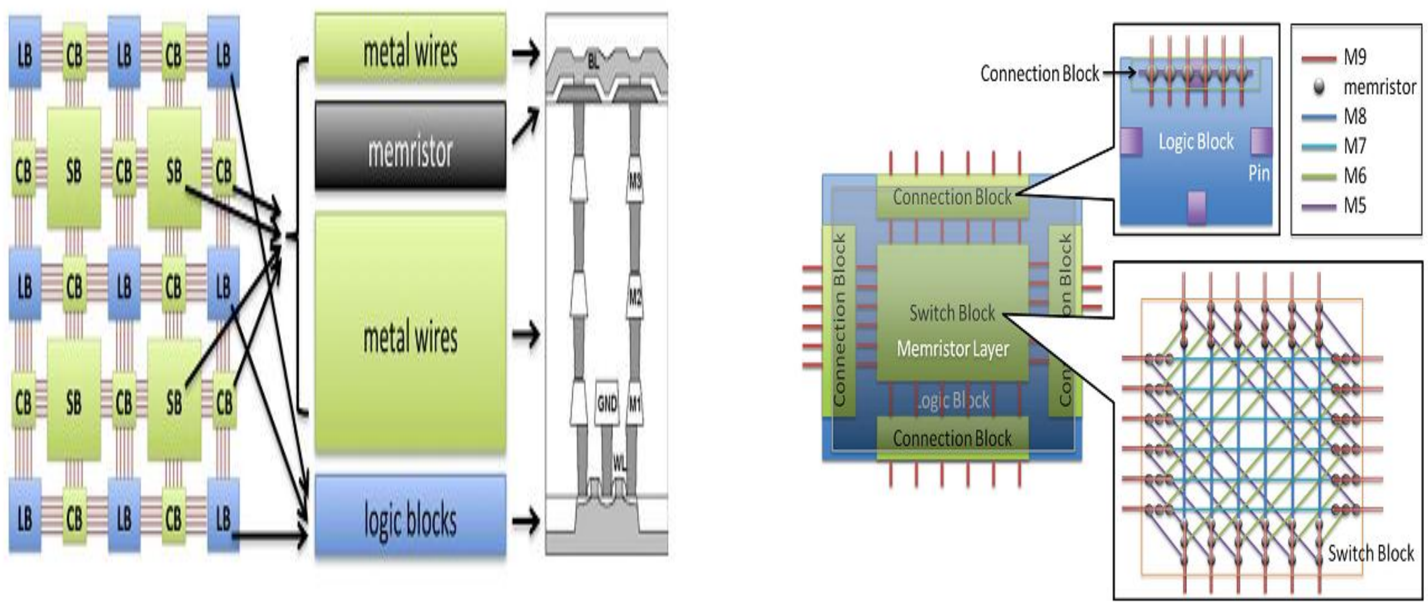
2 Field Programmable Gate Arrays

Jason Cong introduces a novel FPGA architecture with memristor-based reconfiguration (mrFPGA).

The programmable interconnects of mrFPGA use only memristors and metal wires.

Thus, the interconnections can be fabricated over logic blocks, resulting in significant reduction of overall area and interconnect delay.

Applications of Memristors in Logic & FPGA

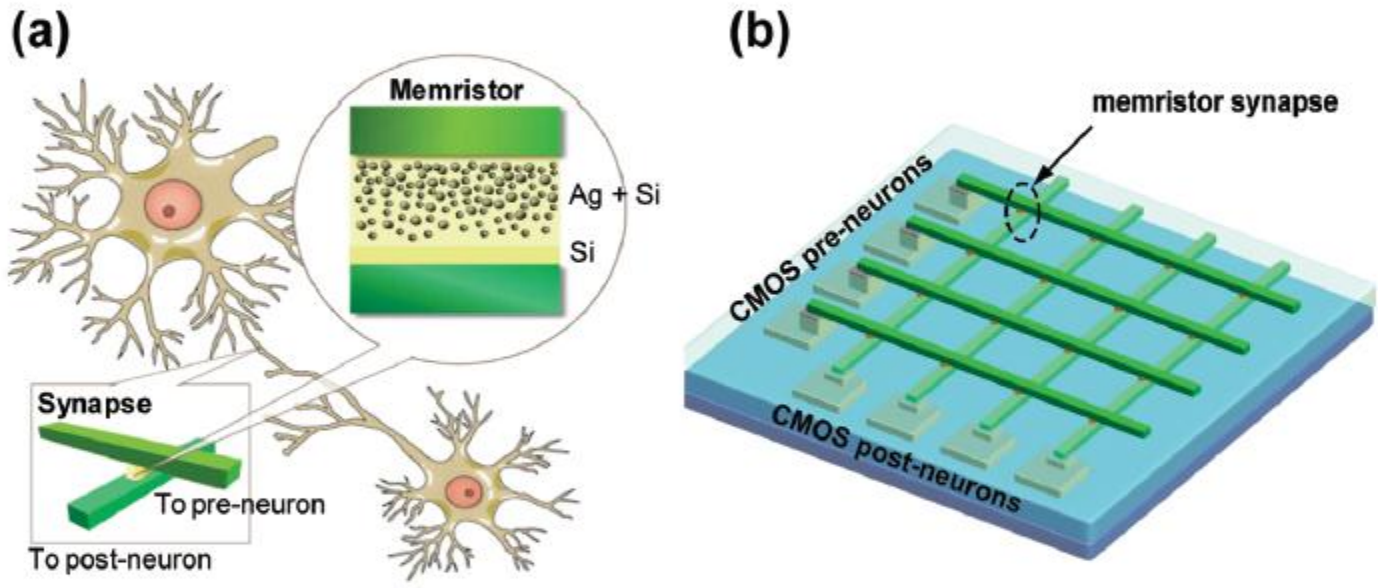


mrFPGA (a) Architecture (b) Design of connections and switching blocks

Applications of Memristors in Neural Networks

MEMRISTORS NEUROMORPHIC APPLICATIONS

The memristor based neuromorphic applications is a very promising field.



Applications of Memristors in Neural Networks

- **Using memristors as synapses in neuromorphic circuits can potentially offer both high connectivity, and high density required for efficient computing.**

- **<u>Spike-timing-dependent plasticity (STDP)</u> is a biological process that adjusts the strength of connections between neurons in the brain.**

The process adjusts the connection strengths based on the relative timing of a particular neuron's output and input action potentials (or spikes).

Applications of Memristors in Analog Circuits

MEMRISTORS ANALOG APPLICATIONS

- Memristors can be used to implement programmable analog circuits, Amplifiers, and oscillators.

fine-resolution programmable resistance

Applications of Memristors in Analog Circuits

A Pulse-coded programmable resistor using memristor is shown in figure.

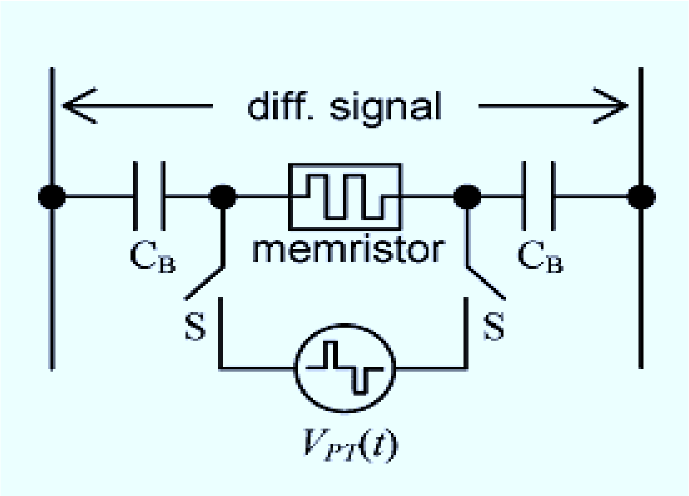
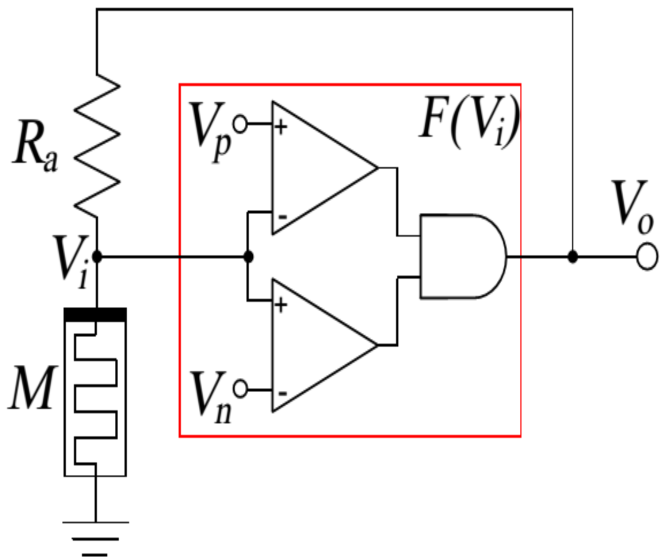


Fig. Pulse-coded programmable resistor using a memristor

Applications of Memristors in Analog Circuits

- **M. Affan Zidan presented a memristor-based oscillator without using any capacitors or inductors.**



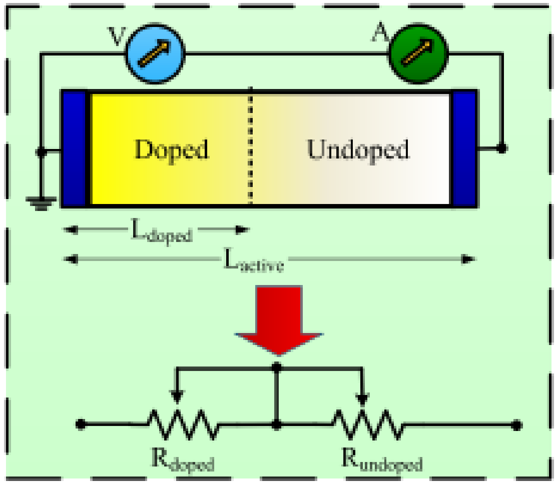
Memristor based reactance-less oscillator

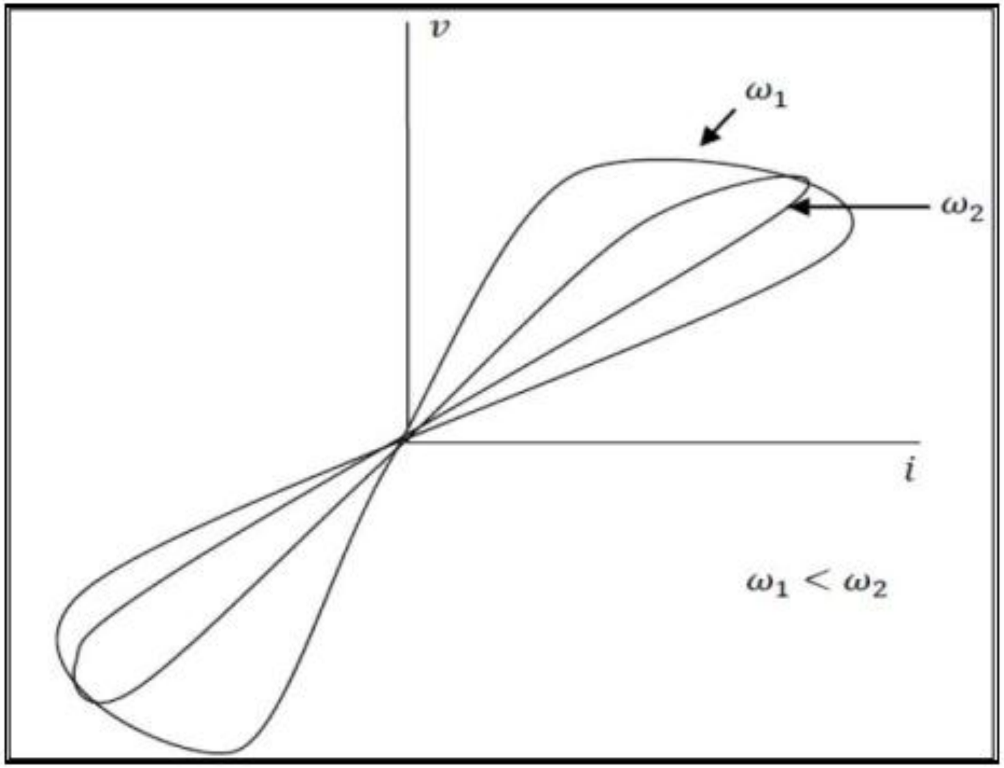
Questions??

Thank You

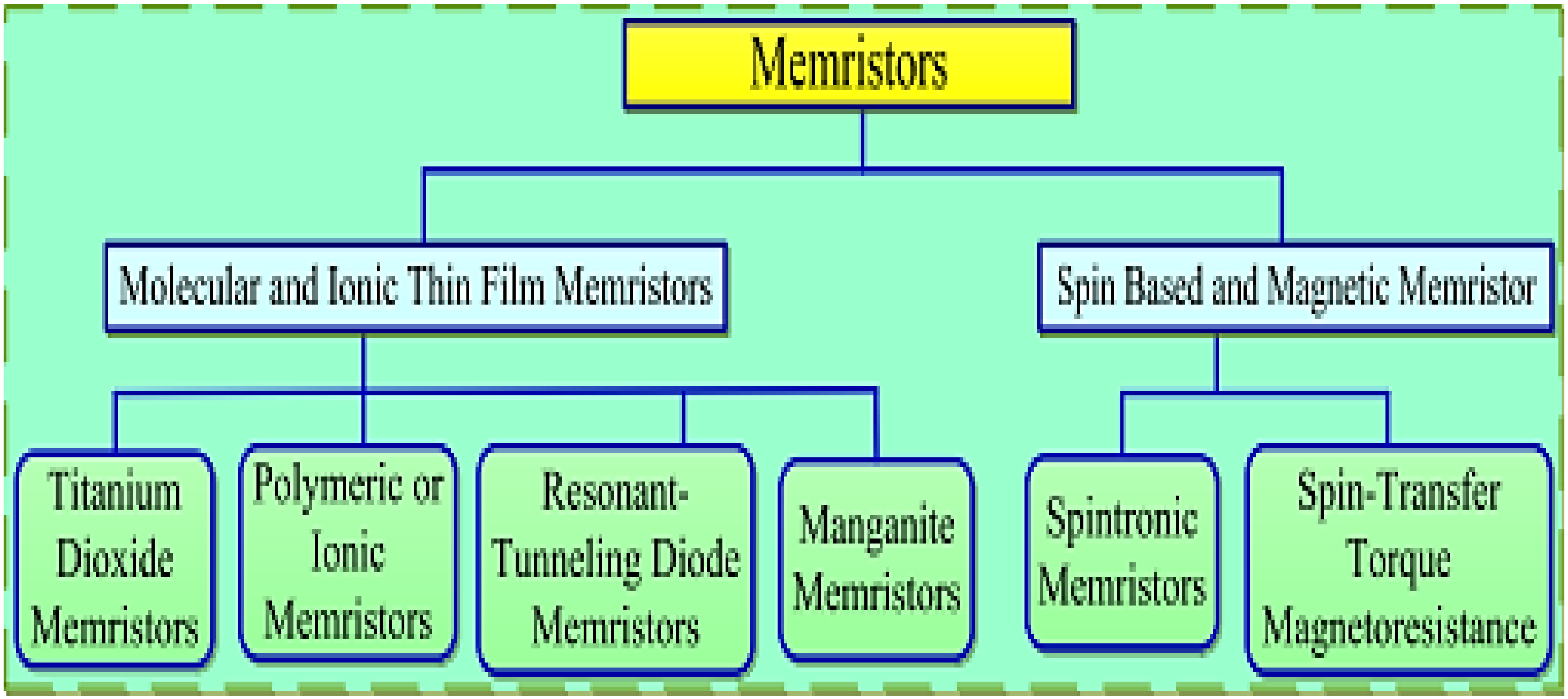
Basic Operation

- The pinched hysteresis loop and the loop shrinking with the increase in frequency.



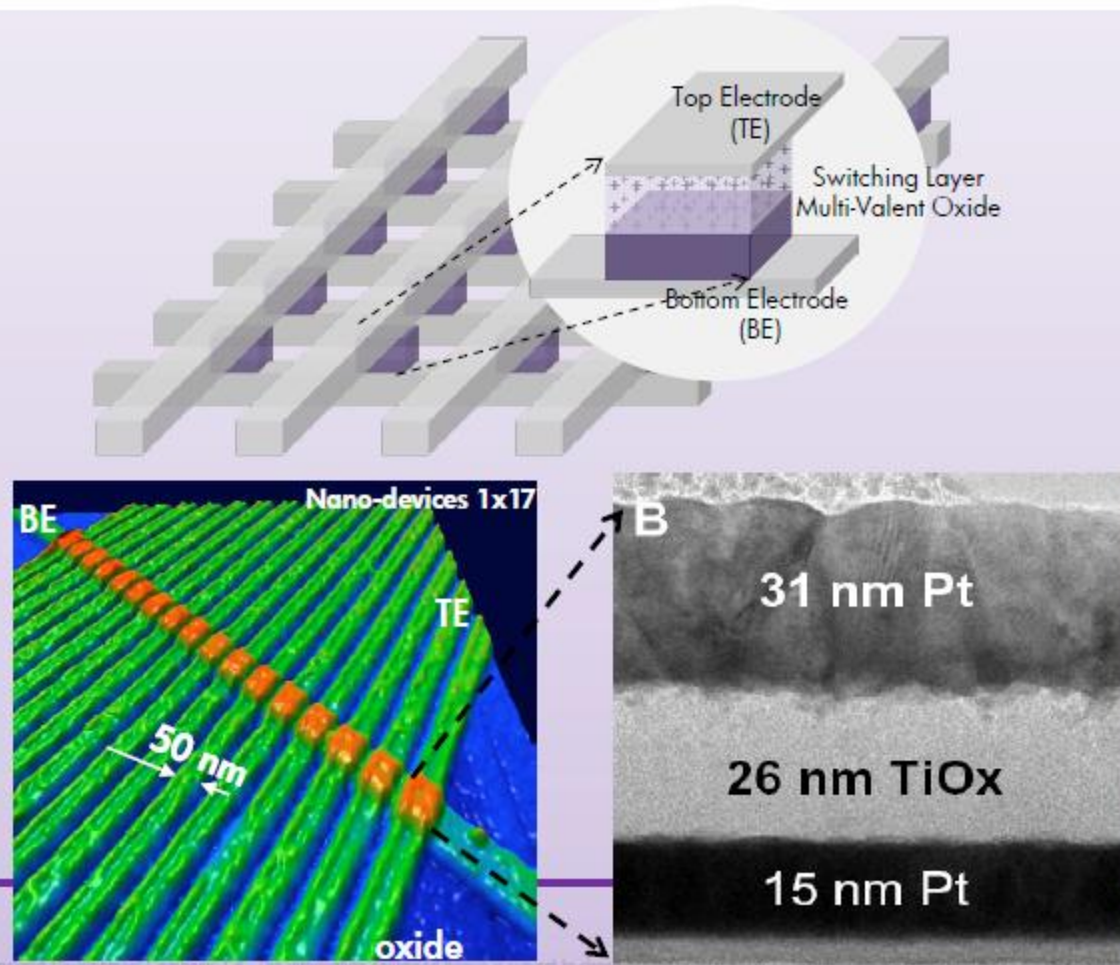


Types of Memristors



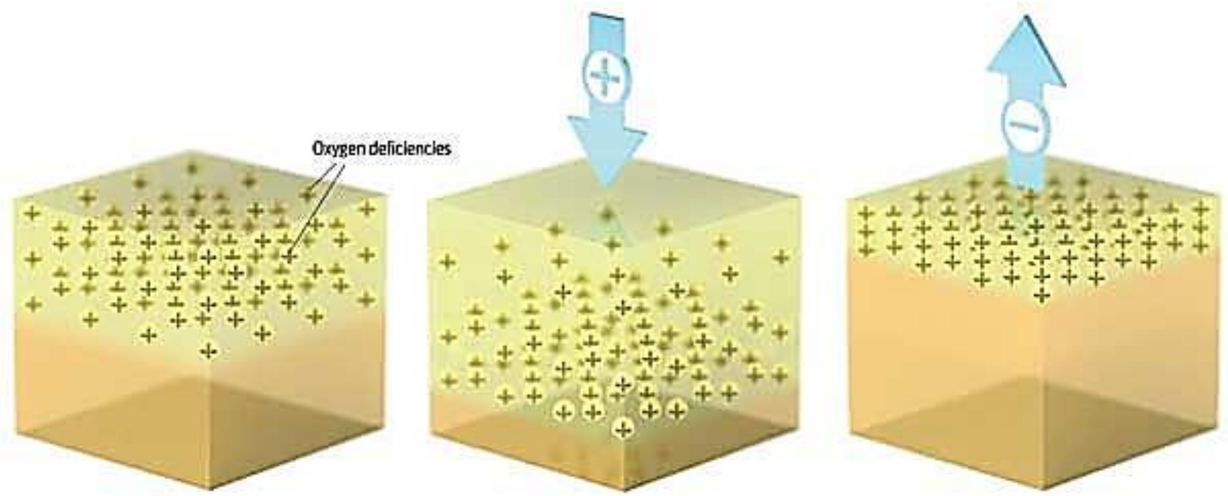
What exactly is it?

Cross-bar device with multi–valent oxide

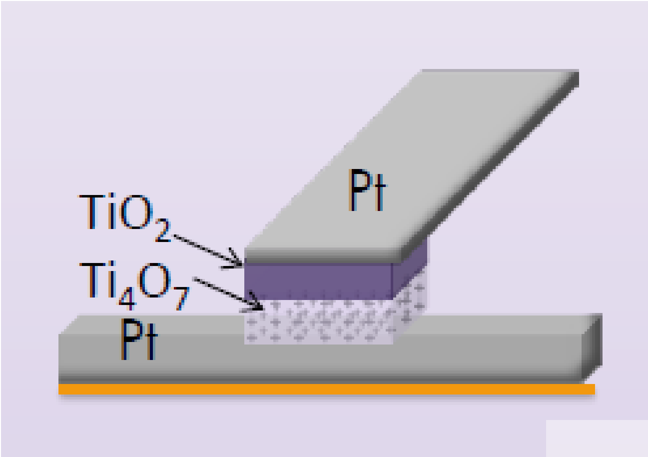


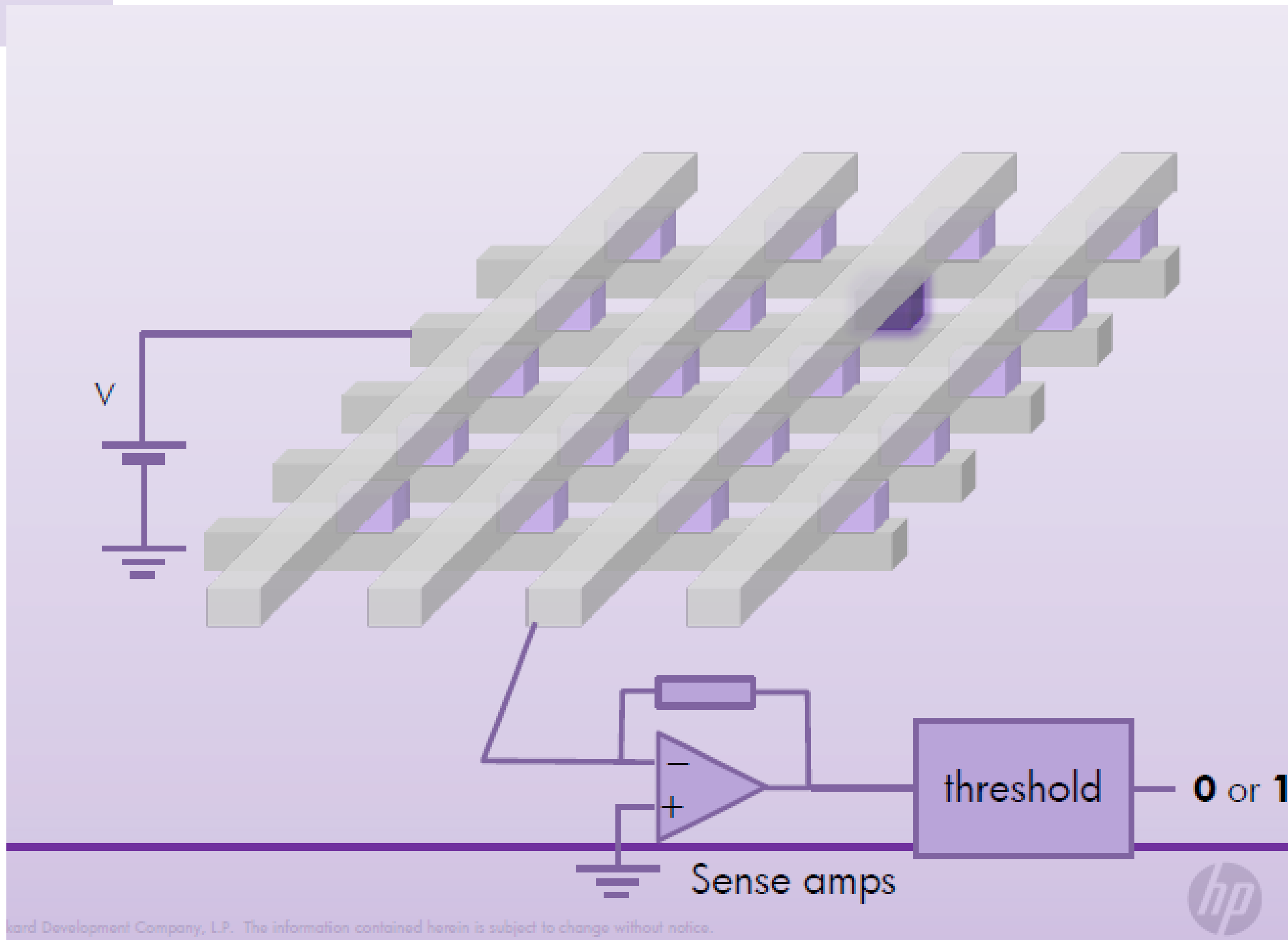
How does it work?

- Semiconducting Bipolar Switch



Previously: Fixed semiconductor structure and only electronic motion
Now: Ionic motion dynamically modulates the semiconductor structure
controlling the electronic current.


Pt
TiO_2
Ti_4O_7
Pt


V
threshold
0 or 1
Sense amps
kard Development Company, L.P. The information contained herein is subject to change without notice.

How Does it Stand Up as a Memory?

	Memristor	PCM	STTRAM	DRAM	Flash	HDD
Density (F^2)	<4	8–16	37–64	6–8	4–6	2/3
Energy per bit† (pJ)	0.1–3	2–27	0.1	2	10000	$1–10x10^9$
Read time (ns)	10-100(?)	20–70	10–30	10–50	25000	$5–8x10^6$
Write time (ns)	~10	50–500	13–95	10–50	200000	$5–8x10^6$
Retention	years	years	weeks?	<<second	years	years
Endurance (cycles)	$>10^{12}$	10^7	10^{15}	10^{15}	10^6	10^4

The usual Resistance: $\frac{dv(t)}{di(t)} = R$

So, M = R in case of constant charge!

Memristor depending on Charge Flux:

$$M\left[q(t)\right] = \frac{d\varphi(q)}{dq} = \frac{\frac{d\varphi(q)}{dt}}{\frac{dq}{dt}} = \frac{dv(q)}{di} = R(q)$$

While, M will be an R with memory effect in case of varying charge!

$\boxed{\text{Mem}}\text{ory}$

$\text{Resi}\boxed{\text{stor}}$

MEMRISTOR

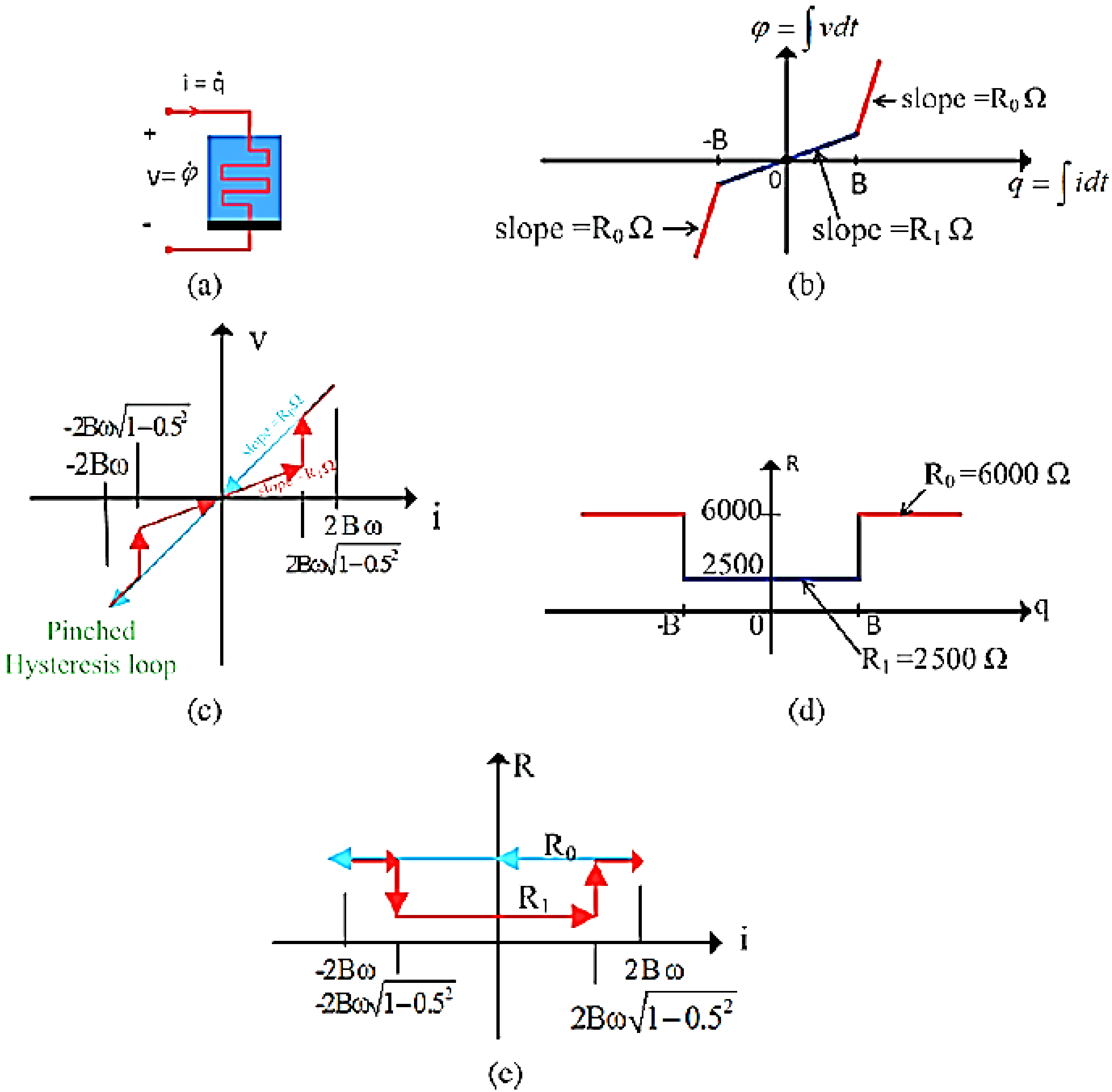
$$v(t) = \left(R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right) i(t)$$

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{ON}}{D} i(t)$$

$$w(t) = \mu_V \frac{R_{ON}}{D} q(t)$$

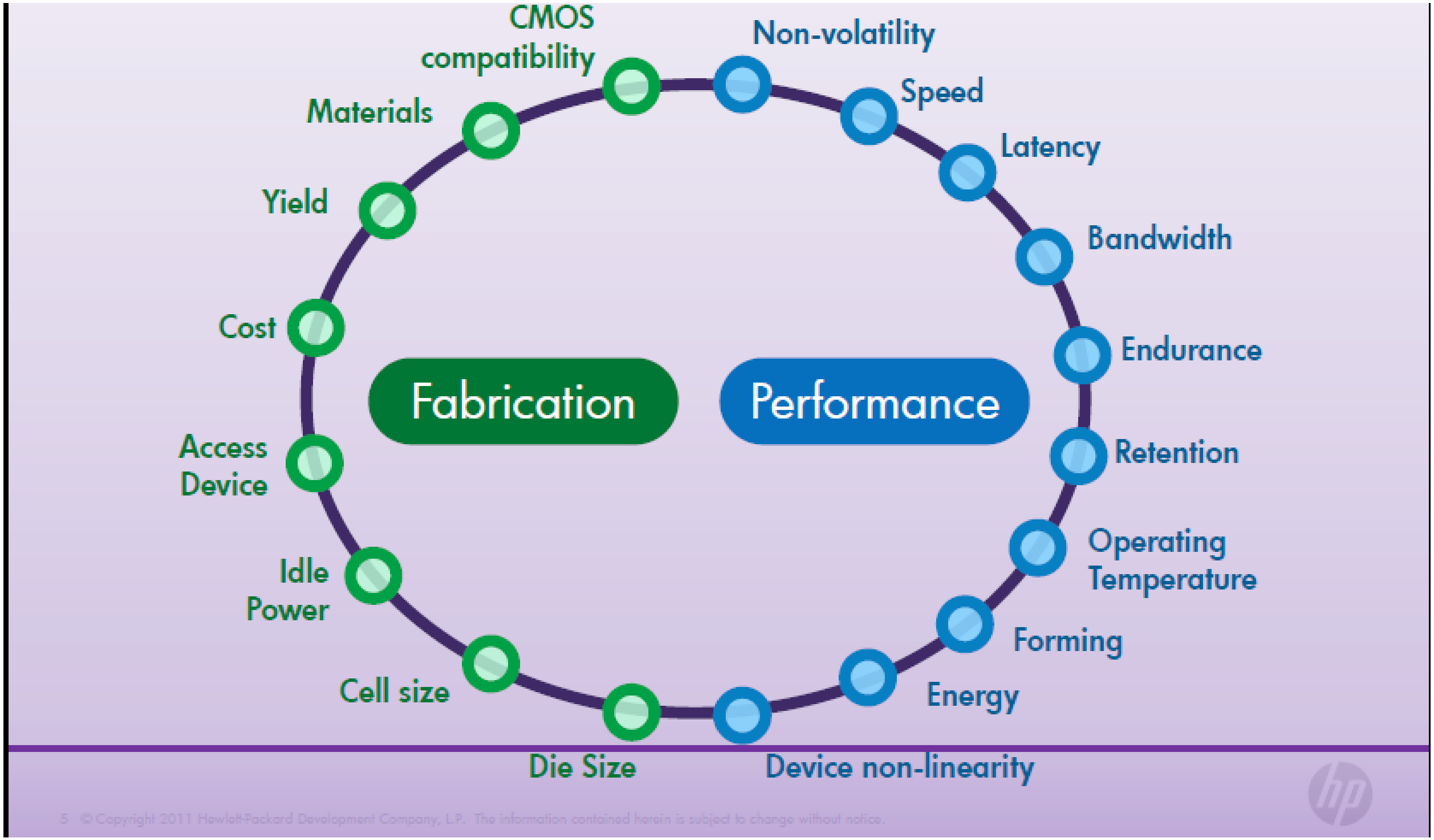
$$M(q) = R_{OFF} \left(1 - \frac{\mu_V R_{ON}}{D^2} q(t) \right)$$

More evident at nano-scale!

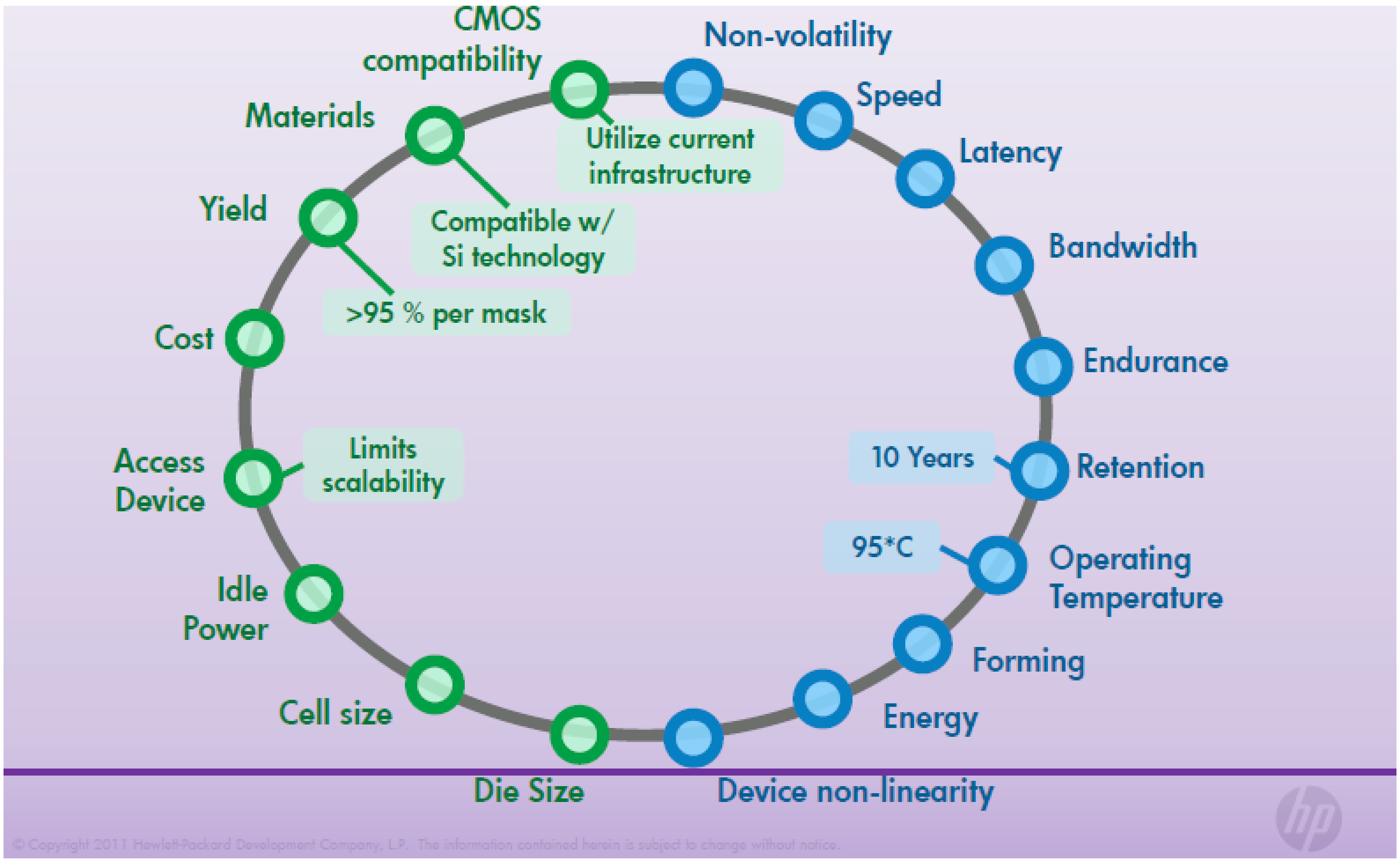


i = q̇
+
v= φ̇
-
(a)
φ = ∫vdt
slope =R₀ Ω
-B
0
B
q = ∫idt
slope =R₀ Ω
slope =R₁ Ω
(b)
v
-2Bω√1−0.5²
-2Bω
2 B ω
2Bω√1−0.5²
i
Pinched
Hysteresis loop
(c)
R
R₀=6000 Ω
6000
2500
-B
0
B
q
R₁ =2500 Ω
(d)
R
R₀
R₁
i
-2Bω
-2Bω√1−0.5²
2B ω
2Bω√1−0.5²
(e)

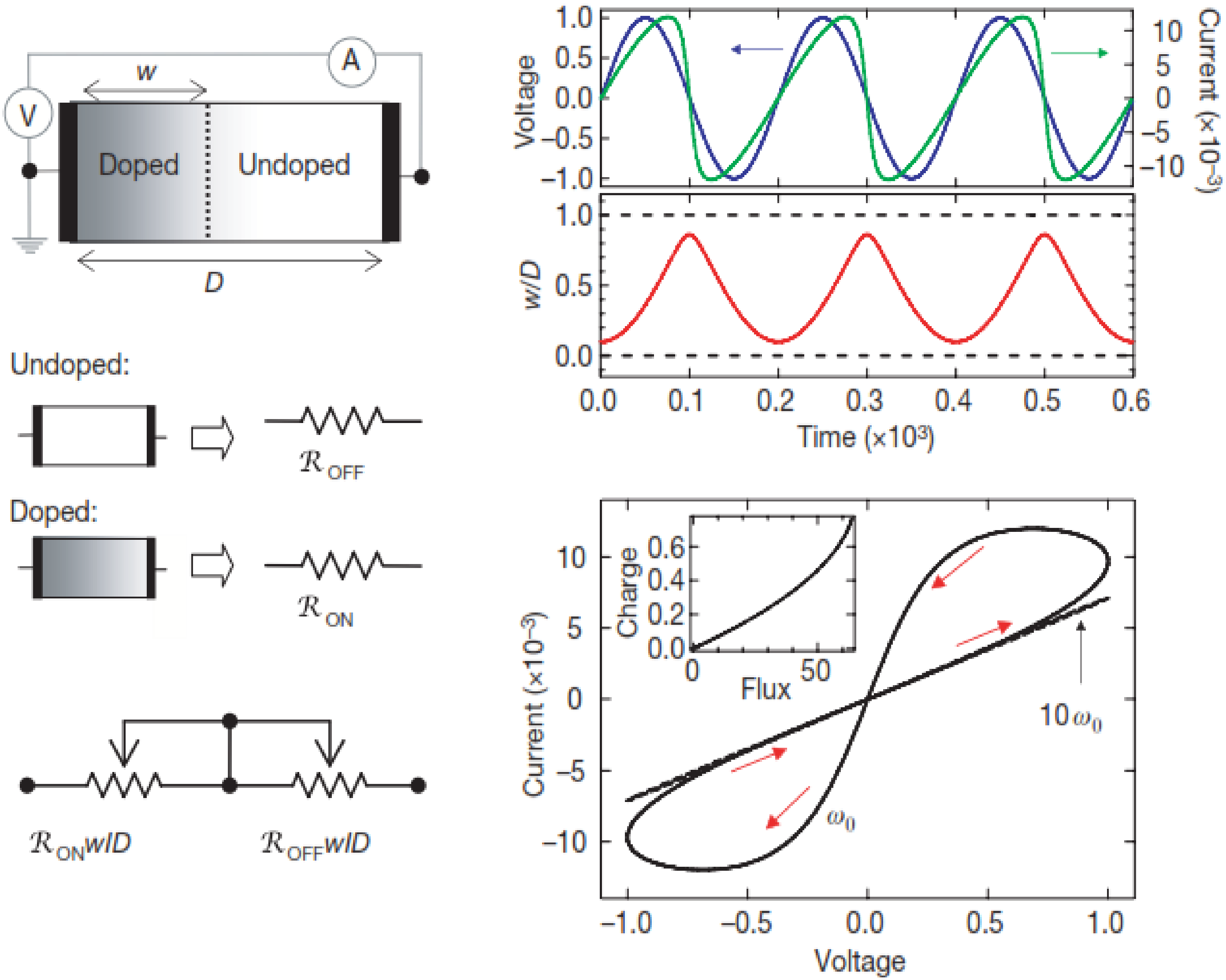
Considerations for Replacement Technology



Considerations for Replacement Technology (Memristor)



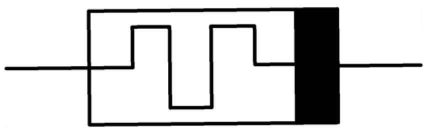
Memristor

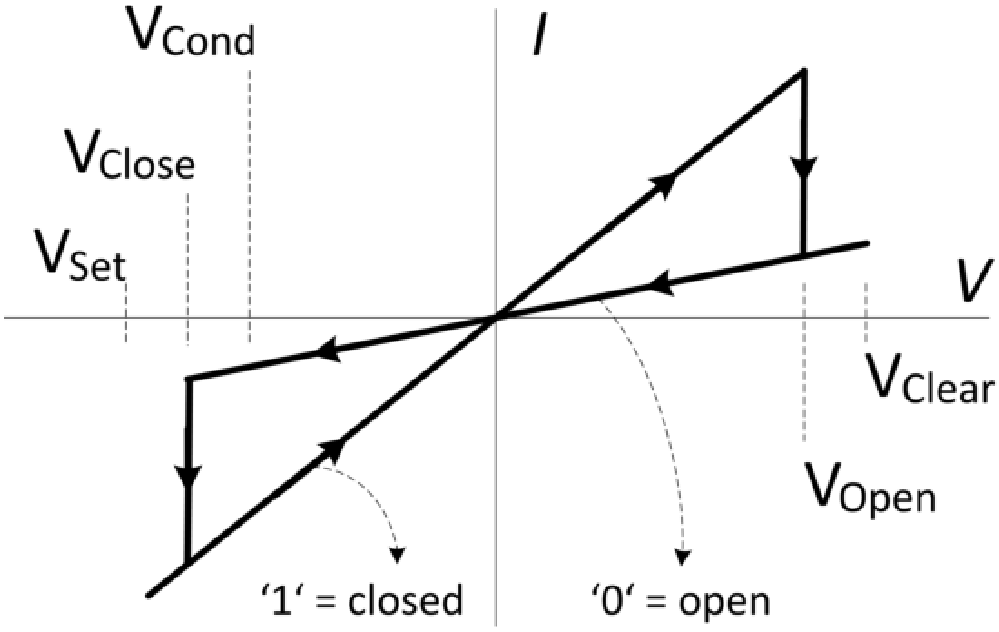


w
A
V
Doped
Undoped
D
Undoped:
$\mathcal{R}_{OFF}$
Doped:
$\mathcal{R}_{ON}$
$\mathcal{R}_{ON}w/D$
$\mathcal{R}_{OFF}w/D$
Voltage
Current ($\times 10^{-3}$)
w/D
Time ($\times 10^{3}$)
Charge
Flux
$10\omega_0$
ω_0
Current ($\times 10^{-3}$)
Voltage

Memristor

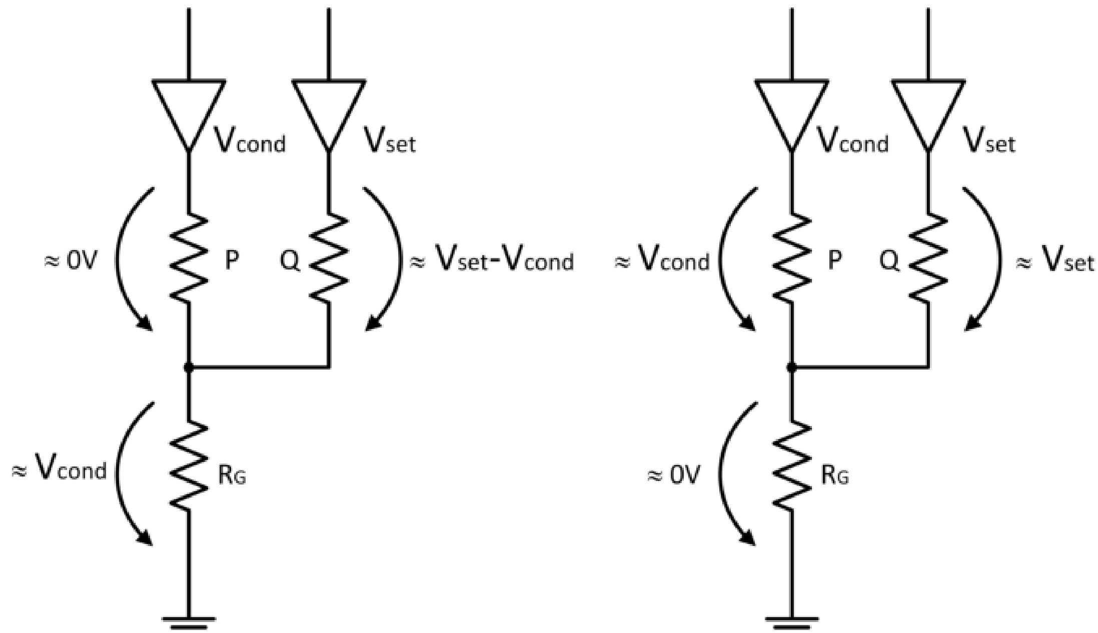
- One type of new emerging nano-devices
- Memory-Resistor postulated by Leon Chua in 1971
- First physical implementation found by HP in 2008





IMPLY Logic

- Two memristors can perform material implication with one pulse – IMPLY
- Consider memristors as a switch with two states – Ron, Roff
- Voltage drop over P affects voltage drop over Q
- Result will be stored in Q
  - Q is input and output memristor



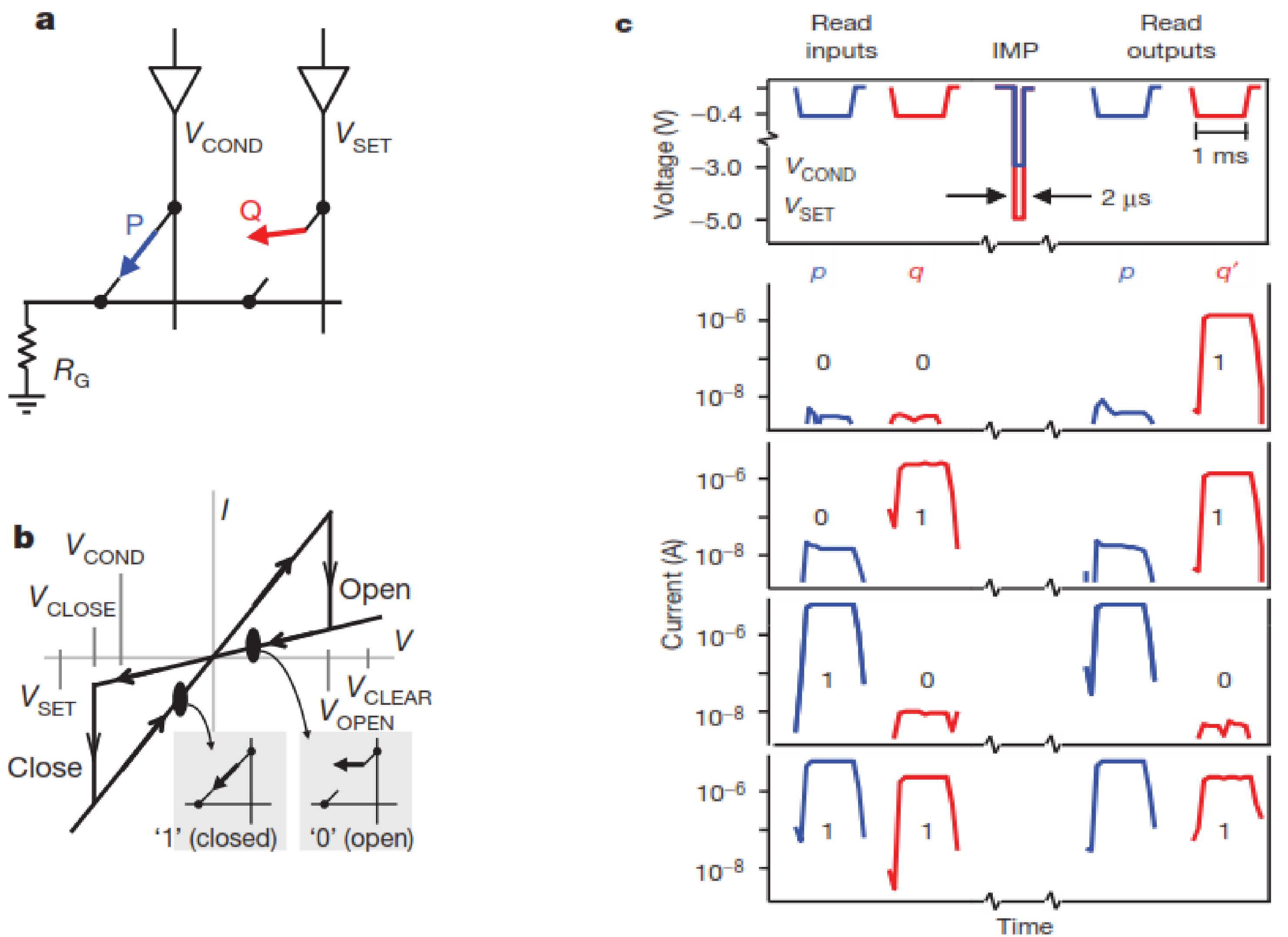
(a) P = closed = logic '1'
Q = open = logic '0'

(b) P = open = logic '0'
Q = open = logic '0'

IMPLY Logic - Notes

- Explains the conditions for Q changing its state
- Q is pre-set to “0” (low conductance / high resistance)
- Voltage level V_Rg determines voltage drop over Q
- Only if P = “0” V_Rg remains low and allows Q to change

Material Implication with Memristors



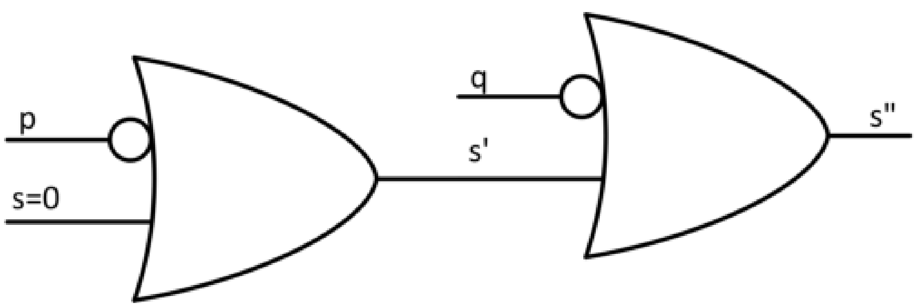
Why are we interested in that?

- CMOS technology scaling is approaching limits
- Main limitation in modern CPUs is heat

- 2-terminal device of 10nm size
  - Allow much higher/denser device integration
- Switching between states can be done with pico Joule

Building NAND from IMPLY

- IMPLY & FALSE is a computationally complete set of operators
- 2 input memristors and one work memristor can build NAND gate
  - Having NAND we are creating a link to known logic synthesis algorithms



Step 1
$s = \text{FALSE}$

s
0
0
0
0

Step 2
$p \rightarrow s = s'$

p	s	s'
0	0	1
0	0	1
1	0	0
1	0	0

Step 3
$q \rightarrow s' = s''$

q	s'	s''
0	1	1
1	1	1
0	0	1
1	0	0

Structure

- The device developed by HP Labs consists of a 50nm thin film of titanium dioxide with 5nm electrodes on either side. There are two layers to the film, one of which is oxygen depleted.