Memristor Emulator for Memristor Circuit Applications

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***Abstract*—A memristor emulator which imitates the behavior of a TiO_2 memristor is presented. Our emulator is built from off-the-shelf solid state components. To develop real world memristor circuit applications, the emulator can be used for breadboard experiments in real time. Two or more memristor emulators can be connected in serial, in parallel, or in hybrid (serial and parallel combined) with identical or opposite polarities. With a simple change of connection, each memristor emulator can be switched between a decremental configuration or an incremental configuration. The hardware and spice simulation of the proposed emulator showed promising results that provides an alternative solution of *hp* TiO_2 memristor model in real circuit.**

***Index Terms*—Decremental configuration, emulator, incremental configuration, memristor, off-the-shelf devices.**

I. Introduction

A MEMRISTOR is a circuit element developed recently, which exhibits excellent features of both memory and neuromorphic applications. For memory applications, it is nonvolatile and has an extremely small size of a few nanometers. For neuromorphic applications, it has features of pulse-based operation and adjustable resistance, which are ideal for tuning the synaptic weights of neuromorphic cells.

The memristor was first postulated by Chua in 1971 as the fourth basic element of electrical circuits [1] and later the concept was generalized to a class of dynamical systems called memristive a device [2]. Recently, the Stanley Williams group [3] from *hp* has built a nano-scale TiO_2 device which is nonvolatile and exhibits synaptic characteristics [3], [4]. A common fingerprint of both the memristor, and the memristive device, is the *pinched* hysteresis loop in the current versus voltage plane, under sinusoidal excitations. Due to these phenomena, the resistance of the device depends upon the past history of the input current or voltage, and hence can function as synapses of neural networks.

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Due to such unusual features of the memristor, many scientists had started to exploit the memristor for analog [6], [7] and digital information processing [8], [9] applications. Others have applied memristive devices as resistive switching devices for memory and logic applications [10]–[12]. Also, the potential for exploiting memristors for neuromorphic applications had been proposed by many scientists [3], [4], [7], and [20]–[22]. The analog signal storing capability of the memristor is very important in neuromorphic applications.

Recently, Jo *et al.* [7] and Kund *et al.* [13] had built memristors using Ag and Si in a sandwiched layer and reported their performances as analog memories. Also, Snider had presented a memristor-based self-organized network employing dedicated memristor connections for inhibitory (negative) weighting [4].

Despite such immense interest among scientists on the memristor, commercially available memristors are not expected to appear in the near future due to the cost and technical difficulties in fabricating nano-scale devices. Therefore, some circuit replacements which behave like memristors are needed to build real-world application circuits which exploit memristor's potentials. Indeed, several research groups presented spice macro models [14]–[17], which are useful for simulating memristor. However, macro models are not hardware, and they cannot be used to build physically implementable memristor application circuits. Therefore, *emulators* which act like the real memristors are needed. Some important features which should be included in any memristor emulator are 1) the memristance (resistance of memristor) should be programmable 2) the memristance should be nonvolatile, and 3) it can be connected directly to other memristor circuit elements. Only a few research groups had made contributions in the area of memristor emulators. Pershin *et al.* had built a memristor model [18] using digital and analog mixed circuits. Since the signals in their circuit are converted between analog and digital to perform the memristor operation, instant interoperability with other analog circuit element is limited. On the other hand, Mutlu *et al.* had presented a memristor emulating circuit via pure analog technology [19], where the features of the TiO_2 memristors are well emulated. Though, it is pedagogically useful, the serial, parallel, hybrid expandable, and the connectivity with other circuit elements are difficult in their design. Also, the memristance does not remain constant for a long enough time sufficient for application study, thereby reduces and limits the usefulness of their work.

In this paper, we propose a memristor emulating circuit which is built with off-the-shelf solid state devices. Our proposed memristor emulator includes the features of the TiO_2 memristor faithfully; its memristance does not vary over a relatively long period of time, and it is compatible with other

circuit devices. Various features of our proposed memristor emulator are demonstrated via experiments and simulations.

The concept of the memristor is briefly reviewed in Section II, and the design principle of our memristor emulator circuit is described in Section III. For application studies, an expandable model of our memristor emulator is proposed in Section IV. Various features of our memristor-emulator hardware were tested to verify its performance in Section V. A short conclusion is given in Section VI.

II. Principle of the Memristor

In the memristor, the current and voltage relationship can be defined by

$$v(t) = R(t)i(t) = \frac{d\varphi}{dq}i(t). \tag{1}$$

where $\varphi(t)$ and $q(t)$ denote the flux and charge, respectively, at time t. Thus, the resistance can be interpreted as the slope at the operating point $q = q_0$ at time t on the memristor $\varphi - q$ curve. If the $\varphi - q$ curve is nonlinear; the resistance will vary with the operating point. Without external voltage or current, the operating point does not change and hence the resistance remains constant. Thus, the signal is memorized as the value of the memristor's resistance, namely, the *memristance* M.

Since the flux φ is defined by $\varphi(t) = \int_{-\infty}^{t} v(\tau)d\tau$, the memristance (resistance of memristor) M can be controlled by applying a voltage or current signal across the memristor, where

$$R = M = \left.\frac{d\varphi}{dq}\right|_{(q_Q,\varphi_Q)}. \tag{2}$$

Fig. 1(a) shows the structure of the hp TiO_2 memristor [3]. In the TiO_2 memristor, a thin titanium dioxide (TiO_2) layer and a thin oxygen-poor titanium dioxide (TiO_{2-x}) layer are sandwiched between two platinum electrodes. The TiO_2 layer and the $TiO_2 - x$ layer are referred to as undoped, and doped layers, respectively. When a voltage or current is applied to the device, the dividing line between the TiO_2 and TiO_{2-x} layers shifts as a function of the applied voltage or current. As a result, the resistance between the two electrodes is altered.

Let D and w denote the thickness of the sandwiched area and the doped area (oxygen deficient area) in the TiO_2 memristor, respectively, and let $R_{\rm ON}$ and $R_{\rm OFF}$ denote the resistances at high and low dopant concentration areas, respectively.

Then, the relation between the voltage and the current is given by

$$v(t) = \left(R_{\rm ON}\frac{w(t)}{D} + R_{\rm OFF}\left(1 - \frac{w(t)}{D}\right)\right)i(t) \tag{3}$$

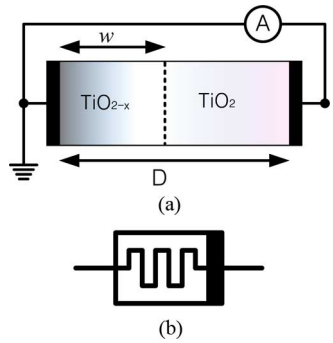


Fig. 1. (a) Structure of the TiO_2 memristor TiO_2 and TiO_{2-x} layers are sandwiched between two platinum electrodes. When a voltage/current is applied, its memristance (resistance of the memristor in Ohms)/ memductance (conductance of the memristor) in siemens) is altered. (b) Symbol of the memristor.

where $w(t)/D$ is defined as the state variable. In the TiO_2 memristor [3], the rate of change of the state variable is defined as a function of current i; namely,

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{\rm ON}}{D}i(t) \tag{4}$$

where μ_v is the dopant mobility. This model is called a linear drift model since the velocity of the width is linearly proportional to the current.

The relationship between the flux and the charge of the TiO_2 memristor is given by [3]; see equation (5) at the bottom of the page.

From (2) and (5), we obtain

$$\begin{aligned} M &= \frac{d\varphi}{dq} \\ &= R_{\rm OFF}\left\{\left[1 + \frac{w_0}{D}\left(\frac{R_{\rm ON}}{R_{\rm OFF}} - 1\right)\right] - \frac{\mu_v R_{\rm ON}}{D^2}\left(1 - \frac{R_{\rm ON}}{R_{\rm OFF}}\right)q(t)\right\} \\ &\approx R_{\rm OFF}\left\{1 - \frac{\mu_v R_{\rm ON}}{D^2}q(t)\right\}. \end{aligned} \tag{6}$$

Observe that the memristance in (6) is a linear function of the charge $q(t)$. Fig. 1(b) shows the symbol of the memristor with the polarity indicated by a black bar at one end. It follows from (6) that the memristance M decreases when current flows from the left side toward the right (black bar) side.

III. Basic Memristor Emulating Circuit

Our memristor emulating circuit is designed in a way of composing the input resistance as a function of applied voltage or current. The circuit in Fig. 2(a) gives the idea on how to implement features of the memristor using an op amp circuit.

In the figure, a voltage equation at the input terminal of Fig. 2(a) is

$$v_{\rm in} = R_s i_{\rm in} + v_x \tag{7}$$

$$\varphi(t) = R_{\rm OFF}\left\{q(t)\left[1 + \frac{w_0}{D}\left(\frac{R_{\rm ON}}{R_{\rm OFF}} - 1\right)\right] - \frac{\mu_v R_{\rm ON}}{2D^2}\left(1 - \frac{R_{\rm ON}}{R_{\rm OFF}}\right)q(t)^2\right\} + \varphi_0 \tag{5}$$

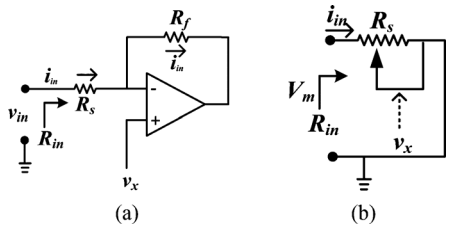


Fig. 2. Concept for implementing the proposed memristor emulator. (a) Input resistance as a function of voltage v_x. (b) Equivalent circuit.

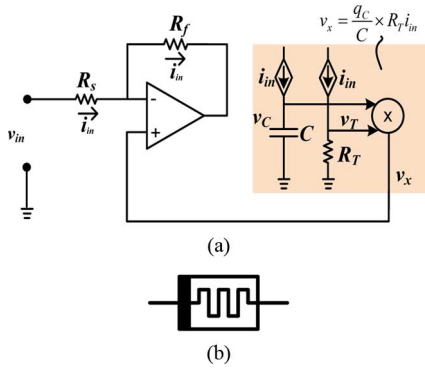


Fig. 3. Basic configuration of the incremental memristor. (a) Simplified circuit. (b) Symbol of the incremental memristor.

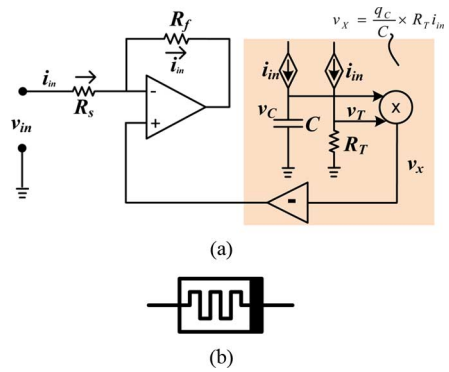


Fig. 4. Basic configuration of the decremental memristor. (a) Simplified circuit. (b) Symbol of the decremental memristor.

where $i_{\rm in}$ the input is current, R_s is a resistance at the inverting input terminal and v_x is the voltage applied to the positive terminal of the op amp.

Assume that the voltage v_x is proportional to input current $i_{\rm in}$, then

$$v_{\rm in} = R_s i_{\rm in} + m i_{\rm in} = (R_s + m)\, i_{\rm in} \tag{8}$$

where m is a proportionality coefficient and $v_x = m i_{\rm in}$. Equation (8) implies that the input resistance of the circuit is $R_s + m$. If we can control m so that it is time integral of the input current $i_{\rm in}$, then, the circuit in Fig. 2 acts as a memristor. To emulate v_x in (8), three devices (a capacitor, a resistor, and a voltage multiplier) are utilized, in which the voltage from the capacitor and that from the resistor are multiplied using a voltage multiplier as in Fig. 3 [see the right side of Figs. 3(a) and 4(a)].

In the figure, the capacitor produces a voltage v_C by integrating the current $i_{\rm in}$, and the resistor produces a voltage proportional to the current $i_{\rm in}$. These two voltages are multiplied by a voltage multiplier. The output voltage v_x of the voltage multiplier is given by

$$v_x = \frac{q_C}{C} \times R_T i_{\rm in} \tag{9}$$

where R_T is the resistance in Fig. 3(a). Therefore, the input voltage $v_{\rm in}$ is

$$v_{\rm in} = \left(R_s + \frac{q_C}{C} \times R_T\right) i_{\rm in} \tag{10}$$

and the input resistance $R_{\rm in}$ of Fig. 3 is $R_s + (q_C/C) \times R_T$. When a positive pulse is applied at the input terminal, the resistance increases proportional to the time integral of input current with offset R_S. We call this the incremental memristor configuration.

Observe that the memristance in (10) is composed of a fixed part R_S and a variable part $(q_C/C) \times R_T$. Let the voltages corresponding to the fixed part and the variable part of memristance be V_m and v_m, respectively, namely,

$$v_{\rm in} = V_m + v_m. \tag{11}$$

In the *hp* TiO_2 memristor, the fixed part of the memristance is normally much smaller than that of the variable part. Fig. 3(a) shows the simplified circuit of the incremental memristor.

In memristor, if a positive voltage is applied to the opposite polarity of the incremental memristor, the memristance is decreased. We call this the decremental memristor configuration. By adding a voltage inverter after the voltage multiplier, the decremental memristor configuration can be implemented. The input voltage in this case is

$$v_{\rm in} = V_m - v_m. \tag{12}$$

The resultant input resistance of the decremental memristor configuration is

$$R_{\rm in} = R_s - \frac{R_T}{C} q_C(t) = R_s \left(1 - \frac{R_T}{C R_s} q_C(t)\right). \tag{13}$$

Here, the input resistance is equal to the subtraction of the variable part $(R_T/C) \times q_C(t)$ from the fixed part R_s of the memristance. Fig. 4(a) shows the simplified circuit of the decremental memristor and Fig. 4(b) is its symbol. Observe that (13) is the same expression of the memristance in (6), which implies that circuit in Fig. 4(a) acts as memristor.

A full schematic of a basic incremental memristor configuration is shown in Fig. 5. The schematic of a decremental memristor is the same as that of incremental memristor except for an analog inverter inserted at the end of the multiplier. In practice, the resistance R_s is chosen to be small (around 5 kΩ) for the incremental memristor and large (around 16 kΩ) for the decremental memristor configurations.

When an input voltage is applied at a memristor emulator, it is converted into an input current $i_{\rm in}$ with a resistor R_s and op amp U0 via the virtual ground constraint. Since the current $i_{\rm in}$ is used at several places shown in Figs. 3(a) and 4(a), its replicas are generated using current mirrors. Observe that a current mirror copies single directional currents only. For bidirectional (positive and negative) currents, $i_{\rm in}$ must be separated into a positive part and a negative part, and processed separately at different

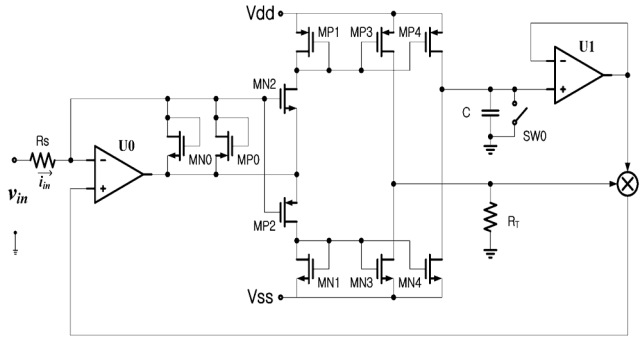


Fig. 5. Schematic of a basic incremental memristor configuration.

parts of the circuit. In the circuit of Fig. 5, the positive part of the current, duplicated by a current mirror MN0 and MN2 is fed into a resistor $\mathrm{R_T}$ and a capacitor C by current mirror MP3 and MP4 with couple of MP1 respectively. On the other hand, MP0 and MP2 acts as the negative part of current mirror that flows out from resistor $\mathrm{R_T}$ and capacitor C by current mirror MN3 and MN4 with MN1 couple transistor, respectively.

One of the distinguished features of a memristor is the capability of keeping the programmed information for a long time until new programming inputs are presented. The charge stored at capacitor C is the programmed information in our memristor emulator. To avoid discharging during the period when an input signal does not exist, the path to the output terminal is connected to the gate of a MOS type buffer U1.

IV. Expandable Model of Memristor Emulator

A. Serial Connection

One of the important function of the memristor emulator is for the development of memristor application circuits. In such applications, the compatibility with other devices is very important.

When a voltage is applied at serially connected memristors, the input voltage is distributed to every memristor according to the voltage law so that the sum of each memristor voltage is equal to the input voltage like in ordinary resistors. Also, a voltage measured in front of the K_{th} memristor is the sum of voltages from the K_{th} memristor to the last memristor. Let such voltage measured in front of the K_{th} memristor be $v\,(k)$. Then, $v\,(k)$ is

$$\begin{aligned} v\,(k) &= (V_m^k + v_m^k) + (V_m^{k+1} + v_m^{k+1}) \\ &\quad + (V_m^{k+2} + v_m^{k+2}) \ldots \\ &= (V_m^k + v_m^k) + v(k+1) \end{aligned} \tag{14}$$

where V_m^k and v_m^k are the voltages corresponding to the fixed part and the variable part of the K_{th} memristor as in (11). Also, $v(k+1)$ is the sum of the voltages from the $(k+1)th$ memristor to the last memristor.

Equation (14) can be rearranged as

$$v\,(k) = V_m^k + (v_m^k + v(k+1)). \tag{15}$$

From (15), each memristor requires three parts of voltage addition. The addition between the fixed voltage V_m^k and the variable voltage $(v_m^k + v(k+1))$ are performed with an op amp. However, the addition in $(v_m^k + v(k+1))$ is implemented by an analog Adder as shown at the bottom of Fig. 6(a) and (b), where the terminal indicated as $v(k+1)$ is for the voltage of the next memristor.

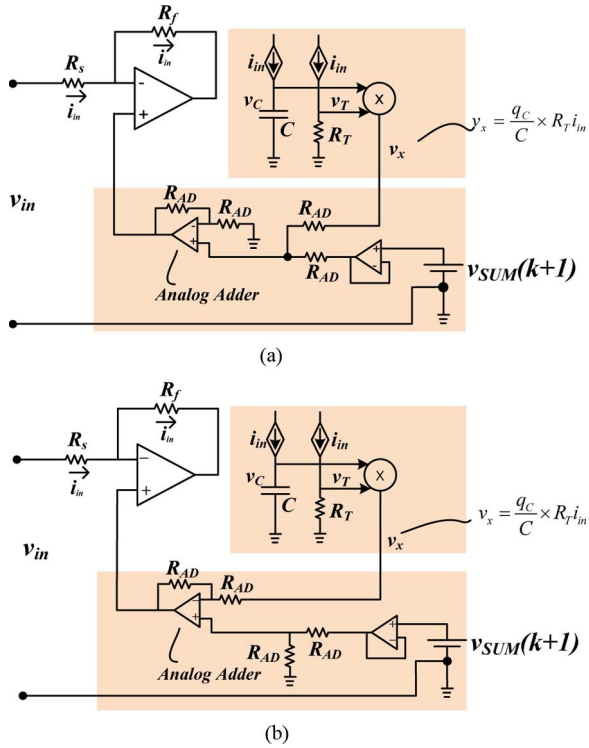


Fig. 6. Expandable memristor configurations. (a) Incremental configuration. (b) Decremental configuration.

The expandable structure of an incremental memristor is shown in Fig. 6(a). Since the memristance of the decremental memristor configuration is reduced by subtracting the variable part from the fixed part of the memristance as in (13), its slightly different expandable structure is shown in Fig. 6(b). The full schematic including the expandable structure is shown in the Appendix.

Fig. 7 illustrates an example of two serially connected memristors with opposite polarities, where Fig. 7(a) is a symbol connection and Fig. 7(b) is its simplified circuits. In serially connected devices, the currents at each device should be common. To implement this constraint, the input current of the first memristor is replicated and fed to every memristor individually to produce its voltage in the memristor emulator. The dependant current source shown at the beginning of the second memristor in Fig. 7(b) is to implement this common current constraint.

B. Parallel Connection

In the case of parallel connection, the same input voltage v_{in} must be applied at both input terminals of the parallel devices. Fig. 8 illustrates an example of a parallel connection of two memristors with opposite polarities, where Fig. 8(a) is a symbol connection and Fig. 8(b) is its simplified circuits. For two memristor with opposite polarities, the connection diagram is shown in Fig. 8. The two component memristor currents are

$$\begin{aligned} i_{\mathrm{in}1} &= \frac{v_{\mathrm{in}} + v_{C1} R_T i_{\mathrm{in}1}}{R_s} \\ i_{\mathrm{in}2} &= \frac{v_{\mathrm{in}} - v_{C2} R_T i_{\mathrm{in}2}}{R_s} \end{aligned} \tag{16}$$

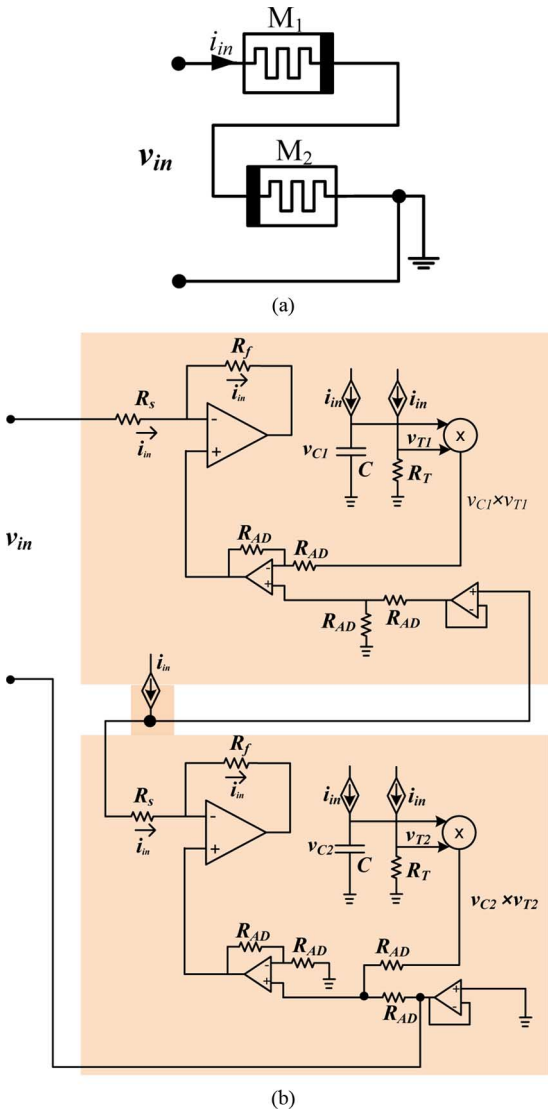


Fig. 7. Two serially connected memristors with opposite polarities. (a) Symbol connection. (b) Connection diagram of the simplified circuits.

where the first one is the equation for a decremental memristor and the second one is that for an incremental memristor. Rearranging the equations in (16), we obtain

$$i_{\text{in1}} = \frac{v_{\text{in}}}{R_s - v_{C1}R_T}$$
$$i_{\text{in2}} = \frac{v_{\text{in}}}{R_s + v_{C2}R_T}. \tag{17}$$

The total input current i_{in} is

$$i_{\text{in}} = i_{\text{in1}} + i_{\text{in2}} = \left(\frac{1}{M_1} + \frac{1}{M_2}\right) v_{\text{in}}. \tag{18}$$

Therefore, the total memristance M is

$$M = \frac{M_1 M_2}{M_1 + M_2}. \tag{19}$$

It follows that Fig. 8(a) acts as a parallel connection of the memristors M_1 and M_2 and Fig. 8(b) represents its connection symbol.

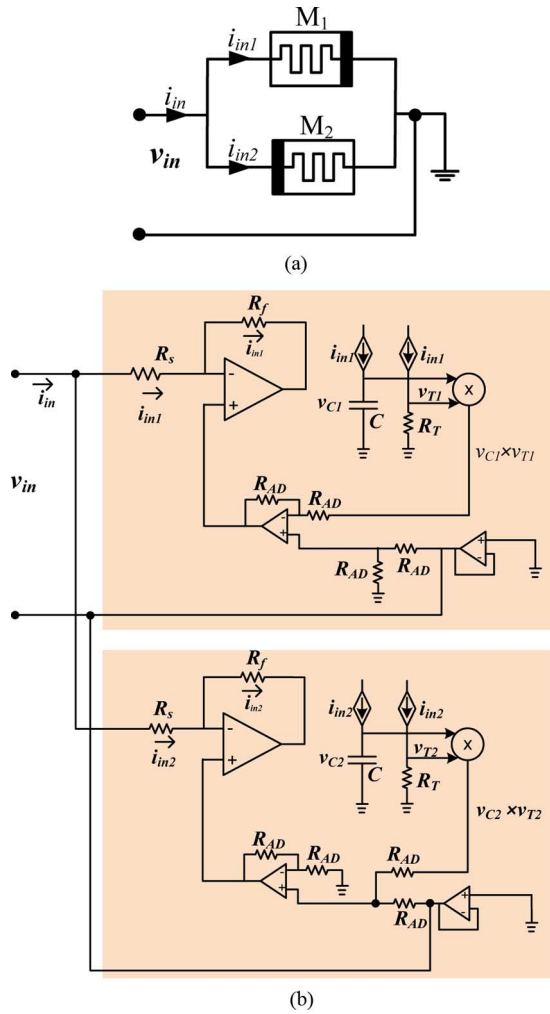


Fig. 8. Parallel connection of two memristors with opposite polarities. (a) Symbol connection. (b) Connection diagram of the simplified circuits.

C. Hybrid Connection

More complicate circuit is with hybrid model composited with serial and parallel circuits. There could be many different combinations in hybrid model. One of them is a circuit consisting of three memristors in which one memristor is connected serially to two parallel memristors as illustrated in Fig. 9. Fig. 9(a) is its symbol connections and Fig. 9(b) is the corresponding circuit which is built with the proposed expandable memristor emulating circuit shown in Fig. 6. The composite memristor circuit acts as a single memristor is given by

$$M_{\text{composite}} = M_1 + \frac{M_2 M_3}{M_2 + M_3}. \tag{20}$$

V. Experiments and Simulations

We have built a memristor emulator circuit which works like a TiO_2 memristor [3] and is expandable via serial, parallel and hybrid connections. It has been tested with hardware experiments and simulations. The supplied power is $+5$ V and -5 V and it was designed for both current controlled and voltage controlled memristor models.

The first experiment is to show our memristor emulator can be implemented with ordinary circuit devices. The decremental

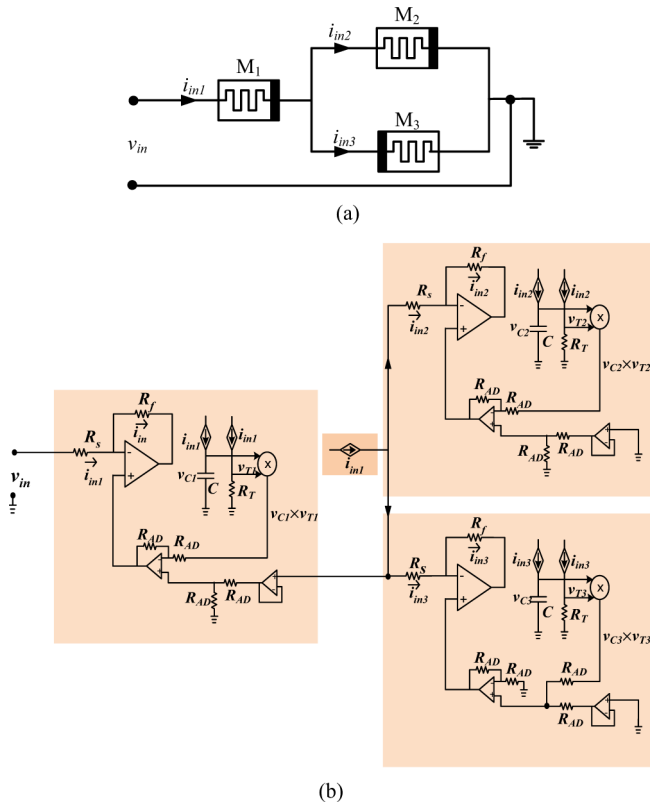


Fig. 9. A hybrid circuit in which one memristor is connected serially to two memristors in parallel. (a) Symbol connections. (b) Simplified circuit.

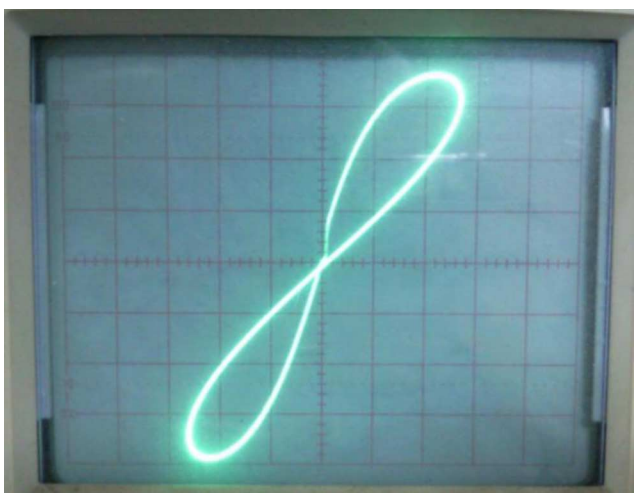


Fig. 10. Oscilloscope trace of the pinched hysteresis loop of our memristor emulator at 100 Hz.

memristor in Appendix A was built on a breadboard with the devices listed in Appendix B. Experiments were conducted to confirm the pinched hysteresis loop fingerprint of the memristor. The input signal was a 100-Hz sinusoidal voltage with 2 Vp-p. Fig. 10 shows an oscilloscope display of a pinched hysteresis loop measured from the memristor emulator. The pinched loop shows that the memristance varies according to the input voltage/current, where the inverses of slope at various points of the loop are the memristances. Voltage waveforms measured at several nodes are shown in Fig. 11.

The variations of the pinched hysteresis loop for various frequencies at 100, 200, 400, and 800 Hz are also shown in Fig. 12.

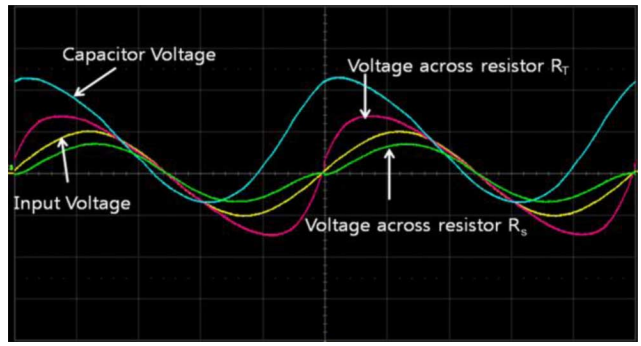


Fig. 11. Voltage waveforms measured at several nodes of the hardware circuit in Appendix A for the experiment of Fig. 10.

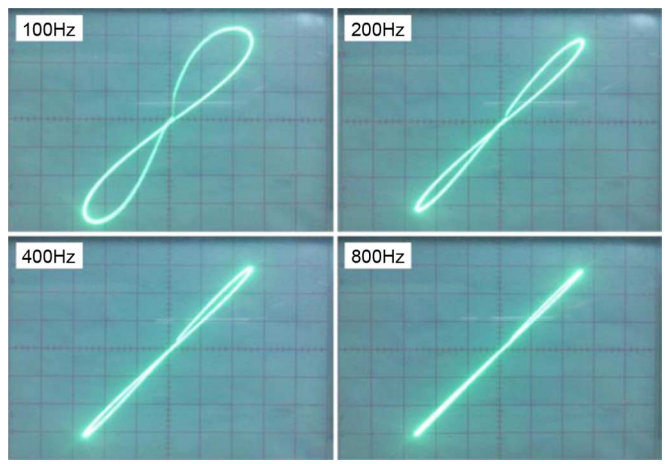


Fig. 12. Oscilloscope tracings of the pinched hysteresis loops recorded from our memristor emulator for input signals with various frequencies.

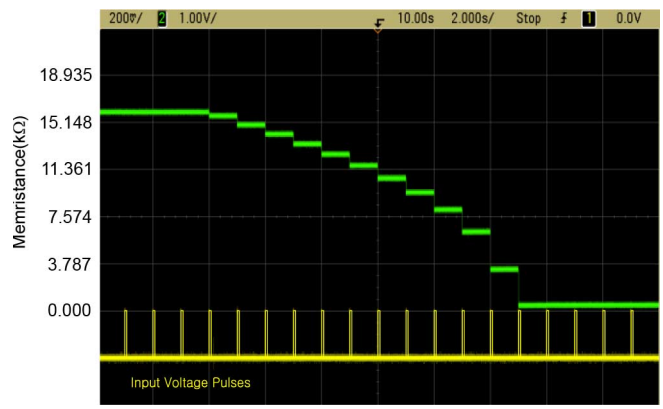
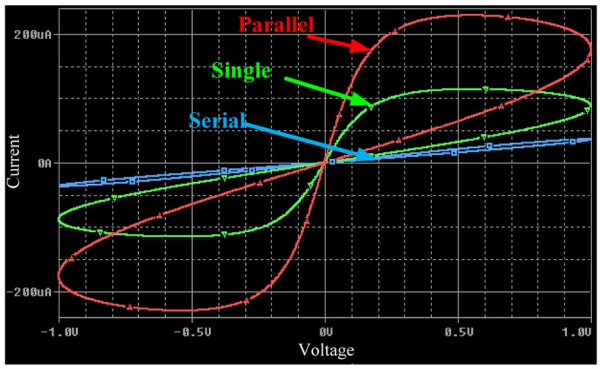


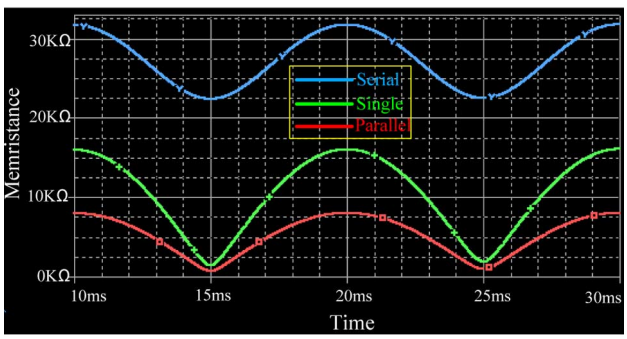
Fig. 13. Oscilloscope trace showing the memristance change measured from the memristor emulator circuit when identical positive rectangular pulses (0.1 V, 2.5-ms duration, 10-s period) are applied repeatedly. During inter-pulse period, the memristance is nonvolatile. Note that the decrement step size is bigger as more pulses are applied since the memristance is reduced proportional to the integration of applied voltage.

Note the frequency dependence of the pinched hysteresis loop is another unique feature of the memristor.

Another unique feature of the memristor is the nonvolatility of its memristance during the idling periods when no input signals are applied. Since most memristor application circuits are expected to operate with pulsed input signals, such nonvolatility feature is very important. Fig. 13 shows the memristance change measured from our implemented memristor emulator circuit, when a rectangular pulse train (0.1 V, 2.5 ms duration, 10-s period) is applied across a decremental memristor once every 10 s.



(a)



(b)

Fig. 14. (a) Pinched hysteresis loops of memristors in single, serial, and parallel connections when sinusoidal voltage signals (2 V p-p, 100 Hz) are applied, where $\mathrm{Rs} = 16\ \mathrm{K\Omega}$, $\mathrm{C} = 0.1\ \mu\mathrm{F}$, and $\mathrm{R_T} = 4\ \mathrm{k\Omega}$. The slope of the pinched hysteresis loop of the serial connection is a half and a quarter of the single and the parallel memristor connections, respectively. (b) Variations of the memristances along the time for these three cases.

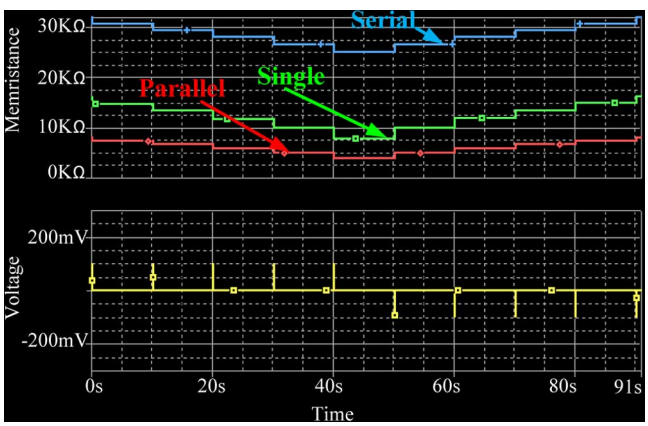


Fig. 15. Variation of memristance when voltage input pulses (0.1-V amplitude, 5-ms width) are applied successively to the single memristor, serial and parallel connected memristors at every 10 s.

Observe that the memristance is nonvolatile during non-pulse period. Whenever, rectangular pulses are presented, the graph changes abruptly. The rate of the memristance change (step size) increases as more voltage pulses are applied since the memristance decreases as input voltage pulses are applied.

To utilize the memristor emulator for developing memristor circuit application, the memristors should be connectable in series, in parallel or in hybrid (series-parallel) with other devices. PSPICE simulations with memristor emulator circuits of same polarities and connected in series, in parallel have been conducted to demonstrate our memristor emulator circuit. Fig. 14(a) shows pinched hysteresis loops of memristors in single, serial, and parallel, when sinusoidal voltage signals (2 V p-p, 100 Hz) are applied where $Rs = 16\ \mathrm{K\Omega}$, $C = 0.1\ \mu\mathrm{F}$, and $R_T = 4\ \mathrm{K\Omega}$ The slope of the pinched hysteresis loop of the serial connection is a half and a quarter of the single and the parallel memristor connections, respectively. Fig. 14(b) shows the variations of the memristances along the time for these three cases.

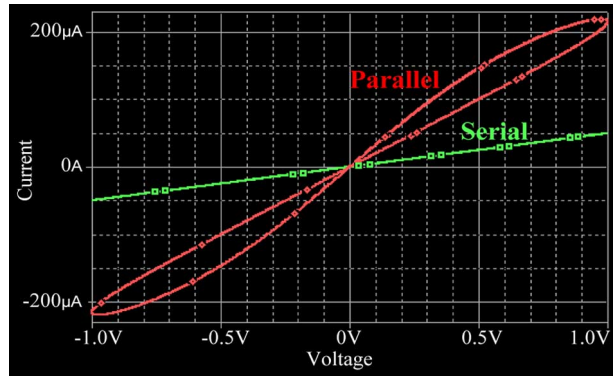
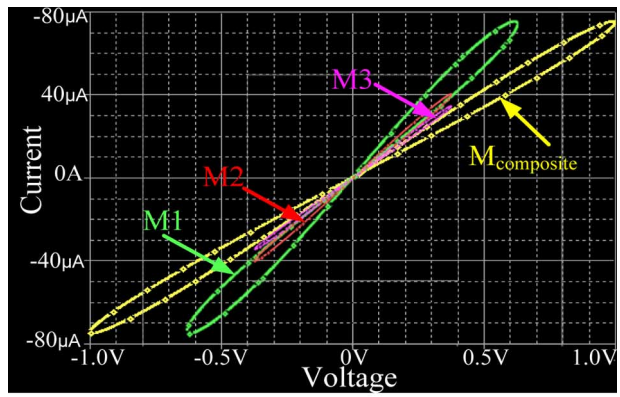
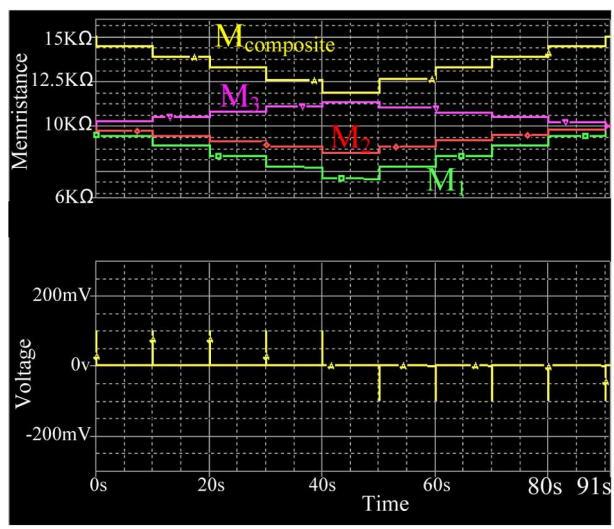


Fig. 16. Voltage-current curve of two-memristor circuit connected in series, or in parallel with opposite polarities. When two memristors with opposite polarities are connected in series, the total change of memristance is negligible due to the complementary action between two memristors.



(a)



(b)

Fig. 17. Simulation results of a hybrid circuit in which a memristor is connected serially to two parallel memristors as in Fig. 9. (a) Pinched hysteresis loops when sinusoidal voltage input signals (2 V p-p, 300 Hz) are applied. (b) Memristance variations when voltage input pulses (0.1-V amplitude, 2-ms width) are applied successively at every 10 s.

Simulations with pulse inputs have also been made for these three configurations. Fig. 15 shows the memristances for a single memristor, and for the series and parallel connected memristors when five positive and five negative voltage pulses (0.1-V amplitude, 5-ms width) are applied successively at every 10 s. The slope of the memristance variation in the serial connection case is two times and four times steeper than those of the single and the parallel circuit cases, respectively.

In contrast to the above cases, the connections of two memristors in opposite polarities as shown in Figs. 7 and 8 have been conducted, where memristances are $\mathrm{M}_1 = 10\ \mathrm{K}\Omega$, $\mathrm{M}_2 = 10\ \mathrm{K}\Omega$, respectively, and the input is a sinusoidal voltage signal (2 V p-p, 300 Hz). When two memristors with opposite polarities are connected in series, the total change of memristance is negligible and its *V-I* curve is linear due to the complementary action between two memristors as in Fig. 16. When two memristors with opposite polarities are connected in parallel, the composite memristance shows still pinched hysteresis phenomenon as shown in Fig. 16.

Simulations for a hybrid circuit in which memristors are connected serially to two parallel memristors as in Fig. 9 have also been conducted. Memristances for these simulation were $\mathrm{M}_1 = \mathrm{M}_2 = \mathrm{M}_3 = 10\ \mathrm{K}\Omega$, where M_1 and M_2 are decremental and M_3 is incremental. The input is a sinusoidal voltage signal (2 V p-p, 300 Hz). Observe in Fig. 17(a) that the graphs of M_2 and M_3 are shrunk pinched hysteresis loops (almost linear in the graph) which implies that the memristance variation of M_2 and M_3 are much smaller than that of M1. This is due to the small amount of current flow through the individual memristor in a parallel memristor circuit. The composite memristance, $M_{composite}$, which is the total memristance among M_1, M_2, and M_3 reveals the biggest among all as we expected. Fig. 17(b) shows the memristance variation of each memristor while a sequence of pulse train is applied as indicated at the bottom. Observe that the memristances of M_1 and M_3 vary in opposite way since they are with opposite polarities.

VI. Conclusion

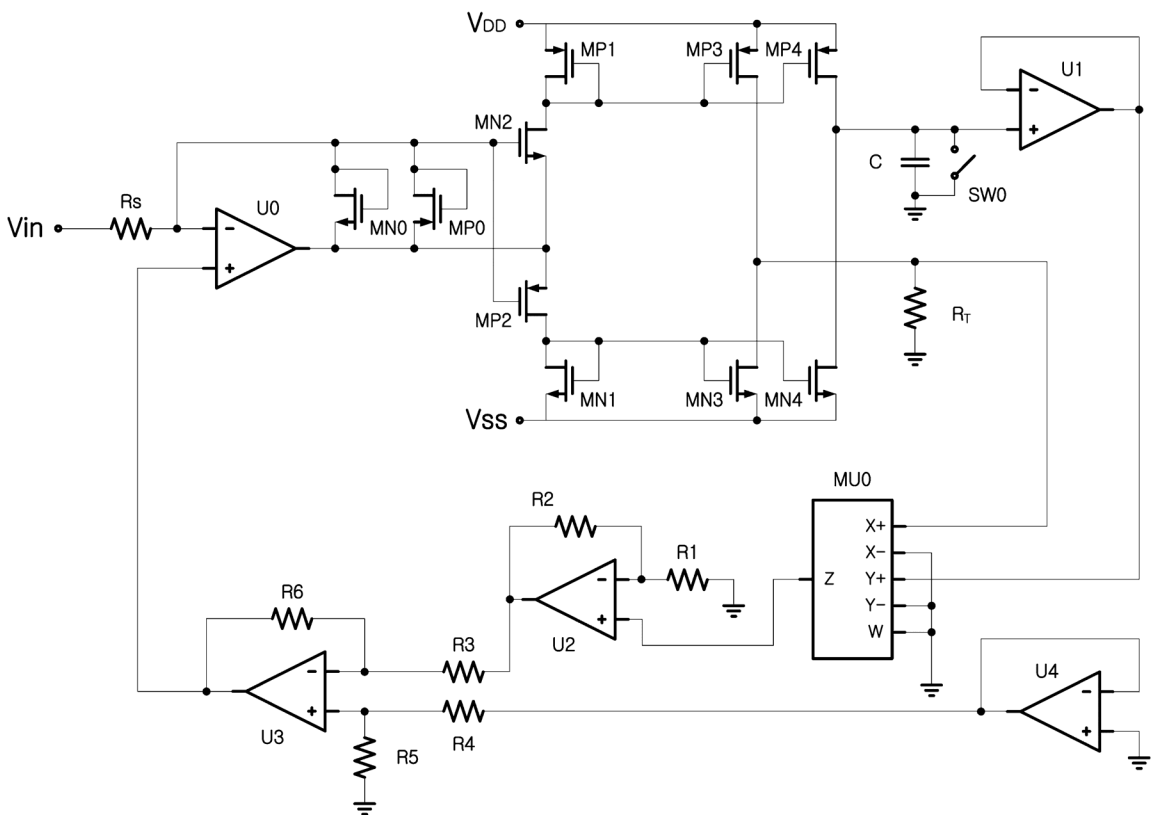
Memristor emulator which acts as a real memristor device is useful for developing memristor application circuits as well as for the memristor circuit demonstrations for educational purpose.

In this study, a memristor emulator has been designed and built with off-the-shelf solid state devices. Various features of this memristor emulator are tested via both circuit measurements and SPICE simulations. Experimental measurements are very similar to the real TiO_2 memristor [3]. We have also confirmed experimentally that our memristor emulator is nonvolatile over the time period of our experiments.

Our memristor emulator is also designed to be expandable. This feature has been proved via simulations; our memristor emulator can be connected in serial, in parallel, or in hybrid (serial and parallel combined) with other memristors with identical or opposite polarities. Also, it is switchable between the incremental and the decremental configuration by a simple change of the connections.

Appendix A

A Full schematics of the decremental memristor emulator with expandable non-volatile architecture.



APPENDIX B
PART LIST OF THE MEMRISTOR EMULATOR IN APPENDIX A

MN0 ~ MN4	ALD1116PAL	N-type MOSFET
MP0 ~ MP4	ALD1117PAL	P-type MOSFET
U0 ~ U4	TL082CP	OPAMP
MU0	AD633ANZ	Analog Multiplier
C	MF 0.1uF	Capacitor
Rs	Axial 1/4W 16KΩ	Resister
R_T	Axial 1/4W 4KΩ	Resister
R1, R3 ~ R6	Axial 1/4W 10KΩ	Resister
R2	Axial 1/4W 90KΩ	Resister
SW0	ITS-1109	Tact Switch

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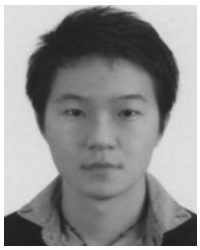
His main research interests include circuit design, cellular neural networks, analog Viterbi decoders, analysis of memristors, and memristive systems.



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