Chapter 4: Memory mapping in 64-bit mode

4.1 The memory mapping register

- Named "Control Register 3" (CR3)
    - A pointer to the top level of a hierarchical collection fo tables in memory which define the translation from virtual to physical addresses.
    - How the CPU starts the translation process
        - In the kernel an initial hierarchy of translation tables is prepared.
        - CR3 is filled with the address of the top level table in the hierarchy
            - The table is given the name Page Map Level 4 (PML4)
            - When the CPU is switched to using memory mapping on the next memory reference it usese CR3 to fetch entries from PMR4

4.2 Page Map Level 4

- Virtual addresses are broken into 6 fields.
    - The top most 16 bits are ignored.
        - supposed to be a sign extension of bit 47, but not part of address translation.
        - In Linux and OS X 47 is left as 0 in user processes.
        - In Kernel addresses they are all 1.
    - The next space is a set of 4 9 bit fields.
        - These undergo trnaslation.
    - Then a 12 bit page offset.

- Pages of memory are 2^12 = 4096 bytes.
    - Addresses are 8 bytes and 8 bytes = 512 = 2^9.
    - Thus the 9 bit fields allow for storing each of the 4 types of mapping tables in a page of memory.
- bits 39 - 47 are used to index into the PLM4 Table.
    - PLM4 is essentially an array of 512 pointers.
    - They point to pages of memory.
    - Not all entries in the PML4 will be valid.
        - the rightmost 12 bits of each pointer can be used to indicate validity.

4.3 Page Directory Pointer

- The next level is the page directory pointer tables.
- Each table is an array of 512 pointers.

4.4 Page Directory Table

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