Faculty of Engineering and Technology
Electrical and Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS
ENCS3330

HOMEWORK No. 1
Introduction on using Electric and LTspice simulator

Report

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Abstract

This report introduces the basic use of *Electric* and *LTspice* for digital integrated circuit design and verification. Electric was used to draw CMOS transistor-level schematics and create the corresponding layouts for an inverter, a 2-input NAND gate, and a 3-input NOR gate, while checking correctness through standard layout rules. LTspice was then used to perform transient simulations, apply input waveforms, and evaluate the timing behavior (rise/fall transitions) of the designed gates under a capacitive load. Finally, the three designed gates were combined in a top-level application to implement a 3-input AND function, demonstrating hierarchical design and end-to-end verification.

Keywords: Electric, LTspice, CMOS, schematic, layout, DRC, ERC, NCC, transient simulation, logic gates. “‘

Contents

List of Figures

1 Inverter (NOT Gate) Design

1.1 Inverter Schematic

The CMOS inverter was designed using one PMOS pull-up and one NMOS pull-down transistor. The sizing factors were chosen as $k_p = 30$ for the PMOS and $k_n = 10$ for the NMOS; therefore, the transistor widths were set to $W_n = k_n$ and $W_p = k_p$ (with the same channel length L for both devices).

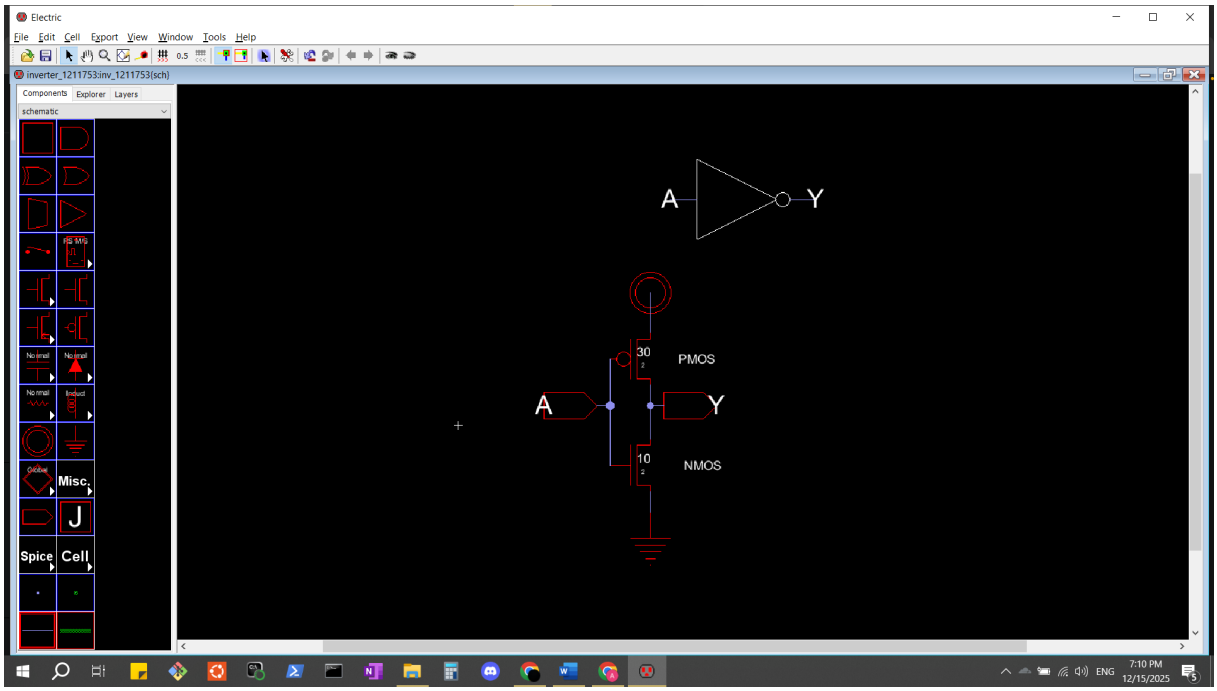

Figure 1: CMOS Inverter Schematic in Electric.

1.2 Inverter Schematic Simulation (LTspice)

The inverter schematic was simulated in LTspice using a PWL input waveform and a capacitive load at the output. The rise time (t_r) and fall time (t_f) were measured from the transient response.

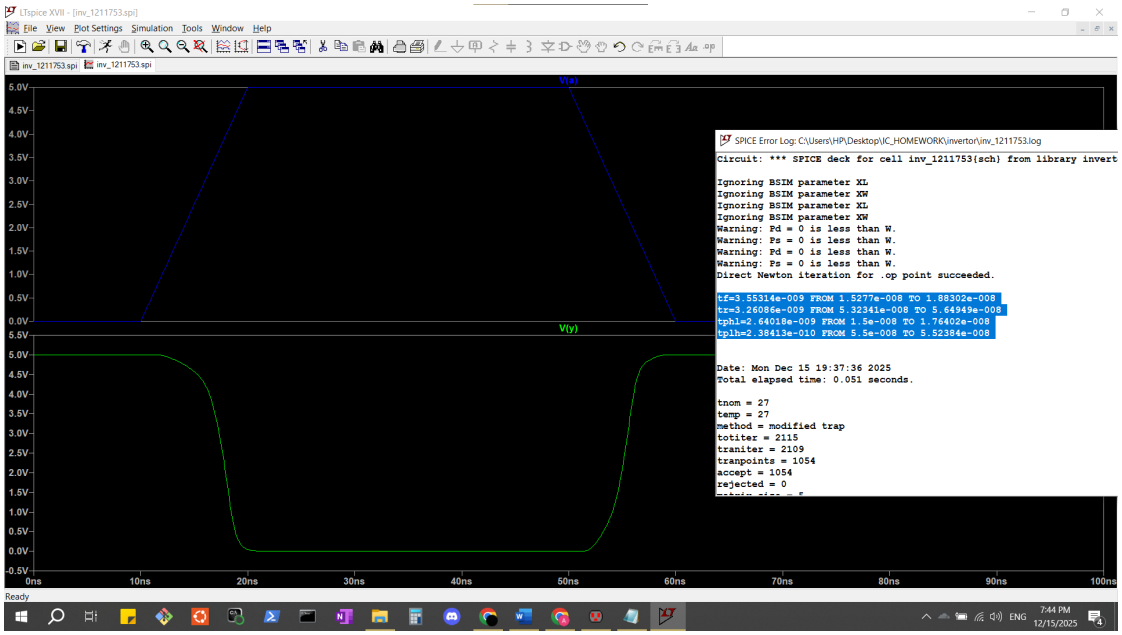

Figure 2: Transient simulation of the inverter schematic (LTspice).

Measured timing parameters (LTspice):

- **Fall time** $t_f = 3.55314 \times 10^{-9}\,\text{s} \approx 3.55\,\text{ns}$
  (from 15.277 ns to 18.8302 ns, 4.5 V $\rightarrow$ 0.5 V).
- **Rise time** $t_r = 3.26086 \times 10^{-9}\,\text{s} \approx 3.26\,\text{ns}$
  (from 53.2341 ns to 56.4949 ns, 0.5 V $\rightarrow$ 4.5 V).
- **Propagation delay** (high$\rightarrow$low output) $t_{pHL} = 2.64018 \times 10^{-9}\,\text{s} \approx 2.64\,\text{ns}$
  (input crosses 2.5 V at 15.0 ns, output crosses 2.5 V falling at 17.6402 ns).
- **Propagation delay** (low$\rightarrow$high output) $t_{pLH} = 2.38413 \times 10^{-10}\,\text{s} \approx 0.238\,\text{ns}$
  (input crosses 2.5 V at 55.0 ns, output crosses 2.5 V rising at 55.2384 ns).

1.3 Inverter Layout

The inverter layout was implemented in Electric and verified using DRC, ERC and NCC.

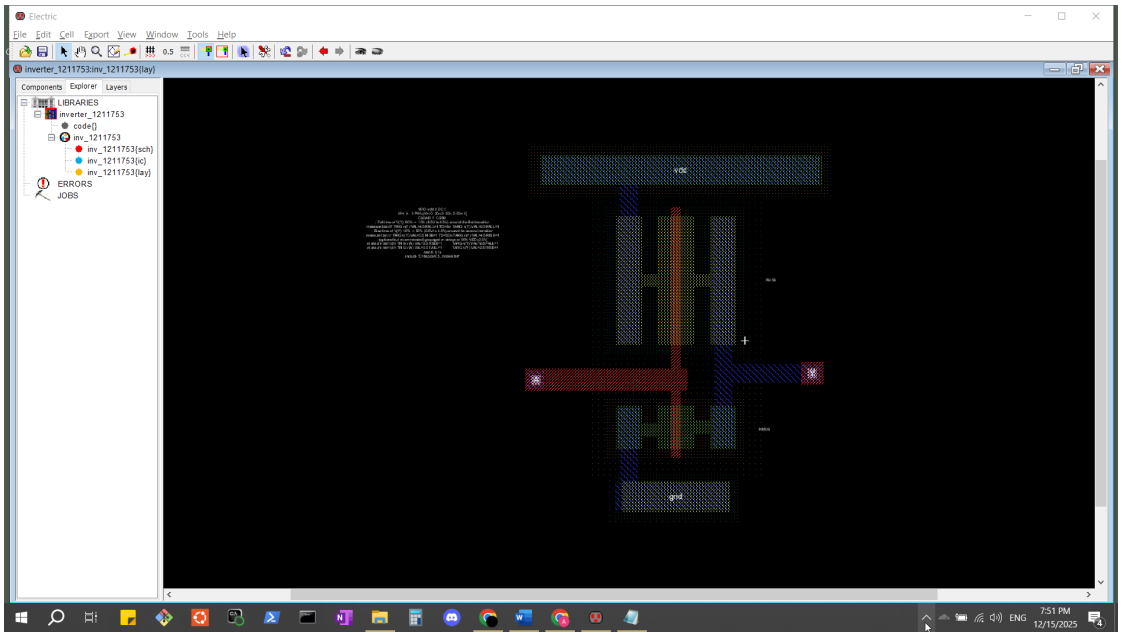

Figure 3: CMOS Inverter Layout in Electric.

LTspice simulation commands used for the extracted layout:

```
VDD  vdd 0 DC 5
VIN  A   0 PWL(10n 0  20n 5  50n 5  60n 0)
CLOAD Y  0 250f

.measure tran tf  TRIG v(Y) VAL=4.5 FALL=1 TD=8n  TARG v(Y) VAL=0.5 FALL=1

.measure tran tr  TRIG v(Y) VAL=0.5 RISE=1 TD=50n TARG v(Y) VAL=4.5 RISE=1

.measure tran tphl TRIG v(A) VAL=2.5 RISE=1          TARG v(Y) VAL=2.5 FALL
   =1
.measure tran tplh TRIG v(A) VAL=2.5 FALL=1          TARG v(Y) VAL=2.5 RISE
   =1

.tran 0 0.1u
.include "C:\ltspice\C5_models.txt"
```

2 Inverter Layout Simulation

After completing the inverter layout in Electric, the extracted netlist was simulated in LTspice to verify correct switching behavior and to measure timing parameters (rise time, fall time, and propagation delays).

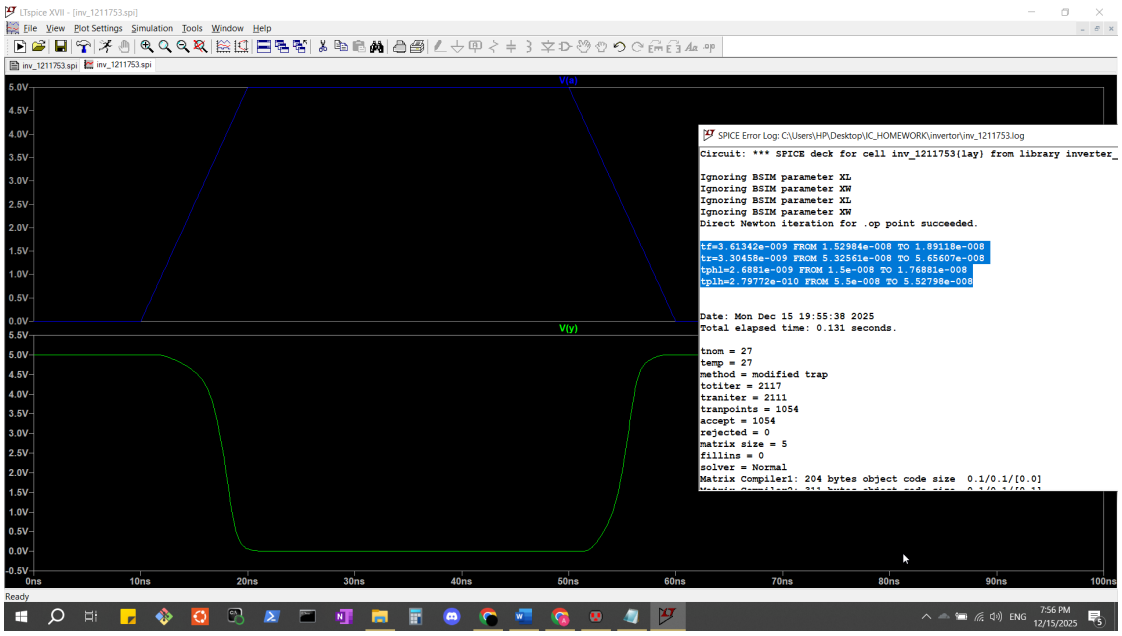

Figure 4: Transient simulation of the inverter layout (LTspice, extracted netlist).

Measured timing parameters (LTspice, extracted layout):

- **Fall time** $t_f = 3.61342 \times 10^{-9}\,\text{s} \approx 3.61\,\text{ns}$
  (from 15.2984 ns to 18.9118 ns, 4.5 V $\rightarrow$ 0.5 V).
- **Rise time** $t_r = 3.30458 \times 10^{-9}\,\text{s} \approx 3.30\,\text{ns}$
  (from 53.2561 ns to 56.5607 ns, 0.5 V $\rightarrow$ 4.5 V).
- **Propagation delay** (high$\rightarrow$low output) $t_{pHL} = 2.68810 \times 10^{-9}\,\text{s} \approx 2.69\,\text{ns}$
  (input crosses 2.5 V at 15.0 ns, output crosses 2.5 V falling at 17.6881 ns).
- **Propagation delay** (low$\rightarrow$high output) $t_{pLH} = 2.79772 \times 10^{-10}\,\text{s} \approx 0.280\,\text{ns}$
  (input crosses 2.5 V at 55.0 ns, output crosses 2.5 V rising at 55.2798 ns).

Comparison: The extracted-layout simulation shows slightly larger timing values than the schematic simulation. This increase is expected because the layout introduces additional parasitic resistance and capacitance from diffusion regions and interconnects, which slows down the output transitions and increases the propagation delay.

3 2-Input NAND Gate Design

3.1 2-Input NAND Schematic

The 2-input CMOS NAND gate was designed using a pull-up network (PUN) consisting of two PMOS transistors in parallel, and a pull-down network (PDN) consisting of two NMOS transistors in series. The sizing factors were chosen as $k_p = 30$ for each PMOS and $k_n = 10$ for each NMOS; therefore, the transistor widths were set to $W_n = 2k_n$ and $W_p = k_p$ (with the same channel length L for all devices).

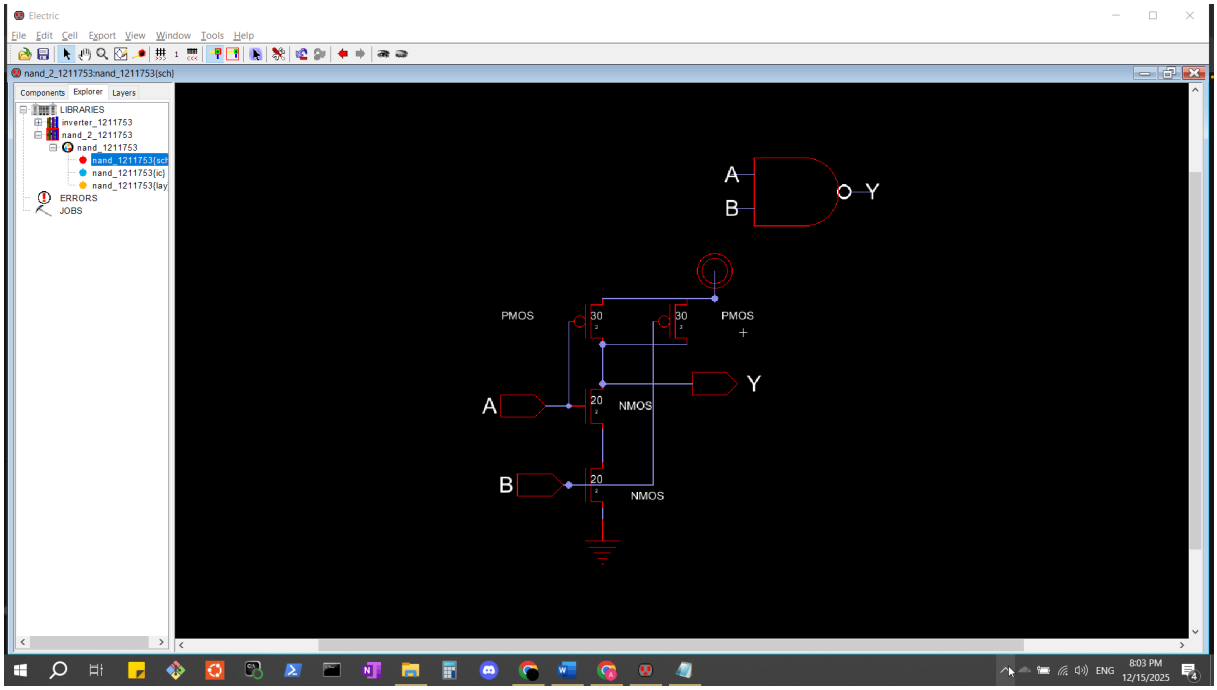

Figure 5: 2-input CMOS NAND schematic in Electric.

3.2 2-Input NAND Schematic Simulation (LTspice)

The NAND schematic was simulated in LTspice using PWL input waveforms and a capacitive load at the output. The rise time (t_r) and fall time (t_f) were measured from the transient response.

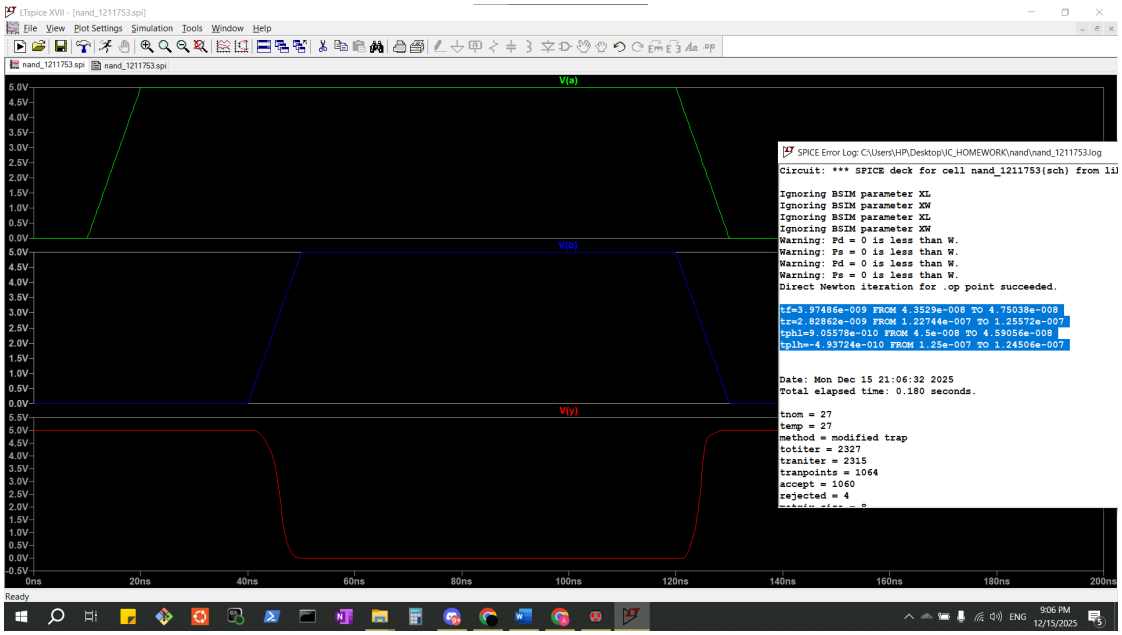

Figure 6: Transient simulation of the 2-input NAND schematic (LTspice).

Measured timing parameters (LTspice):

- **Fall time** $t_f = 3.97486 \times 10^{-9}\,\text{s} \approx 3.97\,\text{ns}$
  (from 43.529 ns to 47.5038 ns, 4.5 V $\rightarrow$ 0.5 V).
- **Rise time** $t_r = 2.82862 \times 10^{-9}\,\text{s} \approx 2.83\,\text{ns}$
  (from 122.744 ns to 125.572 ns, 0.5 V $\rightarrow$ 4.5 V).
- **Propagation delay** (high$\rightarrow$low output) $t_{pHL} = 9.05578 \times 10^{-10}\,\text{s} \approx 0.906\,\text{ns}$
  (input crosses 2.5 V at 45.0 ns, output crosses 2.5 V falling at 45.9056 ns).
- **Propagation delay** (low$\rightarrow$high output) $t_{pLH} = -4.93724 \times 10^{-10}\,\text{s} \approx -0.494\,\text{ns}$
  (input crosses 2.5 V at 125.0 ns, output crosses 2.5 V rising at 124.506 ns).

3.3 2-Input NAND Layout

The 2-input NAND layout was implemented in Electric and verified using DRC, ERC and NCC.

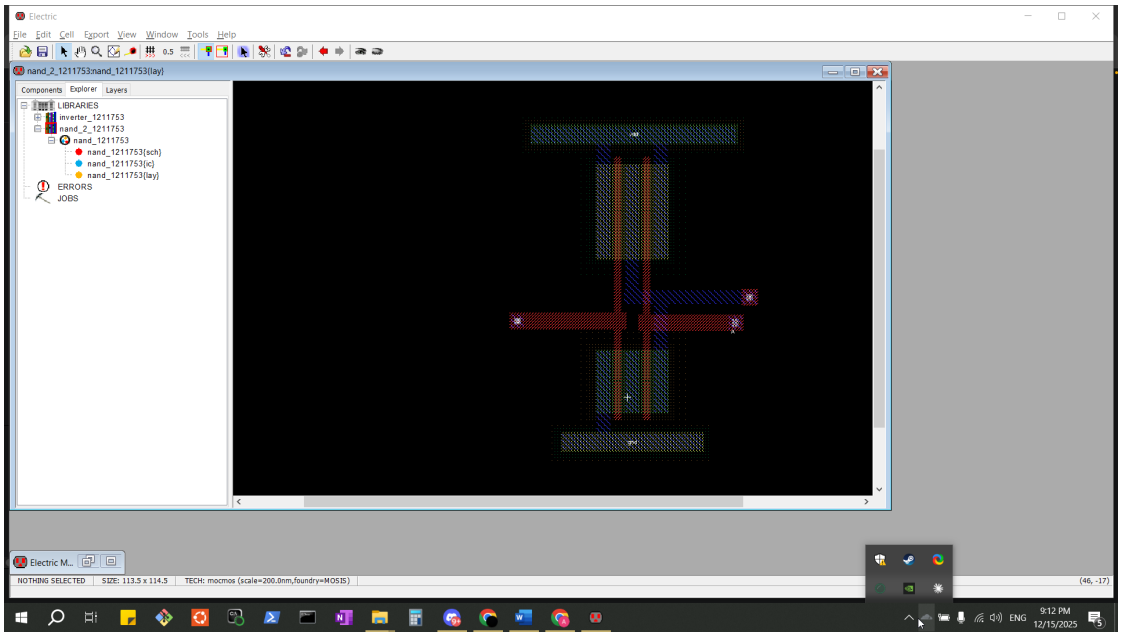

Figure 7: 2-input CMOS NAND layout in Electric.

LTspice simulation commands used for the extracted layout:

```
VDD  VDD 0 DC 5

VA   A   0 PWL(10n 0  20n 5   120n 5  130n 0)
VB   B   0 PWL(10n 0  40n 0    50n 5  120n 5  130n 0)

CLOAD Y 0 250f

.measure tran tf  TRIG v(Y) VAL=4.5 FALL=1          TARG v(Y) VAL=0.5 FALL
   =1
.measure tran tr  TRIG v(Y) VAL=0.5 RISE=1 TD=120n  TARG v(Y) VAL=4.5 RISE
   =1
.measure tran tphl TRIG v(B) VAL=2.5 RISE=1 TD=45n  TARG v(Y) VAL=2.5 FALL
   =1
.measure tran tplh TRIG v(A) VAL=2.5 FALL=1 TD=120n TARG v(Y) VAL=2.5 RISE
   =1
.tran 0 200n
.include "C:\ltspice\C5_models.txt"
```

4 2-Input NAND Layout Simulation

After completing the NAND layout in Electric, the extracted netlist was simulated in LTspice to verify correct switching behavior and to measure timing parameters (rise time, fall time, and propagation delays).

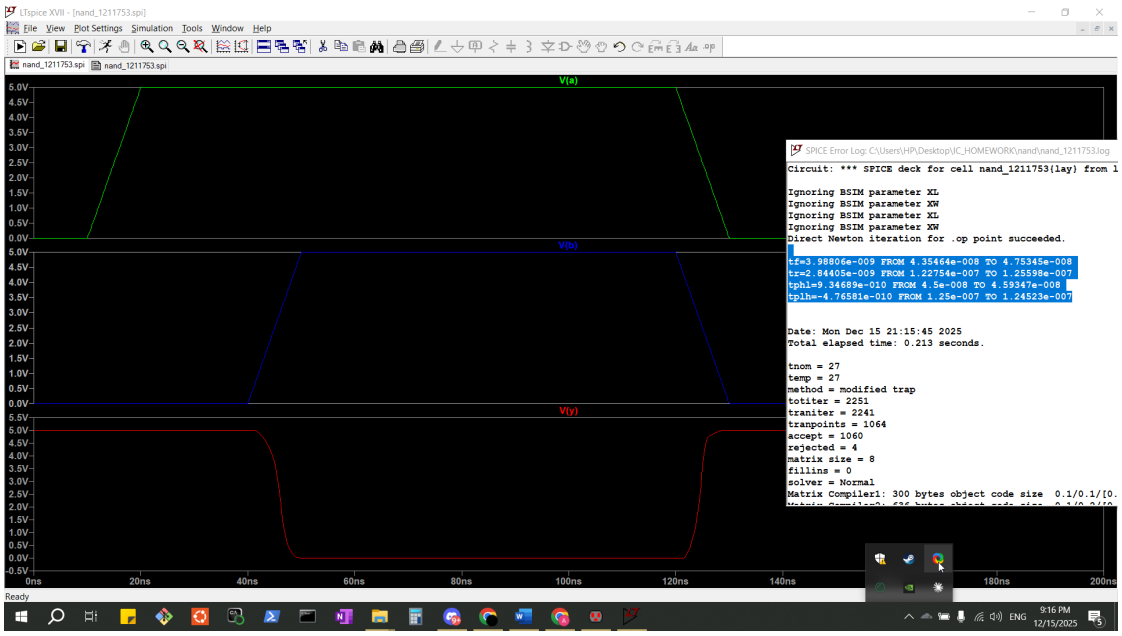

Figure 8: Transient simulation of the 2-input NAND layout (LTspice, extracted netlist).

Measured timing parameters (LTspice, extracted layout):

- **Fall time** $t_f = 3.98806 \times 10^{-9}\,\text{s} \approx 3.99\,\text{ns}$
  (from 43.5464 ns to 47.5345 ns, 4.5 V $\rightarrow$ 0.5 V).
- **Rise time** $t_r = 2.84405 \times 10^{-9}\,\text{s} \approx 2.84\,\text{ns}$
  (from 122.754 ns to 125.598 ns, 0.5 V $\rightarrow$ 4.5 V).
- **Propagation delay** (high$\rightarrow$low output) $t_{pHL} = 9.34689 \times 10^{-10}\,\text{s} \approx 0.935\,\text{ns}$
  (input crosses 2.5 V at 45.0 ns, output crosses 2.5 V falling at 45.9347 ns).
- **Propagation delay** (low$\rightarrow$high output) $t_{pLH} = -4.76581 \times 10^{-10}\,\text{s} \approx -0.477\,\text{ns}$
  (input crosses 2.5 V at 125.0 ns, output crosses 2.5 V rising at 124.523 ns).

Comparison: The extracted-layout simulation shows slightly larger timing values than the schematic simulation. This increase is expected because the layout introduces additional parasitic resistance and capacitance from diffusion regions and interconnects, which slows down the output transitions and increases the propagation delay.

5 3-Input NOR Gate Design

5.1 3-Input NOR Schematic

The 3-input CMOS NOR gate was designed using a pull-up network (PUN) consisting of three PMOS transistors in series, and a pull-down network (PDN) consisting of three NMOS transistors in parallel. The sizing factors were chosen as $k_p = 30$ for each PMOS and $k_n = 10$ for each NMOS; therefore, the transistor widths were set to $W_n = k_n$ and $W_p = 3k_p$ (with the same channel length L for all devices).

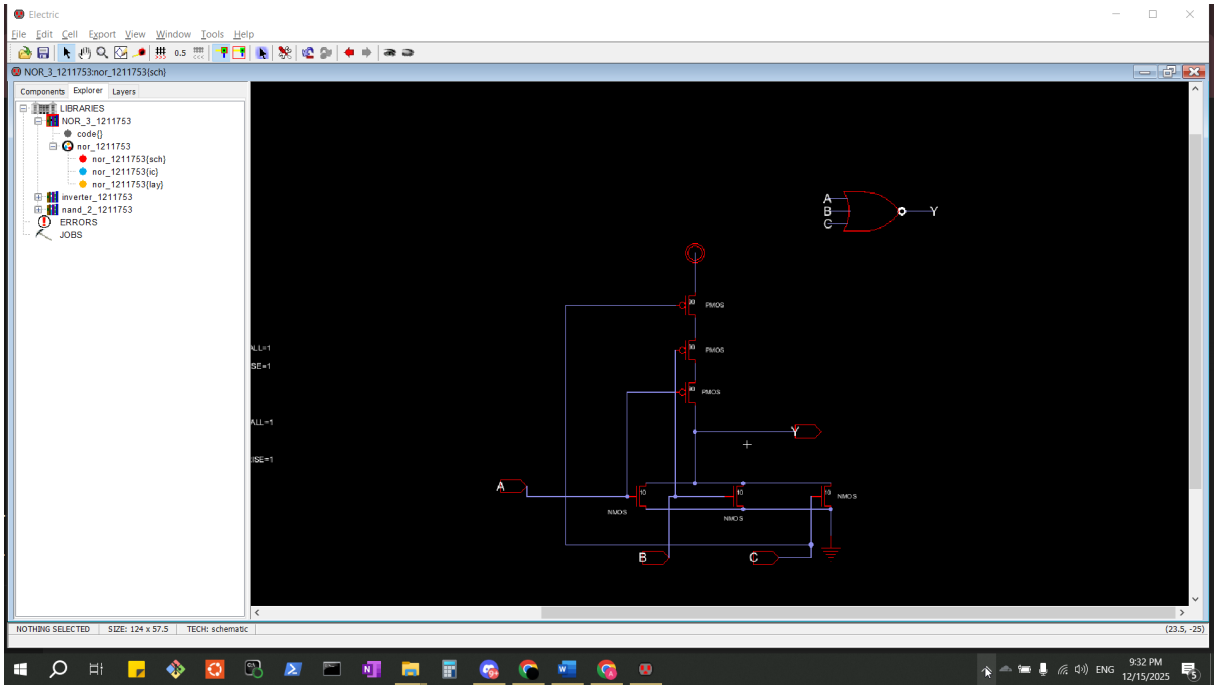

Figure 9: 3-input CMOS NOR schematic in Electric.

5.2 3-Input NOR Schematic Simulation (LTspice)

The NOR schematic was simulated in LTspice using PWL input waveforms and a capacitive load at the output. The rise time (t_r) and fall time (t_f) were measured from the transient response.

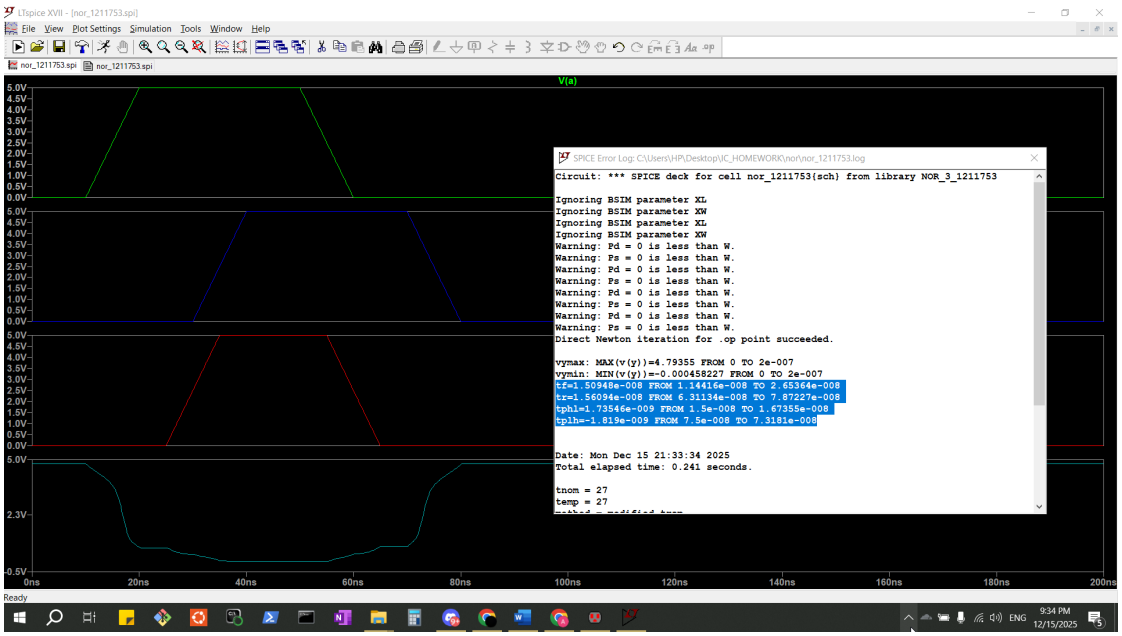

Figure 10: Transient simulation of the 3-input NOR schematic (LTspice).

Measured timing parameters (LTspice):

- **Fall time** $t_f = 1.50948 \times 10^{-8}\,\text{s} \approx 15.09\,\text{ns}$
  (from 11.4416 ns to 26.5364 ns, 4.5 V $\rightarrow$ 0.5 V).
- **Rise time** $t_r = 1.56094 \times 10^{-8}\,\text{s} \approx 15.61\,\text{ns}$
  (from 63.1134 ns to 78.7227 ns, 0.5 V $\rightarrow$ 4.5 V).
- **Propagation delay** (high$\rightarrow$low output) $t_{pHL} = 1.73546 \times 10^{-9}\,\text{s} \approx 1.74\,\text{ns}$
  (input crosses 2.5 V at 15.0 ns, output crosses 2.5 V falling at 16.7355 ns).
- **Propagation delay** (low$\rightarrow$high output) $t_{pLH} = -1.81900 \times 10^{-9}\,\text{s} \approx -1.82\,\text{ns}$
  (input crosses 2.5 V at 75.0 ns, output crosses 2.5 V rising at 73.1810 ns).

5.3 3-Input NOR Layout

The 3-input NOR layout was implemented in Electric and verified using DRC, ERC and NNC.

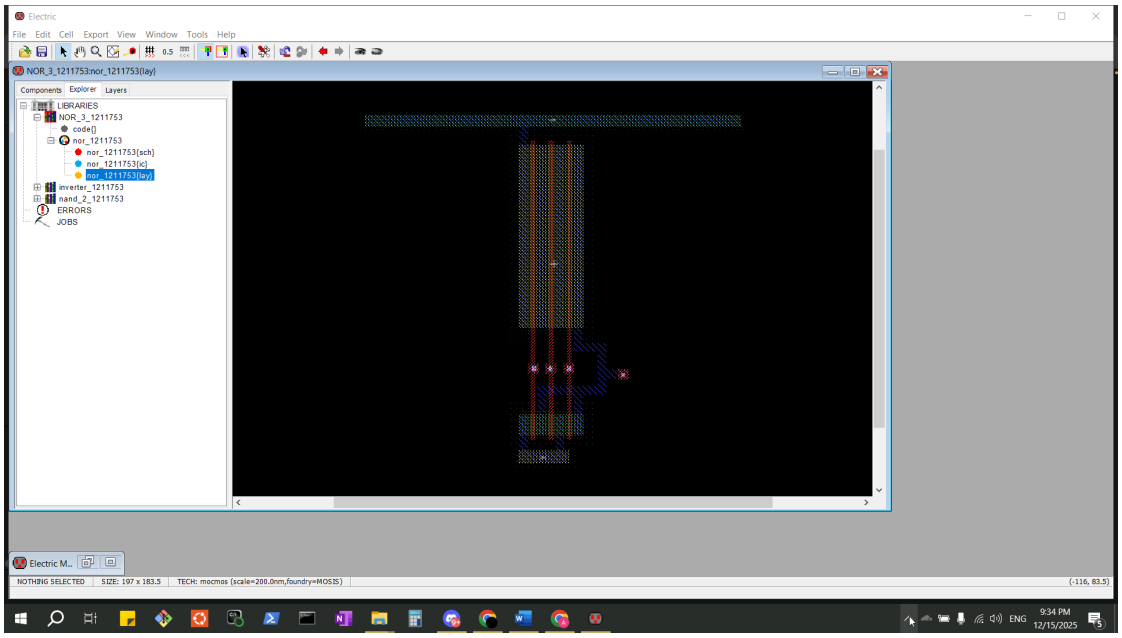

Figure 11: 3-input CMOS NOR layout in Electric.

LTspice simulation commands used for the extracted layout:

```
VDD  VDD 0 DC 5
VINA A 0 PWL(10n 0  20n 5  50n 5  60n 0  200n 0)
VINB B 0 PWL(10n 0  30n 0  40n 5  70n 5  80n 0  200n 0)
VINC C 0 PWL(10n 0  25n 0  35n 5  55n 5  65n 0  200n 0)
CLOAD Y 0 250f
.measure tran tf   TRIG v(Y) VAL=4.5 FALL=1  TARG v(Y) VAL=0.5 FALL=1
.measure tran tr   TRIG v(Y) VAL=0.5 RISE=1  TARG v(Y) VAL=4.5 RISE=1

.measure tran tphl TRIG v(A) VAL=2.5 RISE=1  TARG v(Y) VAL=2.5 FALL=1
.measure tran tplh TRIG v(B) VAL=2.5 FALL=1  TARG v(Y) VAL=2.5 RISE=1

.tran 0 200n
.include "C:\ltspice\C5_models.txt"
```

6 3-Input NOR Layout Simulation

After completing the NOR layout in Electric, the extracted netlist was simulated in LTspice to verify correct switching behavior and to measure timing parameters (rise time, fall time, and propagation delays).

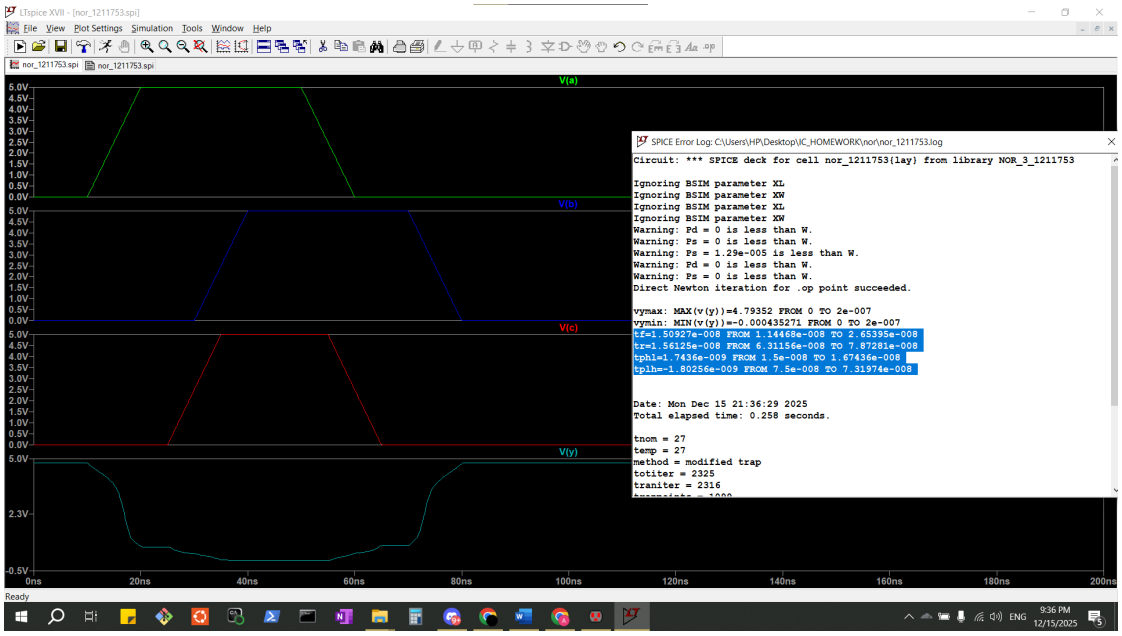

Figure 12: Transient simulation of the 3-input NOR layout (LTspice, extracted netlist).

Measured timing parameters (LTspice, extracted layout):

- **Fall time** $t_f = 1.50927 \times 10^{-8}\,\text{s} \approx 15.09\,\text{ns}$
  (from 11.4468 ns to 26.5395 ns, 4.5 V $\rightarrow$ 0.5 V).
- **Rise time** $t_r = 1.56125 \times 10^{-8}\,\text{s} \approx 15.61\,\text{ns}$
  (from 63.1156 ns to 78.7281 ns, 0.5 V $\rightarrow$ 4.5 V).
- **Propagation delay** (high$\rightarrow$low output) $t_{pHL} = 1.74360 \times 10^{-9}\,\text{s} \approx 1.74\,\text{ns}$
  (input crosses 2.5 V at 15.0 ns, output crosses 2.5 V falling at 16.7436 ns).
- **Propagation delay** (low$\rightarrow$high output) $t_{pLH} = -1.80256 \times 10^{-9}\,\text{s} \approx -1.80\,\text{ns}$
  (input crosses 2.5 V at 75.0 ns, output crosses 2.5 V rising at 73.1974 ns).

Comparison: The extracted-layout simulation shows slightly larger timing values than the schematic simulation. This increase is expected because the layout introduces additional parasitic resistance and capacitance from diffusion regions and interconnects, which slows down the output transitions and increases the propagation delay.

7 Triple AND Gate (Application) Design

7.1 Triple AND Schematic

The Triple AND gate was implemented at the transistor level using a combination of basic CMOS building blocks: a 2-input NAND gate, an inverter, and a 3-input NOR gate. The logic function is:

$$Y = A \cdot B \cdot C = \overline{\overline{A \cdot B} + \overline{C}}$$

First, the NAND gate generates $n1 = \overline{A \cdot B}$, the inverter generates $n2 = \overline{C}$, and finally the NOR stage produces $Y = \overline{n1 + n2 + 0}$.

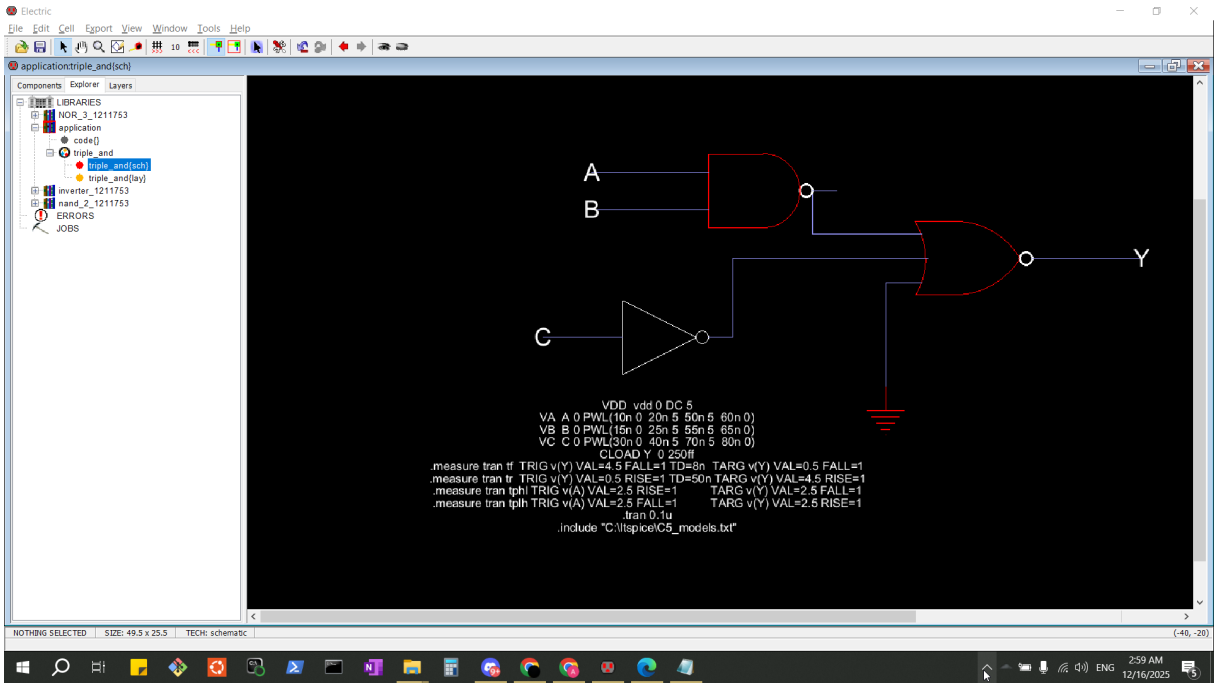

Figure 13: Triple AND (Application) schematic in Electric.

7.2 Triple AND Schematic Simulation (LTspice)

The Triple AND schematic was simulated in LTspice using PWL input waveforms for A, B, and C and a capacitive load at the output node Y. The transient response verifies correct logic behavior for different input transitions and combinations.

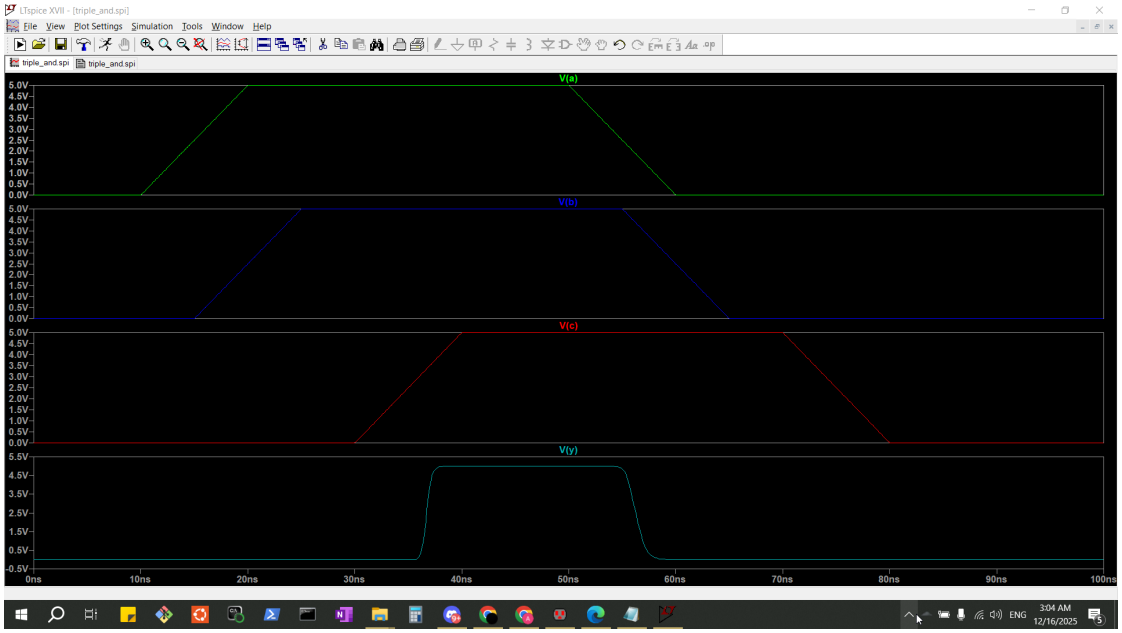

Figure 14: Transient simulation of the Triple AND schematic (LTspice).

8 Summary

In this work, three CMOS logic gates were designed and verified using Electric and LTspice. A CMOS inverter was implemented first to establish the basic pull-up/pull-down structure and sizing approach. Then, a 2-input NAND gate and a 3-input NOR gate were designed using standard static CMOS topology (PUN/PDN dual networks). For each gate, the schematic was created in Electric and simulated in LTspice to confirm correct switching behavior under time-varying inputs. After that, the layout was drawn in Electric and verified using DRC, ERC and NCC, and the extracted netlists were simulated in LTspice to evaluate the impact of parasitic capacitances and resistances on timing.

Overall, the extracted-layout simulations showed slightly slower transitions compared to schematic simulations, which is expected due to layout parasitics. The final results confirm that the designed gates operate correctly and that the layout implementations are consistent with their schematic behavior.

9 References

References

[1] CMOSedu, *LTspice and Electric Tutorial*.
https://cmosedu.com/cmos1/ltspice/ltspice_electric.htm