pre-Lab

Experiment No. 5 - Sequential Logic Circuits

*Student name: Abdulrahman shaheen.

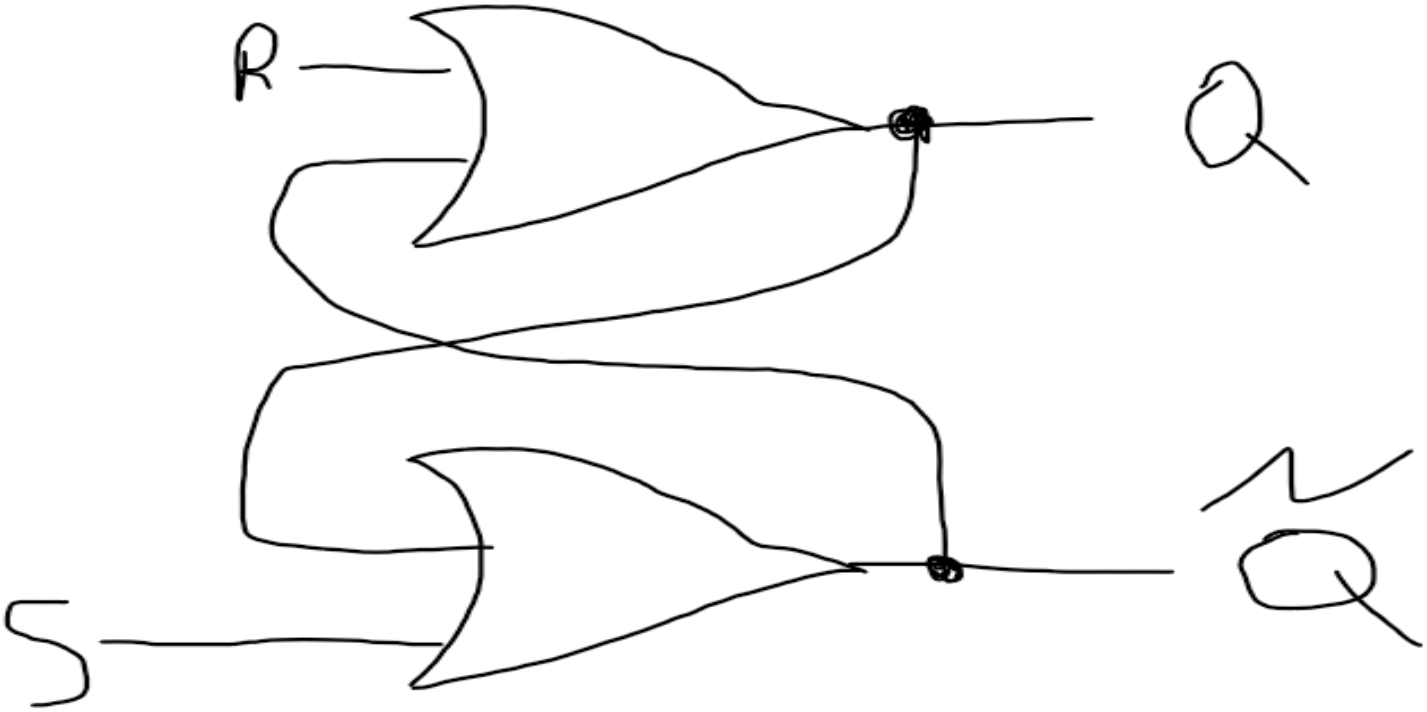
* ID#: 1211753.

* Instructor Name: Dr. Qadri Mayyala

* Date: 3/5/2023.

* Section: 2.

Q1) Design the Logic Diagram, function table of the SR latch using NOR gates, and explain how it works.



The R = S = 1 combination is called a restricted combination or a forbidden state because, as both NOR gates then output zeros, it breaks the logical equation Q = Q. The combination is also inappropriate in circuits where both inputs may go low simultaneously.

INPUT		OUTPUT		State
S	R	Q	$\bar{Q}$	
1	0	1	0	SET
0	0	1	0	No Change/ Memory
0	1	0	1	RESET
0	0	0	1	No Change/ Memory
1	1	0	0	Invalid