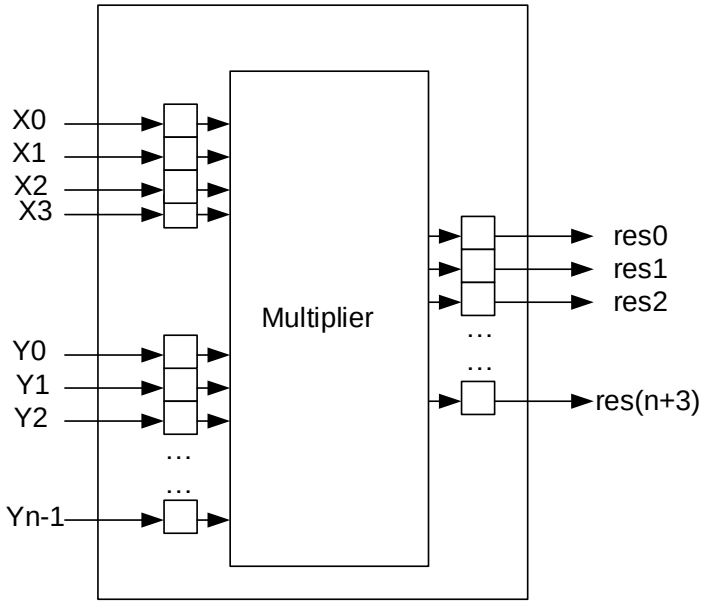
FACULTY OF ENGINEERIN AND TECHNOLOGY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
ADVANCED DIGITAL DESIGN
COURSE PROJECT

Objective:

The task is to design a fast multiplier and then to write a complete code for verification. You should search for information about the following types of adders: Ripple Adder, Look-ahead Adder, and the multiplier.

The Task:

Your task is to create a library element that has the following appearance:



The multiplier has two inputs: the multiplier x which is 4 bits, and the multiplicand y which is generic (n bits). Also, it has one output called res which is (n+4) bits. The inputs and the output are fed through flip-flops.

The multiplier is to be built **structurally from a library of gates**, which contains the following devices and delays in nanosecond (ns). (delay for each gate is specified in the following table).

Gate	delay
INV	2
AND	4
OR	4
NAND	5
NOR	5
XOR	7
XNOR	8

Stages of the project:

The project is split into two stages of complexity, and you can choose how complex a system you wish to attempt to implement.

Stage 1

The multiplier should be implemented using adders and the required gates. The first type of the adders to be used is the ripple carry adder which should be built structurally as follows:

- Built 1-bit full adder from the basic gates given above.
- Use the full adder to **build 4-bit adder**.
- Use as many blocks as you need of the **4-bit adder** when you build the multiplier.

You should produce complete verification (or large number of random cases) to demonstrate the multiplier working as expected. You should determine the maximum latency of the multiplier. And therefore, what is the maximum frequency of clock that can be applied to the flip-flops. Also, you should introduce an error in your design and to do a verification that will discover the error**.**

Stage 2

The second type of adders to be used is the carry look-ahead adder. You should implement a 4-bit adder structurally using the basic gates given above. Use as many blocks as you need of the 4-bit adder when you build the multiplier.

You should produce complete verification (or large number of random cases) to demonstrate the multiplier working as expected. You should determine the maximum latency of the multiplier. And therefore, what is the maximum frequency of clock that can be applied to the flip-flops. Also, you should introduce an error in your design and to do a verification that will discover the error**.**

Key Points:

- Technical achievement in design is linked to the degree of functionality that was attempted, as explained below.
- Technical achievement in implementation is based on the quality of your Verilog code. This includes issues such as legibility of code, use of meaningful variable names, good comments, clear structure, and modifiability of the design.
- Technical achievement in evaluation is based on the quality of your simulation results.