post-Lab

Experiment No. 3 - Encoders, Decoders, Multiplexers, and Demultiplexers Logic Circuits.

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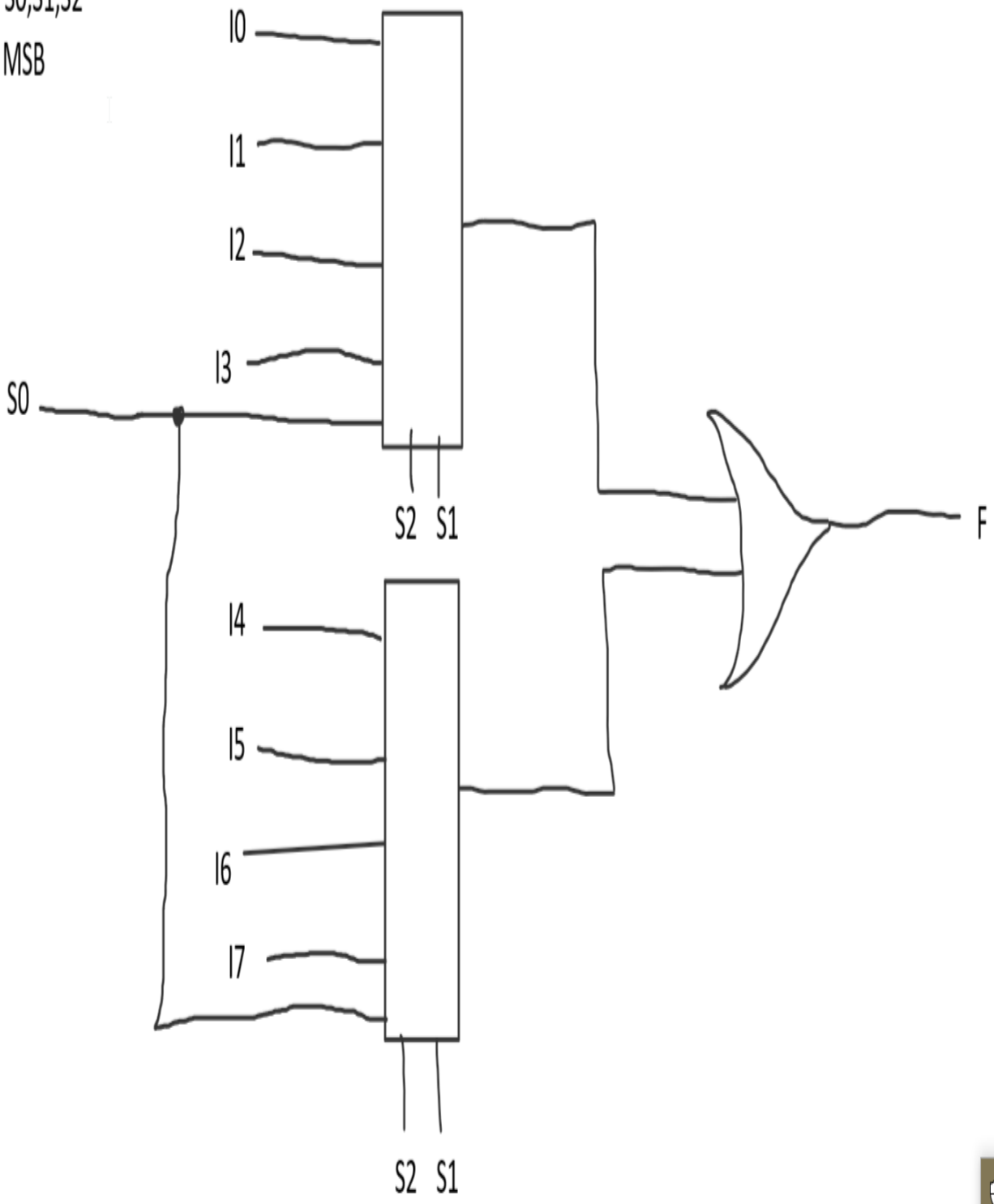
* Section: 2.

Q1) Implement 8x1 Multiplexer using lower order Multiplexers Show how to solve it.

INPUTS			Output
S_2	S_1	S_0	F
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

8x1 mux needs two 4x2 mux so the inputs will fill in , the selection will be separated as follow: S1 and S2 will be the selection of the two 4x2 muxes and S0 will be placed as a 1x2 decoder So the right mux will be selected when needed. Now the two muxes outputs have to be connected to an OR gate because if we use and gate every time the output will be 0 since each time one of the muxes will be off

Assume we have
3 inputs S0,S1,S2
With S2 MSB



Q2) Design a Majority Circuit; a circuit that takes 4 inputs A, B, C, D and 1 output Y. Its output equals 1 when 3 or 4 of the inputs are 1. You can only use two 4×1 multiplexers.

Sol 1)

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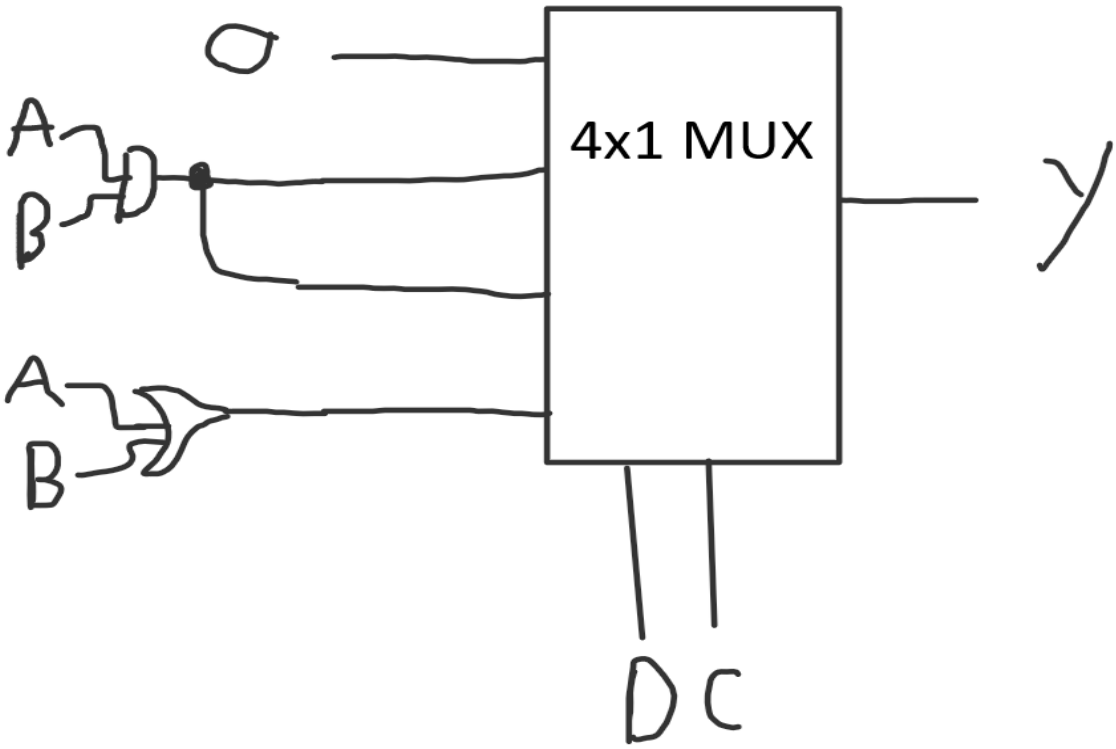

Sol 2)