Electrical and computer engineering department.

Circuit analysis (ENEE 2304).

PSPICE assignment.

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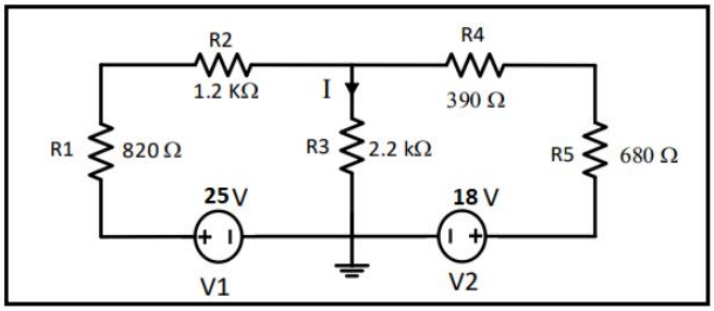
Date: 24/6/2023.

Question # 1: Superposition Technique

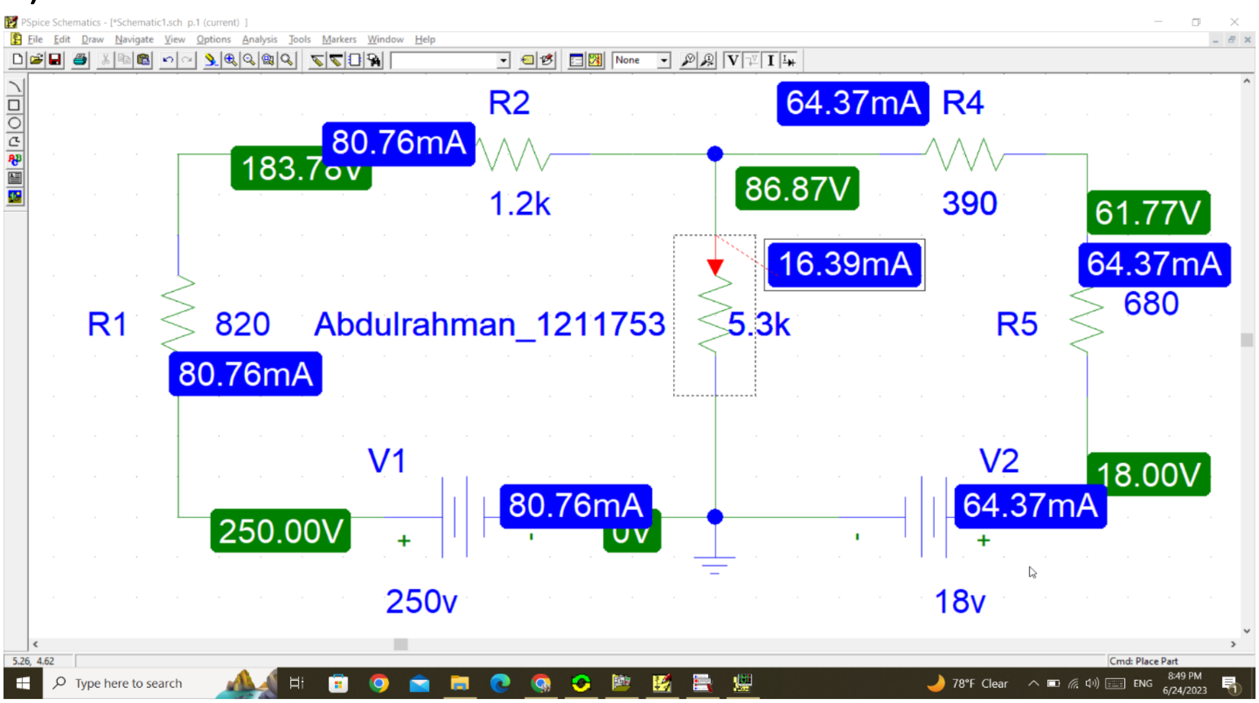
-R3 name: abdulrahman_1211753 / R3 value: 5.3k

For the circuit:



1. Use Pspice software to simulate the circuit and get the voltage across and the current through the resistor R3.
2. Apply superposition theorem to get the voltage across and the current through the resistor R3. You have to show all the results of simulation.
3. Compare the results obtained from step 1 and step 2.

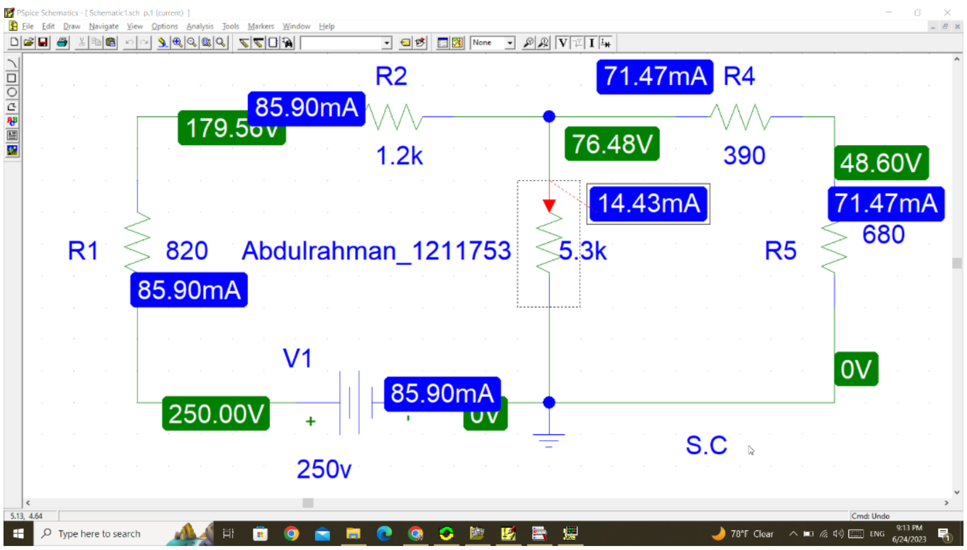
1)



-according to the results, the voltage across R3 is (86.87 -0) = 86.87 volt. And the current through R3 is 16.39mA

2) We need to apply superposition theorem.

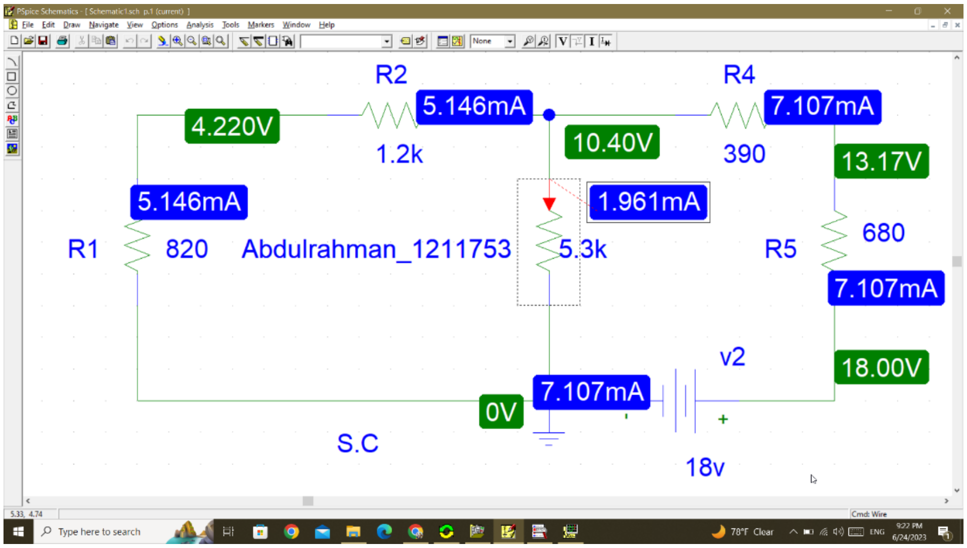
- let's start from (I and V) by v1:



-V by v1 is 76.48 volt and I is 14.43mA

V0 = 76.48 volt, I0 = 14.43mA

- Now (v and I) by v2:



-V by v2 is 10.40 volt and I is 1.961mA

V1 = 10.40 volt, I1 = 1.961mA

-using superposition theorem:

-V on R3 should equal to V0 + V1:

V0 + V1 = 76.48 + 10.40 = 86.88 volt

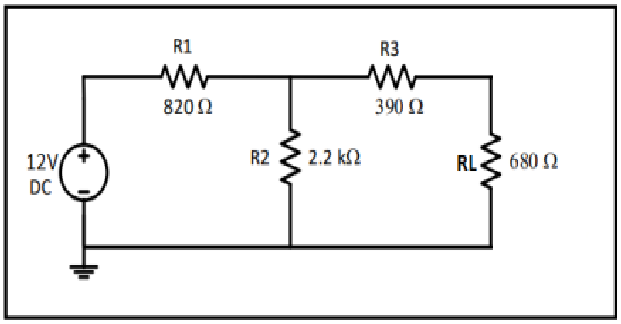
-I on R3 should equal to I0 + I1:

I0 + I1 = 14.34m + 1.961m = 16.301 mA

3) V3 = 86.88 volt ≈ 86.87 volt (correct).
I3= 16.301 mA ≈ 16.39 mA (correct).

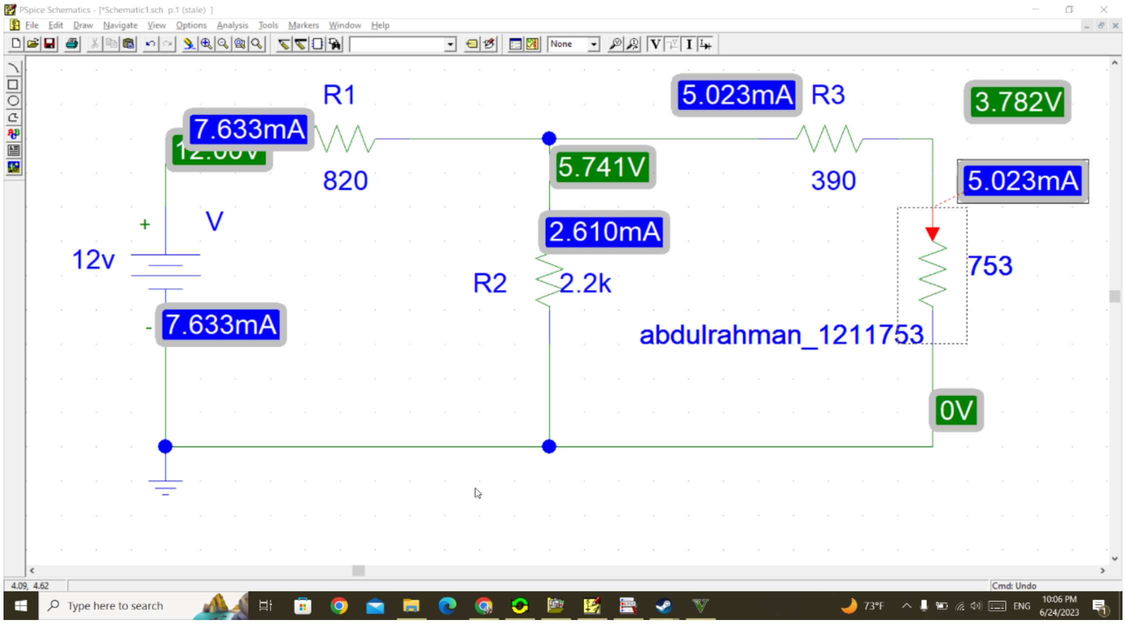
Question #2: Thevenin's Theorem & Maximum Power Transfer

For the circuit:



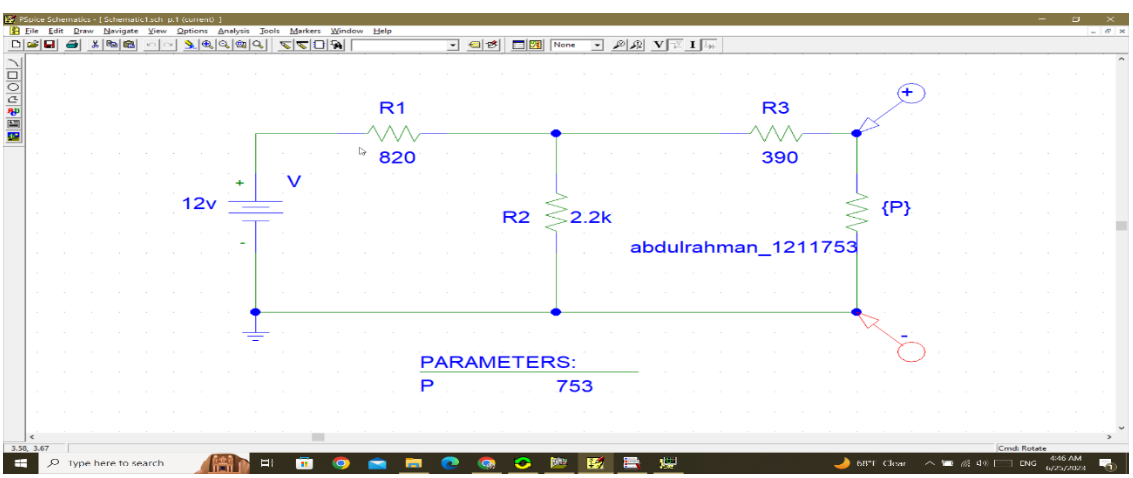
1. Use Pspice software to simulate this circuit and get the voltage across and the current through the resistor RL (xxx (last three digits) Ω).
2. Using DC sweep, set RL as a parameter that varies from 50 Ω to 1.5 kΩ and **plot** the power dissipated by RL as it varies (plot the power of RL versus the value of RL). With the help of cursors on Pspice simulation window, approximate at which value of RL the power maximizes)
3. Use Pspice software to calculate $R_{thevenin}$ seen by the resistor RL. **Use V_{oc} and I_{sc} method only**. You have to show all the simulation results when getting V_{oc} and I_{sc}.
4. Compare the value of RL at P_{max} obtained from step 2 and the value of $R_{thevenin}$ obtained from step 3.
5. Build and then simulate the Thevenin equivalent circuit with the load resistor RL and show the voltage across and the current through the resistor RL.
6. Compare the results obtained from step 1 and step 5.

1)

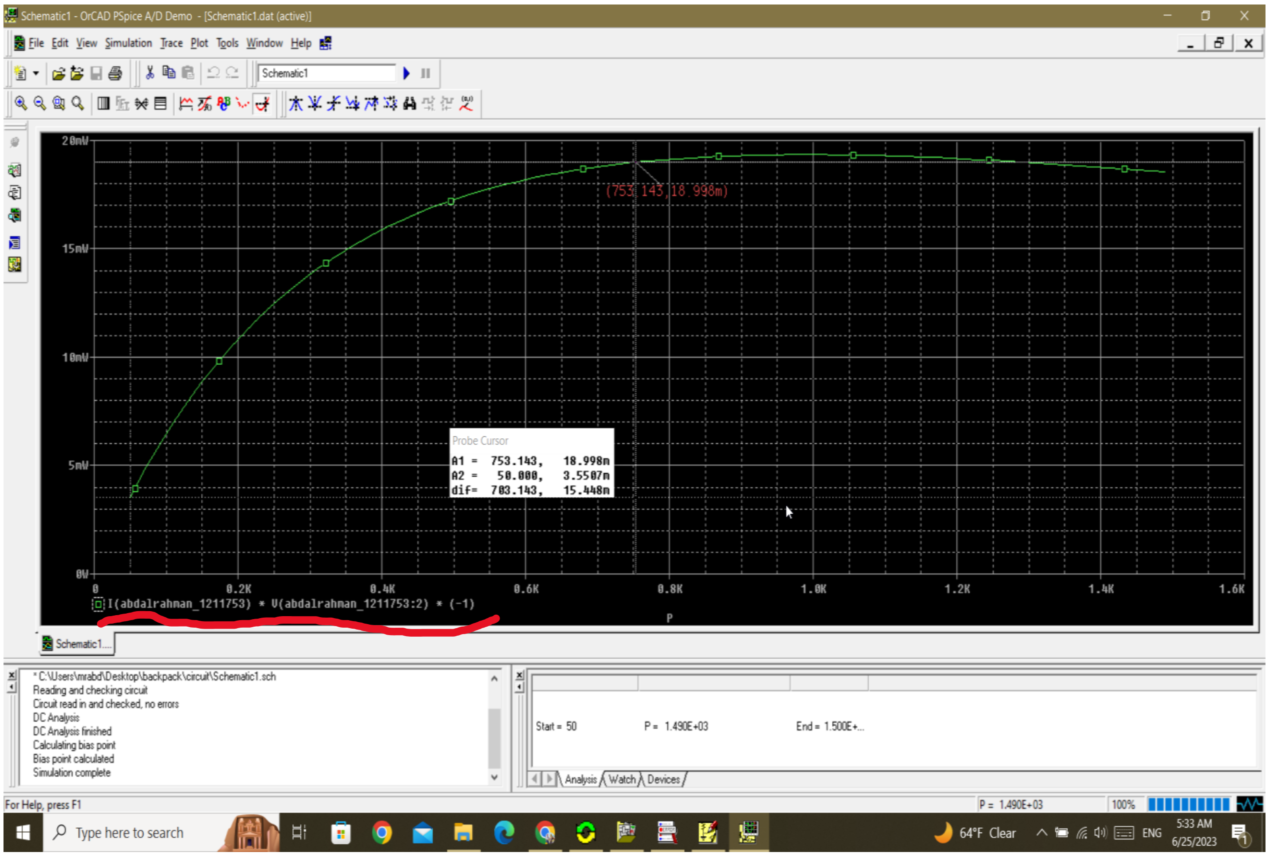


-V = 3.782 volt and I = 5.023mA

2)



-R load value will change from 50 to 1.5k ohm by 20 increment



-Power = current * voltage.

P RL = 5.023 * 3.782m = 18.998mw

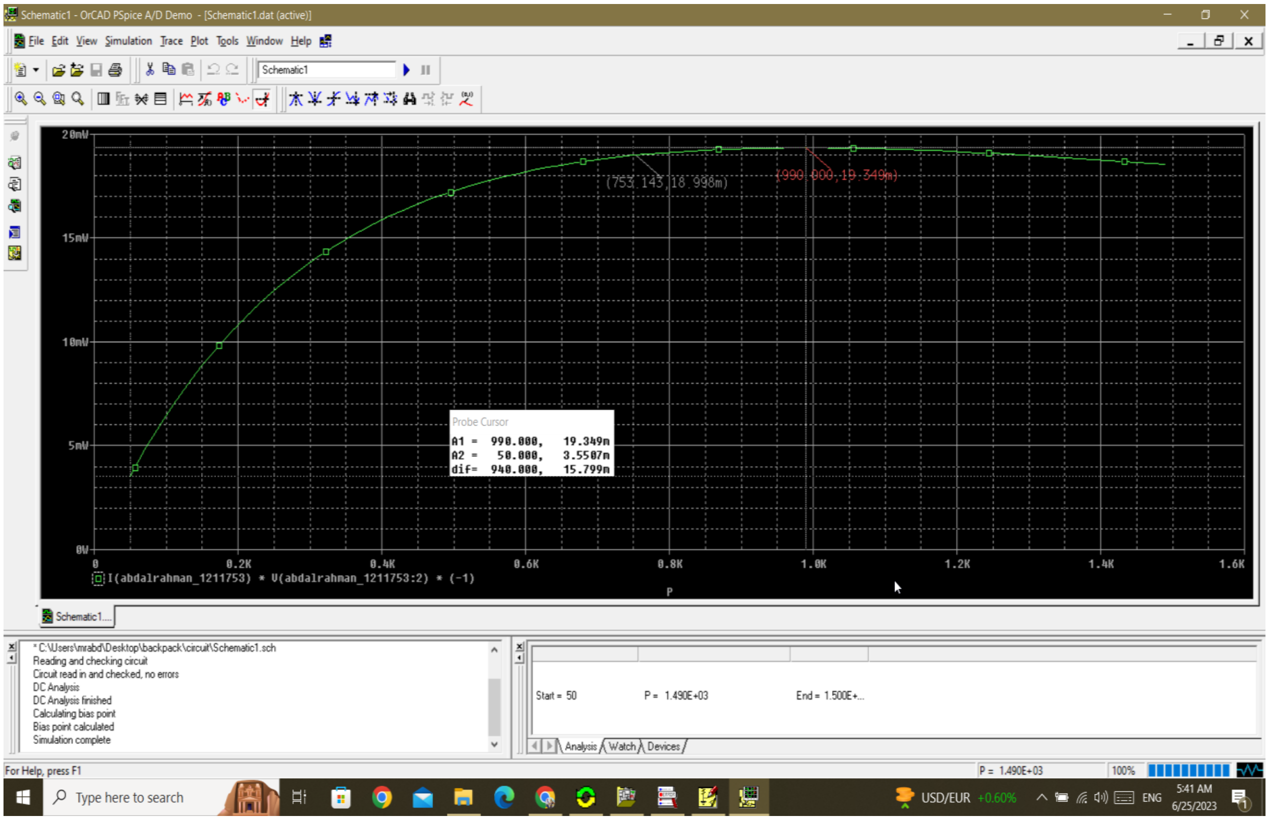
-Since PRL is right at RL = 753 ohm then everything is right.

(I multiplied P by (-1) since the power of the resistors never supply power)

- I assumed that the given p is

(The power extracted from the circuit by RL)

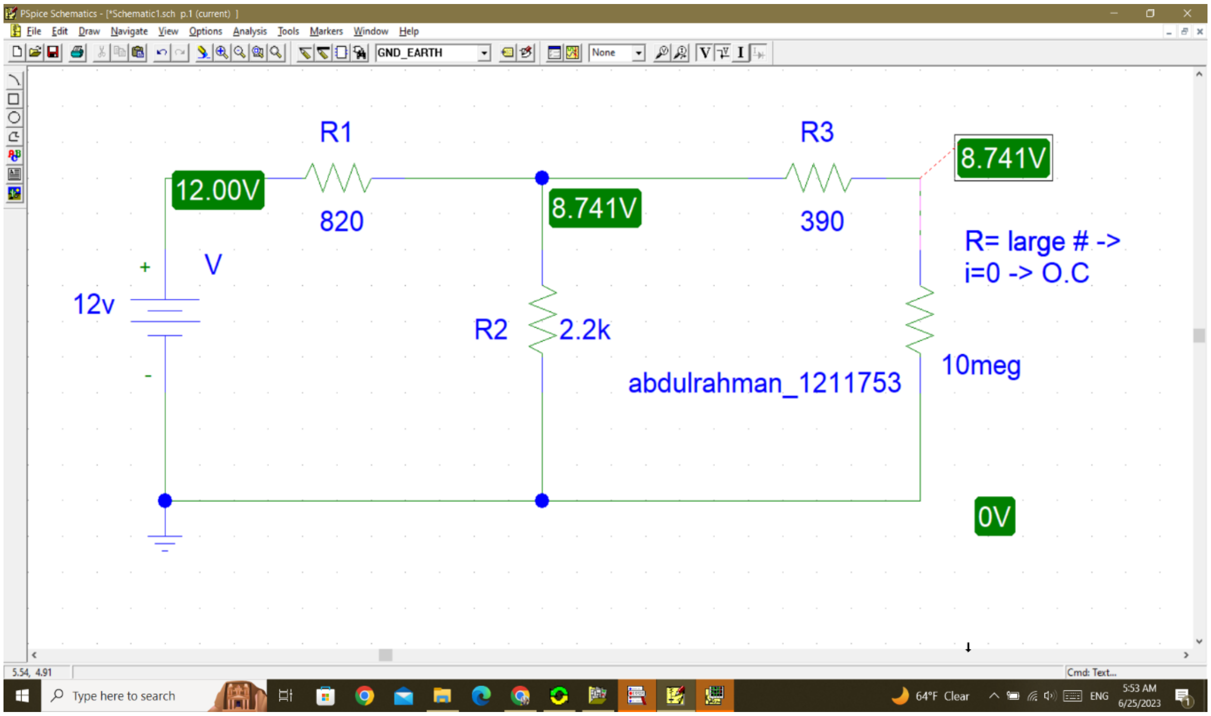
-By using curser peak tool, I managed to get the value of RL when p is max



-As shown in the plot RL = 990 ohm when p is max.

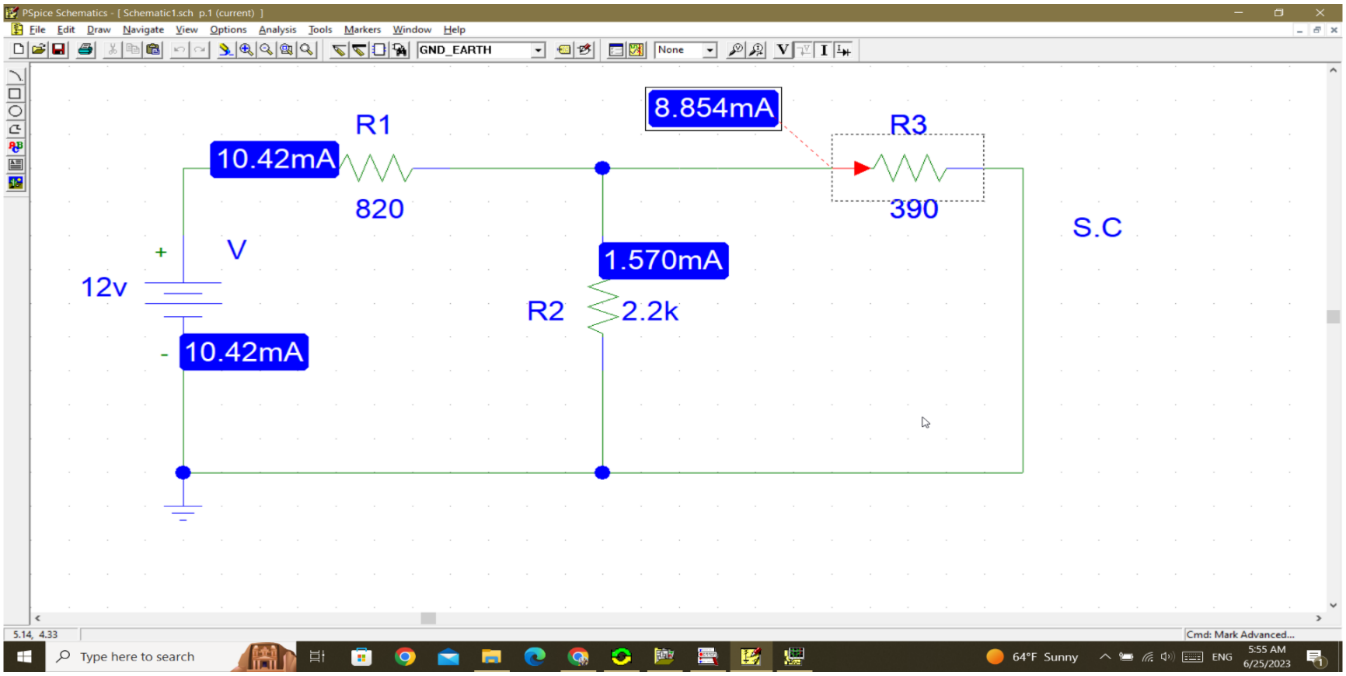
3)

Voc:



Voc =8.741 volt.

Isc:



Isc = IR3 = 8.854mA

-Rth = Voc/Isc = 8.741 / 8.854m = 987 ohm.

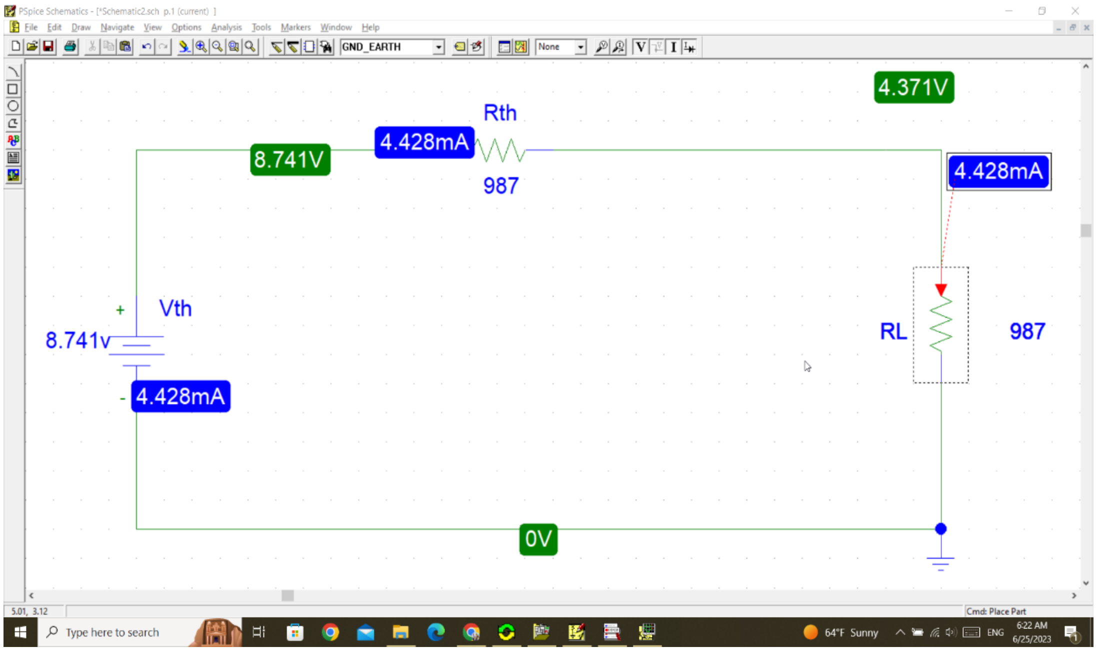
- RL when Pmax = Rth = 987 ohm

4)

-from step 2 RL at Pmax = 990 ohm

- from step 3 RL at pmax = 987 ohm

5)



V = 4.371 volt and I = 4.428mA

6)

In step 1: V = 3.782 volt and I = 5.023mA

But in step 5: V = 4.371 volt and I = 4.428mA

Question # 3: Sinusoidal Steady State Analysis

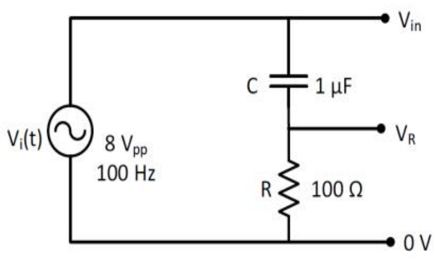


Fig. 3.1 Capacitive circuit

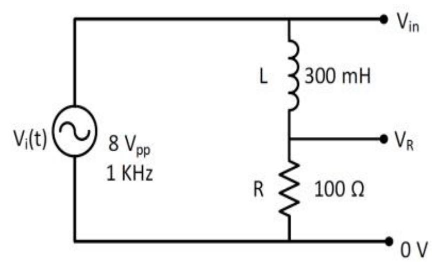
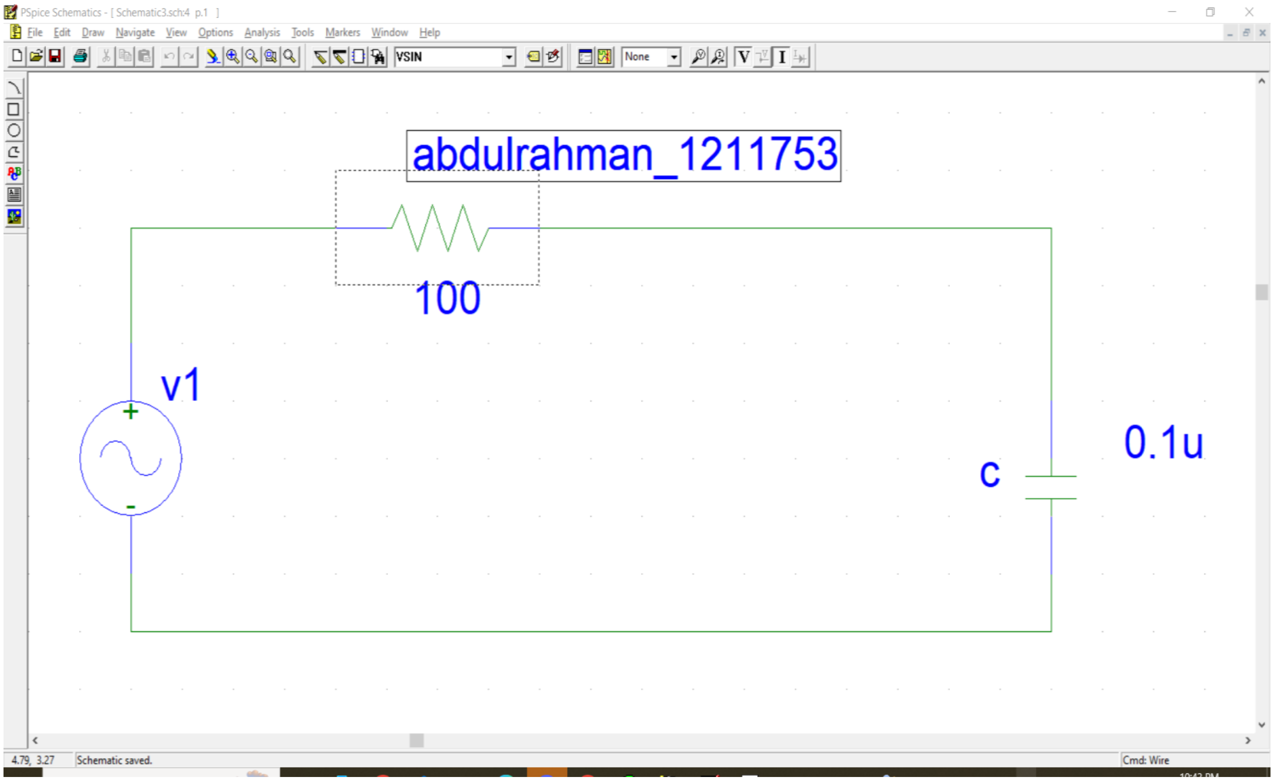


Fig. 3.2 Inductive circuit

For the circuit shown in Fig. 3.1:

1. Use PSPICE to do transient analysis of the circuit, show $V_{in}(t)$ and $V_R(t)$ on one plot (you may need to use different Y-axes).

2. Use cursors to measure the time difference between the peaks of the two signals, then use the following relationship to calculate the phase shift using the measured time $\{\Delta\theta = 360° \times f \times \Delta t\}$.
3. Repeat the same procedure in the step 1and 2 above for the circuit shown in Fig. 3.2.
4. Compare and discuss the results obtained for the two circuits.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abdulrahman_1211753
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v1
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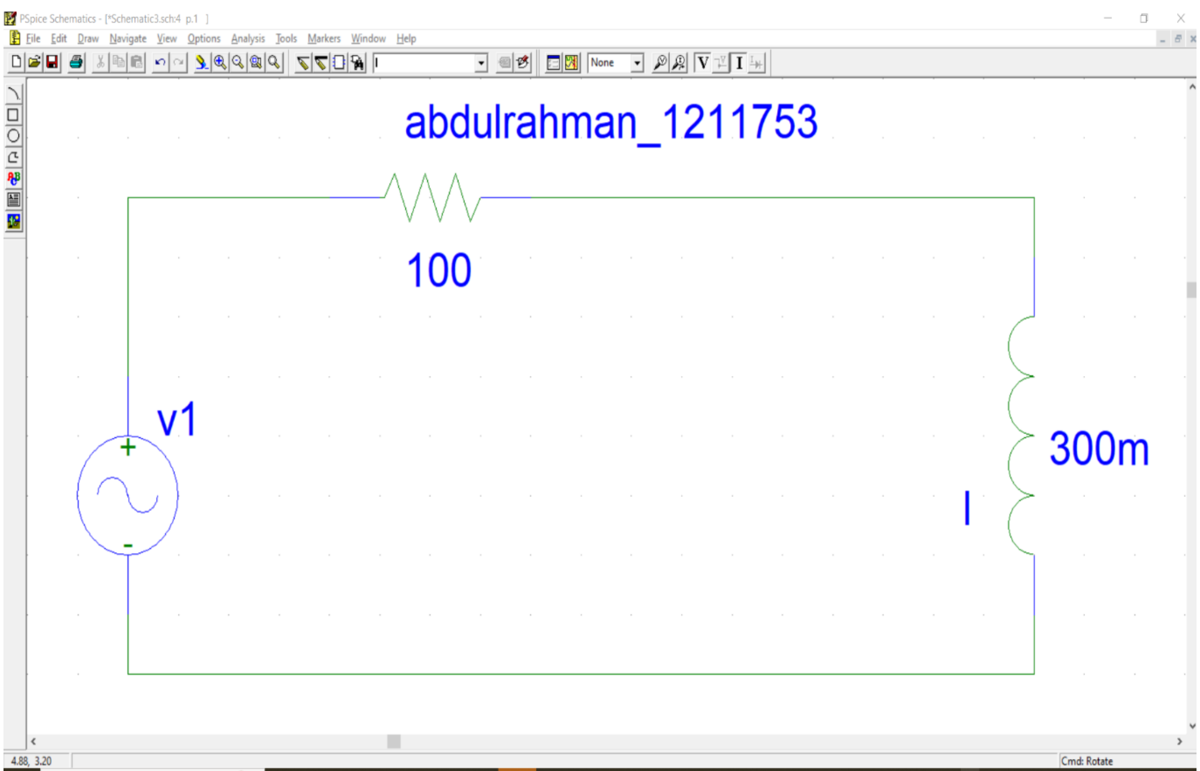
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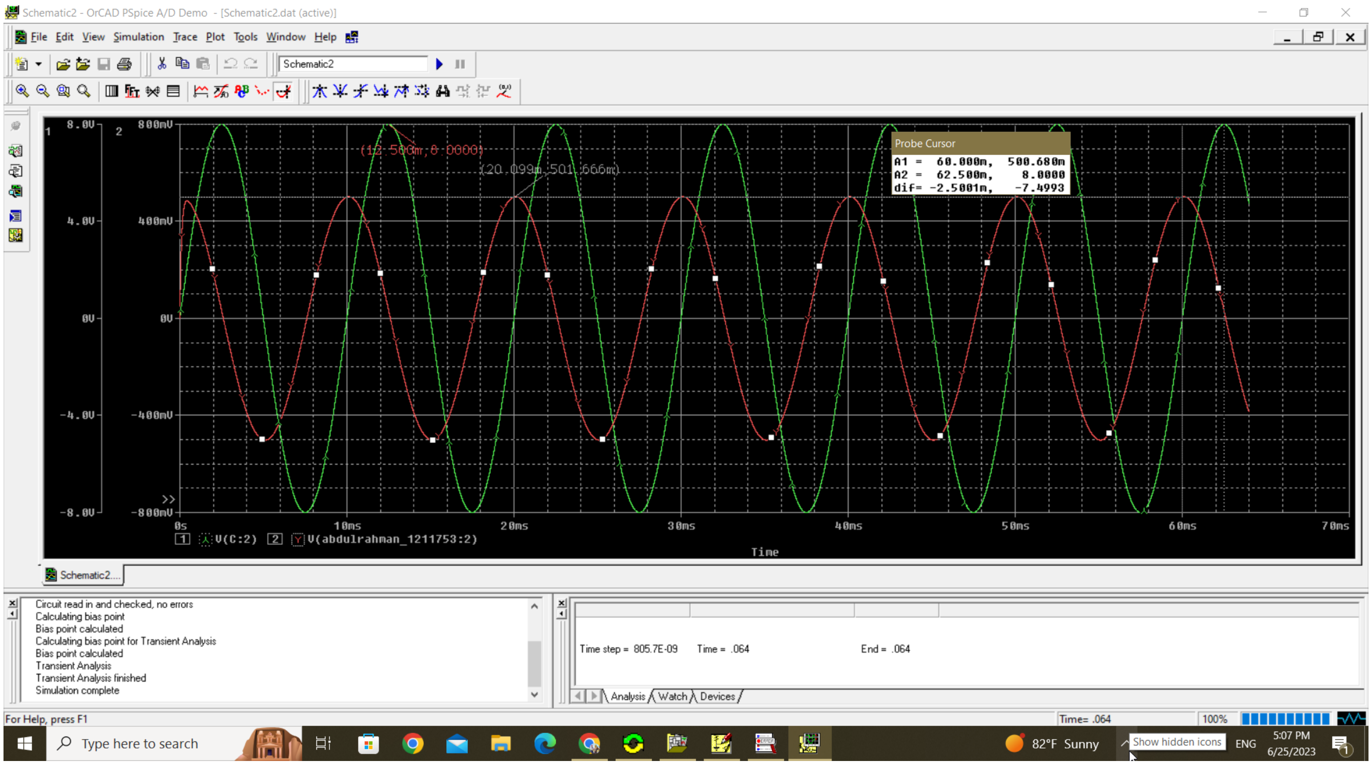
v1
300m
l
4.88, 3.20
Cmd: Rotate

1 + 2)



$\Delta\theta = 360° * f * \Delta t$

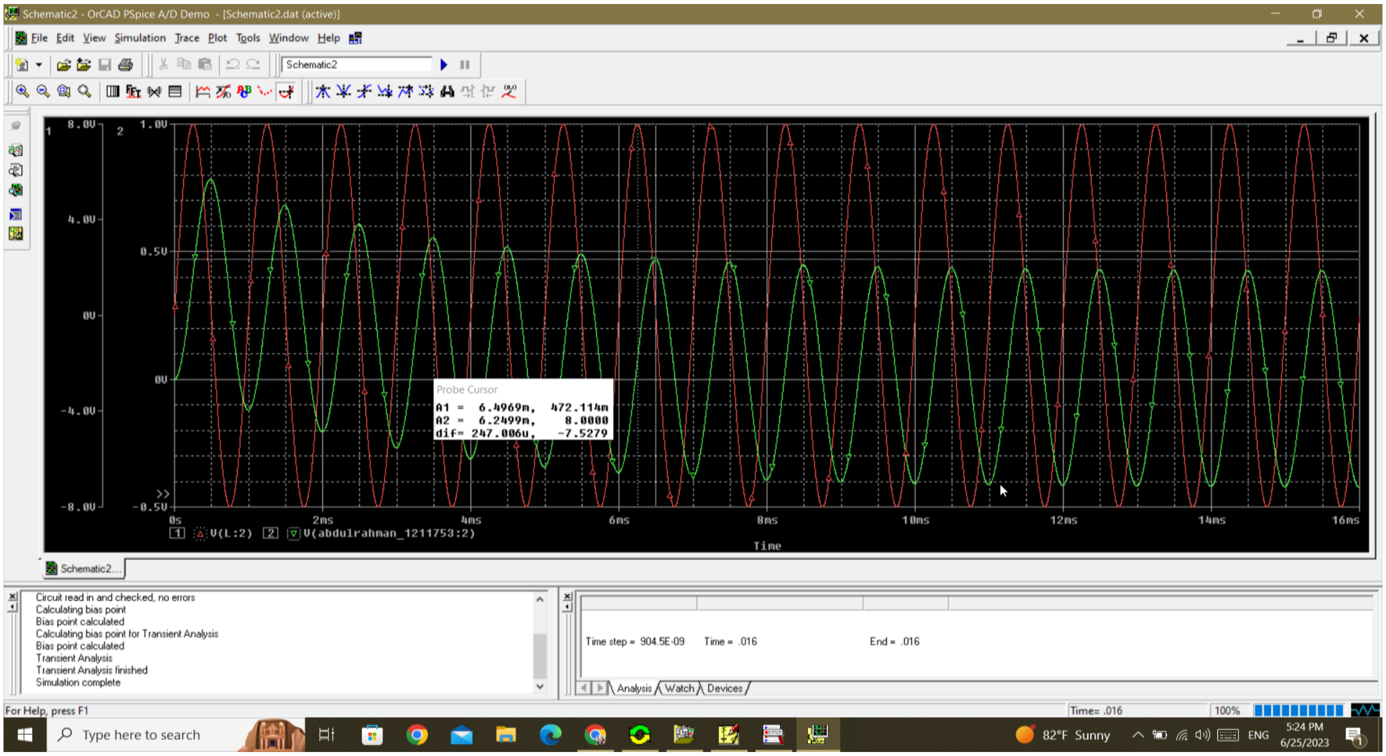
Δt = -2.5 ms

f = 100 hz

$\Delta\theta$ = 360° * 100 *-2.5m = -90°

-When the voltage across a resistor and a capacitor is compared, a phase shift of 90 degrees is expected. This is due to the inherent behavior of capacitors in AC circuits.

3)



$\boldsymbol{\theta}$=360° * **f** * Δt

Δt = -241 us

f = 1k hz

Δ$\boldsymbol{\theta}$ = 360° * 1000 *247u = 88.92° ≈ 90°.

When comparing the voltage across a resistor and an inductor in an AC circuit, a phase shift of 90 degrees is expected because of the inherent behavior of inductors.

4)

Voltage across a Resistor and an Inductor (R and L):

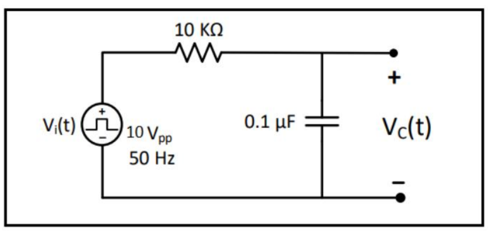
- The voltage across a resistor and an inductor in series will have a phase shift between them. The voltage across the inductor lags the voltage across the resistor by 90 degrees.

Voltage across a Resistor and a Capacitor (R and C):

- The voltage across a resistor and a capacitor in series will also have a phase shift between them. The voltage across the capacitor leads the voltage across the resistor by 90 degrees.

Question #4: First Order RC Circuit Analysis

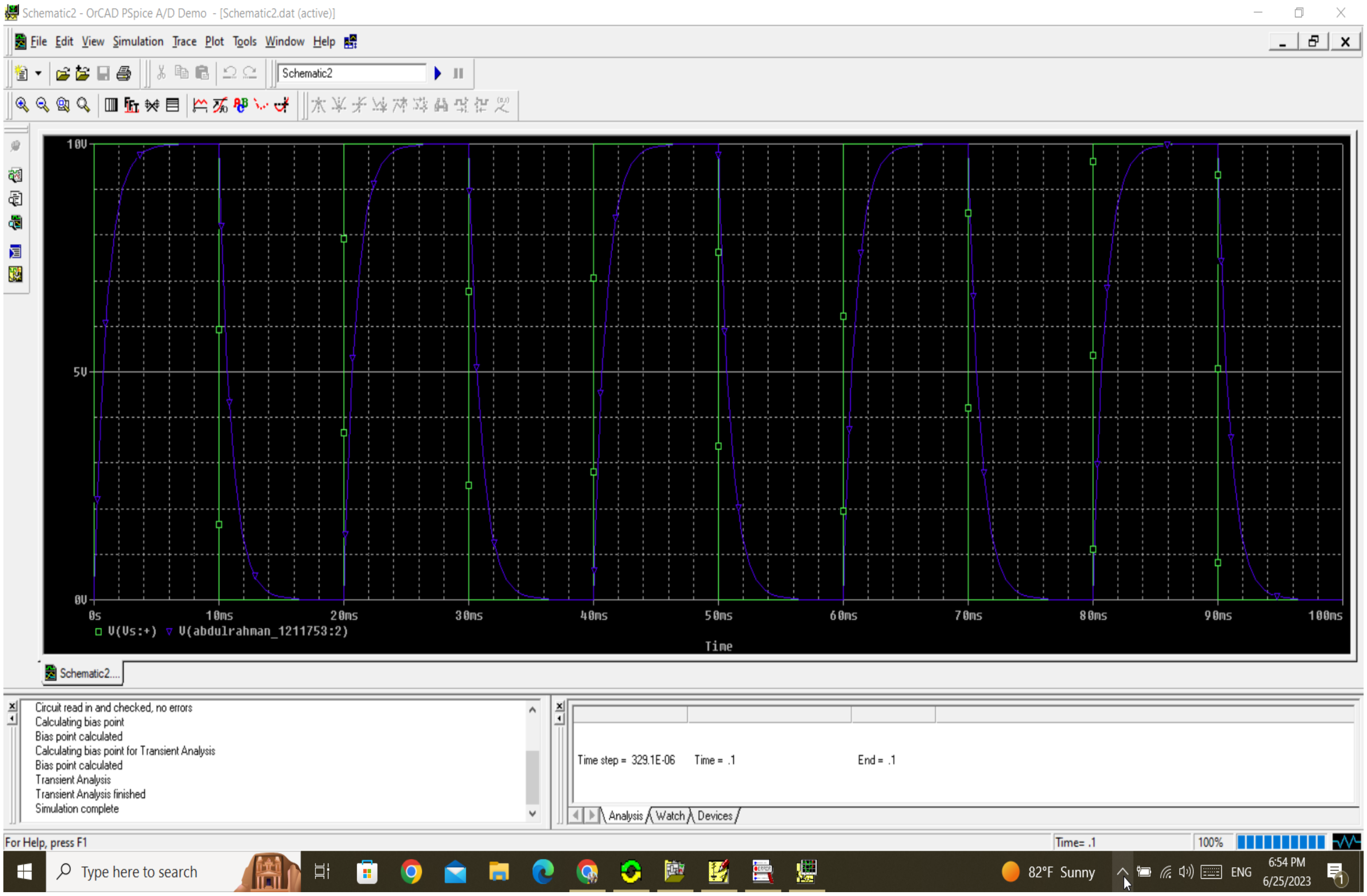
For the circuit:



The input voltage is square signal with 10 $V_{peak\text{-}peak}$ (0 V to 10 V) and frequency of 50Hz.

1. Use Pspice software to plot both $V_i(t)$ and $V_c(t)$ (on the same graph) for a meaningful period of time.
2. With help of cursors on Pspice simulation window, show the value of the time constant (τ). You have to show both the circuit and the simulation result.

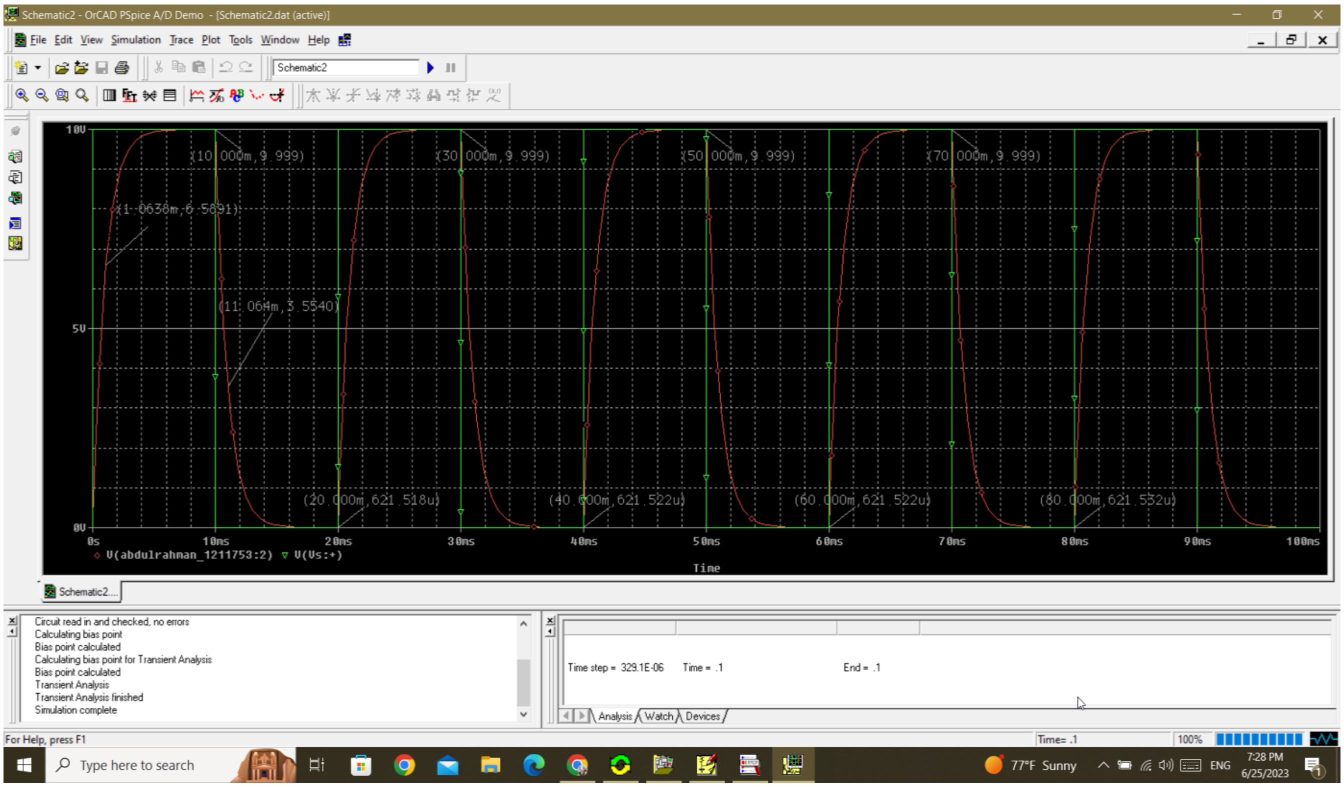
1)



2) the RC circuit's time constant is defined as the product of the resistance and capacitance values (RC), representing the time it takes for the capacitor to charge or discharge to 63.2% of its maximum voltage.

In this circuit time constant = 0.1u * 10k = 1ms

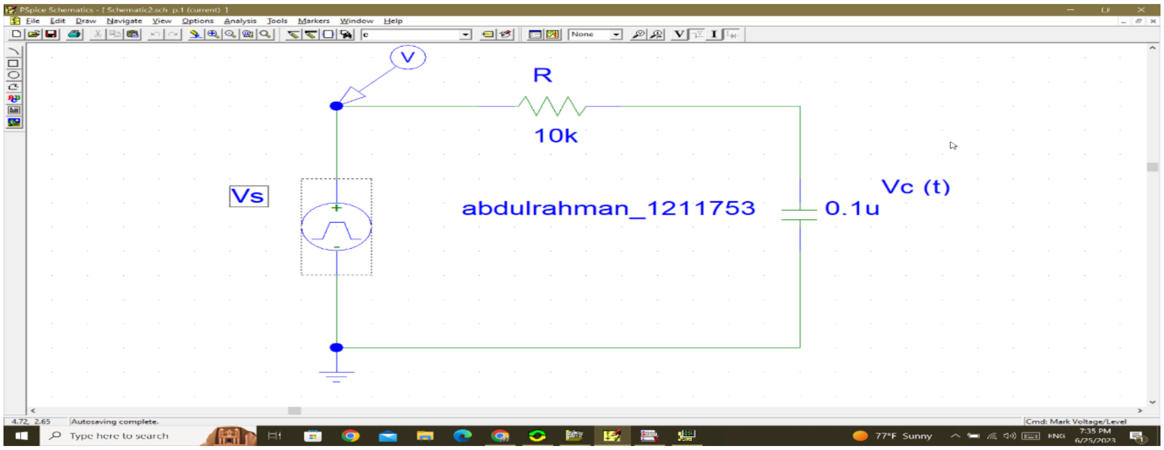
And by the graph you can calculate it by finding 63.2% of the vc when its full charged -> 63.2% * 10 volt = 6.5891, then the time by this voltage value is time constant = 1ms



-As shown in the figure the maximum voltage in the capacitor when it's fully charged Is 10 volts.

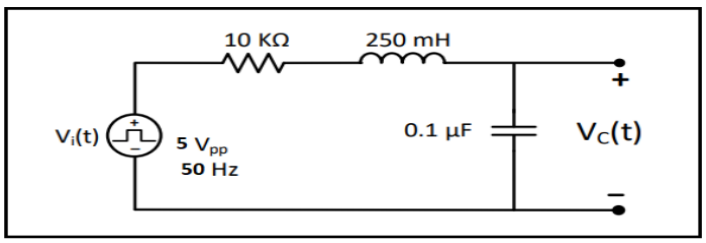
The voltage on t= time constant = 6.5891 volt ≈ 63.2% of 10 volt.

- likely the voltage when time constant passed after 10ms (t = 11ms) the voltage in the capacitor is decreased to 3.5540 volt which means the voltage decreased from 10 volt to 3.5540 volt is 63.2%of 10 volts.



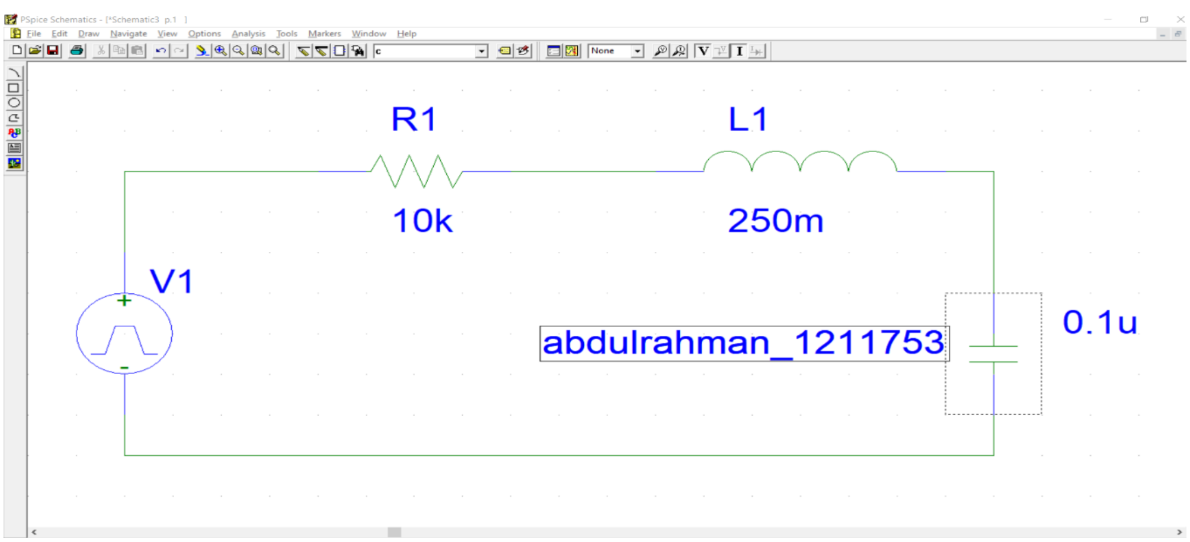
Question #5: Second Order RLC Circuit Analysis

For the circuit:

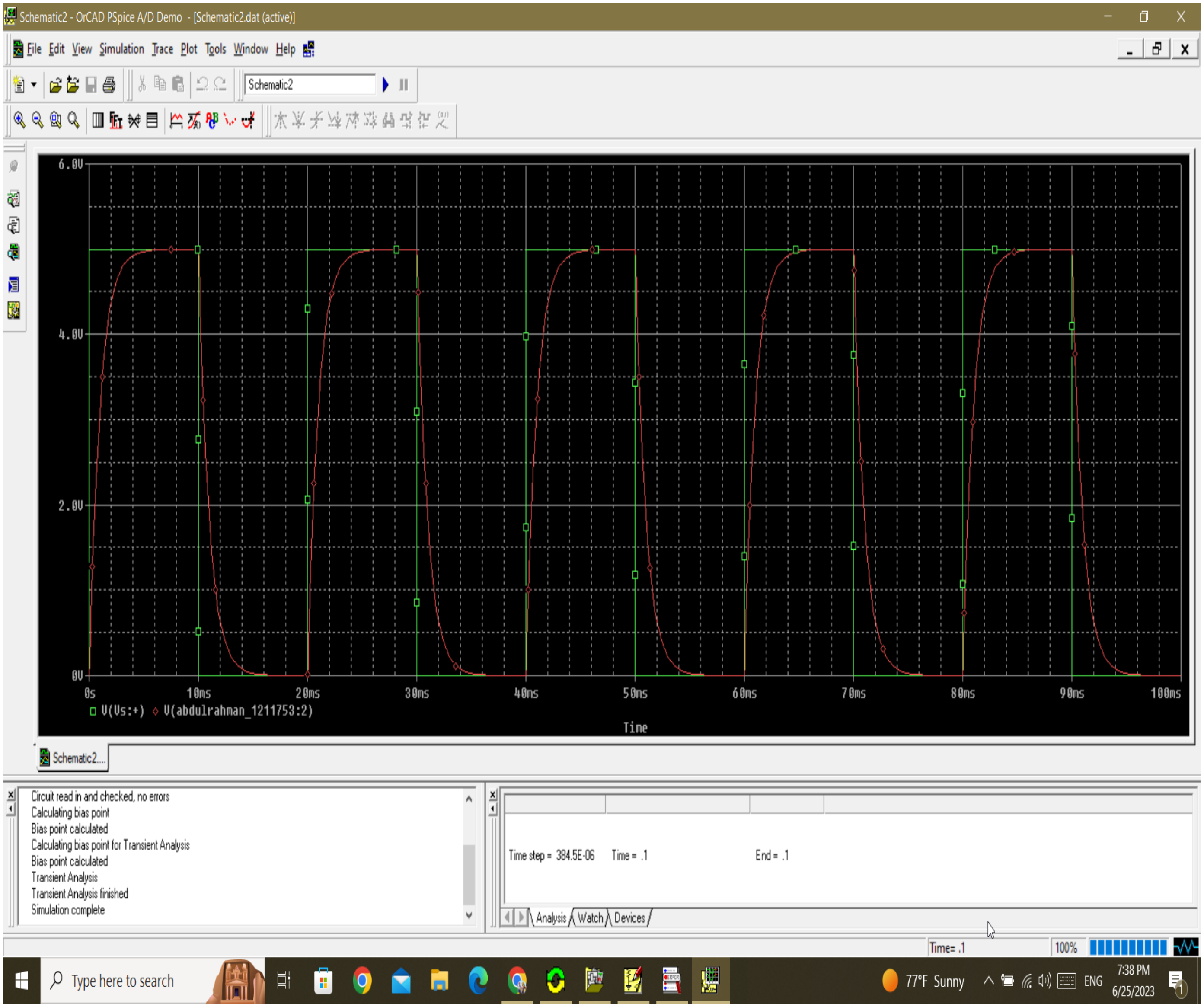


The input voltage is square signal with 5 $V_{peak\text{-}peak}$ (0 V to 5 V) and frequency of 50Hz.

1. Use Pspice software to plot both $V_i(t)$ and $V_c(t)$ (on the same graph).
2. Change the Value of R to 3.162 kΩ, repeat step 1.
3. Change the Value of R to 500 Ω, repeat step 1.
4. Comment on each result: is it over-damping, critical-damping, or under-damping response.



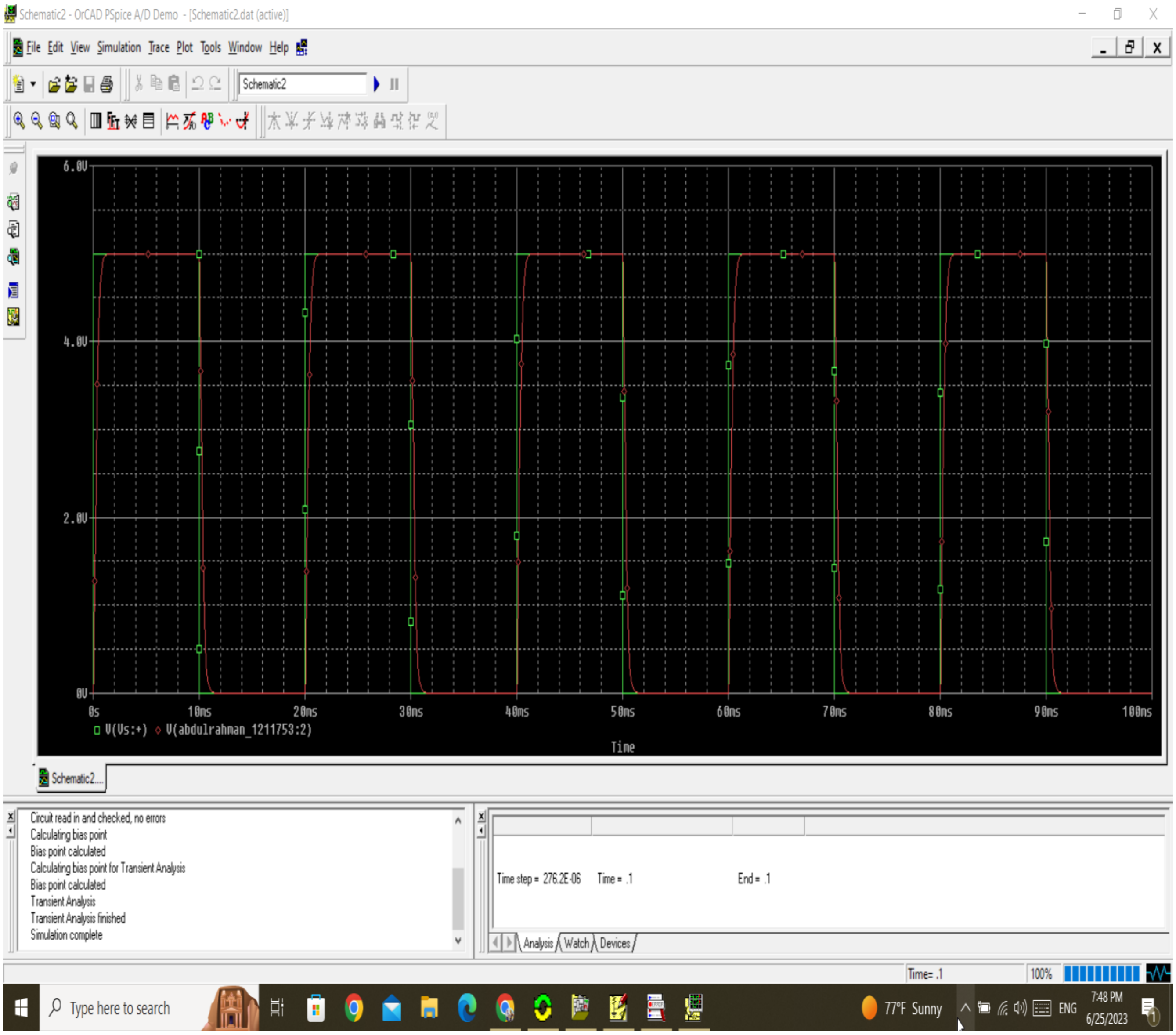
1)



R=10k, alpha= 20000, Wo = 6324

Alpha > Wo ---> over damped

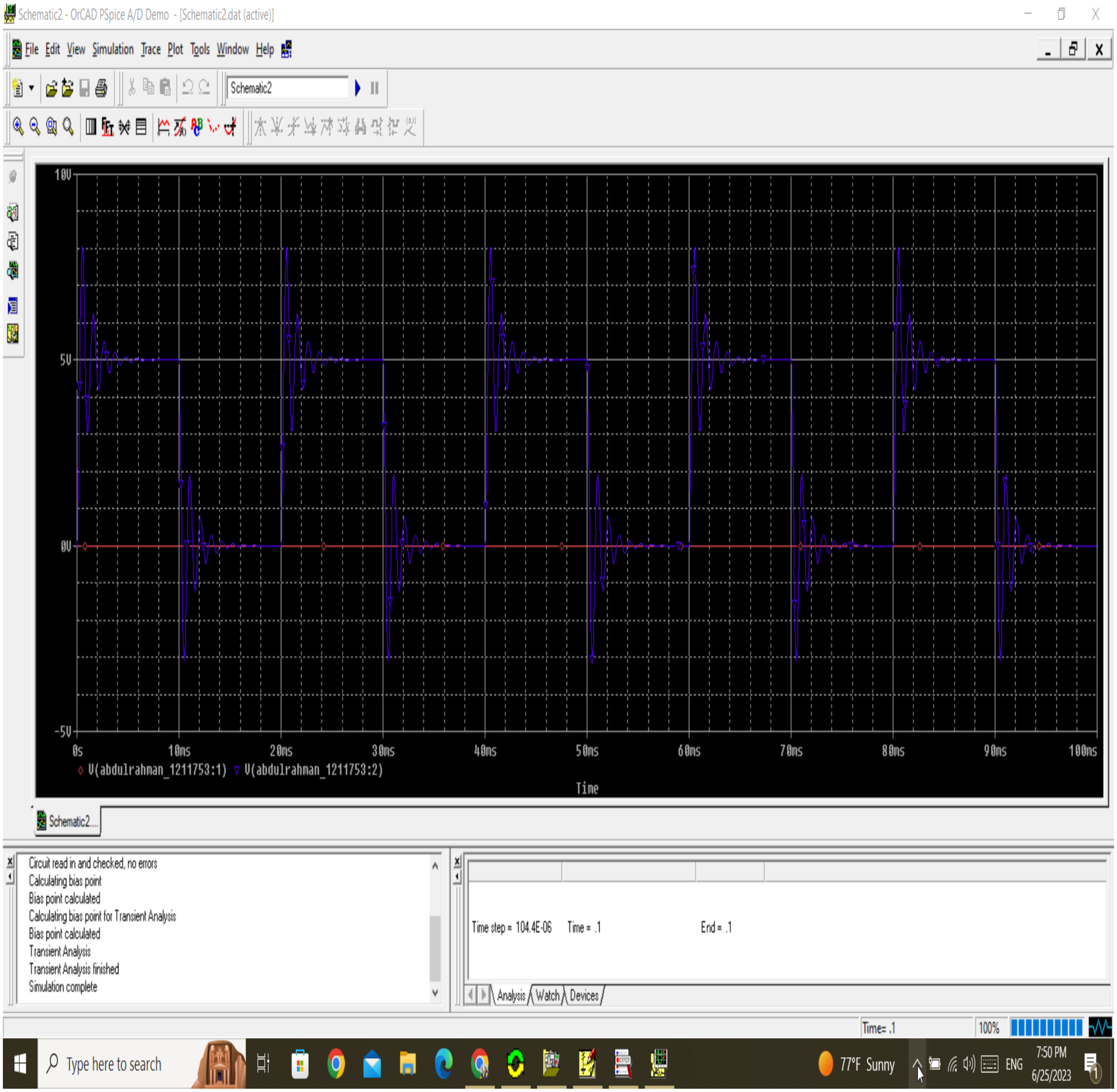
2)



R=3.162k, alpha= 6324, Wo = 6324

Alpha = Wo ---> critically damped

3)



R=500, alpha= 1000, Wo = 6324

Alpha < Wo ---> under damped

(You also can see the state via graphs.)