DISCUSSION

Experiment No. 5 - Sequential Logic Circuits

*Student name: Abdulrahman shaheen.

* ID#: 1211753.

* Instructor Name: Dr. Qadri Mayyala

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1. Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why?

1- Timing Issues: Latches are level-sensitive circuits, which means they are sensitive to the input level while the “enable” signal is active. Sometimes this causes timing glitches. Flip-flops, on the other hand, are edge-triggered, so they respond one time when the transaction happens.

2- Design Constraints: latches are built with more complex control signals compared with flipflops. Since they have an enable signals that have to be managed carefully.

3-power consumption: Latches are generally more power-hungry compared to flip-flops. This is because latches continuously evaluate their inputs as long as the enable signal is active.

2- What is the disadvantage of the RS flip flop?

Invalid State: The RS flip-flop can have an invalid state when both inputs (S and R) are both set to logic 1. This condition is known as the "forbidden" state. In this state, the outputs of the flip-flop can rapidly oscillate, making it impossible to determine the stable output.

3. What is the difference between “synchronous” and “ripple” counters?

Synchronous counters are designed to operate in synchronization with an external clock signal. They use a common clock signal to trigger the state transitions of all the flip-flops within the counter simultaneously. However, in Ripple counters, also known as asynchronous counters, don't rely on a common clock signal for state transitions. Instead, each flip-flop within the counter triggers the next flip-flop in a cascading manner. The output of each flip-flop serves as the clock input for the next flip-flop in the sequence.