F.Y. B. Tech (All Branch)

Basic Electrical Engineering & Digital Electronics

(TA1- Activity)

A

Virtual Lab Report

(Minimum 3 Lab)

Submitted By

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Submitted To

Shirpur Education Society's

R. C. Patel Institute of Technology, Shirpur

(An Autonomous Institute, Affiliated to DBATU, Lonere)

Department of Applied Sciences & Humanities

A.Y. 2024-25

Shirpur Education Society's
R. C. Patel Institute of Technology, Shirpur
(An Autonomous Institute, Affiliated to DBATU, Lonere)

Certificate

This is to certify that, Kajal Sunil Chaudhary ., student of First Year B. Tech, ***Div*** *D* ***Batch ENTC*** *&* ***Roll no 9 .PRN 241102005*** *has successfully Submitted* ***TA-1 Activity (Virtual Lab) Report*** *during the year 2024-25 in partial fulfillment of* ***BEEDE Teacher Assessment Activity-1*** *in the Department of Applied Sciences & Humanities.*

Date: -

Place: - Shirpur

Dept. Seal

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1	Verification of superposition theorem			
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Verification of Superposition Theorem

Theory

If a number of voltage or current source are acting simultaneously in a linear network, the resultant current in any branch is the algebraic sum of the currents that would be produced in it, when each source acts alone replacing all other independent sources by their internal resistances.

Circuit Diagram:

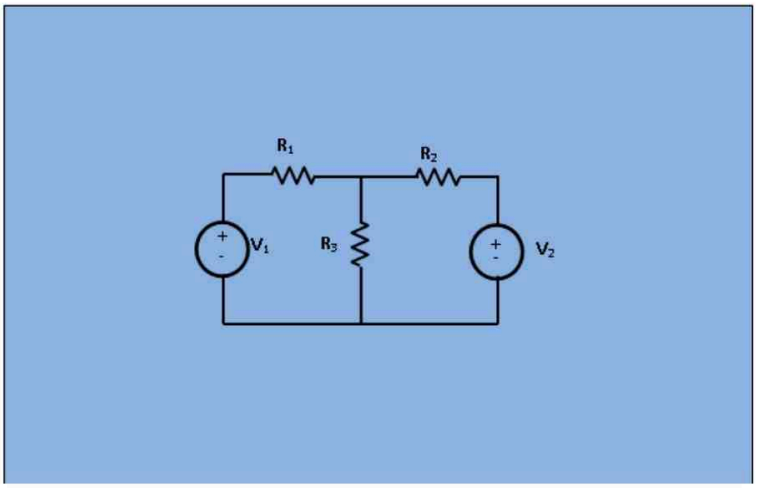


Fig.1 : Circuit for analysis of Superposition theorem

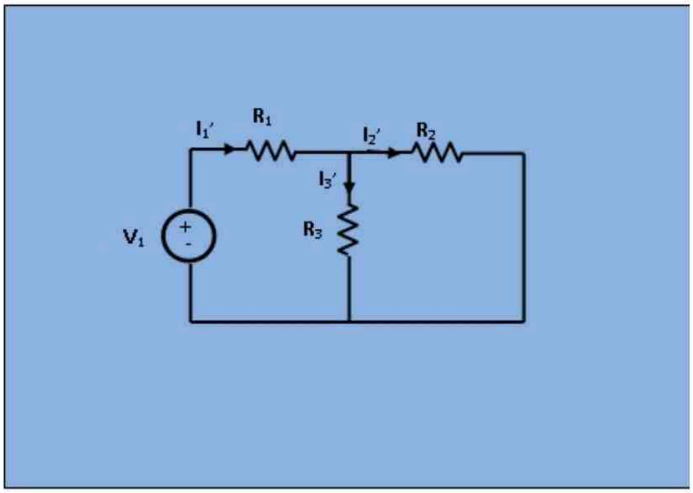


Fig.2 : Circuit with only V_2 short circuited

In given figure 1 apply superposition theorem , let us first take the sources V_1 alone at first replacing V_2 by short circuit as shown in figure 2.Here,

$$I_{1'} = \frac{V_1}{\frac{R_2 * R_3}{R_2 + R_3} + R_1}$$

$$I_{2'} = I_{1'} * \frac{R_3}{R_2 + R_3}$$

In given figure 1 apply superposition theorem , let us first take the sources V_1 alone at first replacing V_2 by short circuit as shown in figure 2.Here,

$$I_{1'} = \frac{V_1}{\frac{R_2 * R_3}{R_2 + R_3} + R_1}$$

$$I_{2'} = I_{1'} * \frac{R_3}{R_2 + R_3}$$

$$I_{3'} = I_{1'} - I_{2'}$$

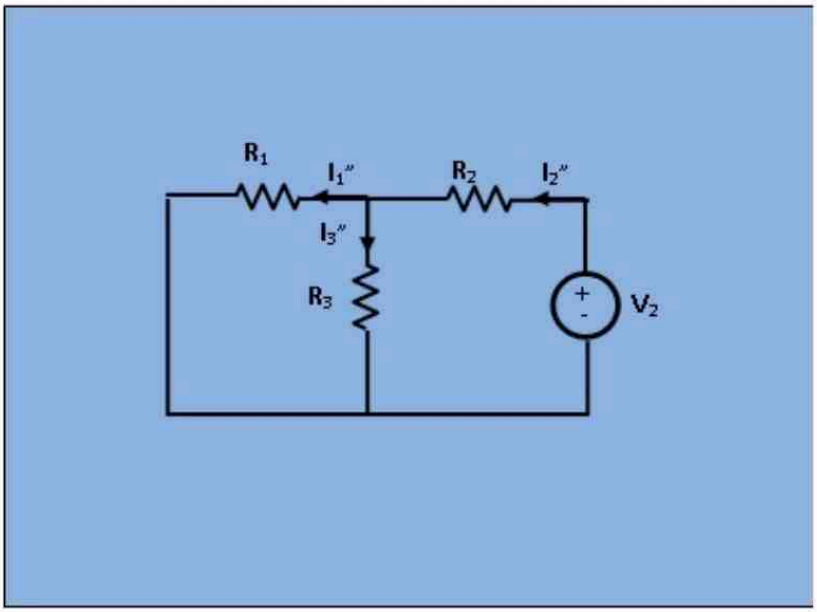


Fig.3 : Circuit with only V_1 short circuited

Next, removing V_1 by short circuit, let the circuit be energized by V_2 only as shown in figure 3. Then,

$$I_{2''} = \frac{V_2}{\frac{R_2 * R_3}{R_2 + R_3} + R_2}$$

$$I_{1''} = I_{2''} * \frac{R_3}{R_1 + R_3}$$

$$I_{3''} = I_{2''} - I_{1''}$$

As per superposition theorem,

$$I_3 = I_{3'} + I_{3''}$$

$$I_2 = I_{2'} - I_{2''}$$

$$I_1 = I_{1'} - I_{1''}$$

'erification of Superposition Theorem

R_2 and R_3 and choose any
l V_2.

ect:

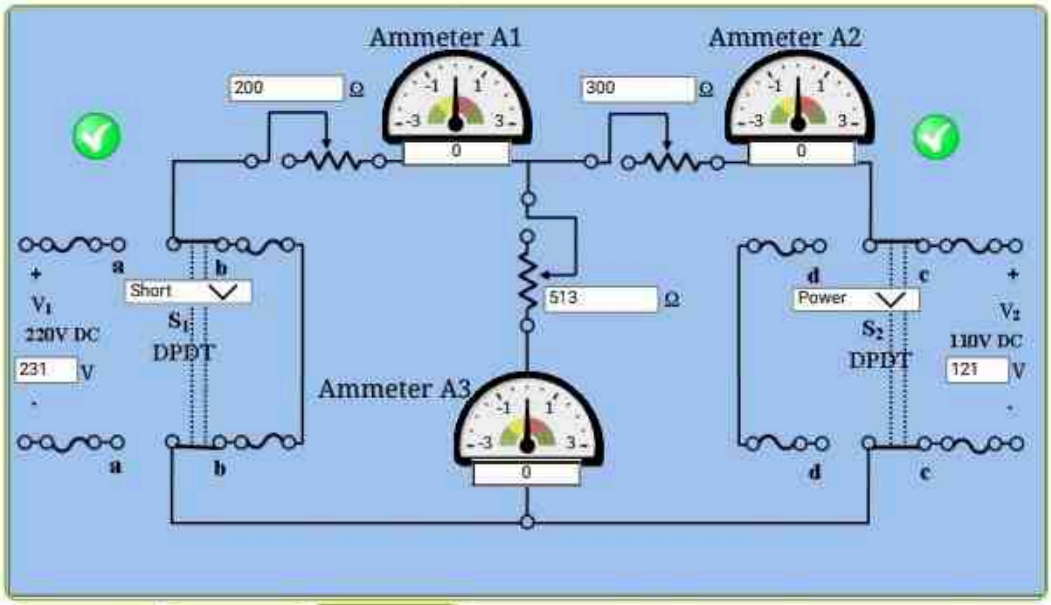
th the sources
to power and Simulate the
ult from case 1 tab.

only
and S_2 to short. Simulate
ter values from Case 2 tab.

only
nd S_2 to power. Simulate
ter values from Case 3 tab.
ble' to update the

take other observations.

le throw.
re in ohms.



Case 1 | Case 2 | Case 3

Determination of branch currents in presence of V_2 sou

Select the switch S_1 to short and S_2 to power.

And then click on Simulate.

Simulate

A1 ammeter reading (in Amp)	A2 ammeter reading (in Amp)	A3 ammeter reading (in Amp)
0	0	0

Fill data to the table

presence of both V_1 and V_2		In presence of V_1 only			In presence of V_2 only		
Brach current I_2 (in amps)	Brach current I_3 (in amps)	Brach current I_1 (in amps)	Brach current I_2 (in amps)	Brach current I_3 (in amps)	Brach current I_1 (in amps)	Brach current I_2 (in amps)	Brach current I_3 (in amps)
-0.10102	0.28746	0.57249	-0.35834	0.21415	-0.18401	0.25732	0.073312
-0.10416	0.28960	0.57960	-0.36360	0.21600	-0.18584	0.25944	0.073600
-0.10325	0.29187	0.58433	-0.36711	0.21722	-0.18922	0.26386	0.074641
-0.10235	0.29412	0.58907	-0.37062	0.21844	-0.19259	0.26827	0.075676
-0.10183	0.29542	0.59337	-0.37442	0.21896	-0.19612	0.27258	0.076461

When viewed inwards from the terminals A and B, the circuit consists of two parallel paths: one containing R_2 and another containing (R_1+r). The equivalent resistance of the network as viewed from these terminals is given as,

$$R_{th} = \frac{(R_1 + r) * R_2}{R_1 + r + R_2}$$

The resistance "R_{th}" is also called Thevenin equivalent resistance.

Consequently , as viewed from terminals A and B, the whole network (excluding R_1) can be reduced to single source (called thevenin's source) whose e.m.f equal to $V_{O.C.}$ and whose internal reistance equal to R_{th} as shown in figure 4.

4) R_L is now connected back across terminals A and B from where it was temporaily removed earlier. Current flowing through R_L is given by,

$$I_1 = \frac{V_{th}}{R_{th} + R_L}$$

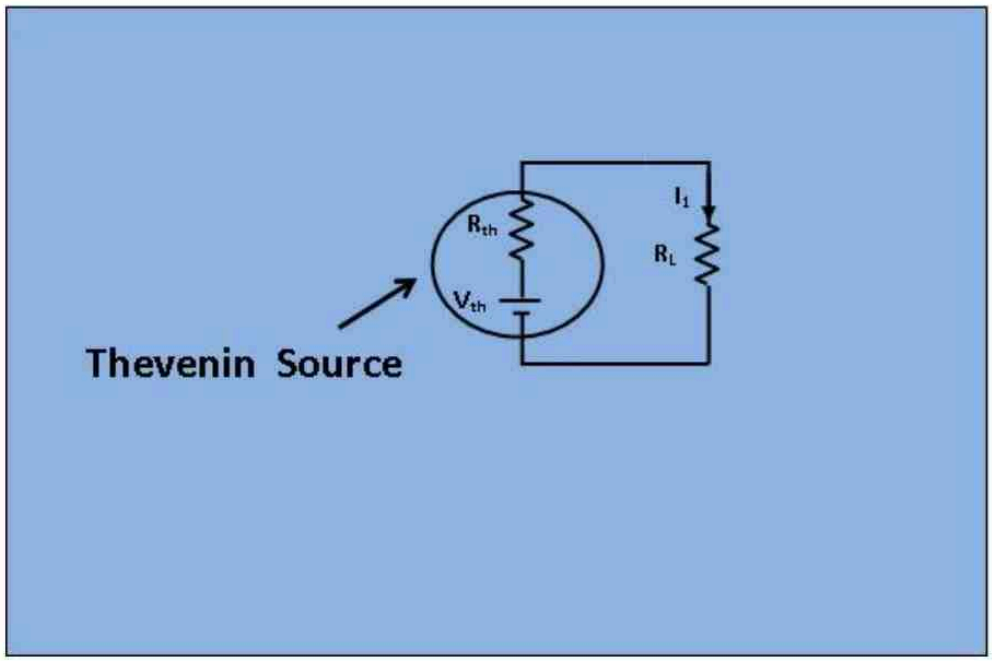


Fig.4 : Thevenin's equivalent circuit

Verification of Thevenin Theorem

Theory

Its provides a mathematical technique for replacing a given network, as viewed from two terminals, by a single voltage source with a series resistance. It makes the solution of complicated networks quite quick and easy. The application of this extremly useful theorem will be explained with the help of following simple example.

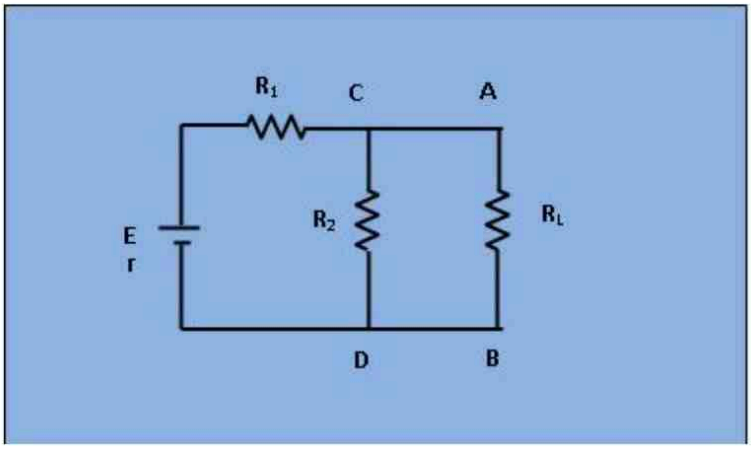


Fig.1 : Circuit with source E and Load R_L

Suppose, it is required to find current flowing through load resistance R_L, as shown in figure 1.

This expression proceed as under:

1) Remove R_L from the circuit terminals A and B and redraw the circuit as shown in figure 2. Obviously, the terminal have become open circuited.

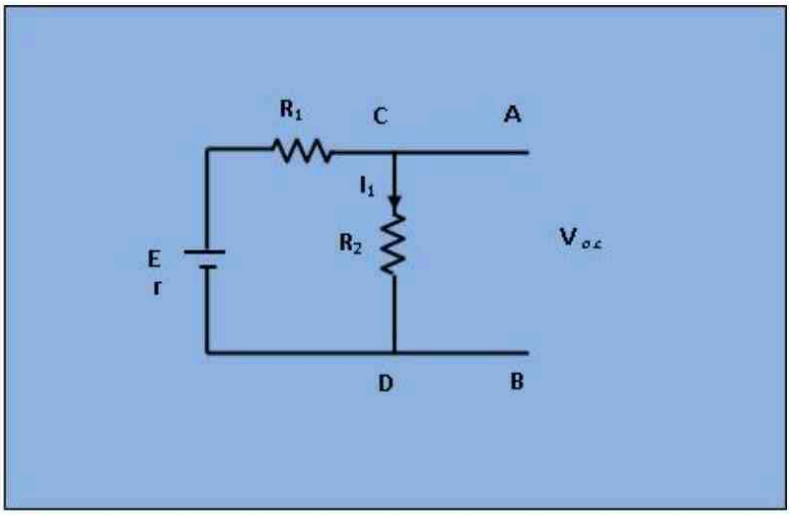


Fig.2 : Circuit with R_L removed

Verification of Thevenin's Theorem

:

resistances (R_1, R_2, R_3, R_L) close to their aximum values. Choose any arbitrary and V_2.

nt Part Select:

ı of S_1 to Power and S_2 to load. Simulate . Observe the result from Table 1.

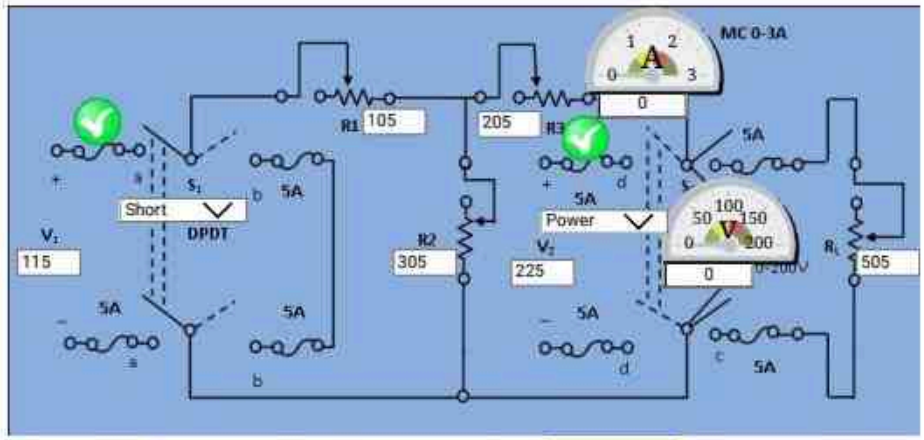
Voltage analysis:
ı S_1 to power and S_2 to intermediate. program.Read Thevenin voltage (V_{th}) tab.

Resistance analysis:
ı S_1 to short and S_2 to power. Simulate . Read Thevenin resistance (R_{th}) from

g V_{th} and R_{th} determine Load

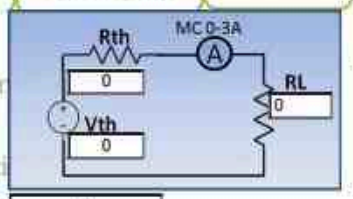
oad resistance in case of the result table load resistance entered in the main late the program. Read Load current e 3 tab. Compare the load currents (I_L) m above two cases.

Coil.
le pole Double throw.
resistances are in ohms.



Case 1 | Case 2(a) | Case 2(b) | Case 3

Click on simulate to get
the Load Current(I_L) from
the Thevenin equivalent
parameter of the above ci



Load Current(I_L) : 0

Simulate

Fill data to the table

ı Table:

ad Current(I_L) from case 1	Load Voltage(V_L)	Load Resistance (R_L)=V_L/I_L	Thevenin Voltage(V_{th}) from case 2(a)	2nd Voltage source(v) for case 2(b)	Ammeter Reading(I) from case 2(b)	Thevenin Resistance R_{th}=V/I	Load current (I_L)=V_{th}/(R_{th}+R_L)
0.10688	53.54688	501	83.112	221	0.79892	276.62	0.10688
0.10730	53.8646	502	83.723	222	0.79785	278.25	0.10730
0.10772	54.18316	503	84.333	223	0.79680	279.87	0.10772
0.10814	54.50256	504	84.941	224	0.79576	281.49	0.10814
0.10855	54.81775	505	85.549	225	0.79474	283.11	0.10855

1) AND gate

The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B or can be written as AB

Y= A.B

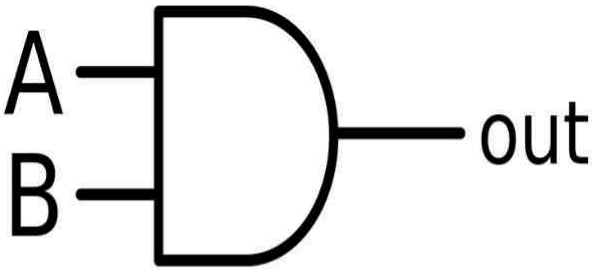


Figure-1:Logic Symbol of AND Gate

Input		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Figure-2:Truth Table of AND Gate

A simple 2-input logic AND gate can be constructed using RTL (Resistor-Transistor-Logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Both transistors must be saturated "ON" for an output at Q.

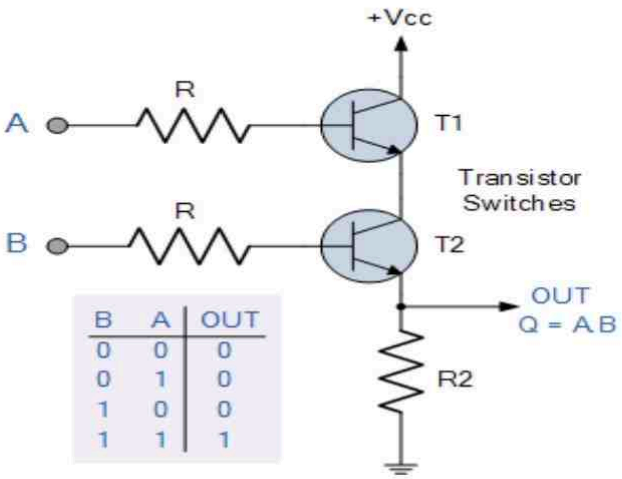
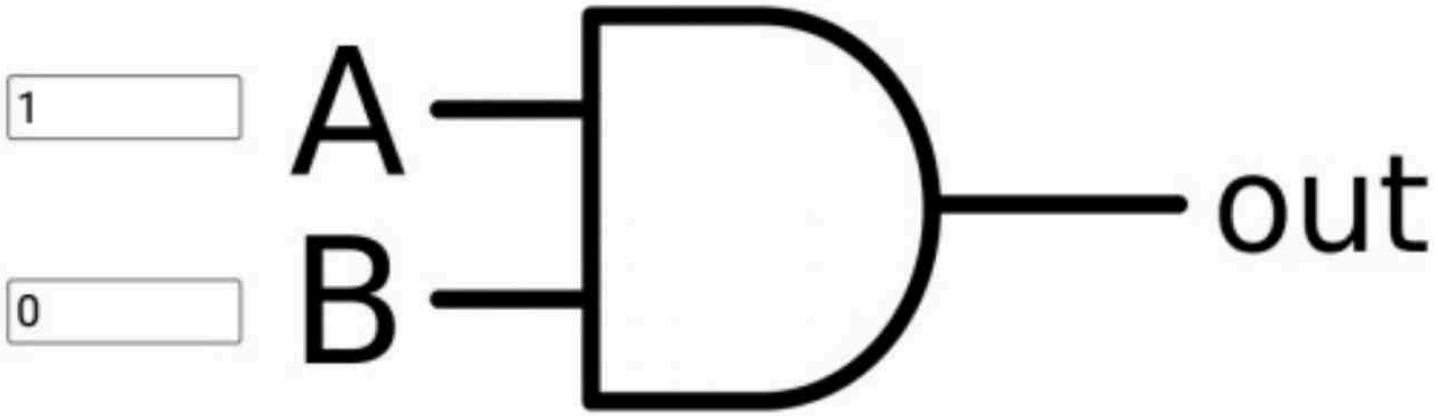


Figure-3:AND Gate through RTL logic

Verification of truth table for AND gate



TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	0	1	0	Correct
2	0	0	0	Correct
3	1	1	1	Correct
4	1	0	0	Correct

Reset

2) OR gate

The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

$$Y = A+B$$

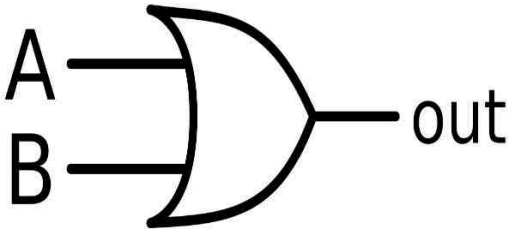


Figure-4:Logic Symbol of OR Gate

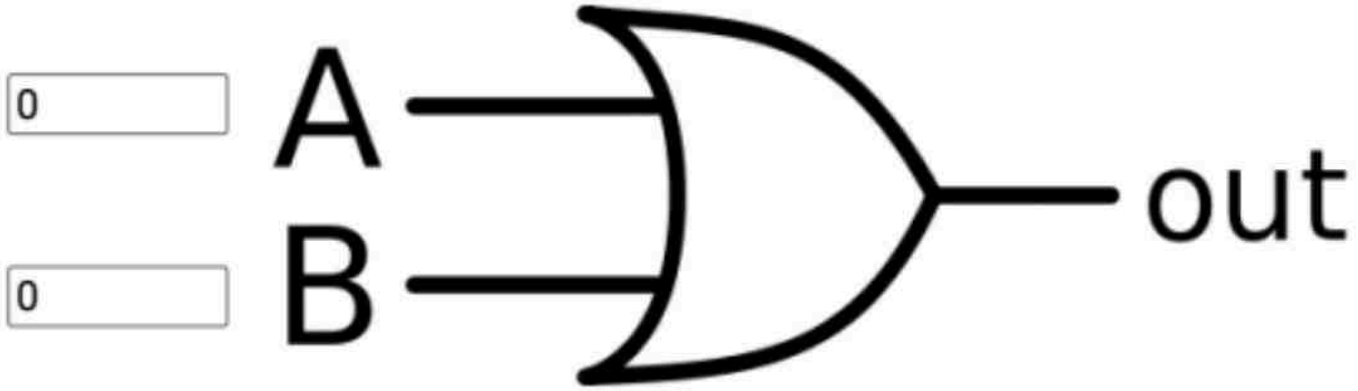
Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Figure-5:Truth Table of OR Gate

OR gate can be realized by DRL (Diode-Resistance-Logic) or by TTL (Transistor-Transistor-Logic). Presently, we will learn how to implement the OR gate using DRL (Diode-Resistance-Logic). To realise OR gate, we will use a diode at every input of the OR gate. The anode part of diode is connected with input while the cathode part is joined together and a resistor, connected with the cathode is grounded. In this case, we have taken two inputs which can be seen in the circuit below.

When both the inputs are at logic 0 or low state then the diodes D1 and D2 become reverse biased. Since the anode terminal of diode is at lower voltage level than the cathode terminal, so diode will act as open circuit so there is no voltage across resistor and hence output voltage is same as ground. When either of the diodes is at logic 1 or high state then the diode corresponding to that input is forward bias. Since this time anode is at high voltage than cathode therefore current will flow through forward biased diode and this current then appears on resistor causing high voltage at output terminal also. Hence at output we get high or logic 1 or +5V. So, if any or both inputs are high, the output will be high or "1".

Verification of truth table for OR gate



TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	1	0	1	Correct
2	1	1	1	Correct
3	0	1	0	Incorrect
4	0	1	1	Correct
5	0	0	0	Correct

Reset

3) NOT gate

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A' or A with a bar over the top, as shown at the outputs.

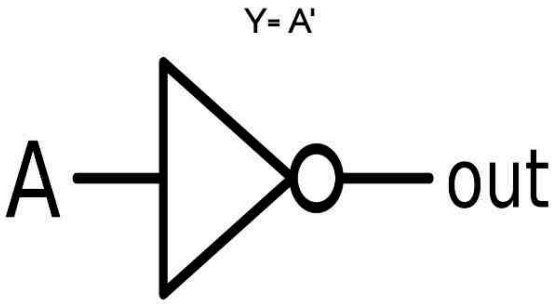


Figure-7:Logic Symbol of NOT Gate

Input	Output
A	Y
0	1
1	0

Figure-8:Truth Table of NOT Gate

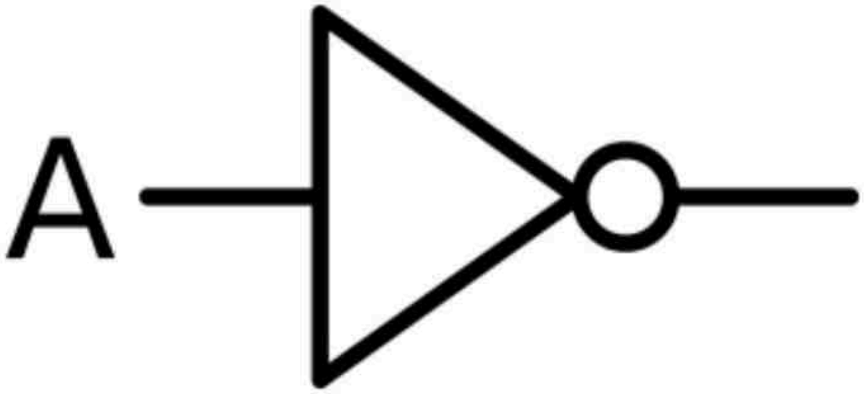
NOT gate can be realized through transistor.The input is connected through resistor R2 to the transistor's base. When no voltage is present on the input, the transistor turns off. When the transistor is off, no current flows through the collector-emitter path. Thus, current from the supply voltage (Vcc) flows through resistor R1 to the output. In this way, the circuit's output is high when its input is low.

When voltage is present at the input, the transistor turns on, allowing current to flow through the collector-emitter circuit directly to ground. This ground path creates a shortcut that bypasses the output, which causes the output to go low.

In this way, the output is high when the input is low and low when the input is high.

Verification of truth table for NOT gate

0



1

Check

Reset

TRUTH TABLE

Print

Serial No.	A	Output	Remarks
1	1	0	Correct
2	0	1	Correct

5) NOR gate

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

$$Y = \overline{A+B}$$

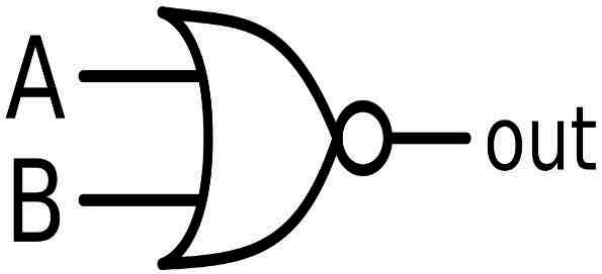


Figure-13:Logic Symbol of NOR gate

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Figure-14:Truth Table of NOR gate

A simple 2-input logic NOR gate can be constructed using RTL (Resistor-transistor-logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Both transistors must be cut-off or "OFF" for an output at Q.

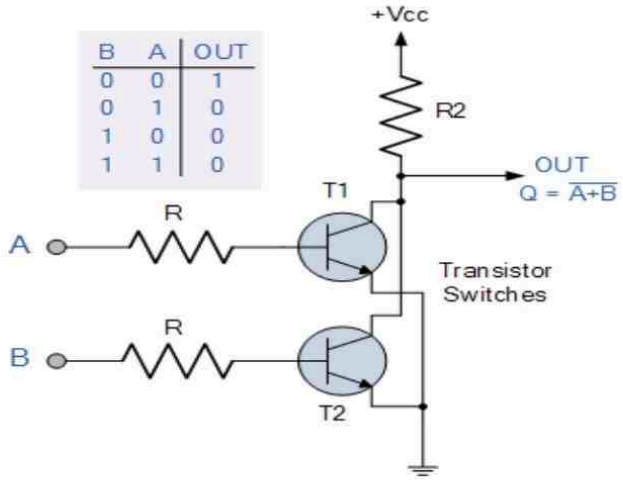
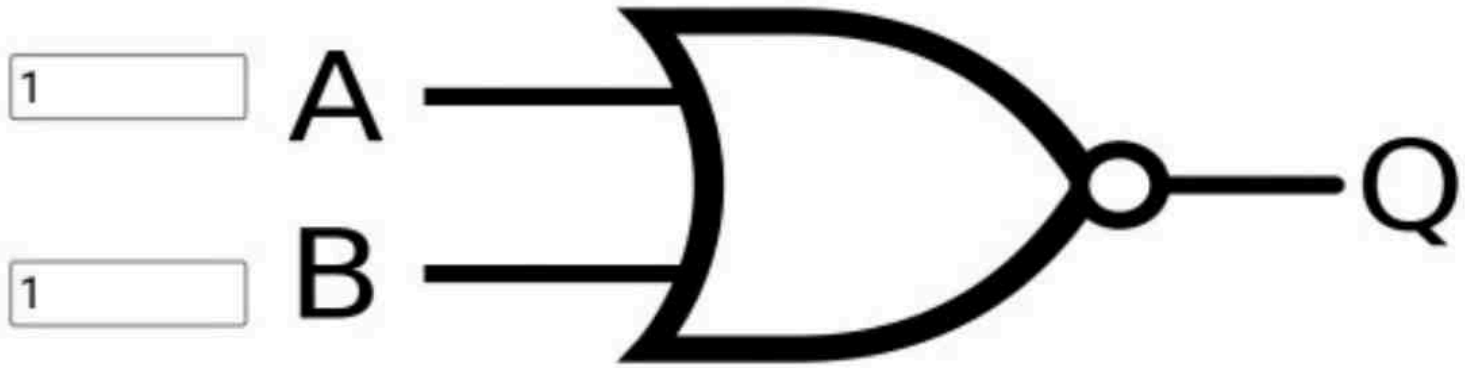


Figure-15:NOR gate through RTL Logic.

Verification of truth table for NOR gate



TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	0	1	0	Correct
3	1	0	0	Correct
4	1	1	0	Correct

Reset

4) NAND gate

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

$$Y = \overline{AB}$$

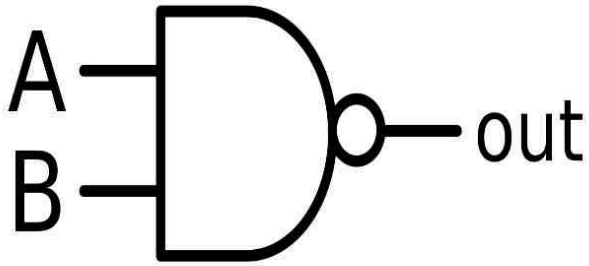


Figure-10:Logic Symbol of NAND Gate

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure-11:Truth Table of NAND Gate

A simple 2-input logic NAND gate can be constructed using RTL (Resistor-transistor-logic) switches connected together as shown below with the inputs connected directly to the transistor bases. Either transistor must be cut-off or "OFF" for an output at Q.

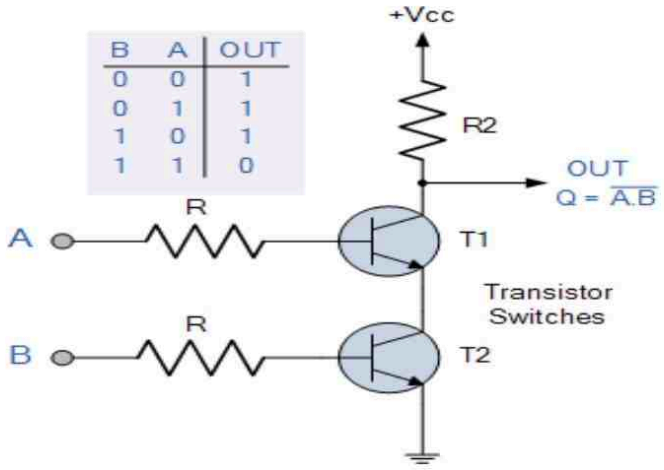
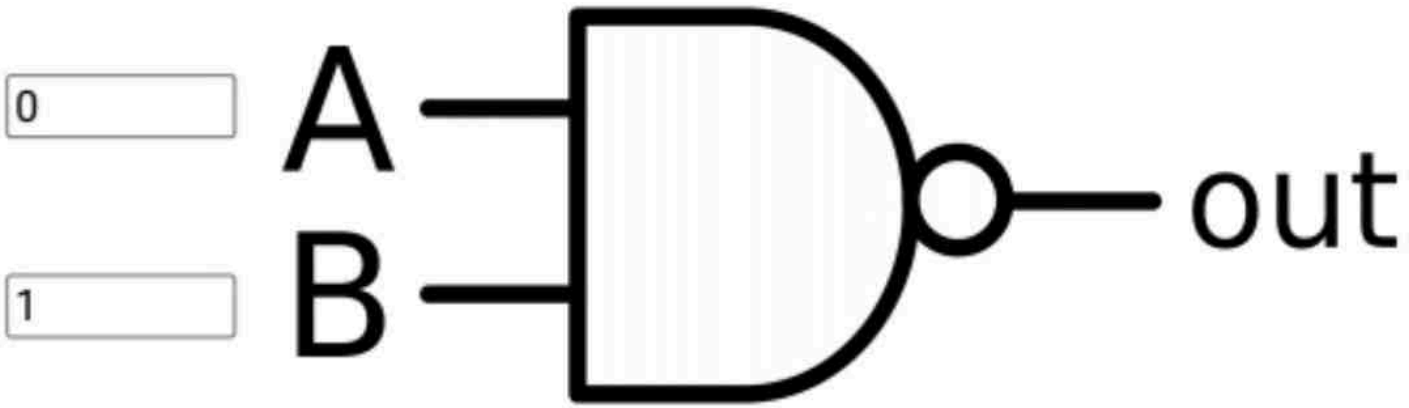


Figure-12:NAND gate through RTL Logic.

Verification of truth table for NAND gate



TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	1	0	0	Incorrect
3	1	0	1	Correct
4	1	1	0	Correct
5	0	1	1	Correct

Reset

6) Ex-OR gate

The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both of its two inputs are high. An encircled plus sign (⊕) is used to show the Ex-OR operation.

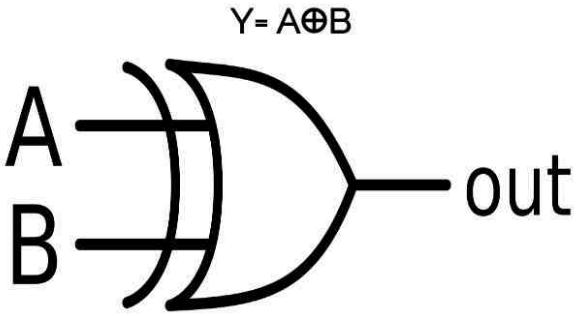


Figure-16:Logic Symbol of Ex-OR gate

A	B	A **XOR** B
0	0	0
0	1	1
1	0	1
1	1	0

Figure-17:Truth Table of Ex-OR gate

Ex-OR gate is created from AND, NAND and OR gates.The output is high only when both the inputs are different.

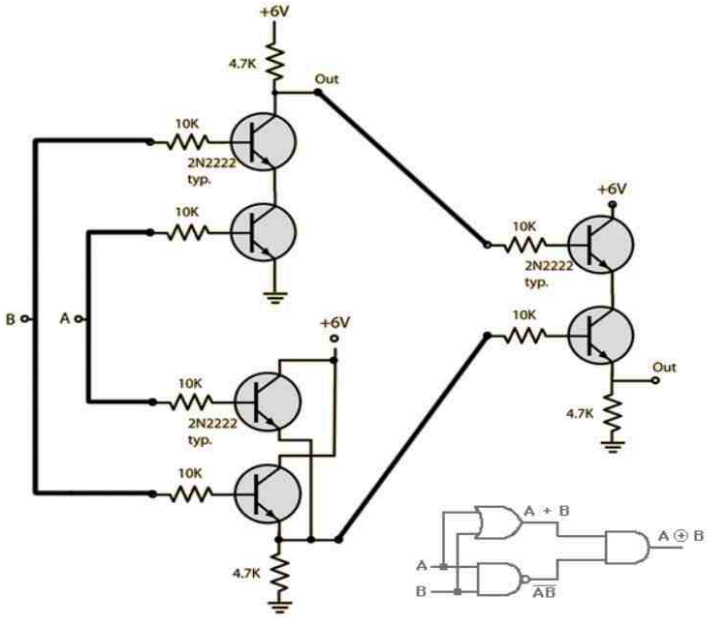
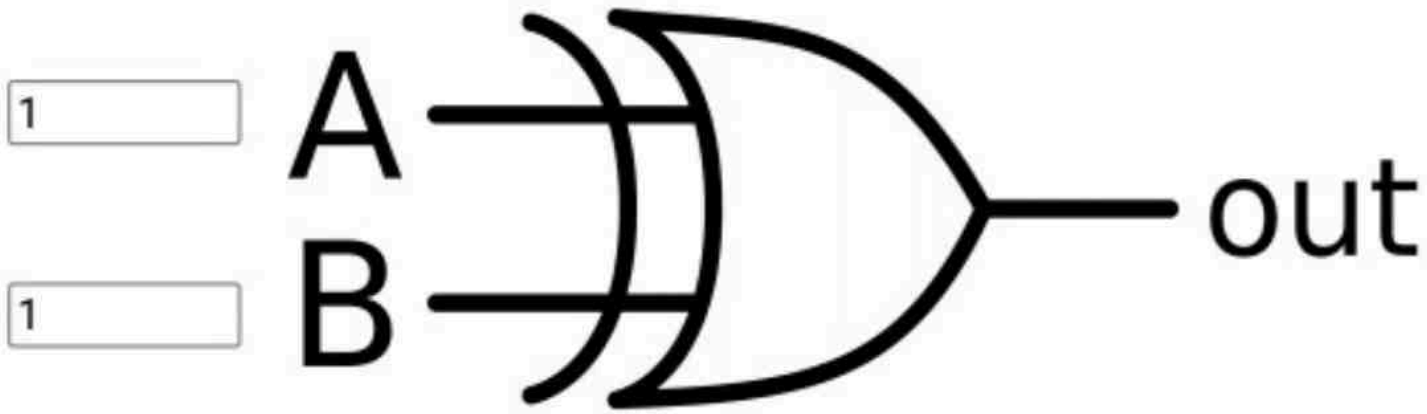


Figure-18:Ex-OR gate through RTL Logic.

Verification of truth table for XOR gate



TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	0	0	0	Correct
2	0	1	1	Correct
3	1	0	1	Correct
4	1	1	0	Correct

Reset

7) Ex-NOR gate

The 'Exclusive-NOR' gate circuit does the opposite to the EX-OR gate. It will give a low output if either, but not both of its two inputs are high. The symbol is an EX-OR gate with a small circle on the output. The small circle represents inversion.

$$Y = \overline{A \oplus B}$$

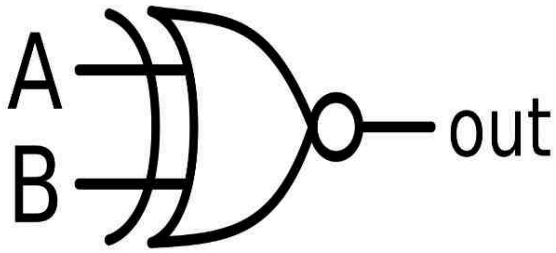
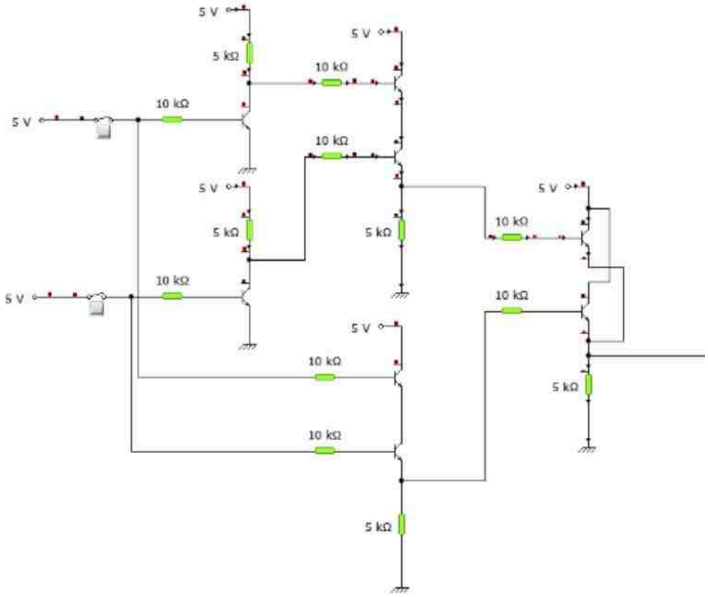


Figure-19:Logic Symbol of Ex-NOR gate

XNOR Truth Table		
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Figure-20:Truth Table of Ex-NOR gate

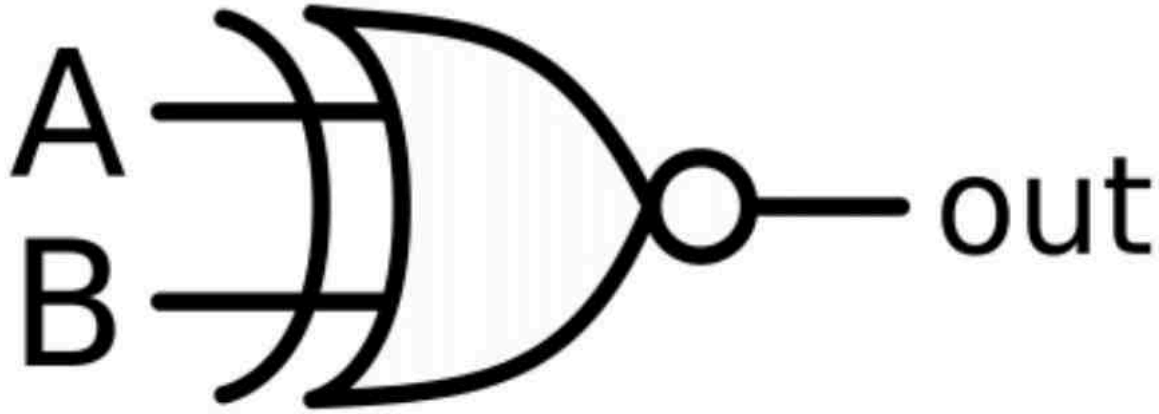
Ex-NOR gate is created from AND, NOT and OR gates.The output is high only when both the inputs are same.



Verification of truth table for XNOR gate

1

0



0

Check

TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	0	1	0	Correct
3	1	1	1	Correct
4	1	0	0	Correct

Reset