University of Tehran
Electrical and Computer Engineering Department

Computer Aided Design of Digital Systems (CAD)
Fall 99
Assignment Description

# CA1: Review on logic design and introduction to FPGA bit-stream generation

***In this assignment, you will review the concepts of FPGA-based logic design.***

***This assignment has three phases: (1) design a combinational and sequential logic, (2) implement in with Verilog, and (3) implement the final design on an FPGA.***

## Phase 2

### PROJECT DESCRIPTION

Implement the 4-bit multiplier that you have already designed in Phase 1 in Verilog. The block diagram of the system is depicted in Figure 1.

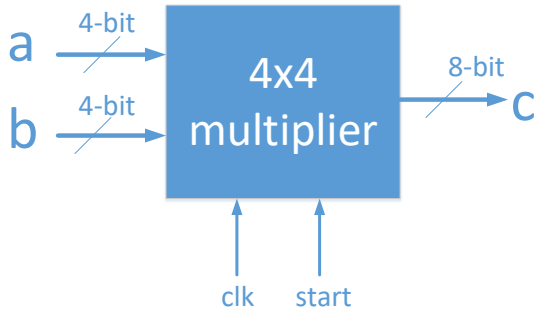


Figure 1. 4x4 multiplier block diagram

You can write the Verilog code in structural (gate-level) or dataflow abstraction levels.

Since you should implement the design on a simple FPGA in Phase 3 of this assignment, it is recommended to write a gate-level Verilog: it facilitates the implementation task of Phase 3.

## Deliverables:

1. The 4x4 multiplier code in Verilog
2. A testbench that applies several inputs and compares the output of the code with the right answer.

## Note:

This assignment can be done in groups (maximum 2 students)