# Experiment 1 - Clock and Periodic Signal Generation

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*Abstract*— **This document gives the final results of the first experiment of digital logic design laboratory.**

## I. Introduction

The goal of this experiment is to introduce the concepts of static characteristics of digital logic gates, delay times, clock frequency generation and digital system using schematic diagram and Verilog HDL.

## II. Clock Generation using ICs and Analog components

### A. *Ring Oscillator*

1. Propagation delay of the chain be calculated by measuring the period time of the output. By using LTspice, propagation delay will be 0.215 µs or 215 ns. This value is equivalent to 6 times the delay of each inverter since we have 3 inverters in the oscillator so by dividing the value above by 6 the delay of an inverter can be achieved. By the calculations mentioned above delay of each inverter will be equal to 0.0358 µs or 35.8 ns.
2. In 7404 TTL datasheet propagation Delay Time LOW-to-HIGH and HIGH-to-LOW is mentioned to be 22 ns and 15 ns respectively, so delay will be equal to 37 ns which is close to the calculated value in the last part.

### B. *LM555 timer*

1. By Implementing LM555 in LTspice and generating the waveform by setting R2 value to 10 kΩ, clock length will be equal to 147 µs so frequency of LM555 will be 6803 Hz. Duty cycle can be calculate from the waveform. The duration in which the clock is on is equal to 76.5 µs, so duty cycle is 52.04%. Waveform of LM555 timer is shown in figure 1.
2. For other values of R2 the procedure is the same. Only the value for R2 changes for the output signal. For 1 kΩ clock cycle length is equal to 21.25 µs so frequency is 47059 Hz also since duration in which clock is on is equal to 14.06 µs so duty cycle is 66.16%.
For 10 kΩ clock cycle length is equal to 147 µs so frequency is 6803 Hz also since duration in which clock is on is equal to 76.5 µs so duty cycle is 52.04%.
For 50 kΩ clock cycle length is equal to 0.7061 ms so frequency is 1416.23 Hz also since duration in which clock is on is equal to 0.3542 ms so duty cycle is 50.16%.
For 100 kΩ clock cycle length is equal to 1.4045 ms so frequency is 712 Hz also since duration in which clock is on is equal to 0.7013 ms so duty cycle is 49.93%.

Now by using the formulas in the description the values will be as shown below:
For 1 kΩ clock cycle length is equal to 20.79 µs so frequency is 48100 Hz also since duration in which clock is on is equal to 13.86 µs so duty cycle is 66.67%.
For 10 kΩ clock cycle length is equal to 145.53 µs so frequency is 6871 Hz also since duration in which clock is on is equal to 76.23 µs so duty cycle is 52.38%.
For 50 kΩ clock cycle length is equal to 0.7 ms so frequency is 1428 Hz also since duration in which clock is on is equal to 0.353 ms so duty cycle is 50.42%.
For 100 kΩ clock cycle length is equal to 1.3929 ms so frequency is 717 Hz also since duration in which clock is on is equal to 0.7 ms so duty cycle is 50.2%.

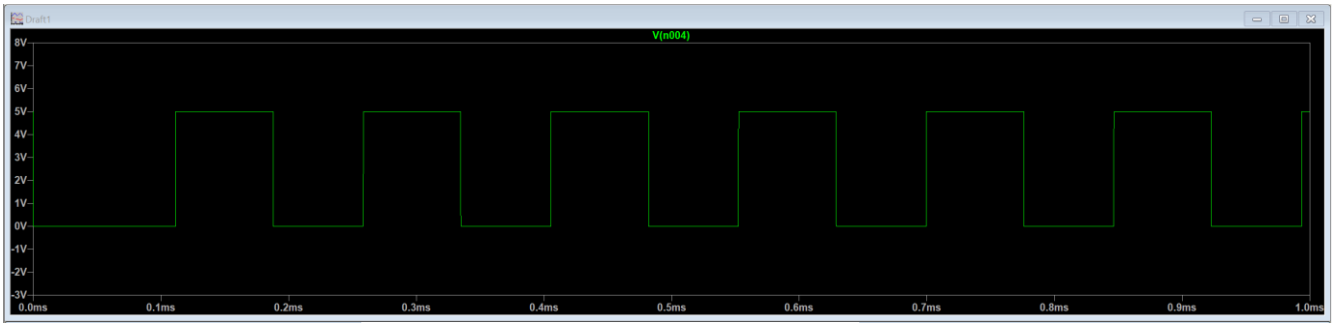


Fig. 1 Waveform LM555 timer

*C. Schmitt Trigger Oscillator*

1. The circuit is designed in LTspice and the files are included in the sent files.
2. For each part capacitor value is equal to 10 nF but resistor value is variable. For 470 Ω clock cycle length is equal to 5.05 µs so frequency is 198019 Hz now putting the values in the formula α will be 0.931.
   For 1 kΩ clock cycle length is equal to 8.5 µs so frequency is 117647 Hz now putting the values in the formula α will be 1.176.
   For 2.2 kΩ clock cycle length is equal to 16.19 µs so frequency is 61766 Hz now putting the values in the formula α will be 1.359.

## III. Clock Generation using Verilog HDL

1. The code is generating clock by using LM555 timer. First the code defines on duration and off duration which their values are computed using the formulas in part B then by getting the log of these values we will know how many bits we want for count_on and count_off. These two will be used for knowing how long the pulse value has been 1 or 0 so by this we can know when to change the output pulse. The second and third always statements are basically counters which will count if their enable is issued. But the on and off enable and reset are the tricky parts. For on enable we must keep it issued until clock changes from 1 to 0 this means until either on counter or off counter has finished their duration which is computed from the formulas that was also mentioned above. For off enable whenever the on duration is over we can issue it since the clock must change from 1 to 0. Now on and off reset is used to keep the clock generating, so if the main reset that is the input of the module or a whole clock duration is over on and off reset will be issued, when off counter reaches its end duration then a whole clock cycle has passed so we need to reset the on and off counter so that we start over again and keep generating clock cycles. The first always statement is used to give out clock pulses. When the on enable changes to 1 it'll output 1 and when off enable changes to 1 it'll output 0 so by this procedure clock cycles are created.

2. Block diagram is shown in figure 2 and the explanation is done in the section above.

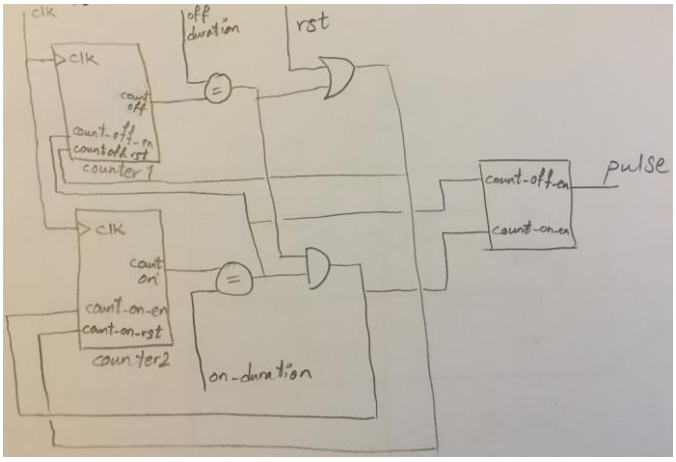


Fig. 2 Timer code block diagram

3. Test bench is included in sent files under the folder named part 2.

4. Using the values from previous parts for R2, for 1 kΩ clock cycle length is 420 µs and duty cycle is 66.67%.
   For 10 kΩ clock cycle length is 2900 µs and duty cycle is 52.41%.
   For 50 kΩ clock cycle length is 14002 µs and duty cycle is 50.41%.
   For 100 kΩ clock cycle length is 27860 µs and duty cycle is 50.25%.
   Duty cycles are pretty close to previous part but clock cycle differ. Since the implementations in both parts can be different and as mentioned in the description of this part that synthesizable and not synthesizable implementations differ in time contrast might happen but all in all the results are pretty close.

5. Alternative code for timer is included in sent files under folder named Part 2. Test bench Waveforms are all included in folder named Part 2 Photos. Duty cycles are pretty close to ones in last section. All waveforms of this whole part are shown below.

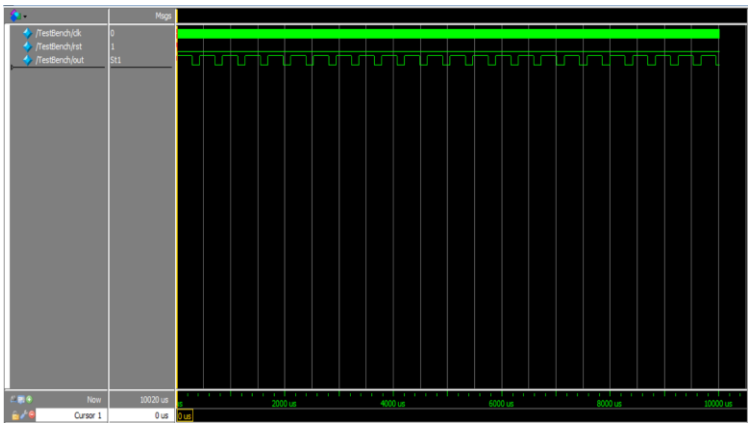

Fig. 3 Waveform timer R2 = 1 kΩ

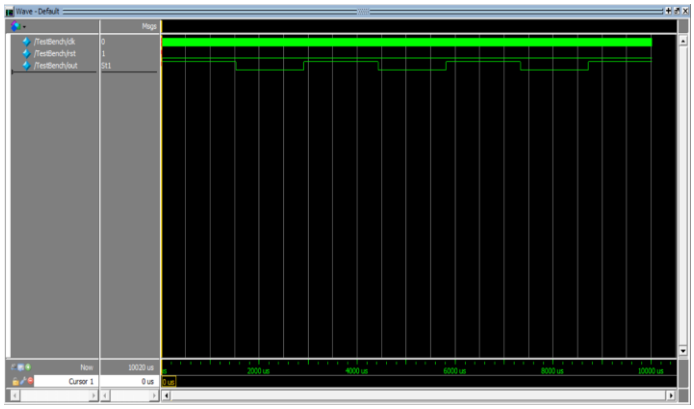

Fig. 4 Waveform timer R2 = 10 kΩ

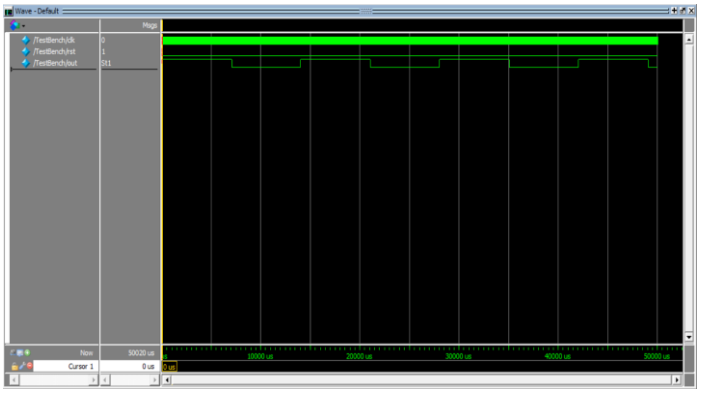

Fig. 5 Waveform timer R2 = 50 kΩ

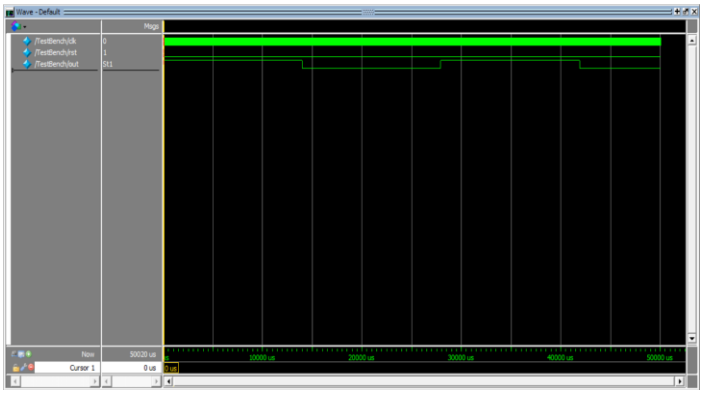

Fig. 6 Waveform timer R2 = 100 kΩ

## IV. FPGA Design

### A. *Ring Oscillator*

1. Ring oscillator code is included in sent files under the folder named 3.1.

2. Test bench code is included in sent files under the folder named 3.1 and the delay values are taken into consideration.

3. Clock cycle length for the ring oscillator is equal to 240 ns so frequency is 4166666 Hz. Waveforms are shown in figure 7.

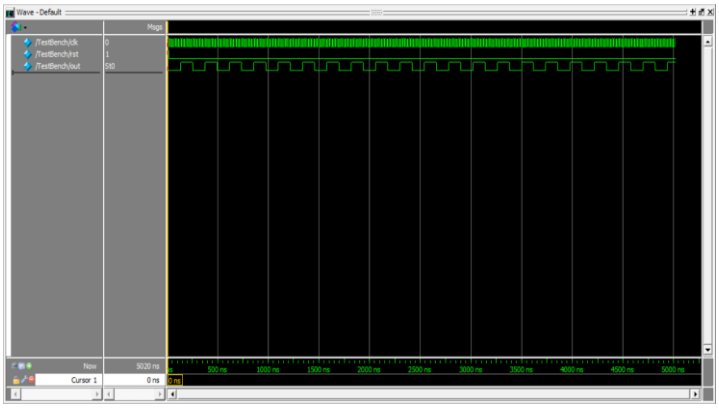

Fig. 7 Waveform ring oscillator

### B. *Synchronous Counter as a Frequency Divider*

1. Done in Quartus
2. Done in Quartus
3. Done in ModelSim
4. Done in ModelSim
5. Frequency of max/min signal is 42.95 Hz but the frequency of input clock which is given by ring oscillator is 4166666 Hz so the frequency has dropped considerably.

### C. *T Flip-Flop*

This part is done for part D in Quartus.

### D. *Display module in FPGA*

1. Done in Quartus
2. Done in Quartus
3. Done in Quartus
4. Done in Quartus
5. Done in Quartus
6. Done in ModelSim
7. T Flip-Flop from last part, according to the description, produces a 50% duty cycle signal, taking this fact into account, in waveform after 46.96 µs the duration will give 96 as an output. Because of 50% duty cycle, half the length of the max/min signal which is the input of T Flip-Flop will be equal to 23.48 µs. This value is half of clock cycle length and according to duty cycle this means that this value is the duration in which signal is one. By having this time and according to the definition of duration output which is mentioned in description of this part, dividing this time value by the duration output will result in ring oscillator clock cycle length. So clock cycle length of oscillator will be 244.5 ns so frequency will be 4098360 Hz and clock cycle length of max/min signal will be 23.48 µs so the frequency will be 42589.44 Hz.

## References

[1] 7404 TTL Datasheet, https://www.futurlec.com/74/IC7404.shtml