UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1398
Computer Assignment 2
Gate Level Structures and Simple Functional Structures in Verilog
Week 5

Name:
Date:

In this problem you are to design and implement a serial multi-broadcasting system with four ports P[0:3], where each port has four lines L[0:3]. The single serial input, serIn, may be broadcasted to several ports selected by PB [0:3] vector that has a 1 for every port that the serial data is being broadcasted to. Data broadcasted to the ports will be broadcasted to only one of the lines of the port. For this, we need a 2-bit LB[1:0] input identifying lines of the ports that data will be broadcasted to. As an example, if PB=1011 and LB=10, then the serial input will be broadcasted to lines 2 of ports 3, 1, and 0. For the design of this system you will be using the gates and the demultiplexers of Assignment 1.

1. Using two-input NOR gates of Computer Assignment 1, design a demultiplexer with a serial input, serIn, and four port outputs, P[0:3]. The select input of this circuit is PB[0:3] that selects all those ports that serIn will be broadcasted to. Use delay values calculated based on transistor delays of the previous assignment.
2. Describe the circuit of Part 1 using **assign** statements.
3. In a testbench, test the circuits of Parts 1 and 2 and back annotate the timing of Part 1 into the **assign** statement of Part 2. Compare the delay values.
4. Using three-input NOR gates of Assignment 1, design a 1-to-4 demultiplexer with four line outputs, L[0:3]. The two bit LB[1:0] decides the only line that the serial input of this circuit will be appearing on.
5. Describe the circuit of Part 4 using **assign** statements with vector indexing, i.e., **assign** L[LB]=inP.
6. In a testbench, test the circuits of Parts 4 and 5 and back annotate the timing of Part 4 into the **assign** statement of Part 5. Compare the delay values.
7. Using one copy of circuit of Part 2, and four copies of circuit of Part 5, design the multi-broadcasting system described above.
8. Use **assign** statements with nested conditions to build the entire circuit of Part 7.
9. In a testbench, test the circuits of Parts 7 and 8 and back annotate the timing of Part 7 into the **assign** statement of Part 8. Compare the delay values. Create a serial input using a repeat statement and see how it displays over the selected lines.