UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Fall 1398
Computer Assignment 1
Basic Switch and Gate Structures in Verilog
Week 3

Name:
Date:

In this problem you are to design and implement a 1-to-2^n demultiplexer circuit that connects a 1-bit input to any of its 2^n outputs. The circuit has an n-bit select input, the binary number on which selects the output that the input will be connected to. We will start with a 1-to-2 demultiplexer, i.e., n value of 1.

1. Show switch level circuit diagram for an inverter, a 2-input NOR gate, and a 3-input NOR gate. Use a minimum number of nMOS and pMOS transistors. Use #(3, 4, 5) delay values for the nMOS transistors and #(5, 6, 7) for the pMOS transistors.
2. Create a testbench and examine gates of Part 1.
3. Using gates of Part 1 create a 1-to-2 demultiplexer that has a 1-bit select input and a 1-bit data input. This circuit is at the switch level.
4. Create a testbench and examine the circuit of Part 3.
5. Using three instances of circuit of Part 3 create a 1-to-4 demultiplexer. This circuit is at the switch level.
6. Create a testbench and examine the circuit of Part 5.
7. Using simulation results of Part 2 and using NOR and NOT primitives instead of switch level gates of Part 1, redo Part 3. This circuit is at the gate level.
8. Create a testbench and examine the circuit of Part 7. Add circuit of Part 3 to this testbench and record and report the differences.
9. Using three instances of circuit of Part 7 create a 1-to-4 demultiplexer. This circuit is at the gate level, and has a hierarchical structure.
10. Create a testbench and examine the circuit of Part 9. Add circuit of Part 5 to this testbench and record and report the differences.
11. Using the three-input NOR gate of Part 1 generate a 1-to-4 demultiplexer. This circuit is at the gate level, and has a flat structure.
12. Create a testbench and examine the circuit of Part 11. Add circuits of Part 5 and Part 9 to this testbench and record and report the differences.